Construction Analysis

Analog Devices ADSP-21062-KS-160 SHARC Digital Signal Processor

Report Number: SCA 9712-575

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Analog Devices ADSP-21062-KS-160 SHARC Digital Signal Processor. Two devices which were packaged in 240-pin Plastic Quad Flat Packages (PQFP) were received for the analysis. The devices were date coded 9641 and 9701. The majority of the analysis was performed on the device date coded 9701.

MAJOR FINDINGS

Questionable Items:[1]

- none.

Special Features:

- Sub-micron gate lengths (0.5 micron).
- Tungsten plugs.

[1]These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 240-pin Plastic Quad Flat Packages (PQFP). A copper heat slug (heatsink) was employed on the top of the package (cavity down orientation). It was internally connected to ground.

- Wirebonding method: A thermosonic ball bond technique employing 1.2 mil O.D. gold wire was used.

- Dicing: Sawn (full depth) dicing.

- Die attach: A silver epoxy compound.

Die Process

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an N substrate.

- Die coat: No die coat was used on the devices.

- Final passivation: A layer of nitride over a layer of silicon-dioxide.

- Metallization: Two levels of metal defined by standard dry-etch techniques. Metal 2 consisted of aluminum with a titanium-nitride cap and barrier. Metal 1 consisted of aluminum, a titanium nitride cap and barrier, and a titanium adhesion layer. Tungsten plugs were used as the vertical interconnect under both metal layers. They were lined with titanium-nitride.

- Interlevel dielectric: Interlevel dielectric consisted of four layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between the third and fourth layer.

- Pre-metal dielectric: This dielectric consisted of a layer of reflow glass over densified oxides.

TECHNOLOGY DESCRIPTION (continued)

- Polysilicon: Two layers of polysilicon were used on the die. Poly 1 (polysilicon and tungsten silicide) was used to form redundancy fuses, all gates on the die, and word lines in the array. Poly 2 was used to form "pull-up" resistors in the cell array, and formed resistors in fuse blocks which were connected to one end of the poly 1 fuses. Both poly layers were defined by a dry-etch of good quality.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. No silicide was present on diffusions. An LDD process was used with the oxide sidewall spacers left in place. N+ diffusions were "pushed down" at tungsten contacts.

- Wells: Planar (no step in LOCOS) twin-well process in the N substrate. No epi layer.

- Redundancy: Fuses consisting of poly 1 were present on the die. Passivation and interlevel dielectric cutouts were made over the fuses. One end of the fuse structure was connected to metal 1, while the other end was connected to a poly 2 resistor. Some laser blown fuses were noted.

- Memory cells: The die employed a 2 Mbit SRAM array. The memory cells used a 4T CMOS SRAM cell design. Metal 2 distributed GND and Vdd (via Metal 1), and formed the bit lines using metal 1 links. Metal 1 was used as "piggy-back" word lines. Poly 1 formed the word lines, select, and storage gates. Poly 2 formed "pull-up" resistors and distributed Vdd.

- Both metals 1 and 2 were used in the bond pads.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 2**

Questionable Items:[1] None.

Special Features: None.

General Items:

- Overall package: The device was packaged in a 240-pin PQFP. A large copper heat slug (heatsink) was employed on the top of the package (cavity down orientation). It was internally connected to GND.

- Wirebonding method: A thermosonic ball bond technique employing 1.2 mil gold wire was used. All bonds were well formed and placed. Bond strengths were normal as determined by wire pull tests.

- Dicing: Sawn (full depth). No large chips or cracks were noted.

- Die attach: A silver epoxy compound of normal quality.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process and Design: **Figures 3 - 39**

Questionable Items:[1]

- None.

Special Features:

- Sub-micron gate lengths (0.5 micron).

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an N substrate.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels.

- Die surface defects: None. No contamination, toolmarks or processing defects were noted.

- Passivation: A layer of nitride over a layer of silicon-dioxide. Passivation coverage and edge seal were good. Integrity test indicated defect free passivation.

- Metallization: Two levels of metallization were used. Metal 2 consisted of aluminum with a titanium-nitride cap and barrier. Metal 1 consisted of aluminum, titanium-nitride cap and barrier, and a titanium adhesion layer. Tungsten plugs were employed under both metal layers. The plugs were lined with titanium-nitride.

- Metal patterning: All metal layers were defined by a dry etch of good quality.

[1]*These items present possible quality concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal defects: None. No voiding, notching or cracking of the metal layers was found. Silicon nodules were found following removal of metal 1.

- Metal step coverage: Virtually no metal thinning was noted due to the use of tungsten plugs. The tungsten plugs were nearly level with the oxide surface, so no large steps were present for the metal to cover.

- Vias and contacts: Vias and contacts were defined by a dry-etch. No significant over-etching was noted.

- Interlevel dielectric: Interlevel dielectric consisted of four layers of silicon-dioxide with a spin-on-glass (SOG) between the third and fourth layers to aid in planarization. No problems were noted.

- Pre-metal dielectric: This dielectric consisted of a layer of reflow glass (BPSG) over densified oxide. No problems were found.

.• Polysilicon: Two layers of polysilicon were employed. Poly 1 (polysilicon and tungsten silicide) formed the redundancy fuses, all gates on the die, and word lines in the array. Poly 2 was used to form resistors in the cell array and outside the fuse blocks. Definition was by a dry etch of good quality. No problems were found.

- Isolation: LOCOS (local oxide isolation). No problems were noted at birdsbeak or elsewhere and no step was present at the well boundaries.

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Oxide sidewall spacers were present to provide LDD spacing. Deep (pushed down) N+ diffusions were noted under contacts in N regions. Diffusions were not silicided. No problems were found.

- Wells: Twin-wells were employed in an N substrate. No step was present at the well boundaries. No problems were noted.

ANALYSIS RESULTS II (continued)

- Buried contacts: Direct poly-to-diffusion (buried) contacts were only used in the SRAM array. No problems were found in these areas.

- Redundancy: Poly 1 fuses were present along the row and column decode logic outside the SRAM array. Passivation and interlevel dielectric cutouts were made over the fuses. Laser blown fuses were noted.

- Memory cells: The die employed a 2 Mbit SRAM array. The memory cells used a 4T CMOS SRAM cell design. Metal 2 distributed GND and Vdd, and formed the bit lines using metal 1 links. Metal 1 was used as the "piggy-back" word lines. Poly 1 formed the word lines, select, and storage gates. Poly 2 formed "pull-up" resistors and distributed Vdd. Cell size was 3.3 x 5.7 microns (19 microns^2).

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decap

SEM of passivation

Passivation integrity test (chemical)

Wirepull test

Passivation removal

SEM inspection of metal 2

Aluminum 2 removal and inspect

Delayer to metal 1 and inspect

Aluminum 1 removal and inspect barrier

Delayer to polycide/substrate and inspect

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity:	G
Die placement:	G
Die attach quality:	G
Wire spacing:	N
Wirebond placement:	N
Wirebond quality:	G
Dicing quality:	G
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die attach method	Silver-epoxy
Dicing	Sawn (full depth)
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	G
Metal registration	G
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

Sample 1	Sample 2
(LOGO) ANALOG DEVICES ADSP-21062 9641 KS-160 ED/C15598.00-2.1 (SHARC LOGO)	(LOGO) ANALOG DEVICES ADSP-21062 9701 KS-160 ED/C16005.00-2.1 (SHARC LOGO)

BOTTOM

WAFER H HONG KONG	WAFER H HONG KONG

WIREPULL TEST

Sample	2
# of wires tested:	25
Bond lifts:	0
Force to break - high:	9g
- low:	5.25g
- avg.:	7.45g
- std. dev.:	1.0

DIE MATERIAL IDENTIFICATION

Overlay passivation:	Nitride over silicon-dioxide.
Metallization 2:	Aluminum with a titanium-nitride cap and barrier.
Interlevel dielectric:	Multiple layers of silicon-dioxide including SOG.
Metallization 1:	Aluminum with a titanium-nitride cap and barrier, on a titanium adhesion layer.
Plugs:	Tungsten, lined with titanium-nitride.
Pre-metal glass:	BPSG reflow glass on densified oxide.
Silicide (Poly 1):	Tungsten.

HORIZONTAL DIMENSIONS

Die size:	11.9 x 14.9 mm (468 x 586 mils)
Die area:	177 mm^2 (274,248 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.4 x 4.4 mils)
Min pad window:	0.09 x 0.09 mm (3.7 x 3.7 mils)
Min pad space:	40 microns
Min metal 2 width:	0.8 micron
Min metal 2 space:	1.0 micron
Min metal 2 pitch:	1.8 micron (uncontacted)
Min metal 1 width:	0.6 micron
Min metal 1 space:	0.7 micron
Min metal 1 pitch:	1.3 micron (uncontacted)
Min via:	0.45 micron
Min contact:	0.5 micron
Min polycide width:	0.5 micron
Min polycide space:	0.7 micron
Min gate length* - (N-channel):	0.5 micron
- (P-channel):	0.5 micron
Min LOCOS:	0.8 micron
SRAM cell size:	19.0 $microns^2$
SRAM cell pitch:	3.3 x 5.7 microns

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.45 mm (18 mils)

Layers

Passivation 2:	0.6 micron
Passivation 1:	0.15 micron
Metal 2 - cap:	0.04 micron (approx.)
- aluminum:	0.7 micron
- barrier:	0.09 micron
- plugs:	0.8 - 1.0 micron
Interlevel dielectric - glass 4:	0.5 micron (average)
- glass 3:	0.15 micron (average)
- glass 2:	0.35 - 0.75 micron
- glass 1:	0.15 micron (average)
Metal 1 - cap:	0.15 micron (approx.)
- aluminum:	0.5 micron
- barrier:	0.1 micron
- plugs:	0.5 - 1.0 micron
Pre-metal glass:	0.65 micron
Polycide - silicide:	0.1 micron
- poly:	0.13 micron
Local oxide:	0.4 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.2 micron
N-well:	2.5 microns (approx.)
P-well:	2.0 microns (approx.)

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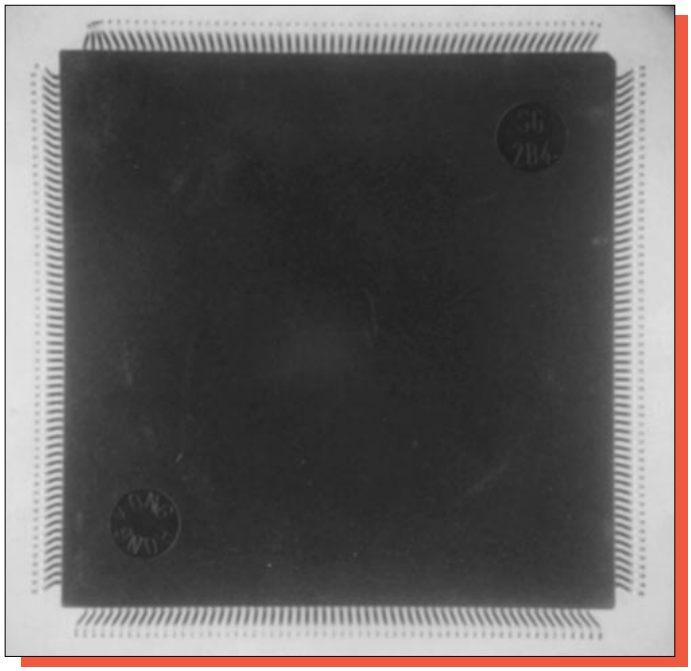
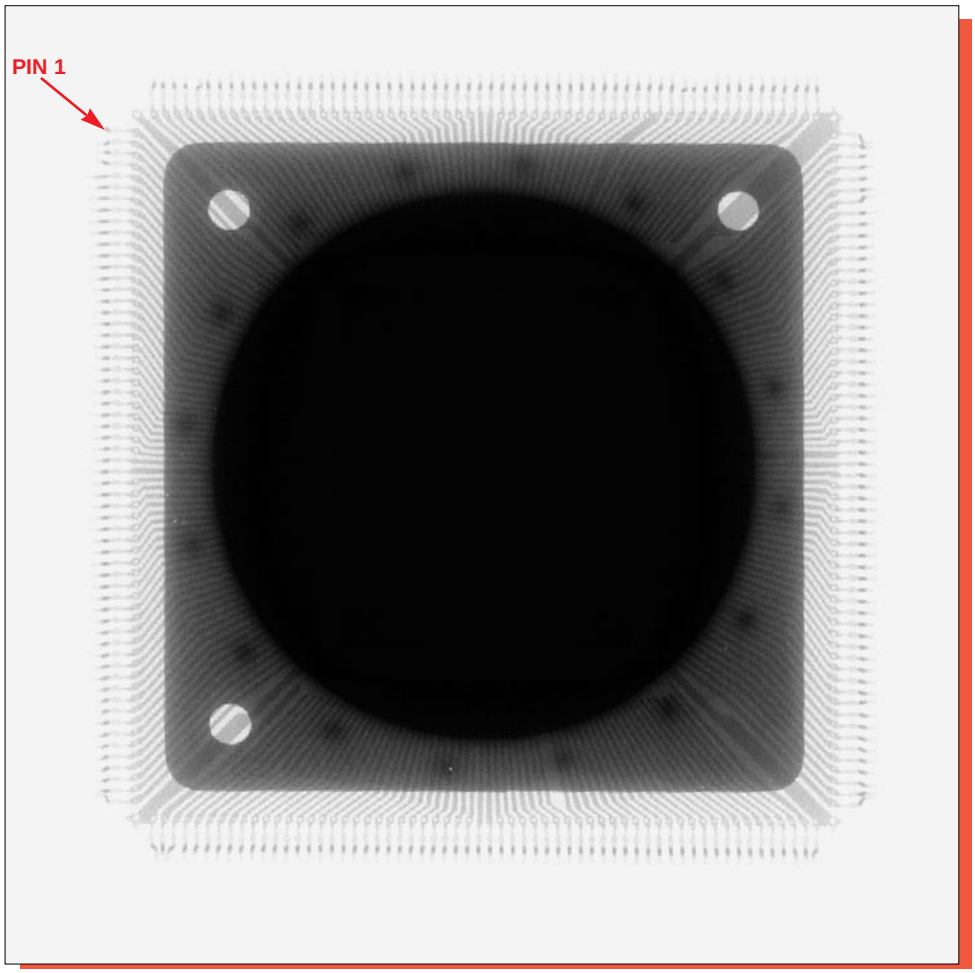


Figure 1. Package photographs of the Analog Devices ADSP-21062-KS-160 SHARC Digital Signal Processor. Mag. 2.5x.



top

Figure 2. X-ray view of the package. Mag. 3x.

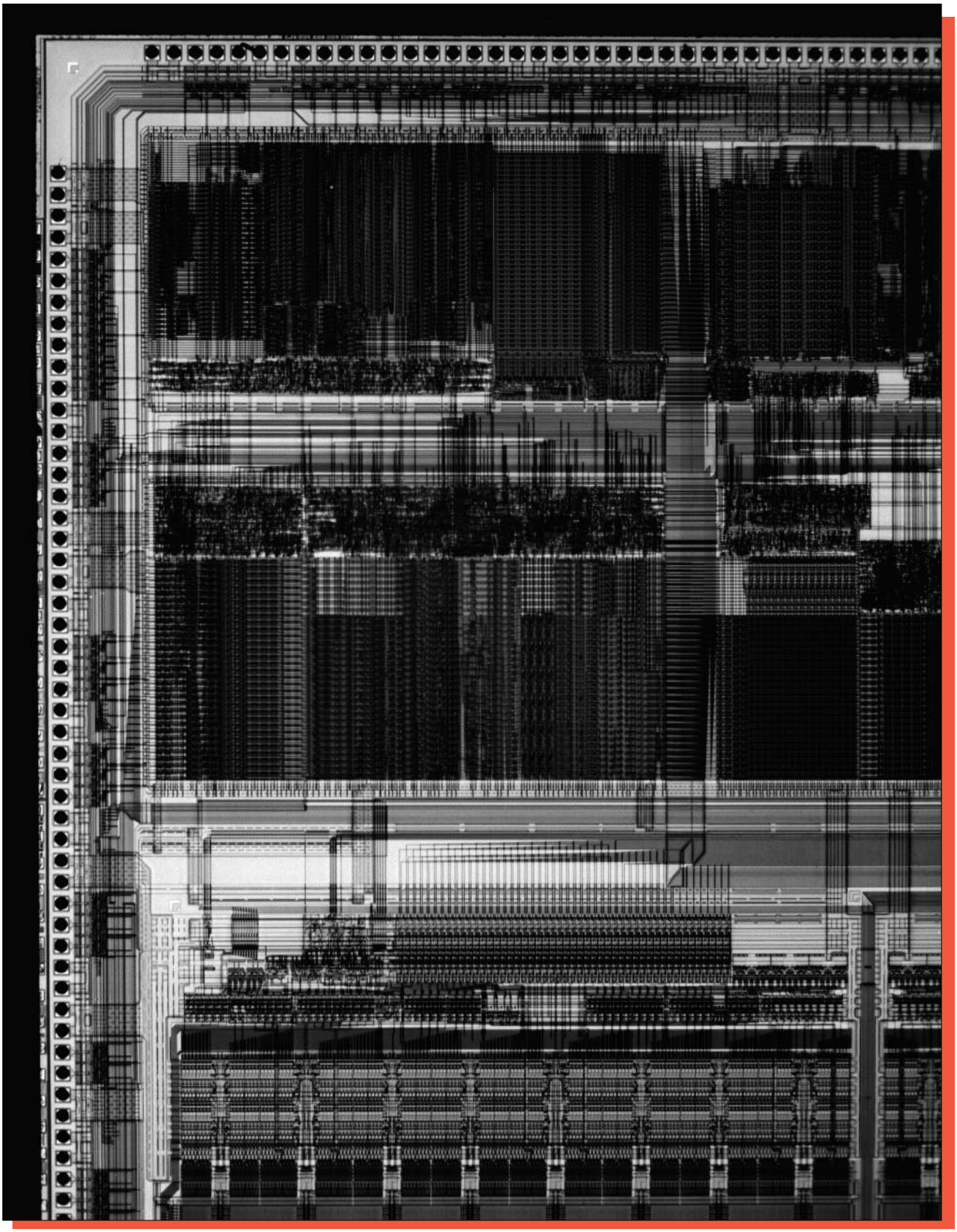


Figure 3. Portion of the Analog Devices ADSP-21062-KS-160 die. Mag. 26x.

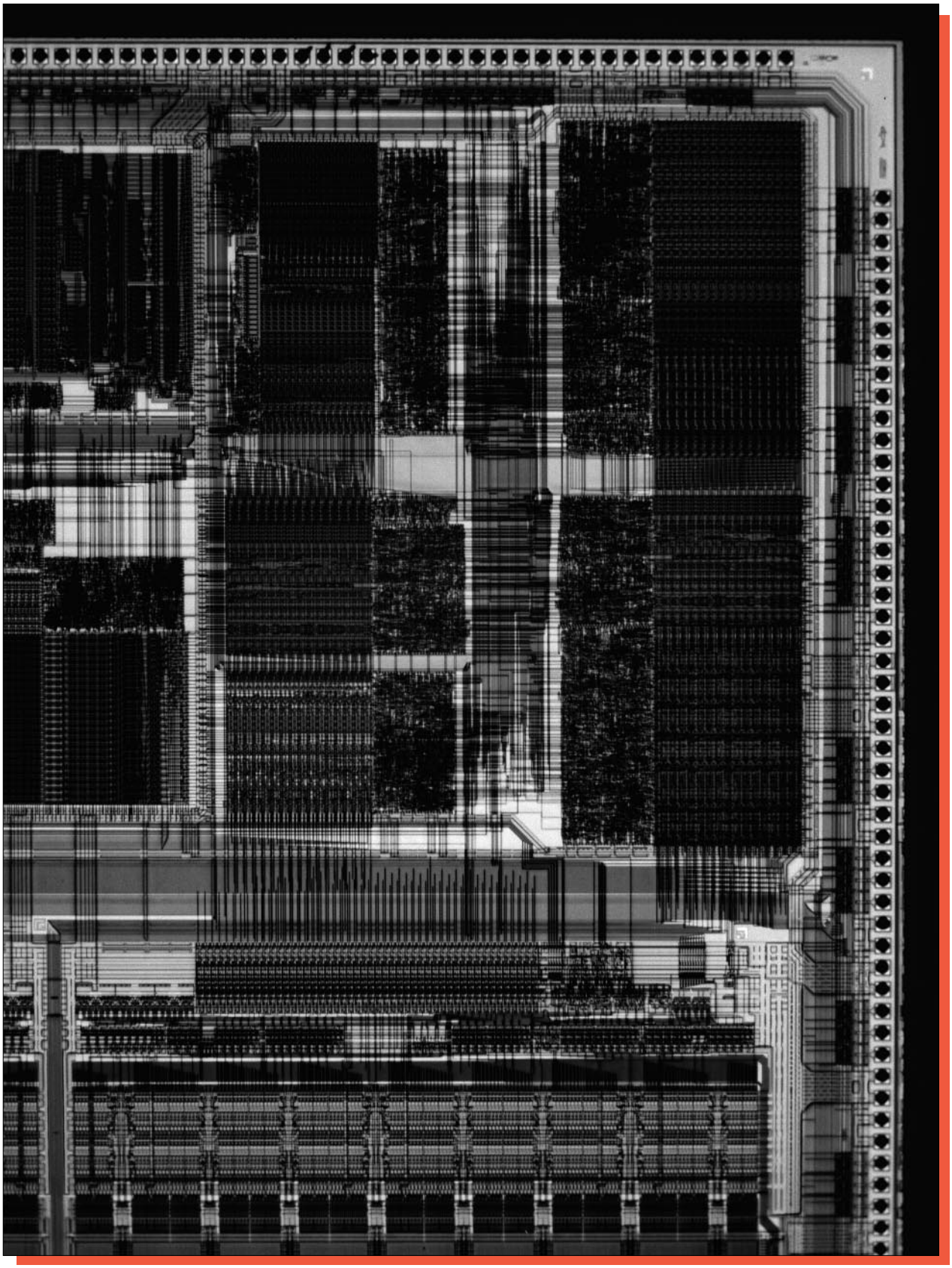


Figure 3a. Portion of the Analog Devices ADSP-21062-KS-160 die. Mag. 26x.

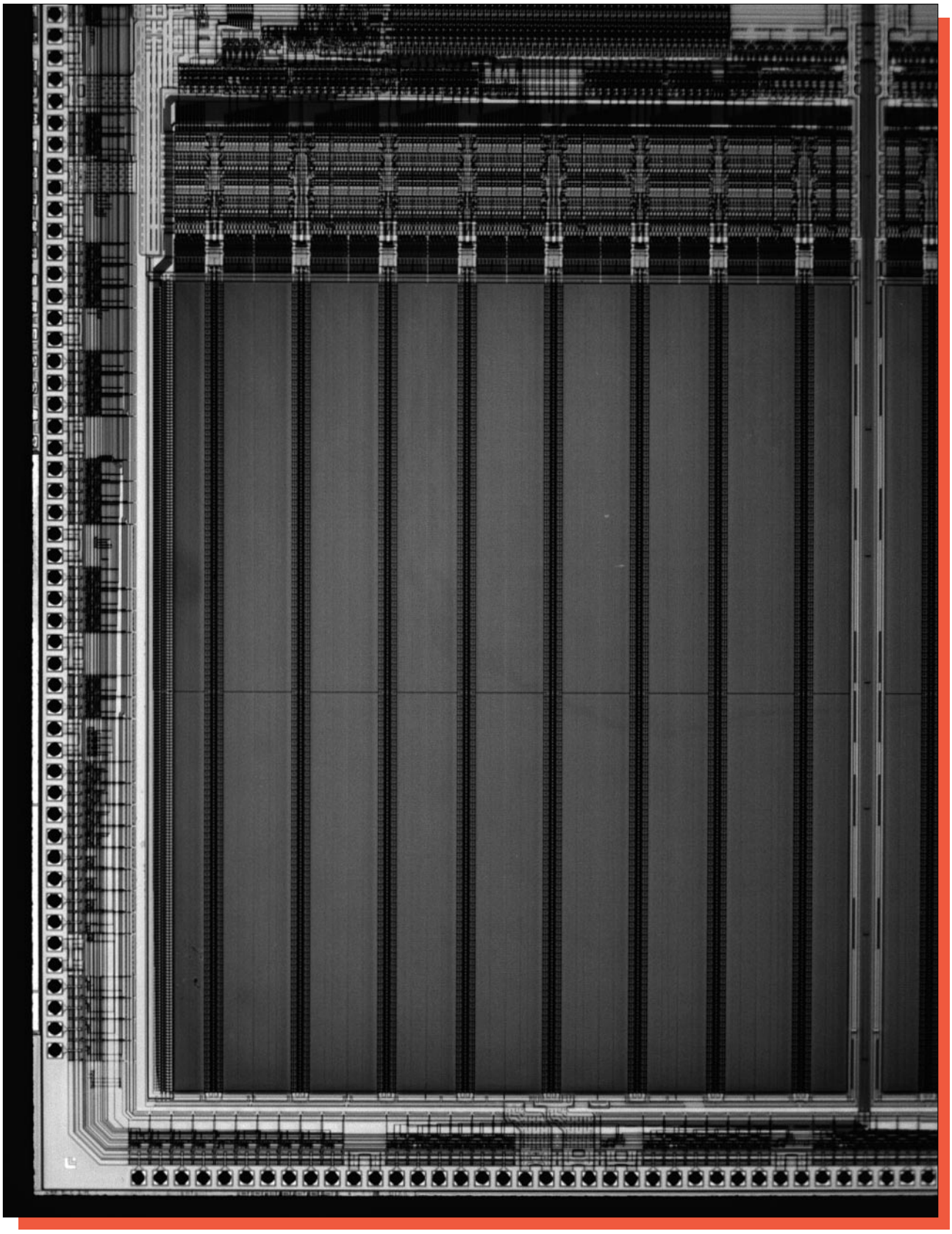


Figure 3b. Portion of the Analog Devices ADSP-21062-KS-160 die. Mag. 26x.

Figure 3c. Remaining portion of the Analog Devices ADSP-21062-KS-160 die. Mag. 26x.

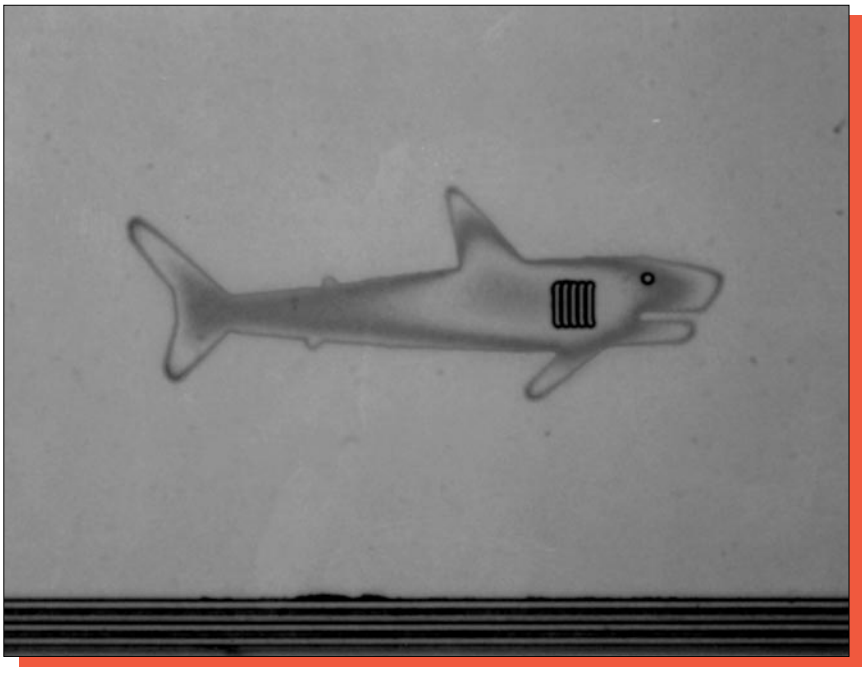


Figure 4. Optical views of die markings. Mag. 500x.

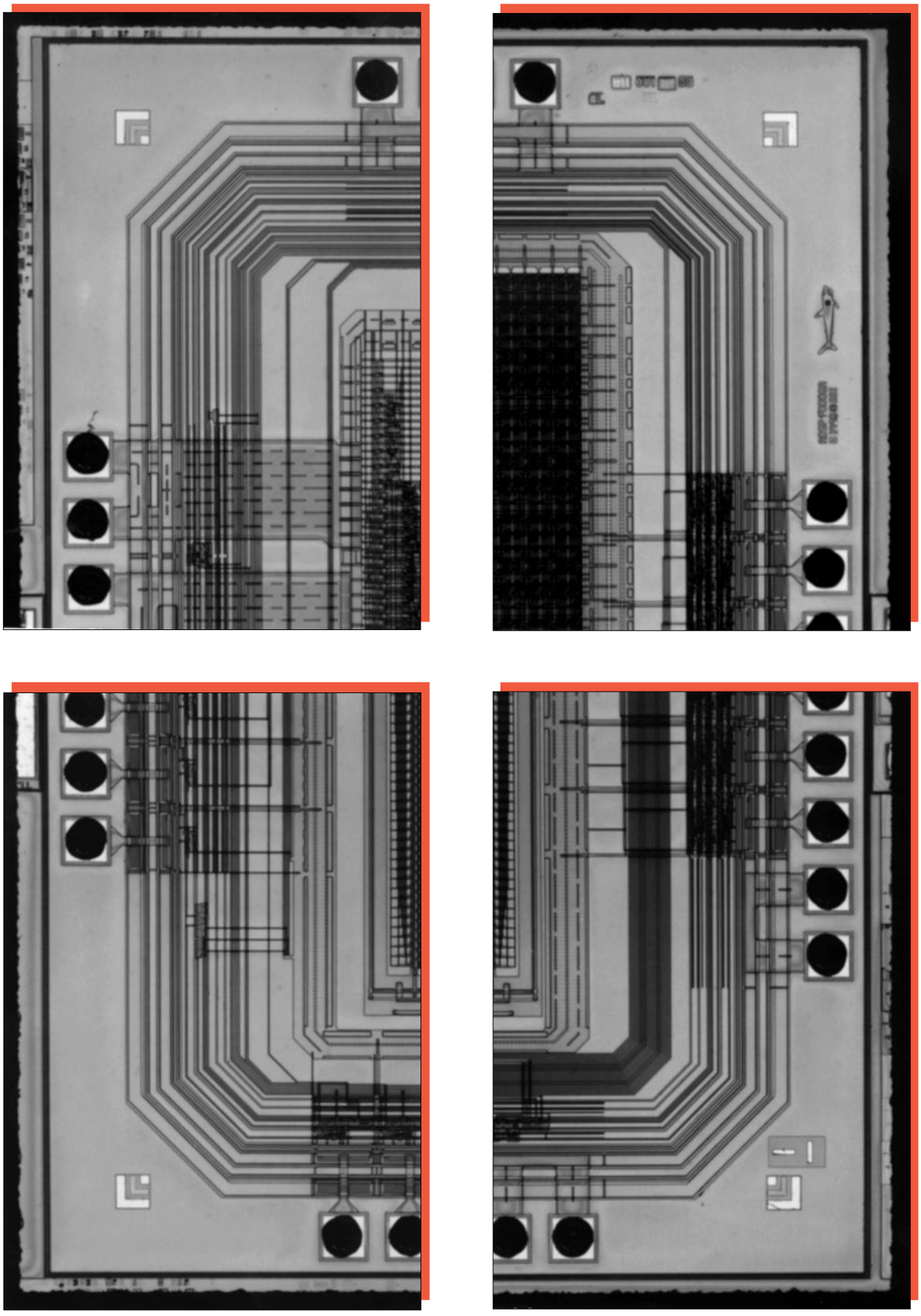


Figure 5. Optical views of die corners. Mag. 80x.

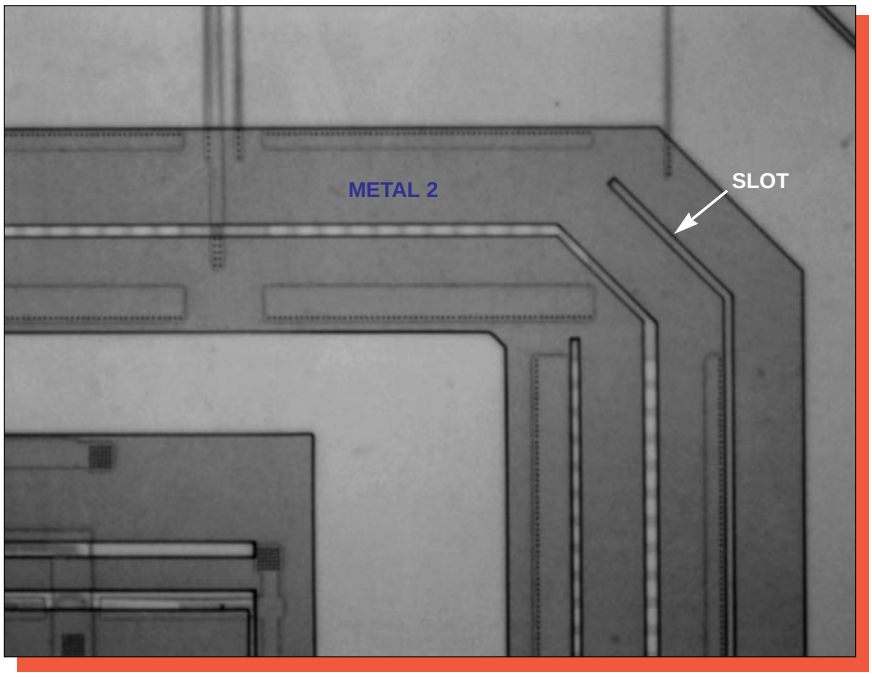
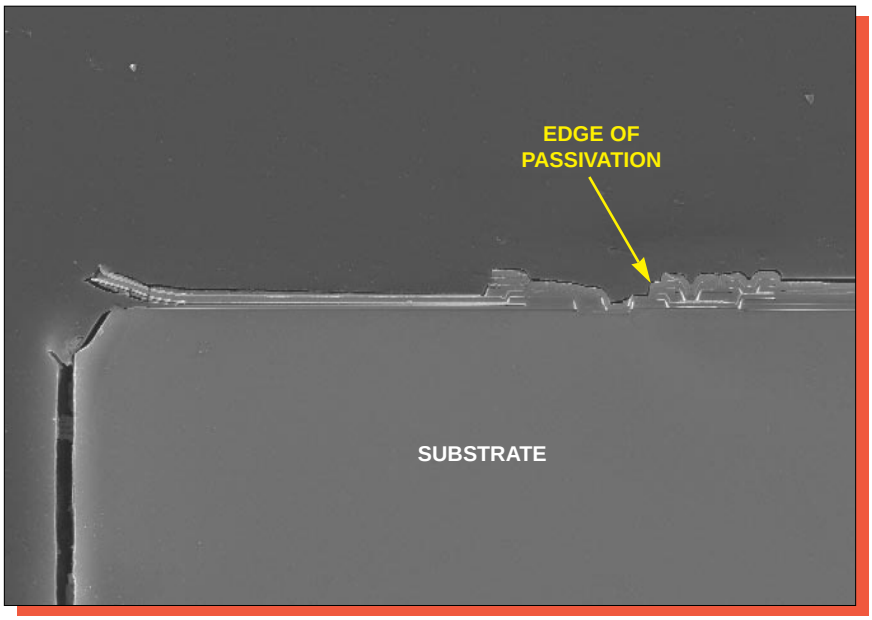
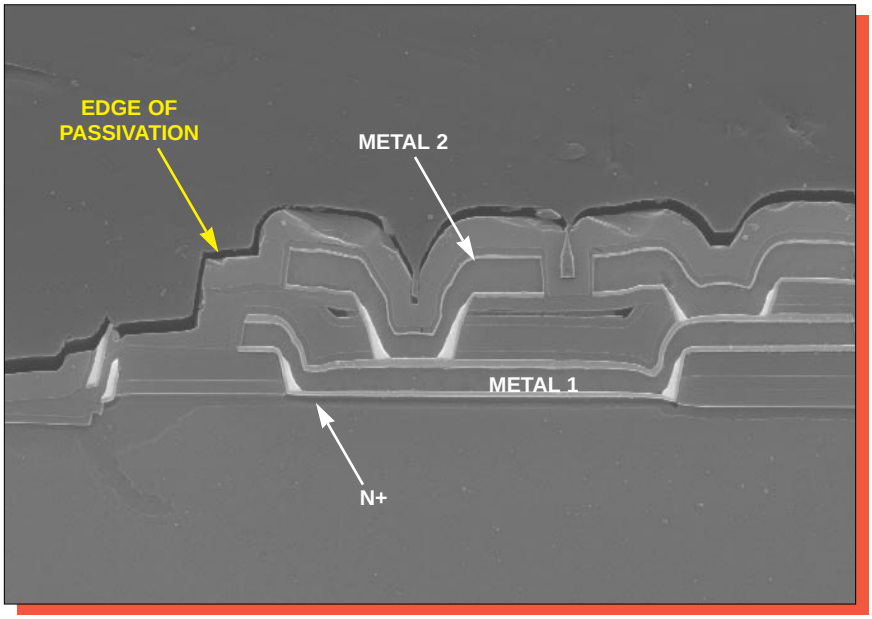


Figure 6. Optical views illustrating a slotted bus line and mask revision numbers. Mag. 400x.

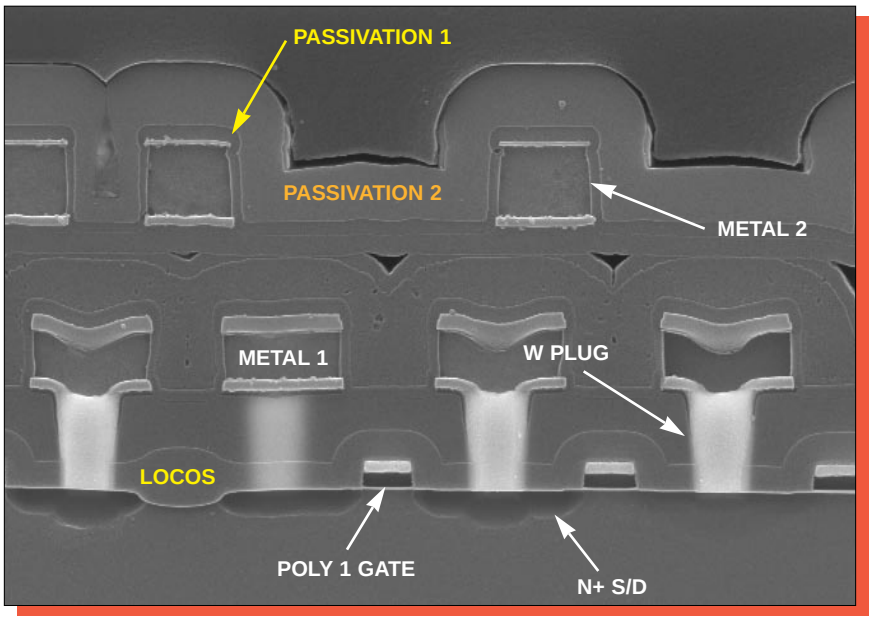


Mag. 1200x



Mag. 6400x

Figure 7. SEM section views of the die edge seal.



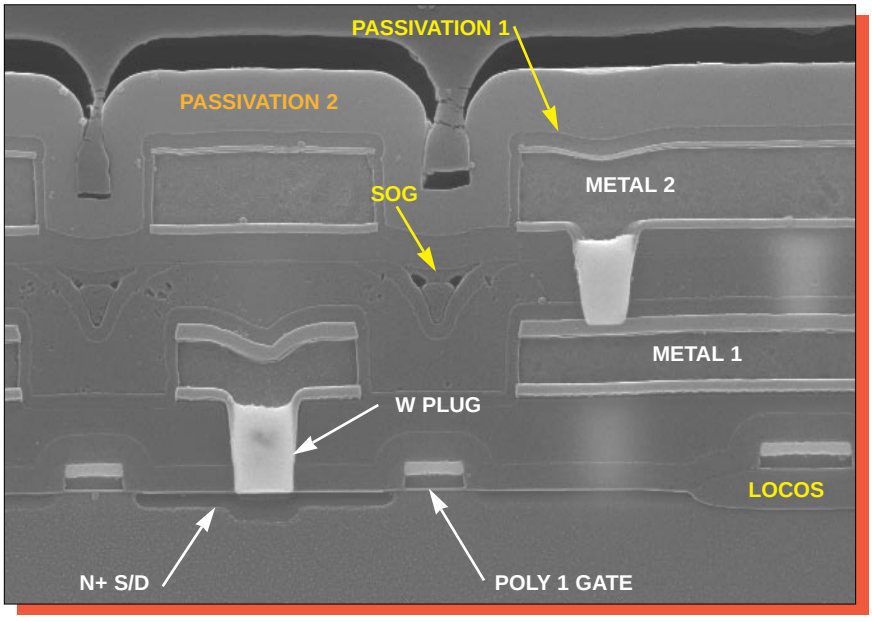
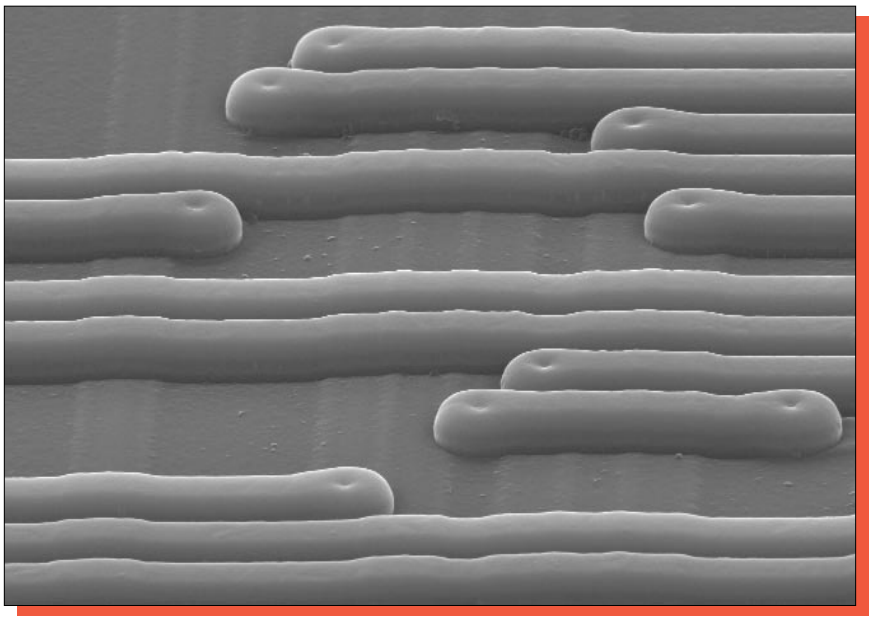
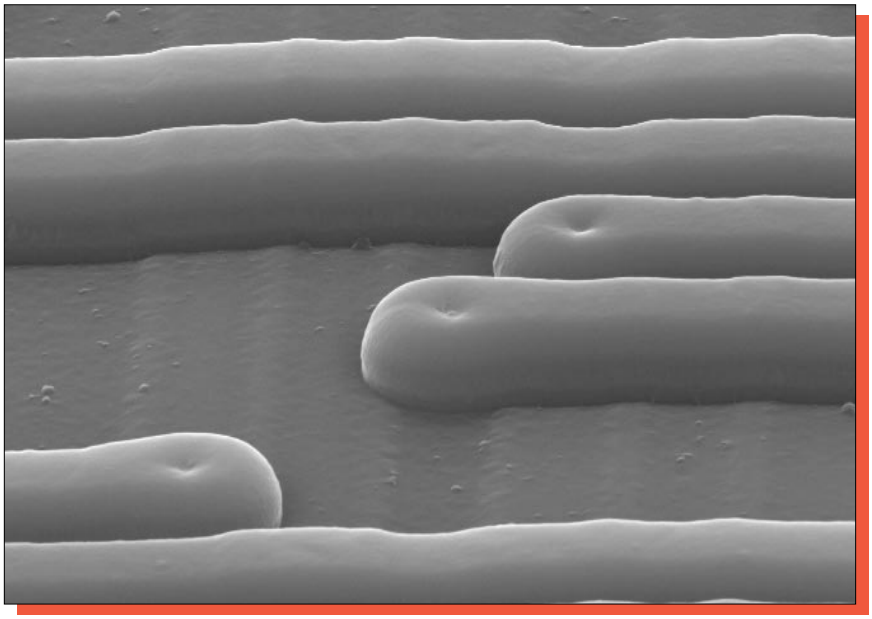


Figure 8. SEM section views illustrating general structure. Mag. 13,000x.

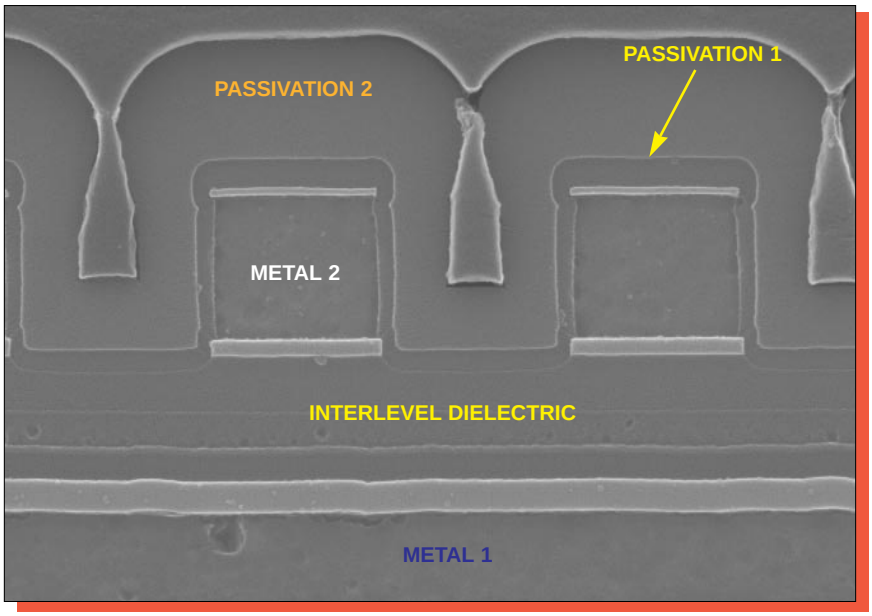


Mag. 4800x

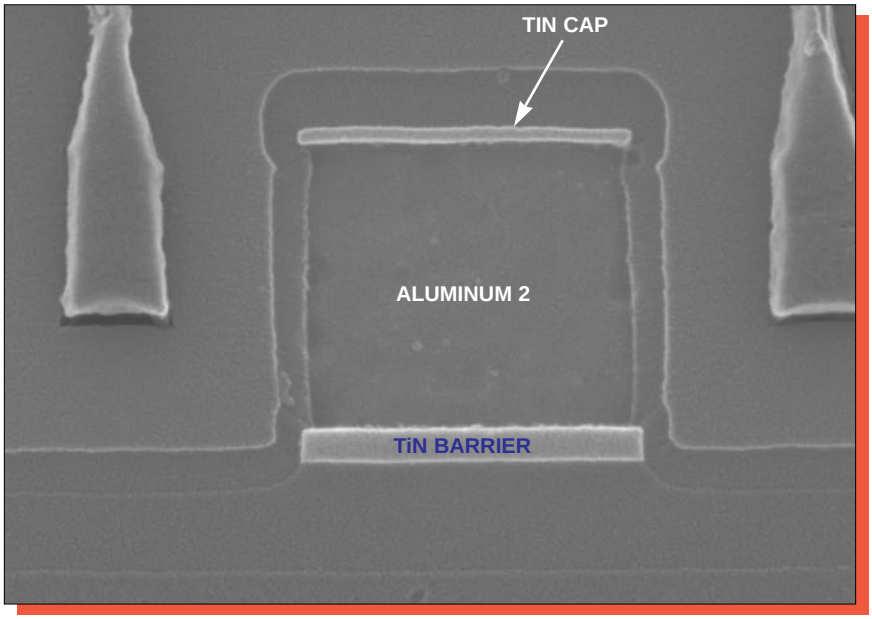


Mag. 9600x

Figure 9. SEM views illustrating final passivation. 60°.

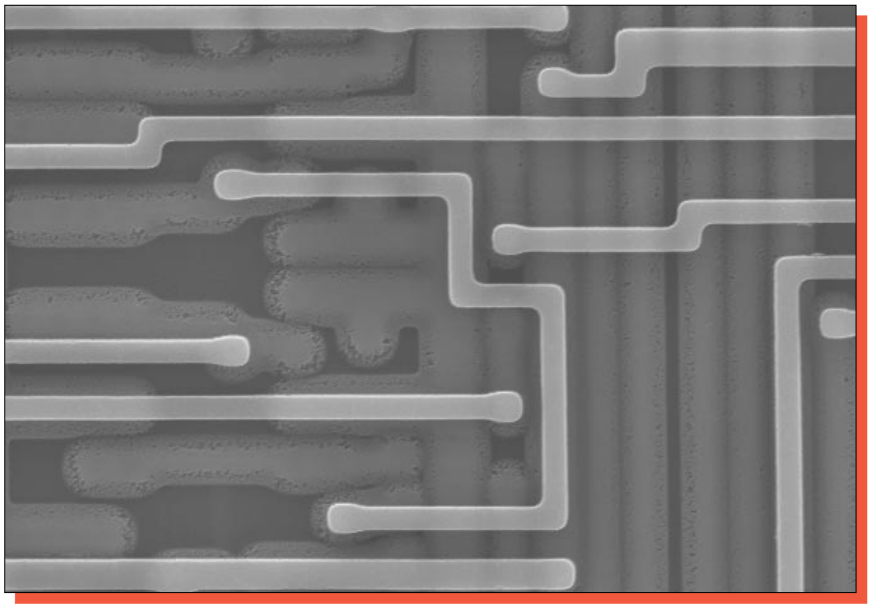


Mag. 26,000x

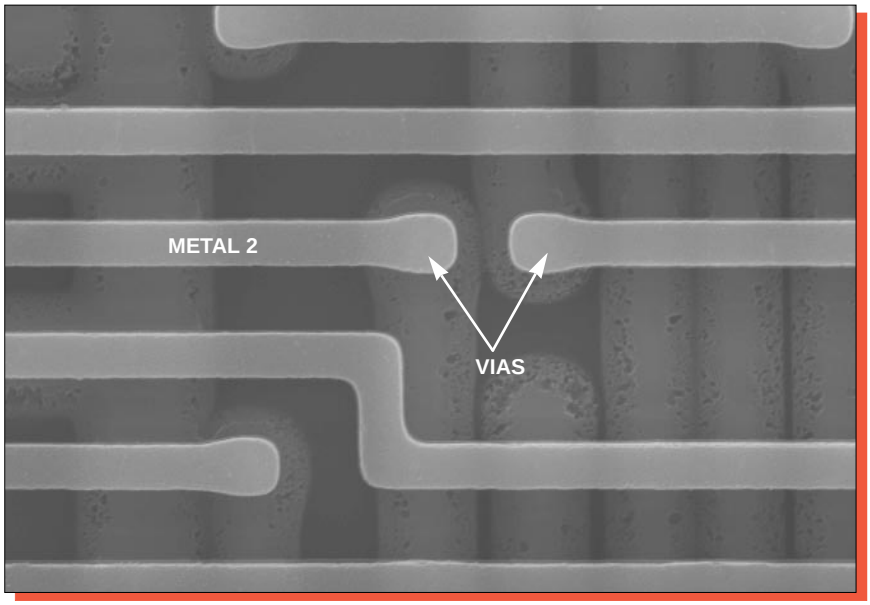


Mag. 52,000x

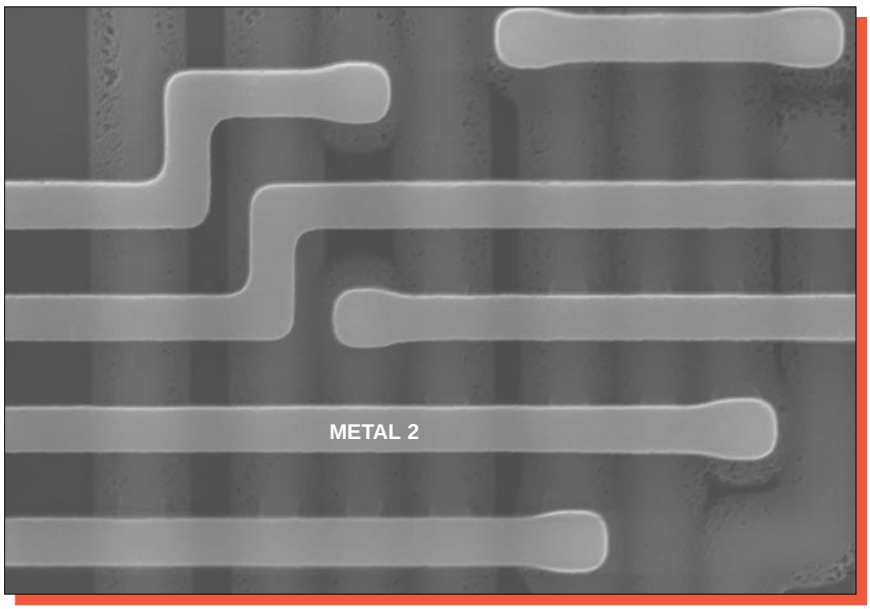
Figure 10. SEM section views illustrating metal 2 line profiles.



Mag. 3250x

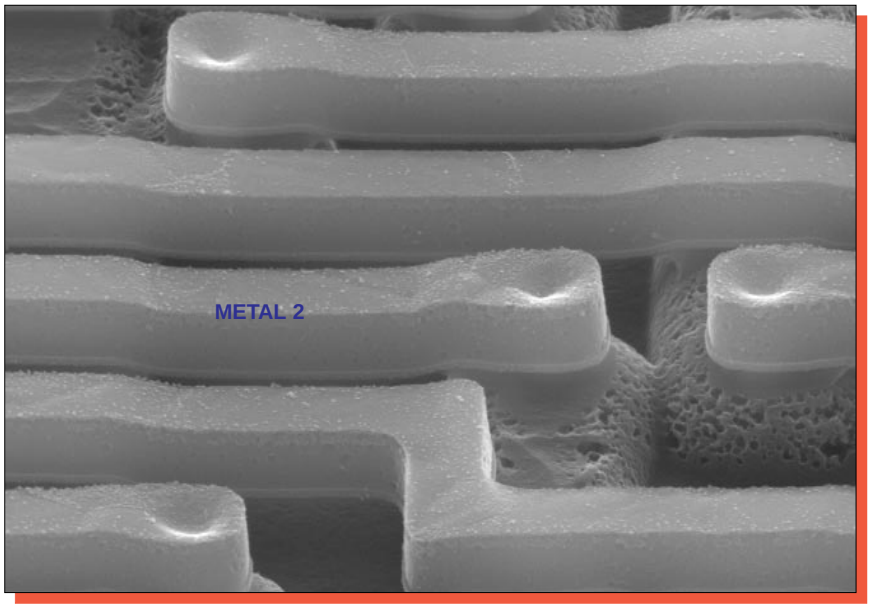


Mag. 6500x

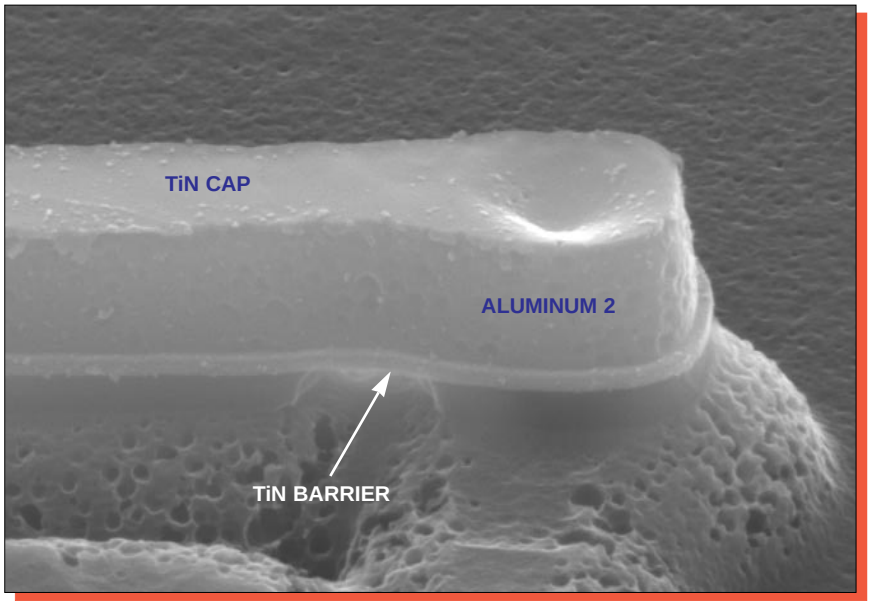


Mag. 6500x

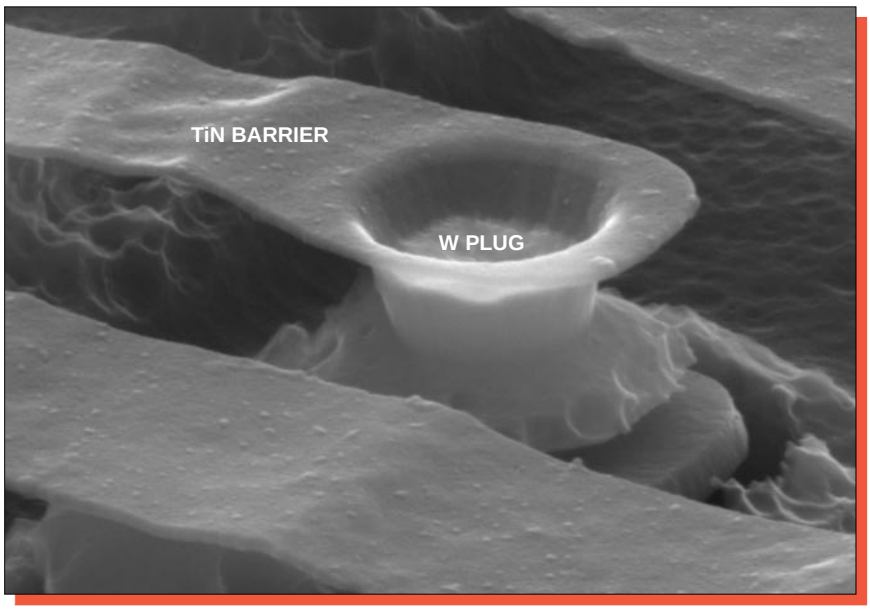
Figure 11. Topological SEM views of metal 2 patterning. 0°.



Mag. 12,400x

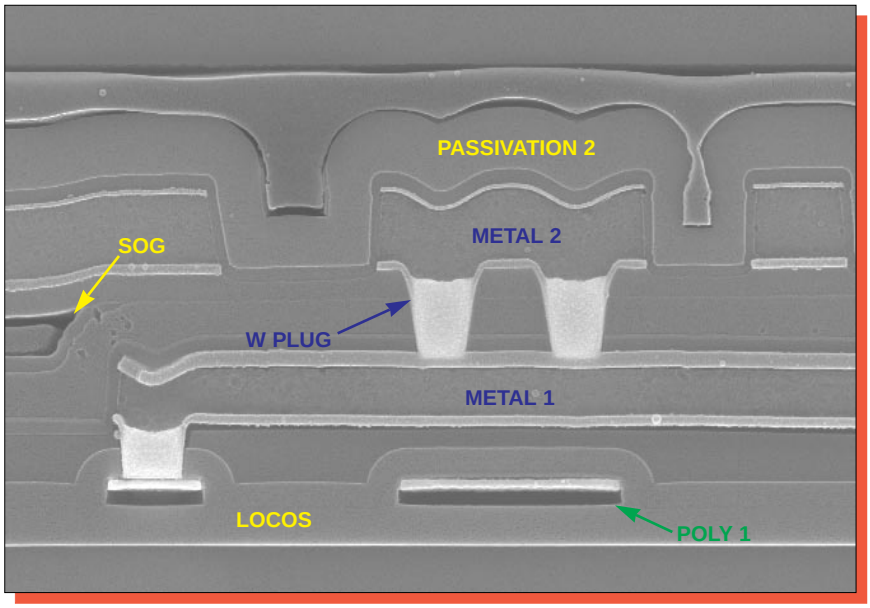


Mag. 26,000x

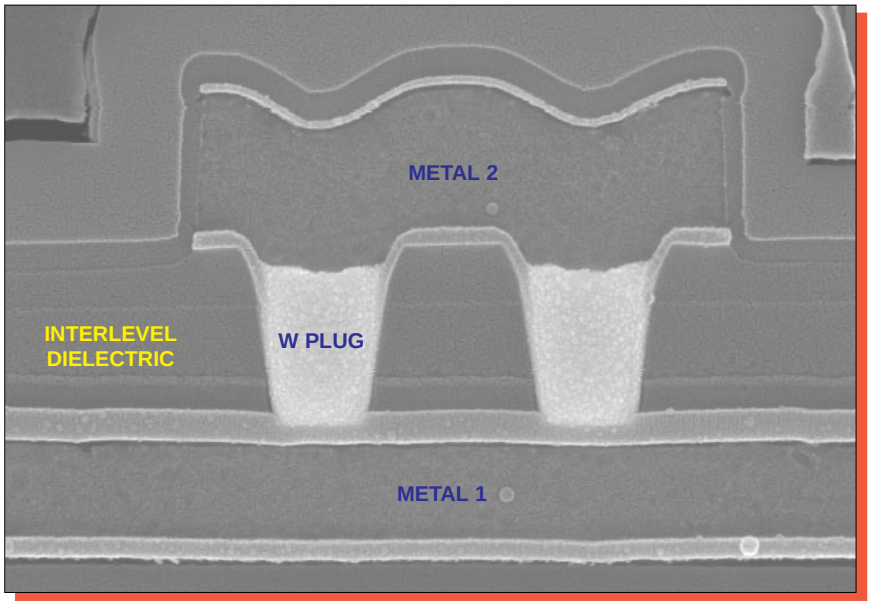


Mag. 40,000x

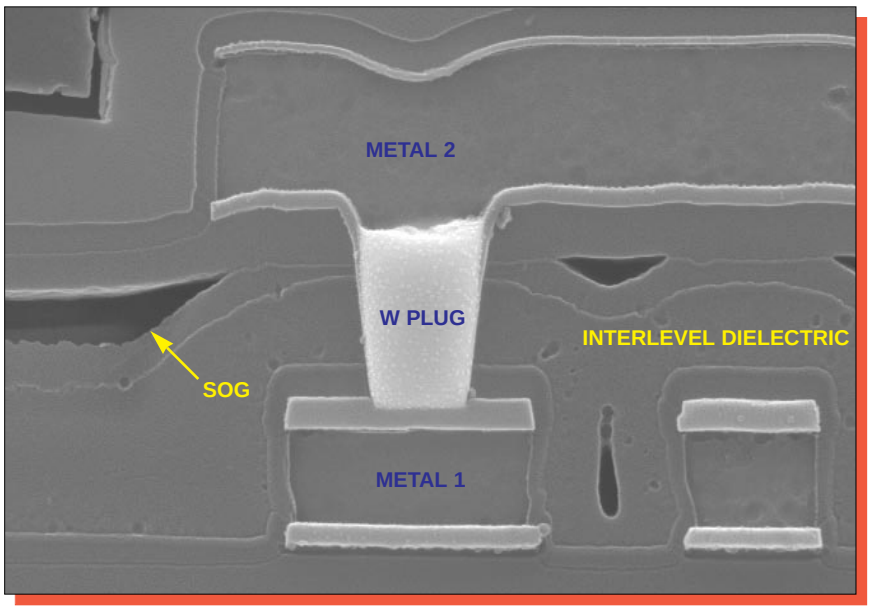
Figure 12. Perspective SEM views of metal 2 step coverage, barrier, and plug. 60°.



Mag. 13,000x

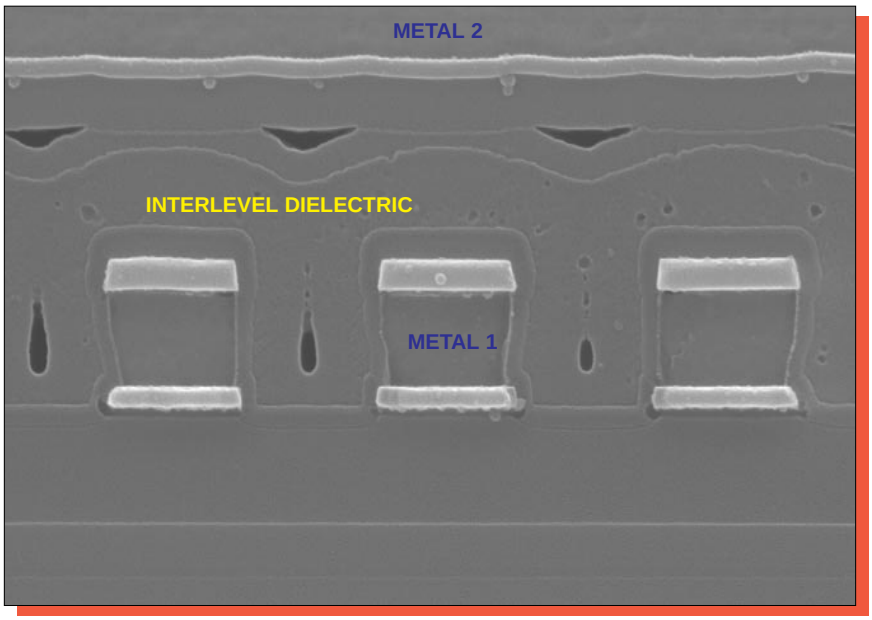


Mag. 26,000x

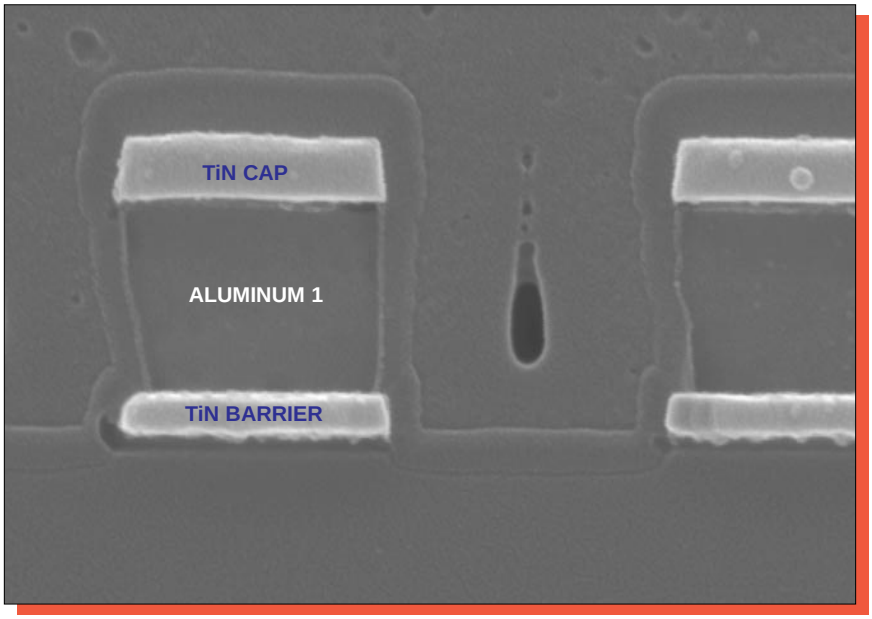


Mag. 26,000x

Figure 13. SEM section views of typical vias.



Mag. 26,000x



Mag. 52,000x

Figure 14. SEM section views of metal 1 line profiles.

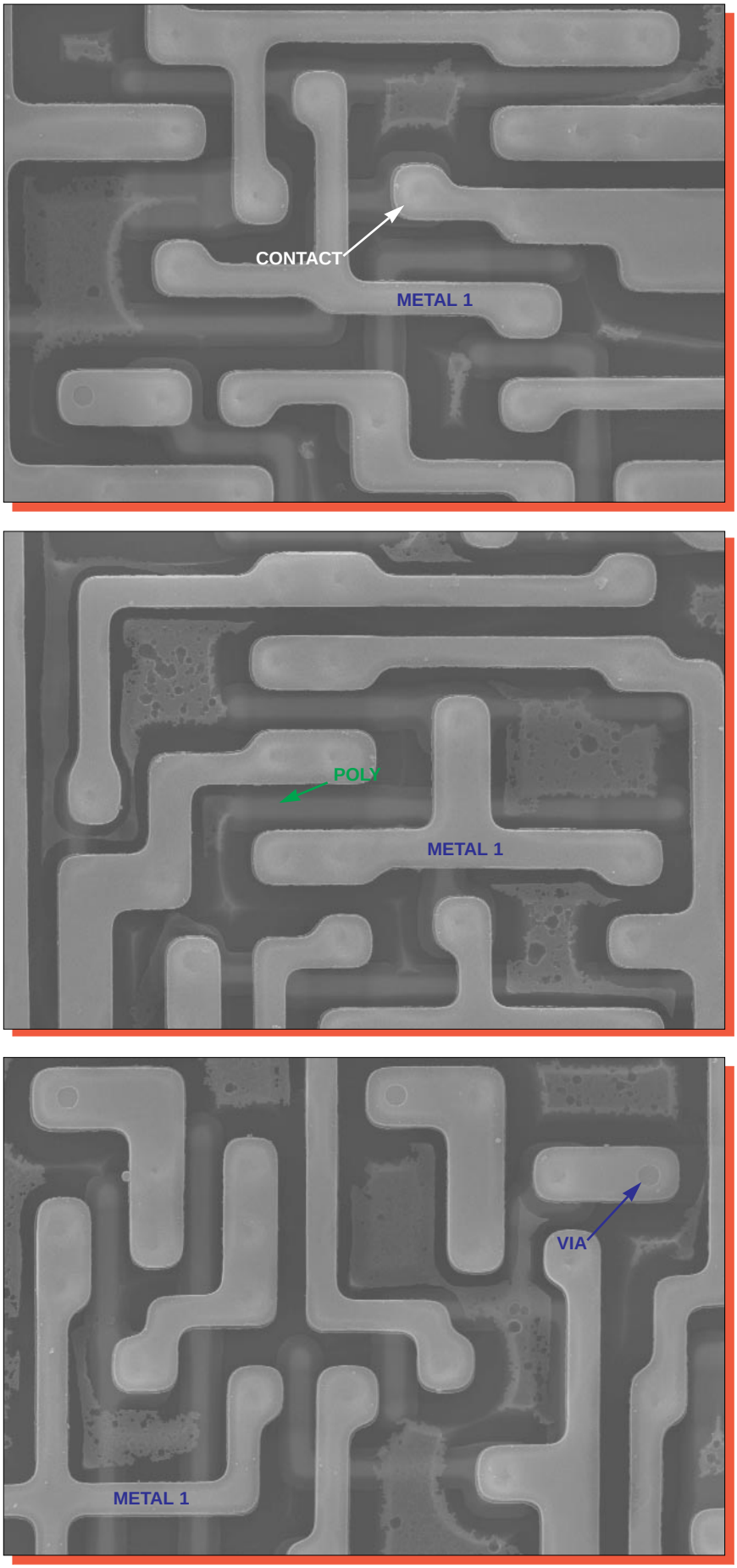
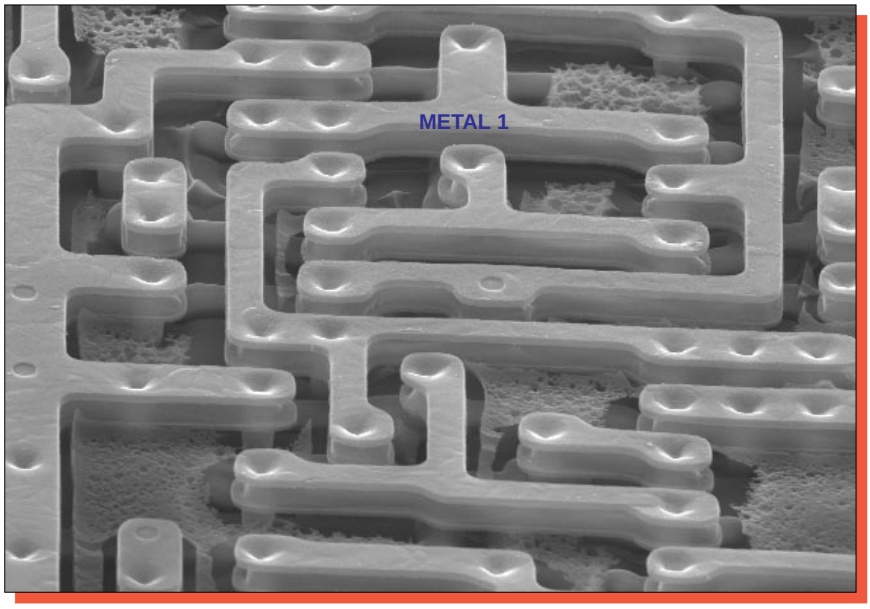
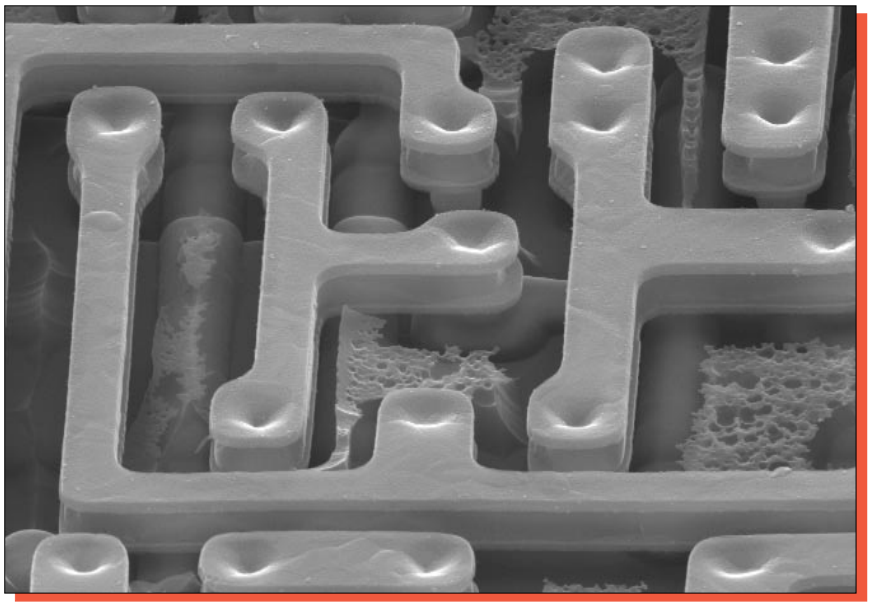


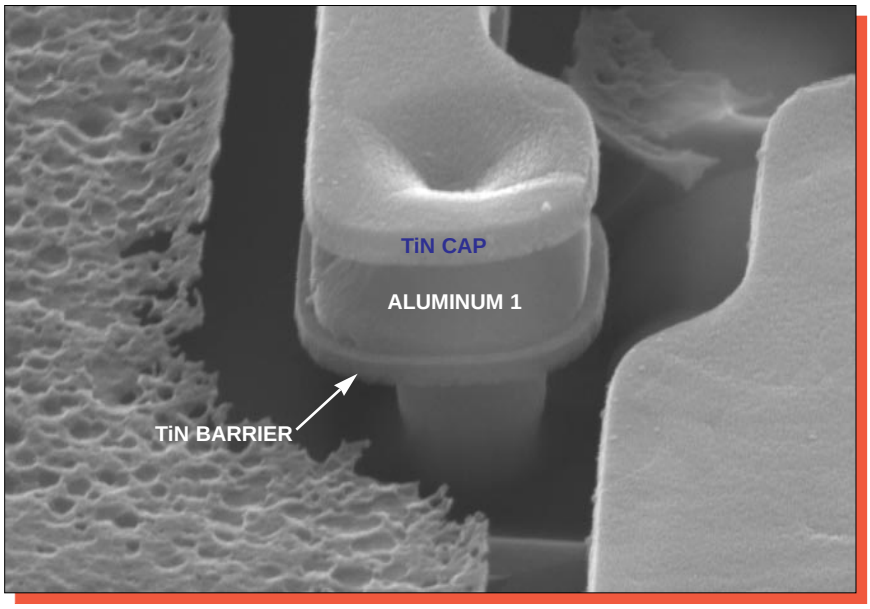
Figure 15. Topological SEM views of metal 1 patterning. Mag. 6500x, 0°.



Mag. 6500x

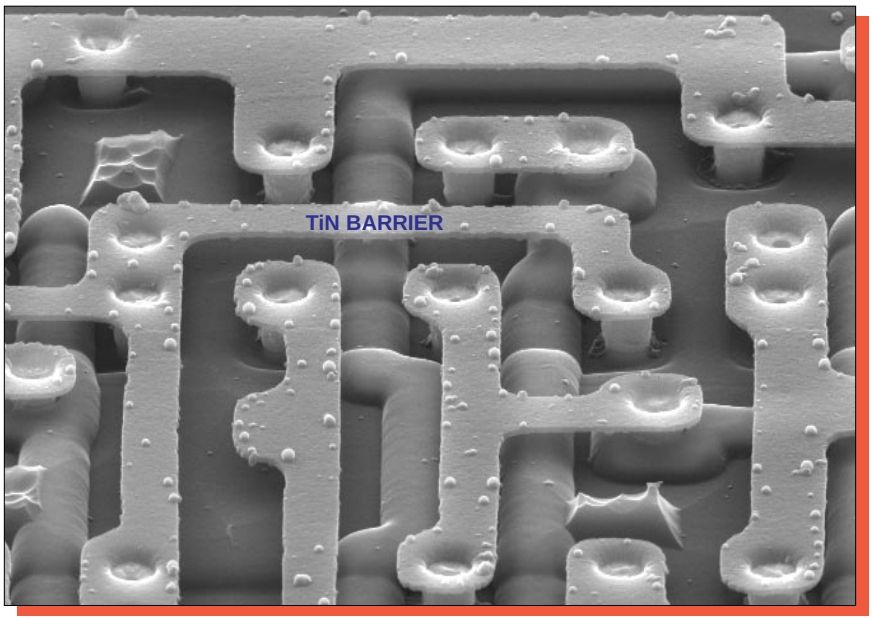


Mag. 10,000x

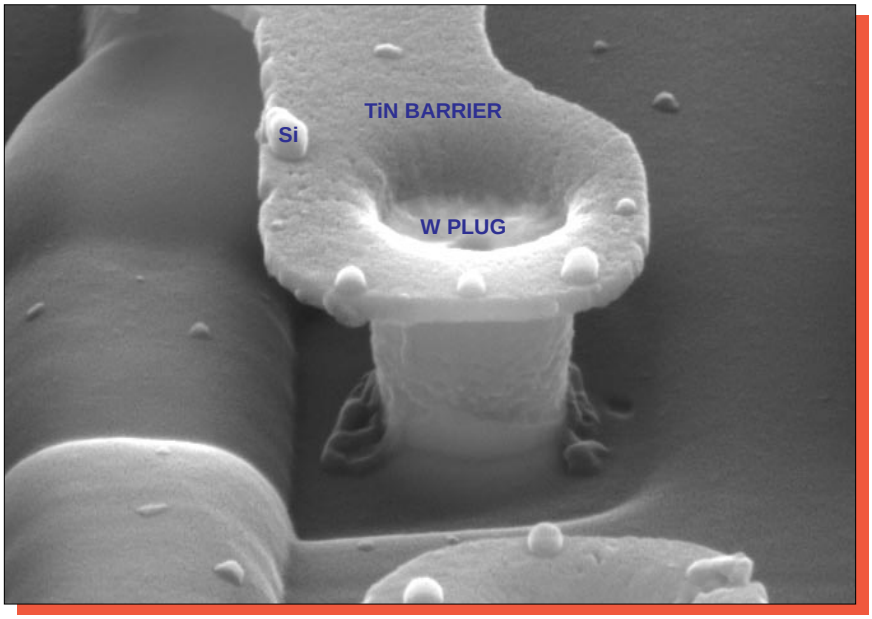


Mag. 30,000x

Figure 16. Perspective SEM views of metal 1 step coverage. 60°.



Mag. 10,000x



Mag. 40,000x

Figure 17. Perspective SEM views of metal 1 barrier and plugs. 60°.

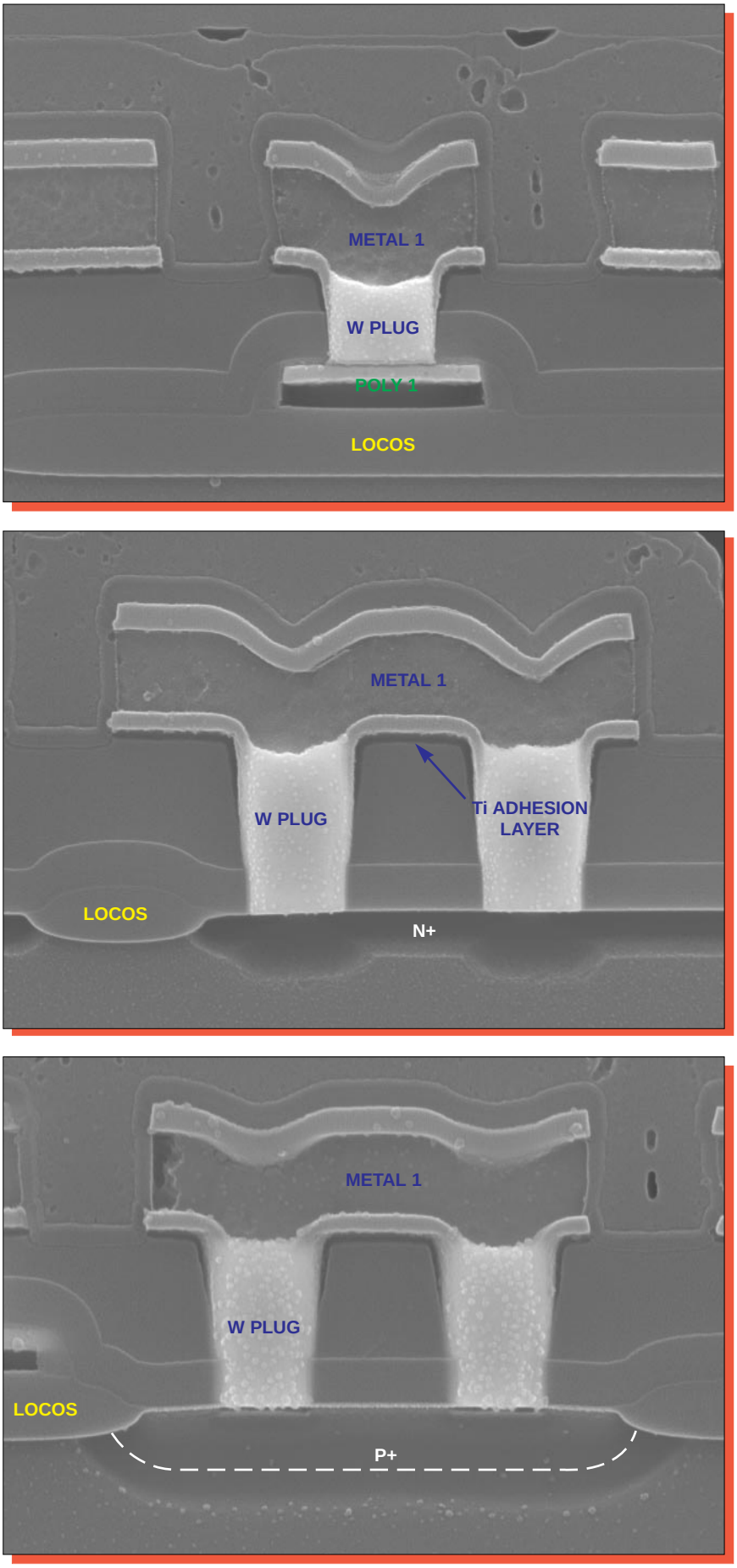
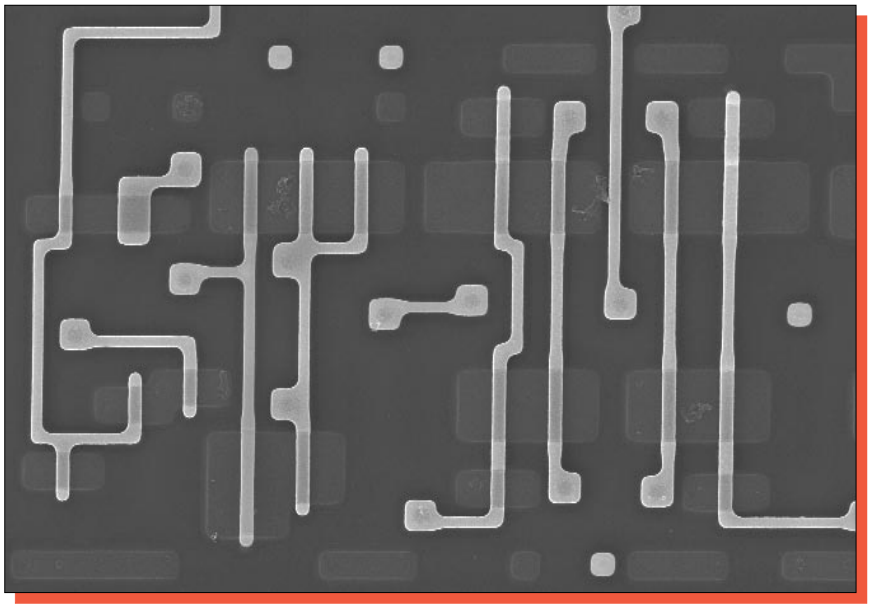
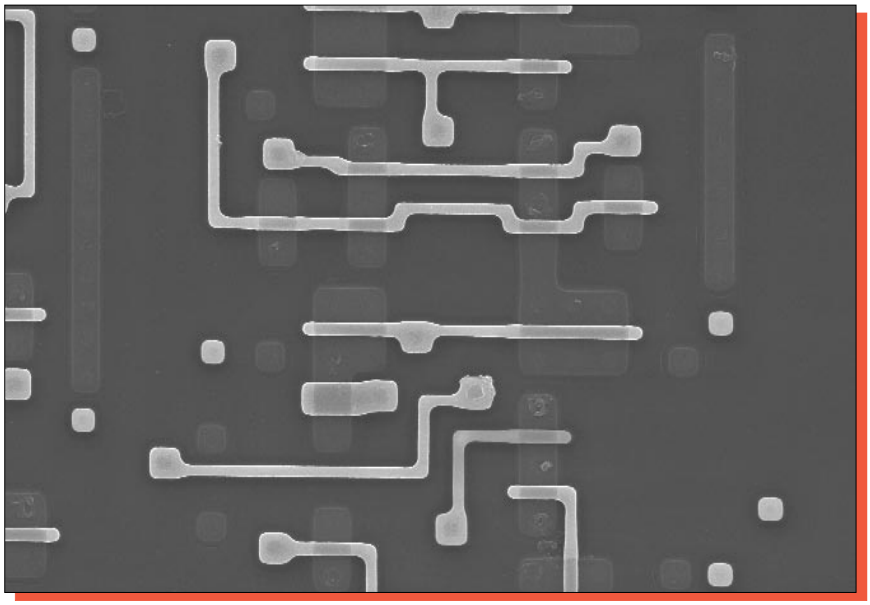


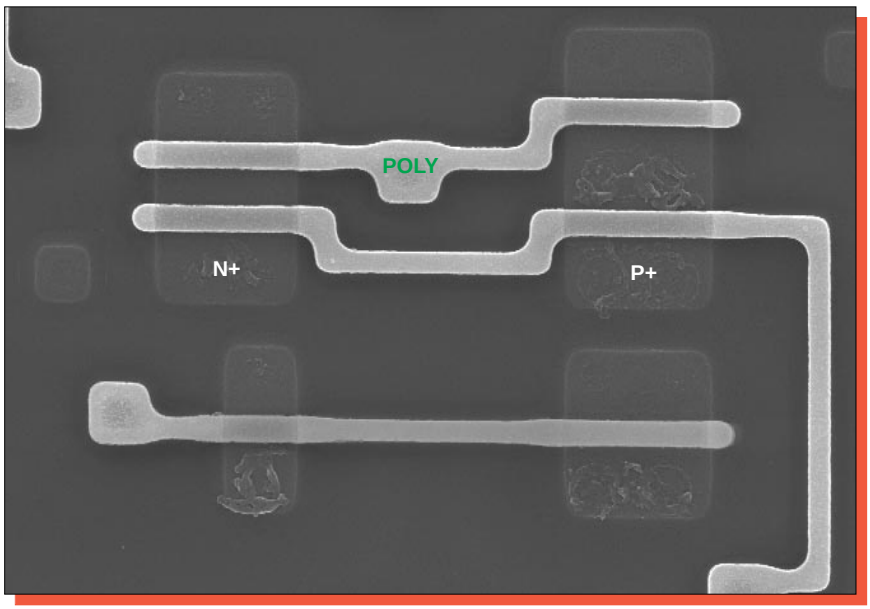
Figure 18. SEM section views illustrating typical metal 1 contacts. Mag. 26,000x.



Mag. 3200x

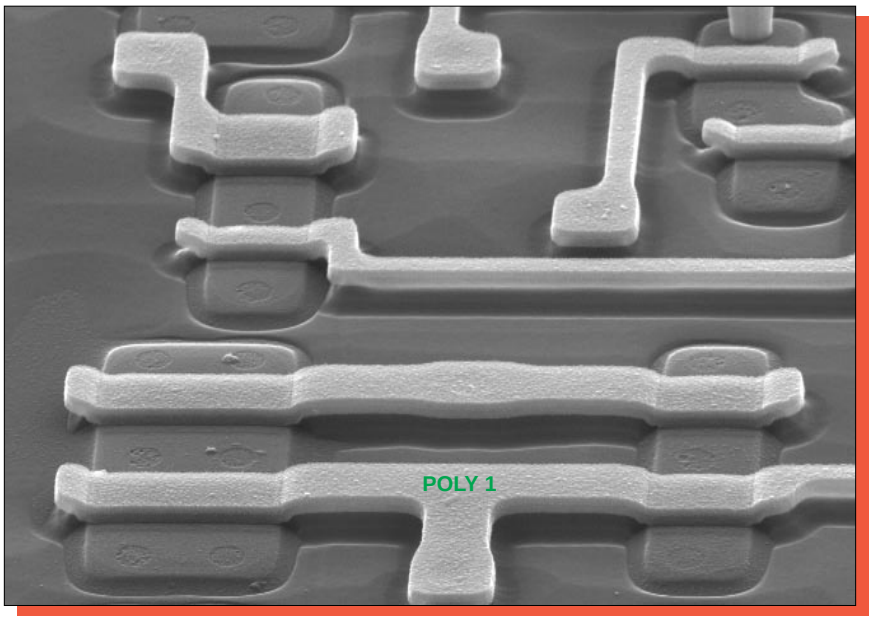


Mag. 3200x

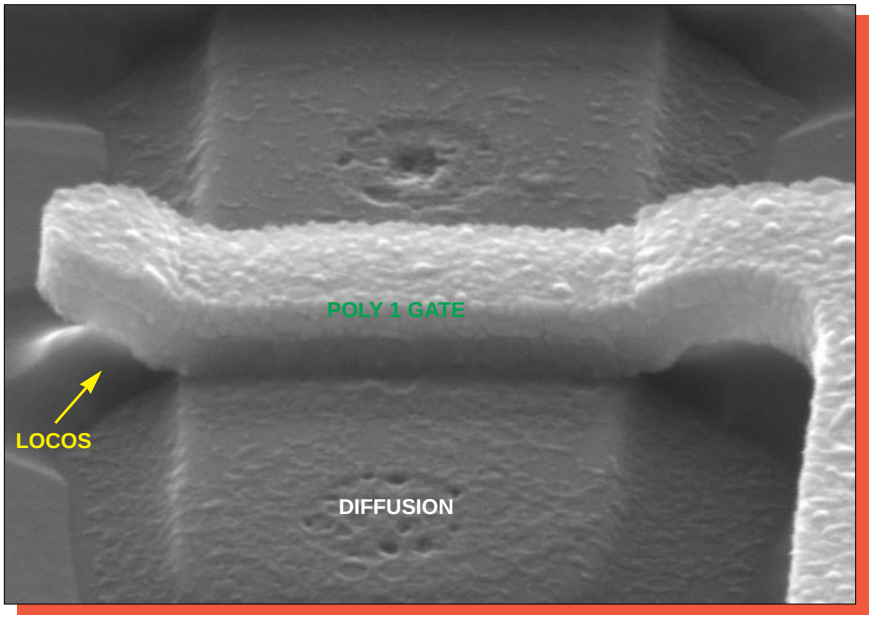


Mag. 6500x

Figure 19. Topological SEM views of poly 1 patterning. 0°.

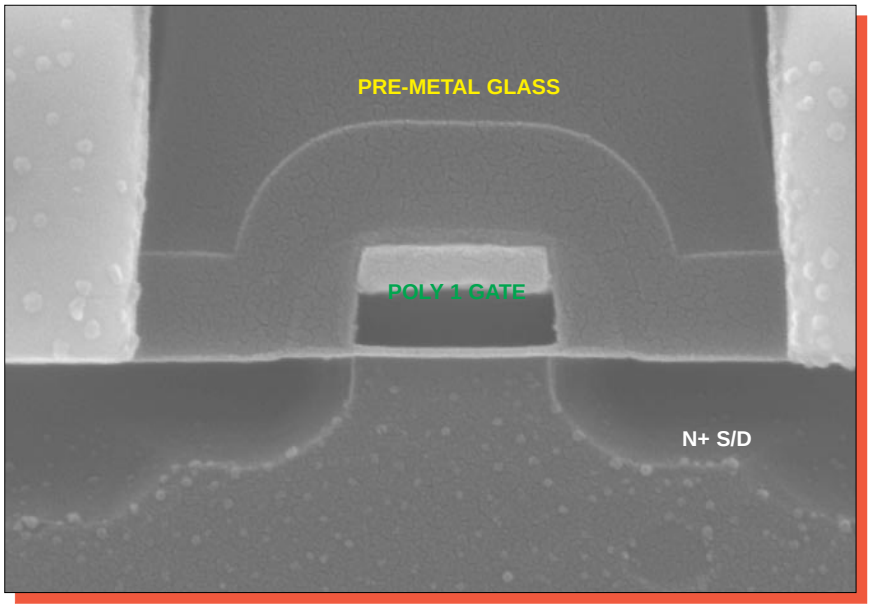


Mag. 9000x

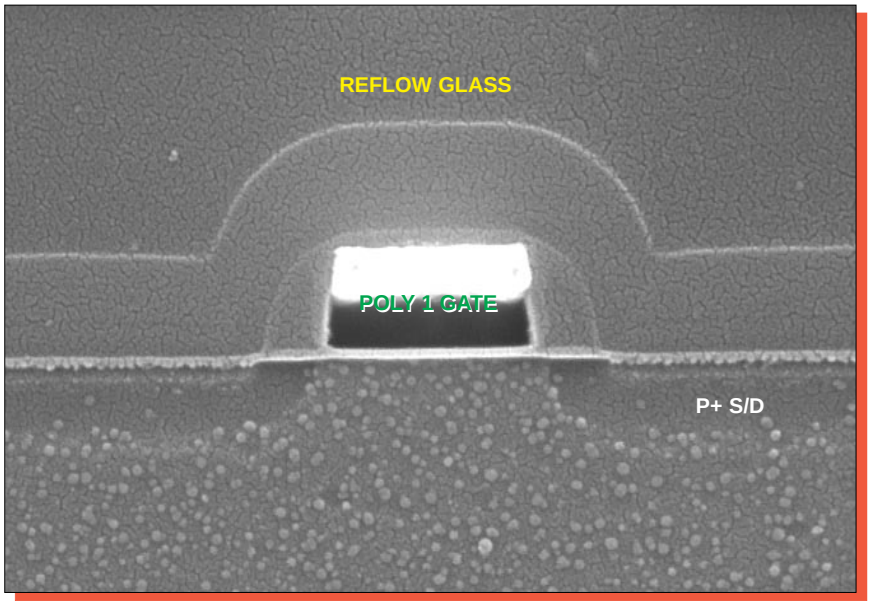


Mag. 40,000x

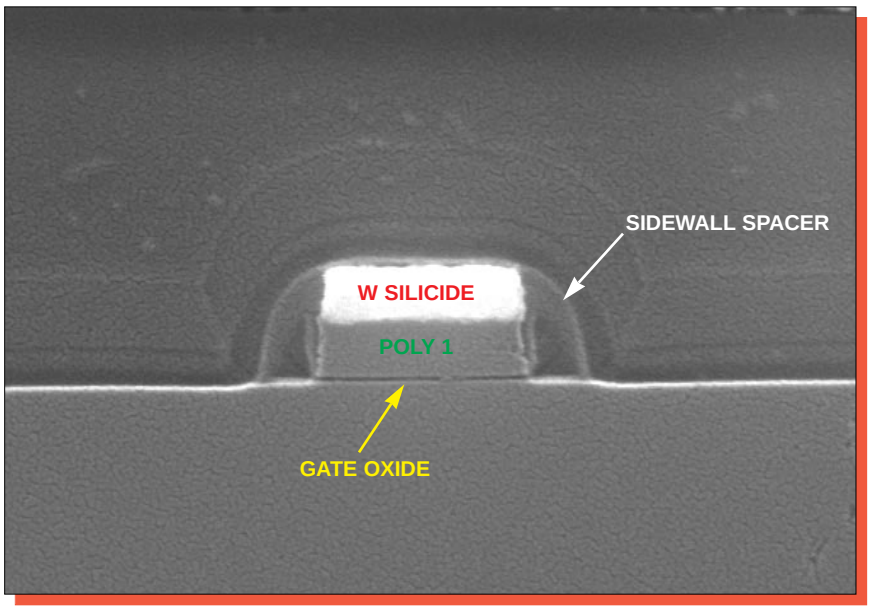
Figure 20. Perspective SEM views of poly 1 coverage. 60°.



N-channel



P-channel



glass etch

Figure 21. SEM section views of typical transistors. Mag. 52,000x.

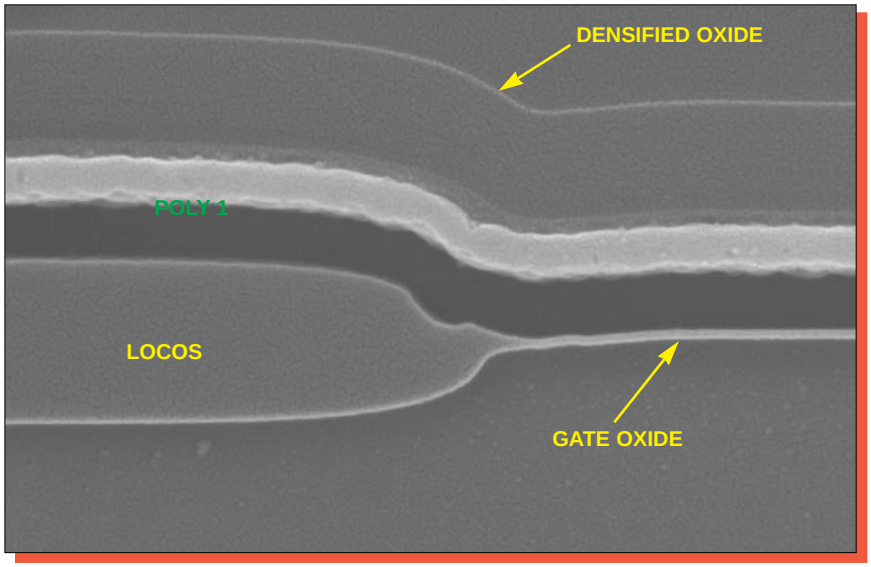
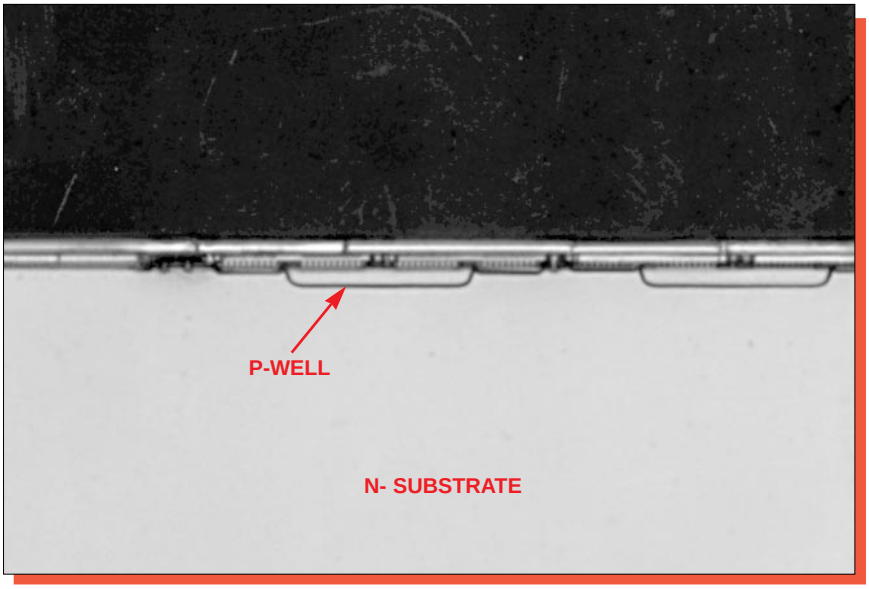
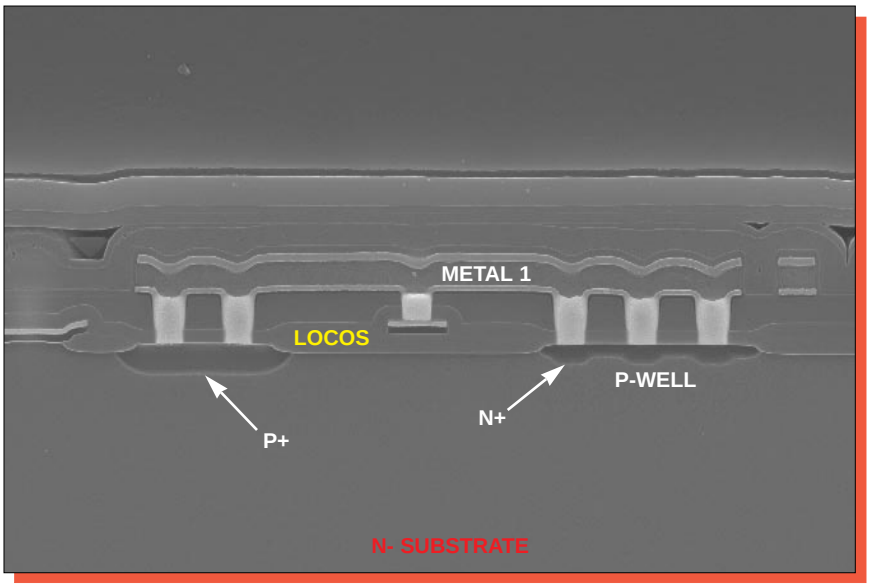


Figure 22. SEM section view of typical birdsbeak. Mag. 52,000x.

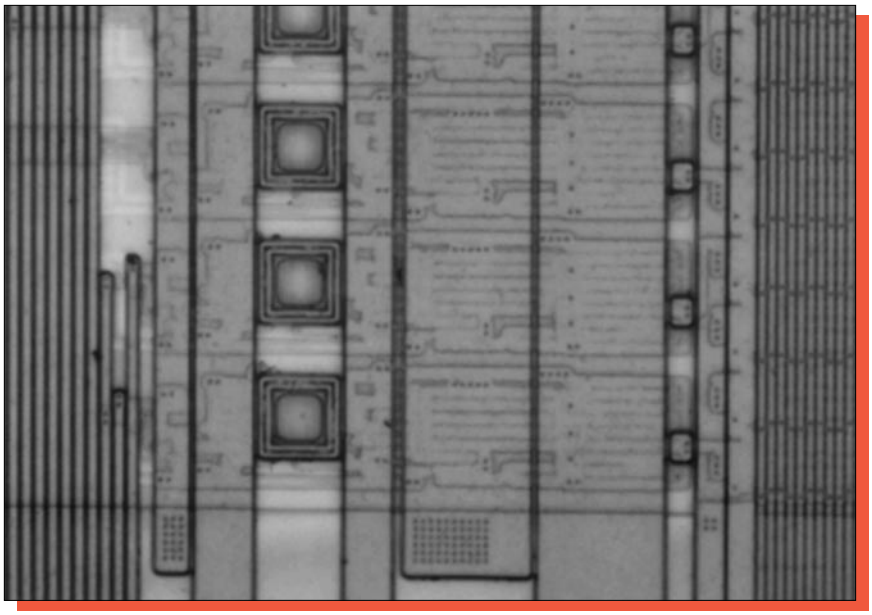


Mag. 800x

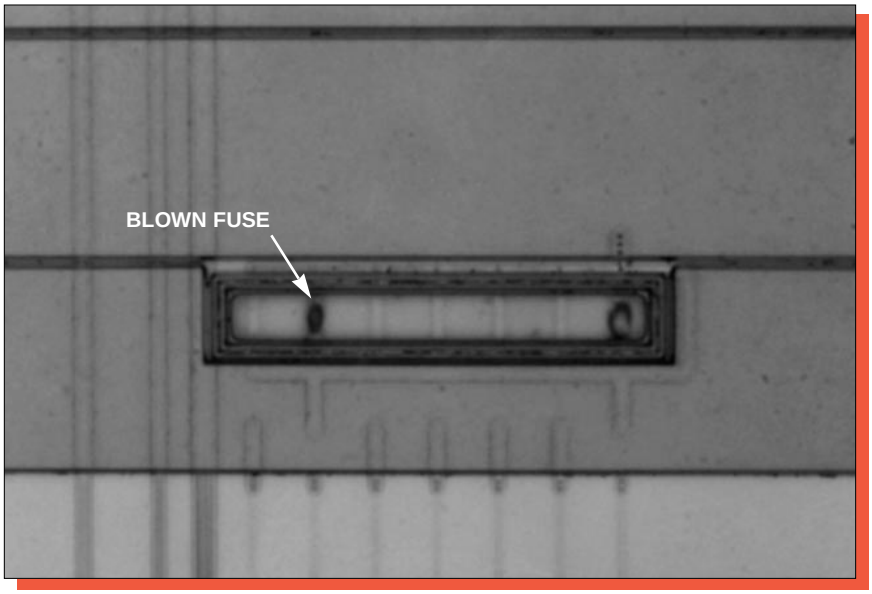


Mag. 6500x

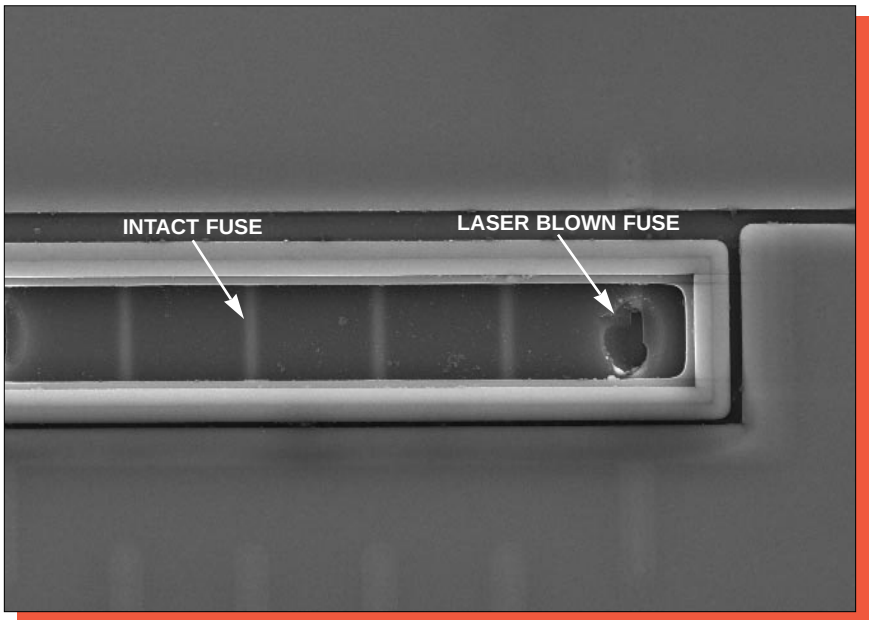
Figure 23. Section views illustrating well structure.



Mag. 800x

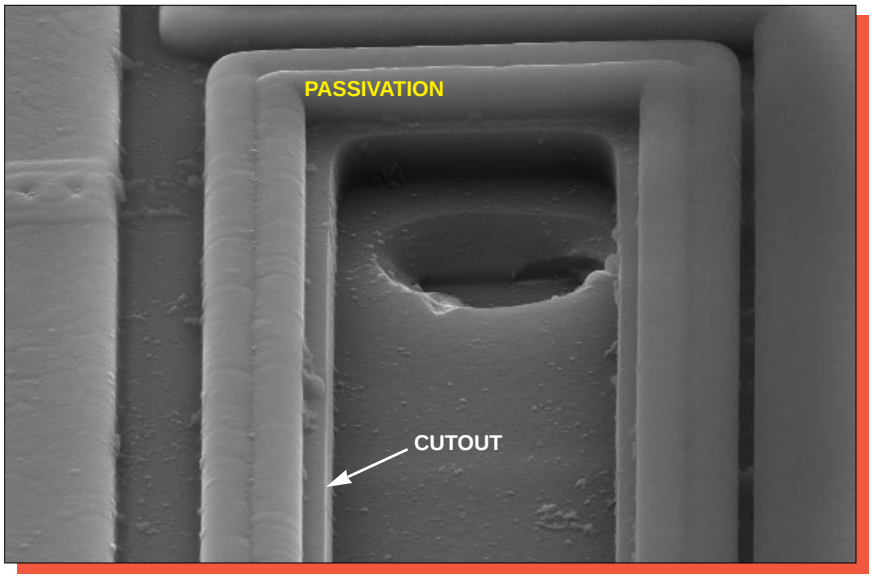


Mag. 800x

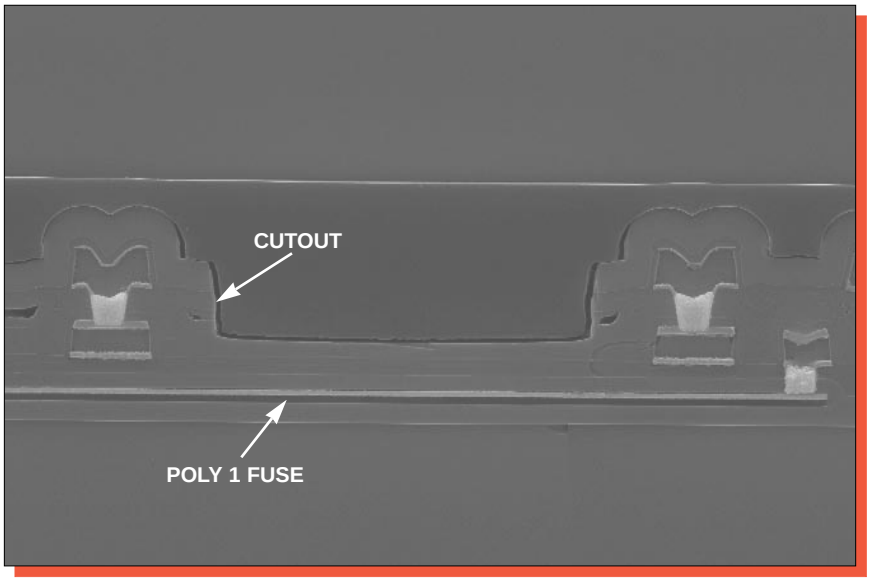


Mag. 1600x

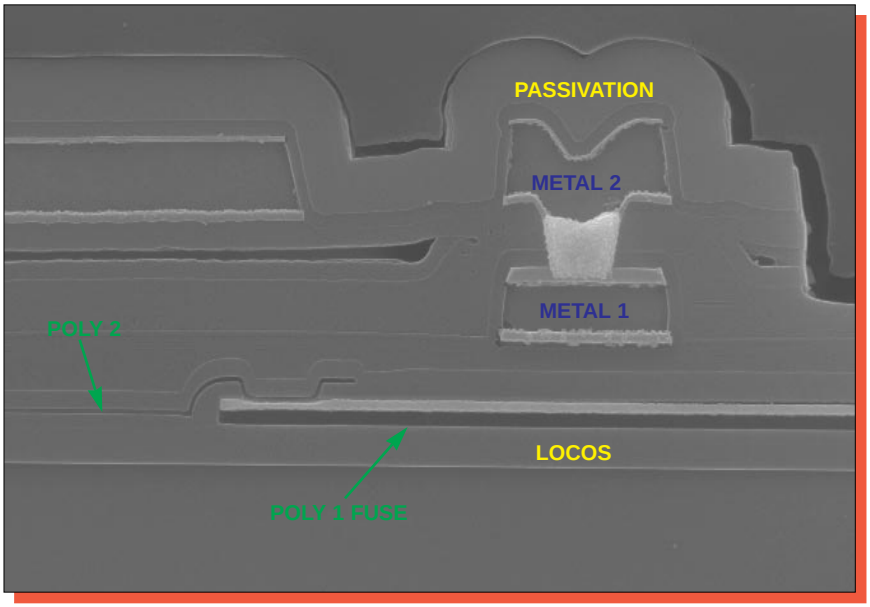
Figure 24. Optical and SEM views of typical fuses.



Mag. 4800x, 60°

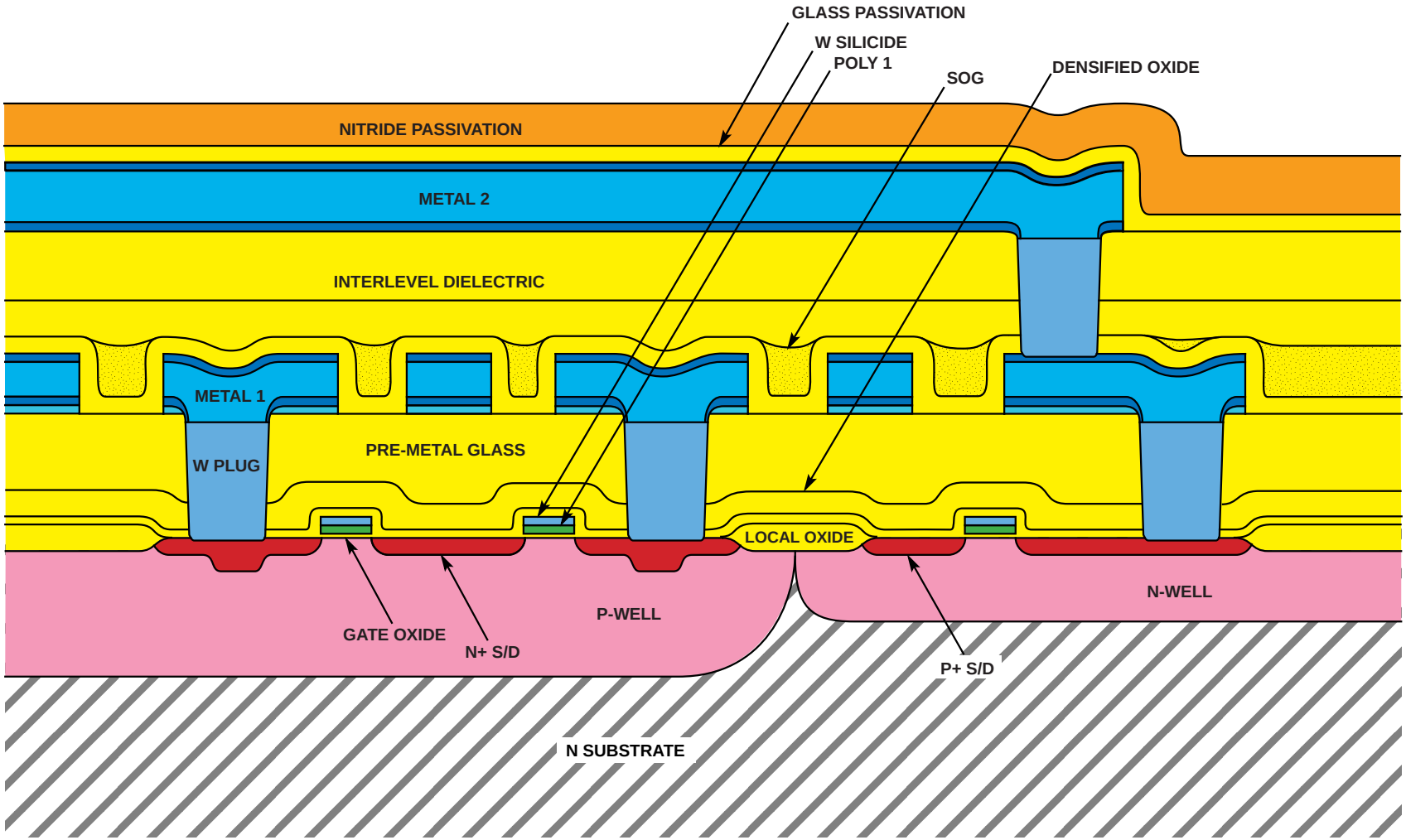


Mag. 6500x



Mag. 13,000x

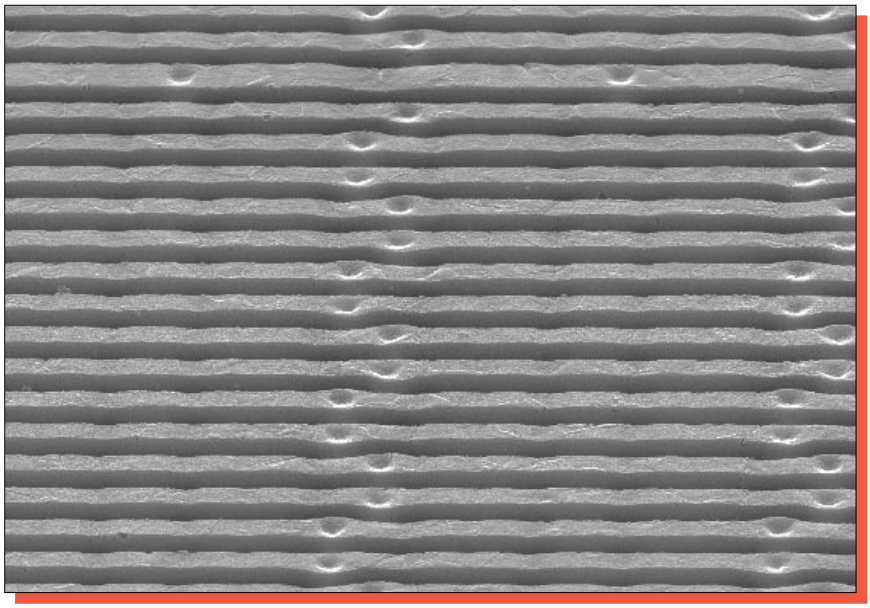
Figure 25. Perspective and cross-section SEM views of typical fuses.



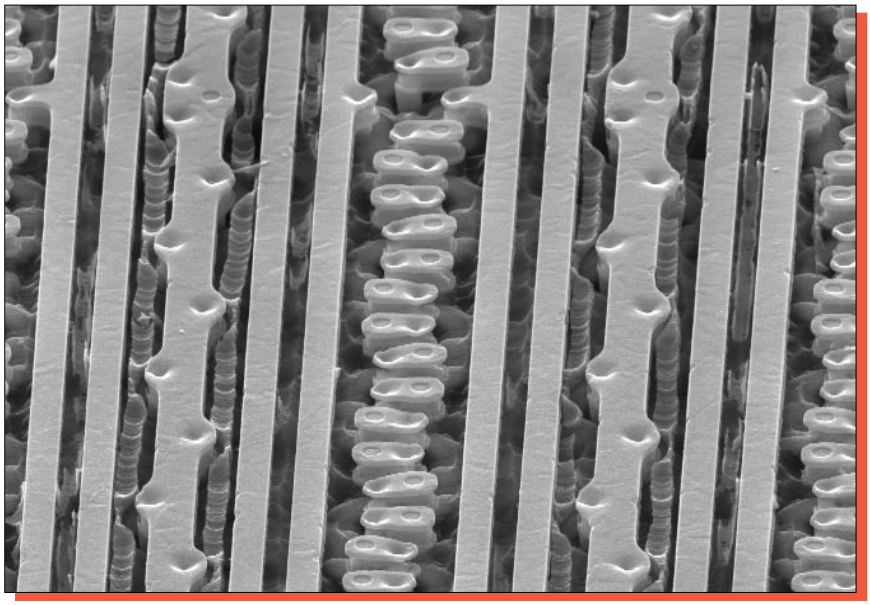
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

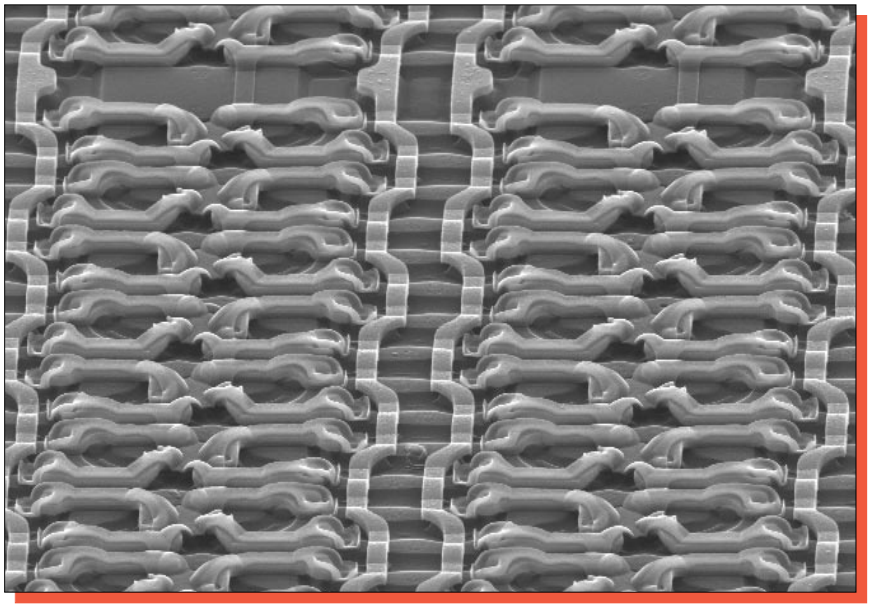
Figure 26. Color cross section drawing illustrating device structure.



metal 2



metal 1



poly

Figure 27. Perspective SEM views of the SRAM cell array. Mag. 5000x, 60°.

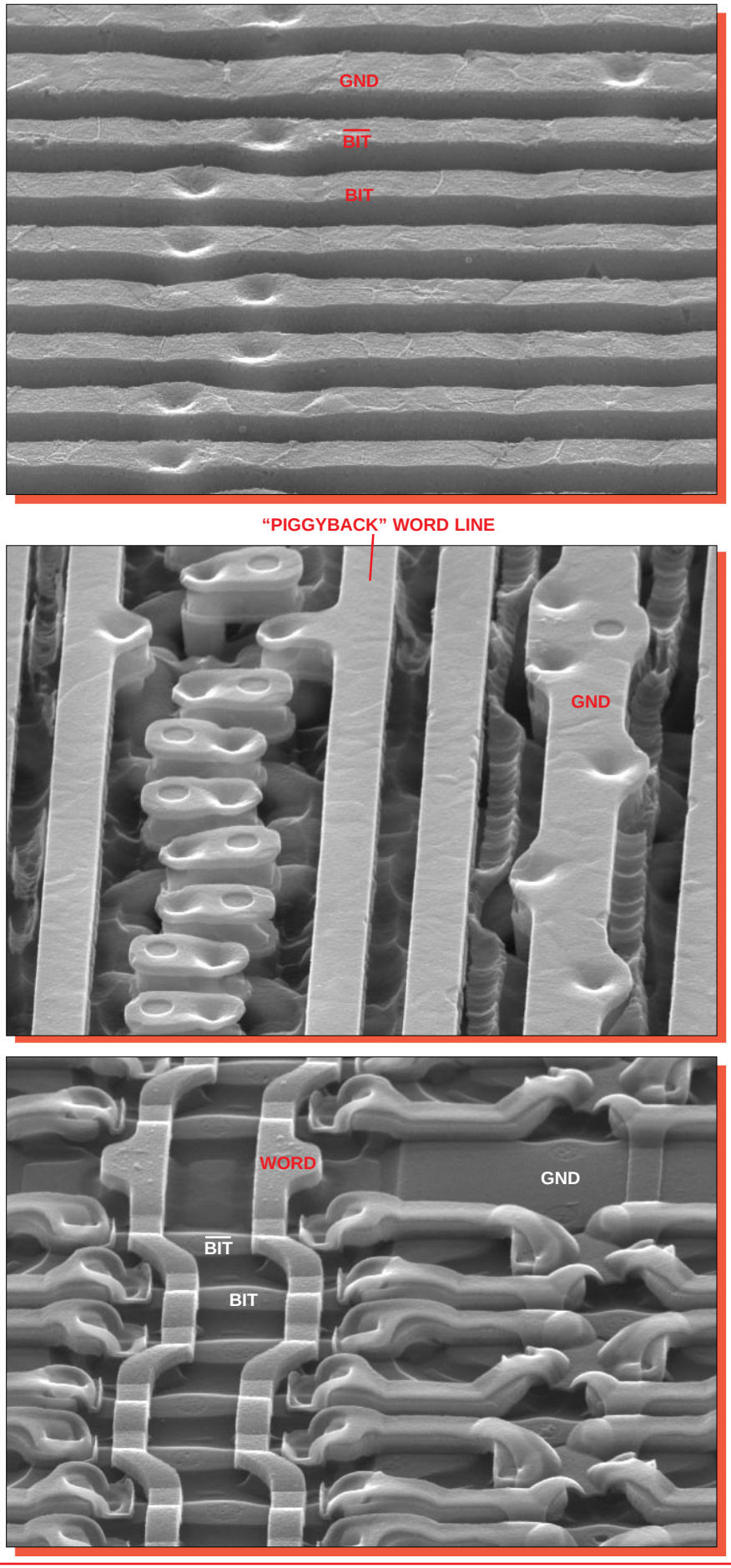
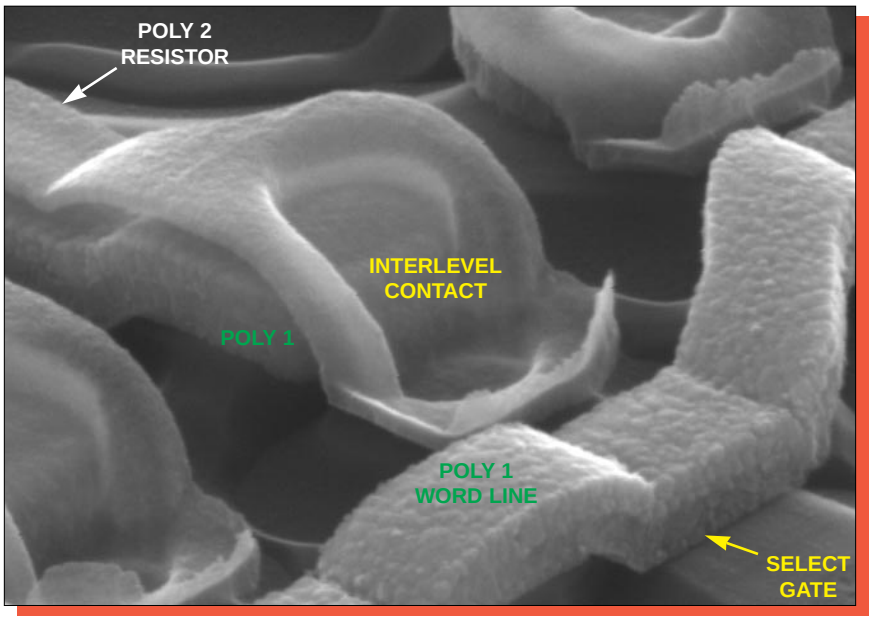


Figure 28. Perspective SEM views of the SRAM cell array. Mag. 10,000x, 60°.



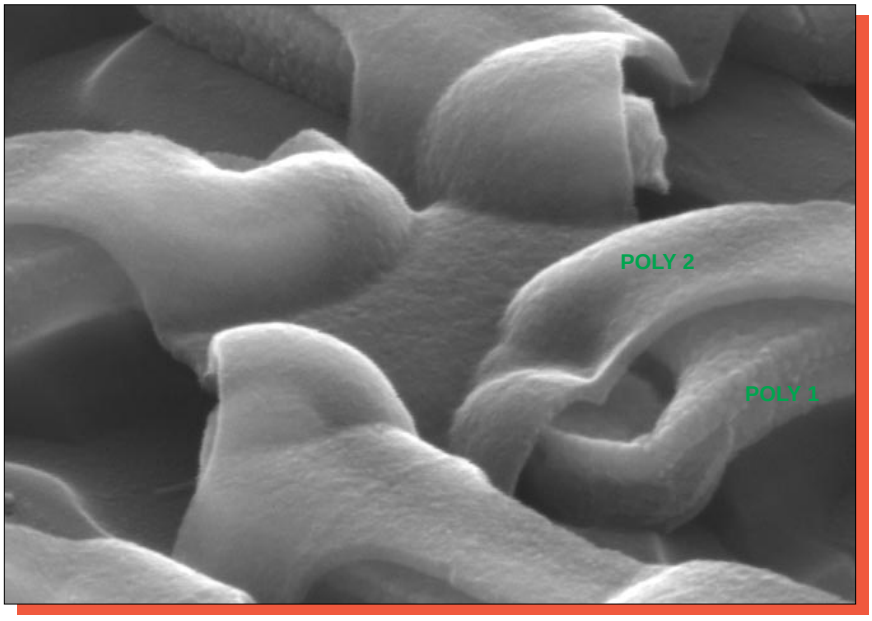


Figure 29. Detailed SEM views of the SRAM cell structures (delayered).
Mag. 42,000x, 60°.

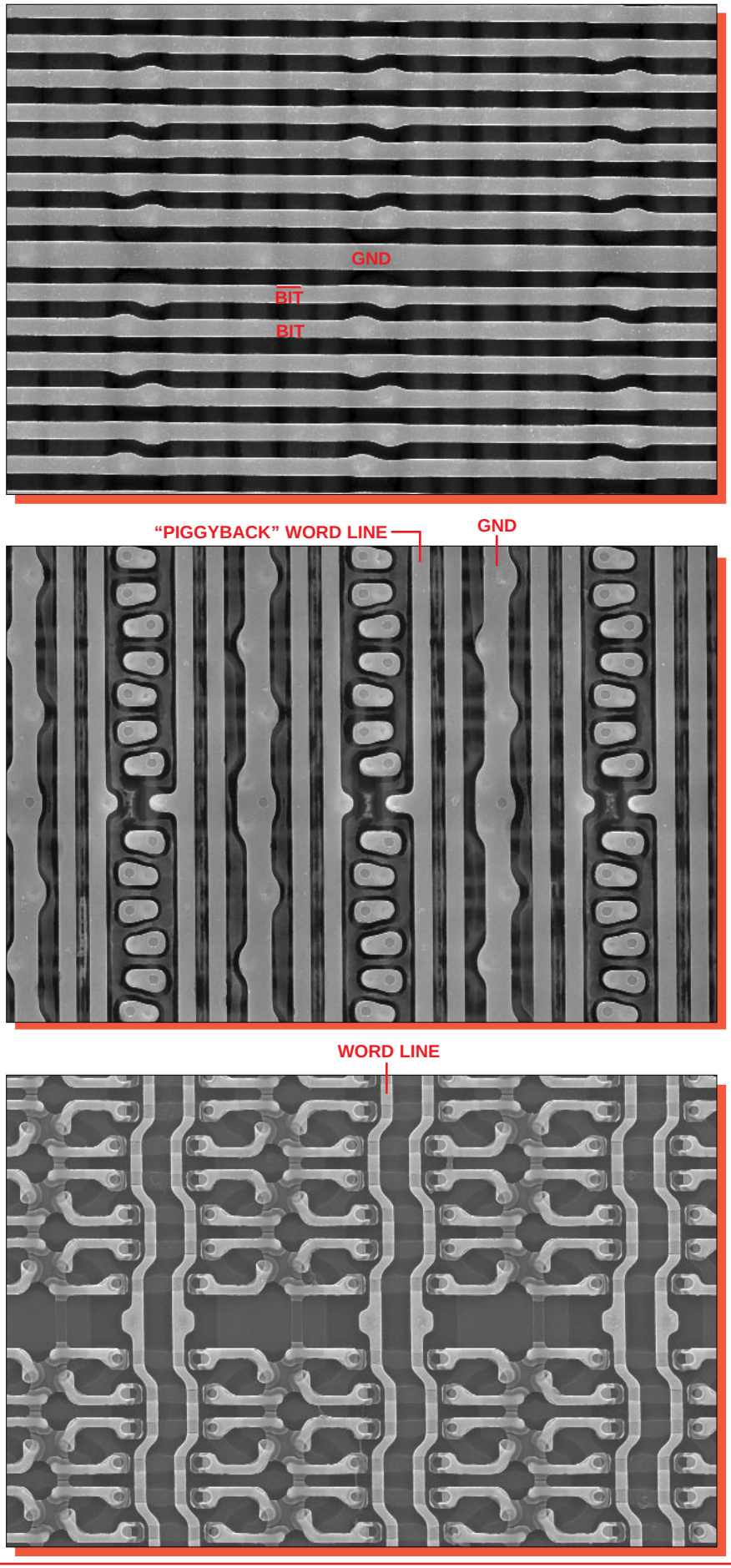
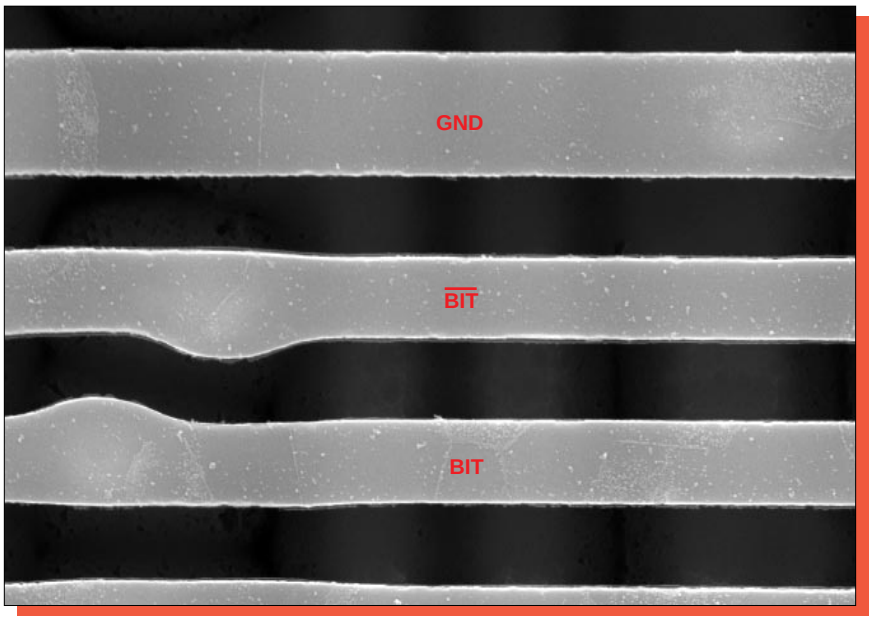
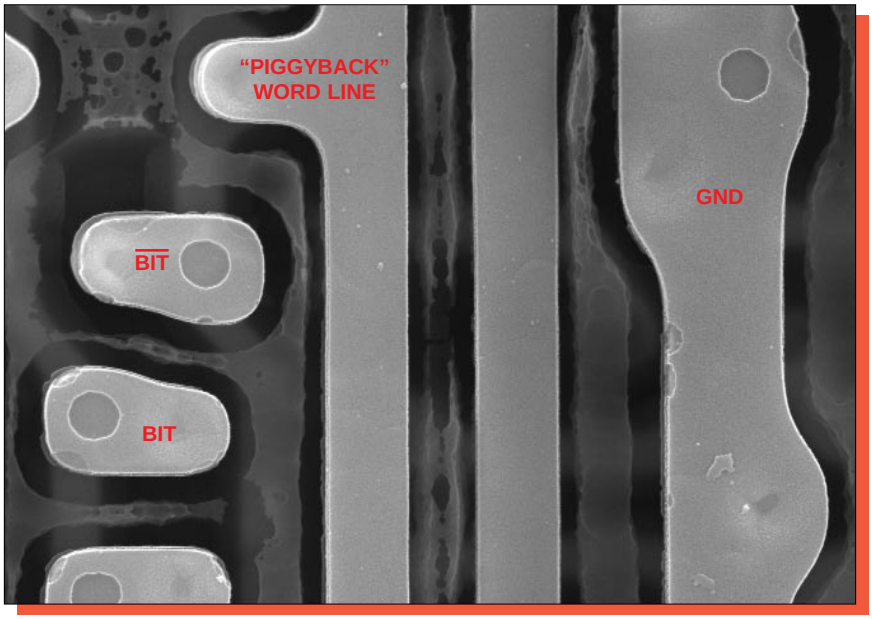


Figure 30. Topological SEM views of the SRAM cell array. Mag. 3200x, 0°.

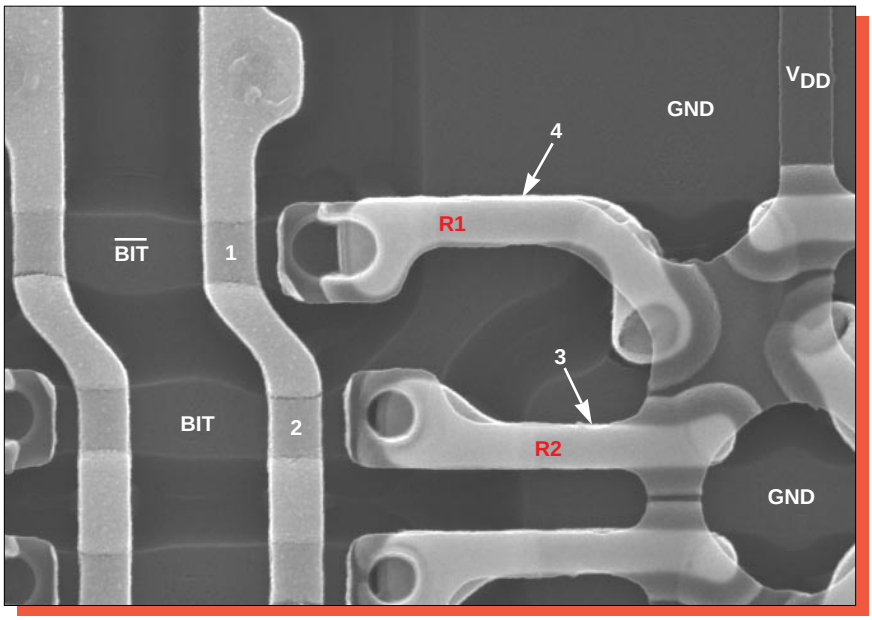


metal 2



metal 1

Figure 31. Detailed topological SEM views of an SRAM cell. Mag. 13,000x, 0°.



unlayered

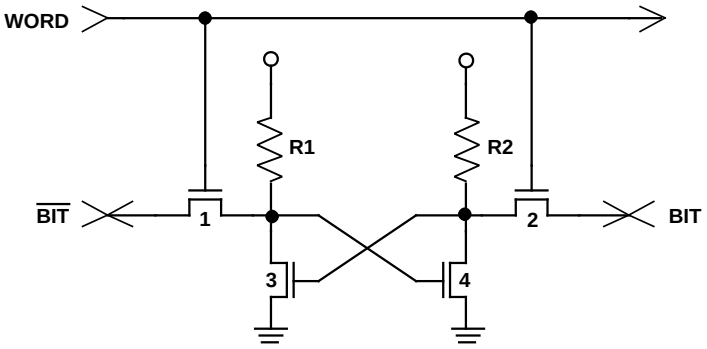
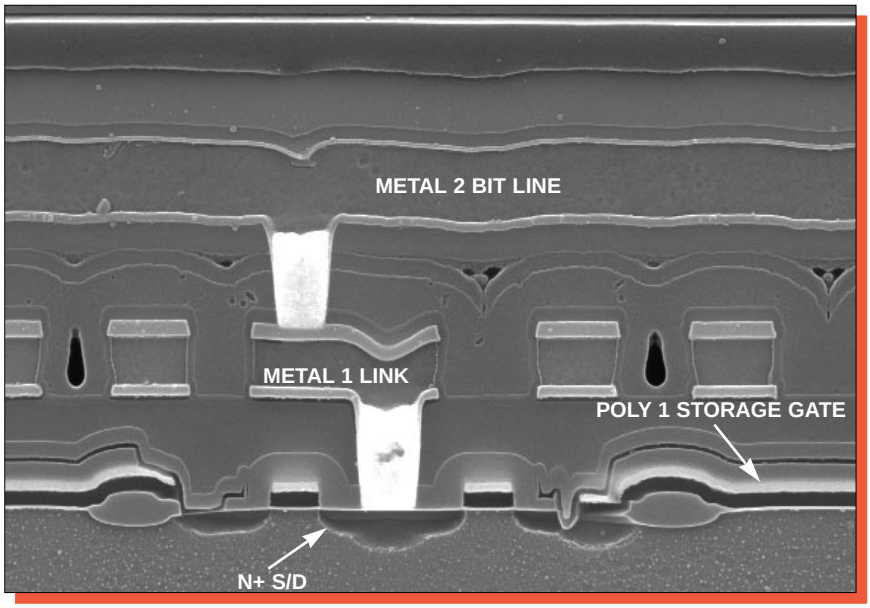
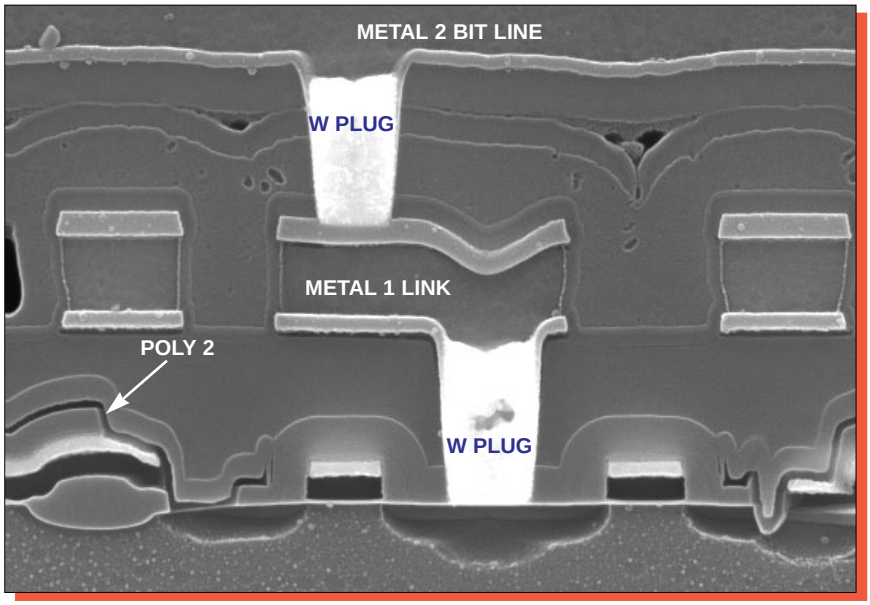


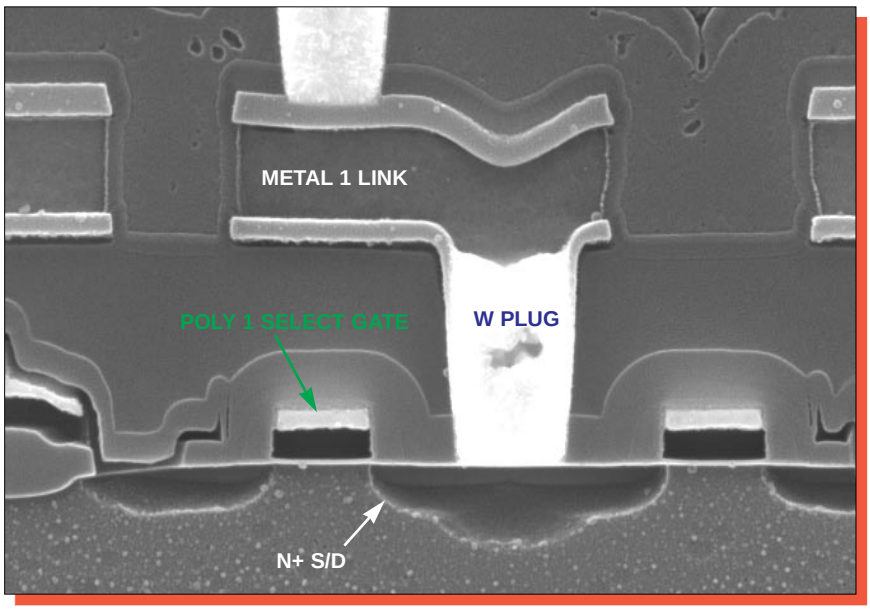
Figure 32. Detailed topological SEM view and schematic of an SRAM cell.
Mag. 13,000x, 0°.



Mag. 13,000x

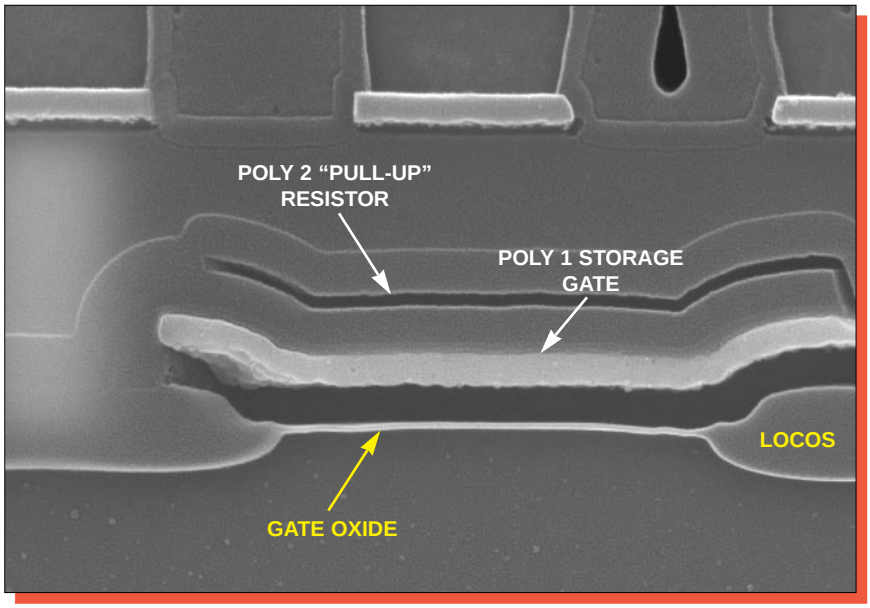


Mag. 20,000x

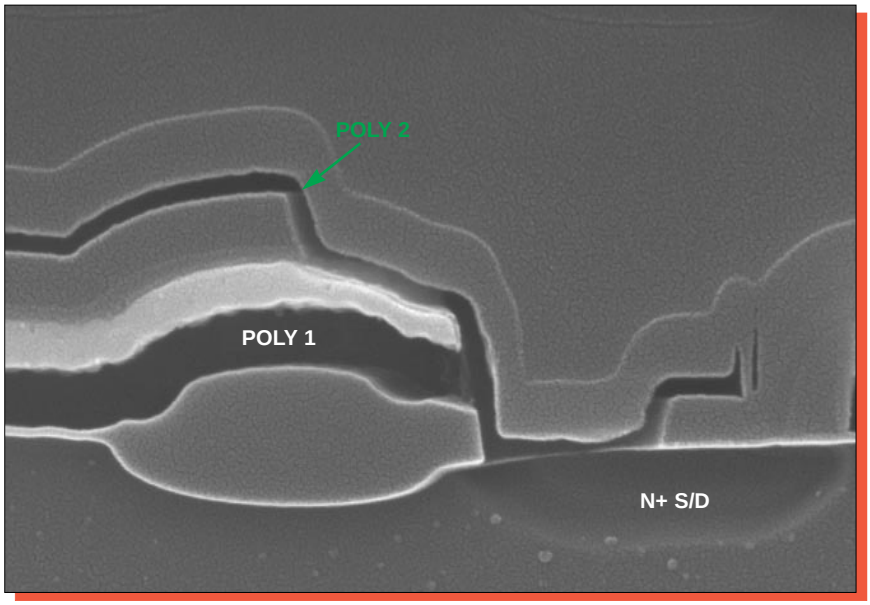


Mag. 26,000x

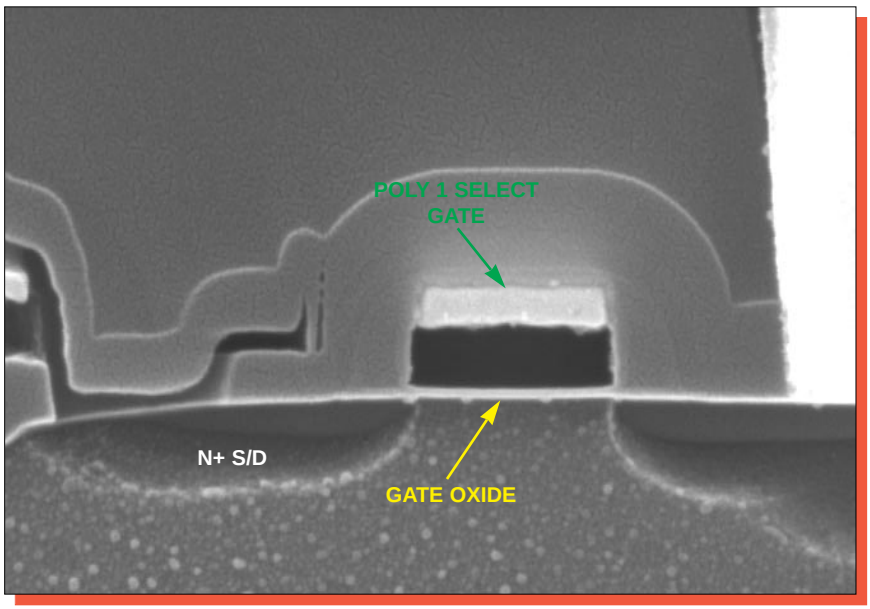
Figure 33. SEM section views of an SRAM cell (parallel to bit line).



Mag. 35,000x

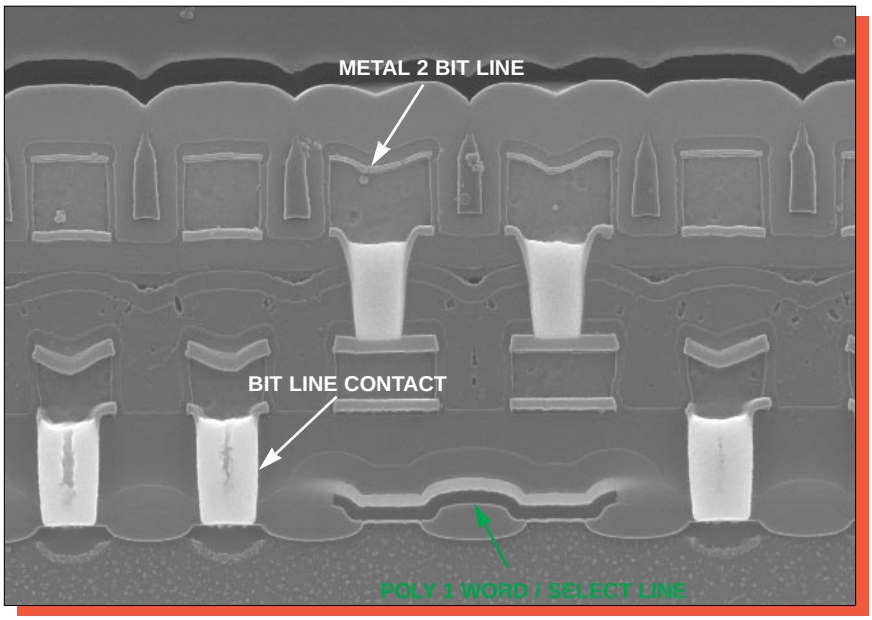


Mag. 52,000x

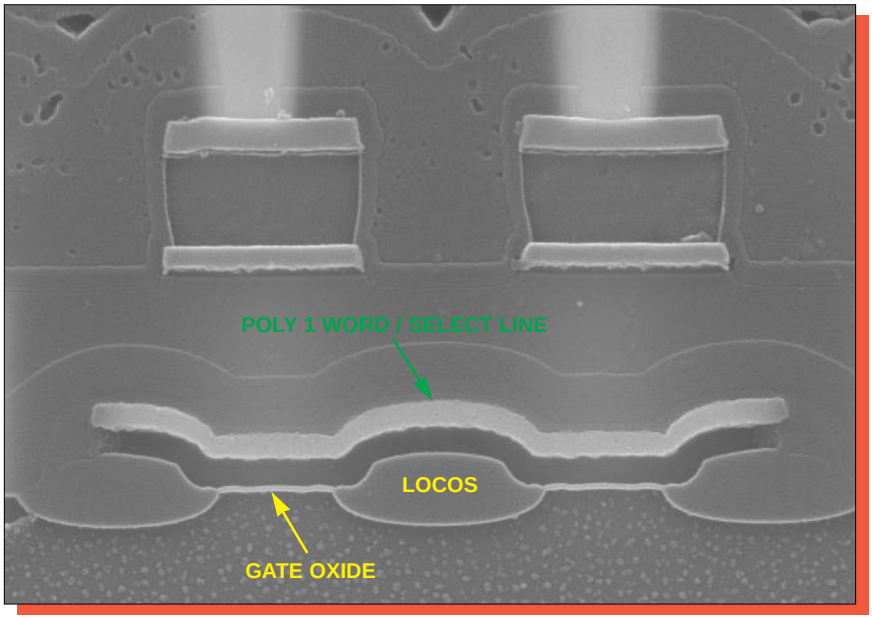


Mag. 52,000x

Figure 34. SEM section views of SRAM cell details (parallel to bit line).

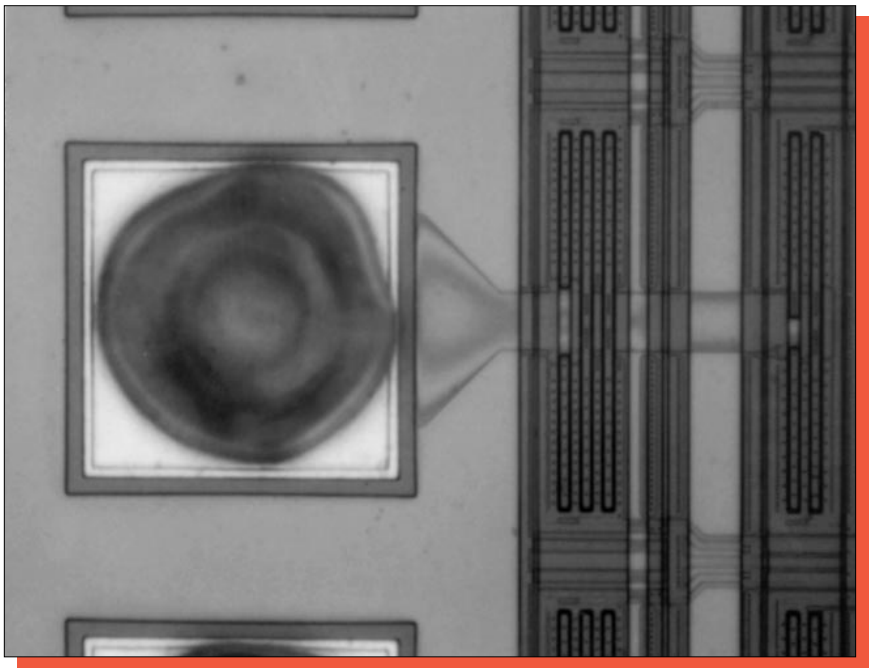


Mag. 13,000x

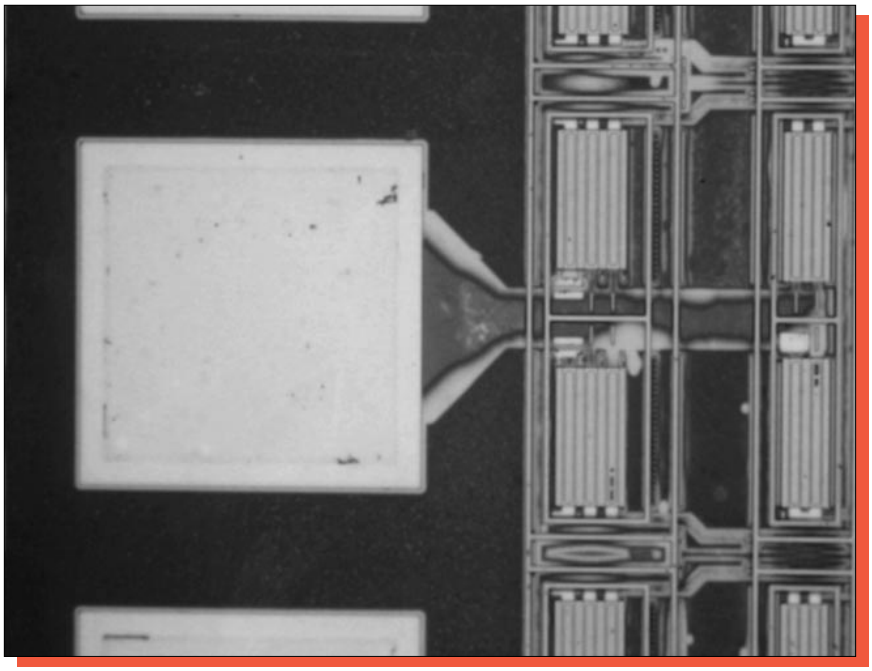


Mag. 26,000x

Figure 35. SEM section views of the SRAM cell array (perpendicular to bit line).

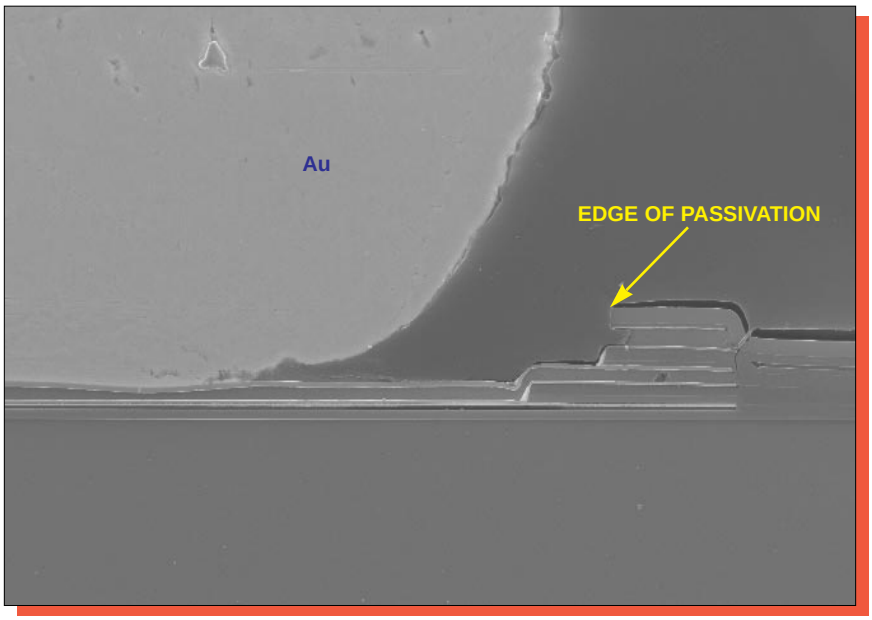


intact

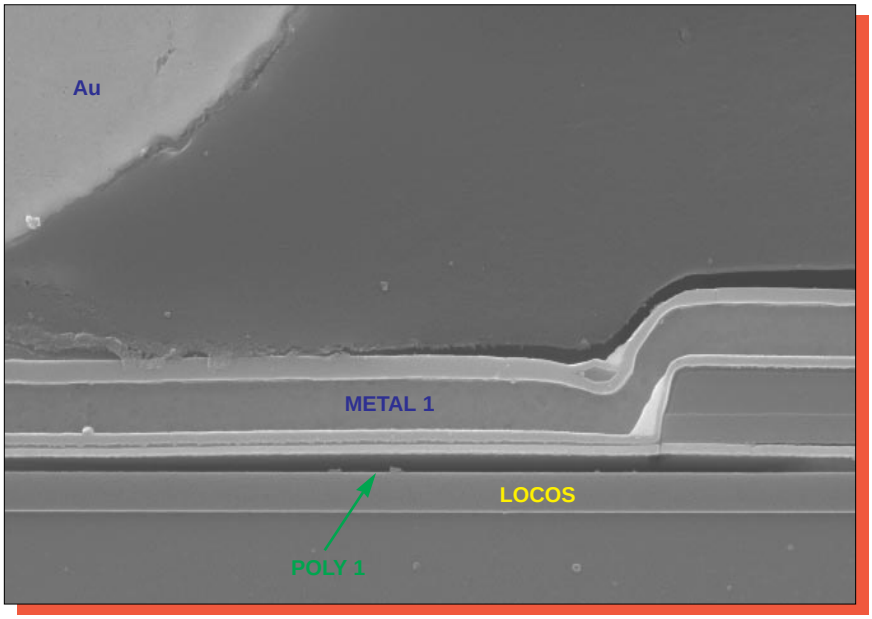


unlayered

Figure 36. Optical views of typical I/O circuitry. Mag. 400x.

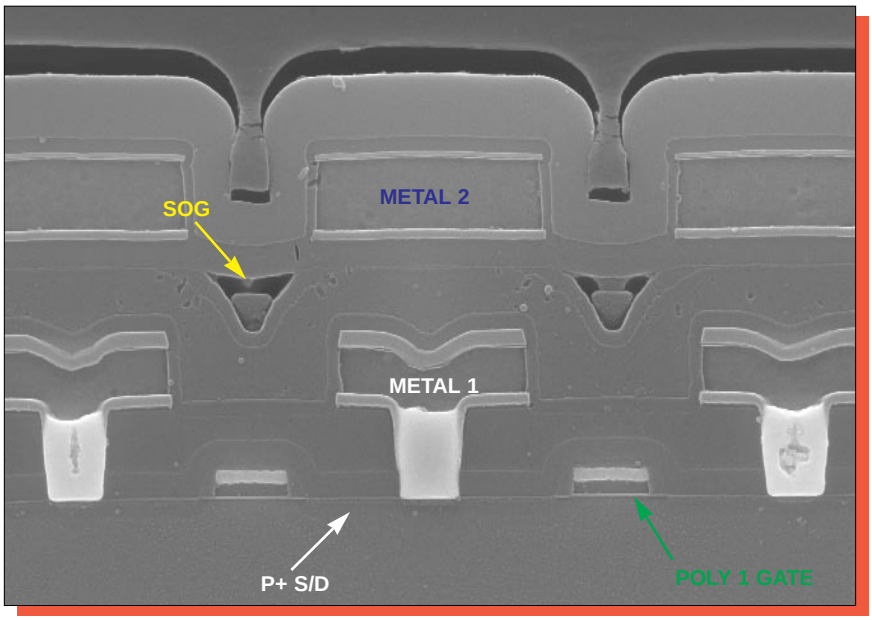


Mag. 3200x

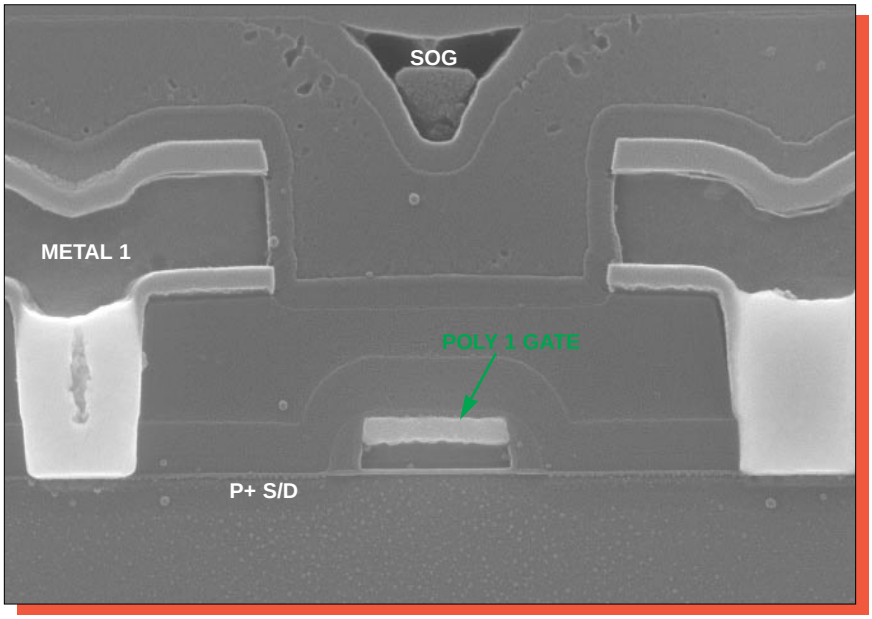


Mag. 13,000x

Figure 37. SEM section views illustrating wirebond interface.

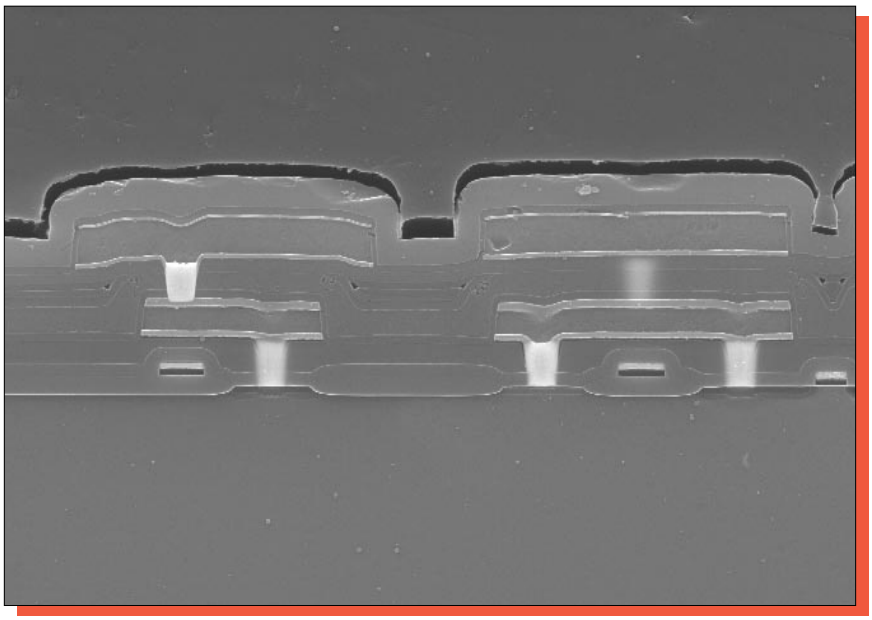


Mag. 13,000x

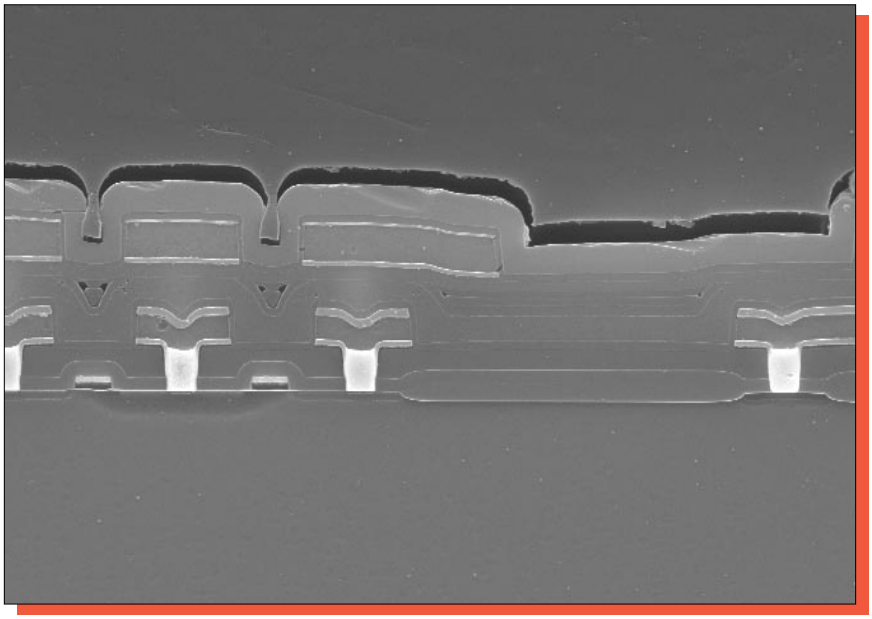


Mag. 26,000x

Figure 38. SEM section views of P-channel I/O circuitry.



N- channel



P-channel

Figure 39. SEM section views illustrating guardbands at the edge of the I/O circuitry.
Mag. 6500x.