Construction Analysis

National Semiconductor LM2672 Simple Switcher® Voltage Regulator

Report Number: SCA 9712-570

INTEGRATED CIRCUIT ENGINEERING

17350 N. Hartford Drive
Scottsdale, AZ 85255
Phone: 602-515-9780
Fax: 602-515-9781
e-mail: ice@ice-corp.com
Internet: http://www.ice-corp.com

INDEX TO TEXT

INTRODUCTION

This report describes a construction analysis of the National Semiconductor LM2672 Simple Switcher voltage regulator. Five devices were supplied, encapsulated in 8-pin Dual-In-Line plastic packages (DIP). Date codes were not identifiable.

MAJOR FINDINGS

Questionable Items:[1]

- Metal cracks were noted at contact edges.
- Significant silicon in contacts.

Special Features:

- Linear Power BiCMOS process which includes a double diffused (DMOS) process.
- Extended shallow source/drain N-channel transistor structure.

Design Features:

- Large area for double diffused (DMOS) process.
- Large capacitor structures.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in 8-pin plastic DIPs.
- Lead-locking provisions (anchors and holes) were present at all pins.
- Thermosonic ball bond method employing 1.3 mil O.D. gold wire.
- Silver-filled polyimide die attach.
- Sawn dicing (full depth).

Die Process and Design

- Fabrication process: Linear Power BiCMOS process with N-epi, P-well, P+ iso, and N+ buried layer, incorporating N and P channel MOS, DMOS, NPN and PNP transistors.
- Final passivation: Two layers of passivation were employed. A layer of nitride over a layer of silicon-dioxide.
- Metallization: Two levels of silicon-doped aluminum defined by dry-etch techniques. No caps or barriers were present. Standard contacts and vias (no plugs). In the DMOS area metal 2 was placed directly on metal 1.
- Intermetal Dielectric (IMD): Intermetal dielectric consisted of single layer of glass. No planarization technique was used.
- Pre-metal glass: A single layer of reflow glass was used. Reflow was done prior to contact cuts. Grown and densified oxides were also present.

TECHNOLOGY DESCRIPTION (continued)

- Polysilicon: Single layer of dry-etched polysilicon (no silicide) was used to form all MOS gates on the die. It was also used as the top plate for the thin oxide capacitors. An LDD process was used with spacers removed.

- DMOS devices: A double diffused Hexfet style process was employed. N+ diffusions formed the sources of the transistor elements. Deep P+ diffusions formed the body and inherent body diode. N- epi/buried layer formed the drain.

- CMOS devices: Standard N+ and P+ implanted diffusions formed the sources/drains for these transistors. Sidewall spacers were selectively used and removed. Long shallow N+ LDD extensions were present on one side of some of the NMOS transistors. P-wells and N-epi were used for N-channel devices.

- Bipolar devices: Standard N+ diffusions were used for emitters and collectors of NPN's and base contacts of PNP devices. The standard base diffusions also used a shallow P+ implant (probably the S/D P+) at contact areas. P+ isolation diffusions were diffused from top and bottom of the epi (to reduce isolation width).

- No buried contacts were employed.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 4a**

Note: Package analysis was not required. The following data was obtained by observation and is given here as general information.

Questionable Items:[1] None.

General Items:

- Devices were packages in 8-pin plastic DIPs.
- Package markings were clear and easy to read. Date codes were not identifiable.
- Overall package quality: Normal. No defects were noted on the external portions of the package. Deflash was of normal quality and workmanship. Lead form was of normal quality and workmanship. No problems were found.
- Die placement: Die was centered and silver-filled polyimide die attach was of good quantity and quality. No problems were found.
- Lead-locking provisions (anchors and holes) were present at all pins.
- Wirebonding: Thermosonic ball bond method using 1.3 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 8). Metal 2 on 1 formed the bond pads. Wire spacing and placement was good. Probe mark damage was noted at some test pads. The damage decreased the metal spacing; however, no shorts were noted.
- Die dicing: Die separation was by full depth sawing with good quality workmanship.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process and Design: **Figures 5 - 31**

Questionable Items:[1]

- Metal cracks were noted at contact edges.
- Significant silicon in contacts.

Special Features:

- Linear Power BiCMOS process which includes a double diffused (DMOS) process.
- Extended shallow source/drain N-channel transistor structure.

Design Features:

- Large area for double diffused (DMOS) process.
- Large capacitor structures.

General Items:

- Fabrication process: Linear Power BiCMOS process with N-epi, P-well, P+ iso, and N+ buried layer, incorporating N and P channel MOS, DMOS, NPN and PNP transistors.
- Design and layout: Die layout was clean and efficient. The identification number on the die was 2675.
- Die surface defects: None. No contamination or processing defects were noted.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Final passivation: The passivation consisted of a layer of nitride over a layer of silicon-dioxide. Passivation integrity test indicated defect free passivation. Edge seal was also good. Some residual metal was noted at the die edge; however, no problems are foreseen (Figures 3 and 3a).

- Metallization: Two levels of metal defined by a dry-etch of normal quality. Metal consisted of silicon-doped aluminum. No cap or barrier metals were employed. Standard vias and contacts were used (no plugs).

- Metal defects: None. No notching of the metal layers was present. There was significant silicon mound growth in contact areas following the removal of the metal in the MOSFET area. Worst case silicon mound growth occupied up to 40 percent of contacts and is shown in Figure 24. Cracks were noted at contact edges see Figures 26, 27 and 29.

- Metal step coverage: No significant metal thinning occurred at vias or contacts due to the sloped contact cuts.

- Contacts: Contact cuts appeared to be defined by a wet-etch technique of good quality. No significant over-etching of the contacts was present. No contact pitting was present. Substrate contacts were used to bias the P-wells (Figure 19).

- Intermetal Dielectric (IMD): Intermetal dielectric consisted of single layer of glass. No planarization technique was used. No problems were present.

- Pre-metal glass: A single layer of reflow glass was used over grown oxides. No problems were found.

ANALYSIS RESULTS II (continued)

- Polysilicon: Single layer of dry-etched polysilicon (no silicide) was used to form all MOS gates on the die. It was also used as the top plate for the thin oxide capacitors and gates for the DMOS structure. The LDD process used sidewall spacers which were removed. Large poly capacitor structures were used throughout entire die. No poly resistors were present. No problems were present.

- Isolation: N-epi islands with N+ buried layer separated by P+ isolation. There was good separation between buried layer and isolation with minimal buried layer shift. P-wells were noted in N-epi for N-channel devices. P+ isolation (up and down) diffusions were used to isolate the N-epi islands. A step in the oxide was noted at the P+ iso diffusions.

- DMOS devices: A double diffused process was employed. N+ diffusions formed the sources of the transistor elements. Deep P+ diffusions formed the body and inherent body diode. N- epi/N+ buried layer formed the drain.

- CMOS devices: Standard N+ and P+ implanted diffusions formed the sources/drains for these transistors. Some NMOS transistors used a unique LDD extension on one side of the gate. The step in the oxide would indicates this although the implant was too light to delineate.

- Bipolar devices: All bipolar devices were located in N-epi/N+ buried layers. Standard N+ diffusions were used for emitters and collectors of NPN's and base contacts of PNP devices. The standard base diffusions also used a shallow P+ implant (probably the S/D P+) at contact areas. P+ isolation diffusions were diffused from top and bottom of the epi (to reduce isolation width).

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

SEM inspection of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal and inspect metal 2

Delayer to metal 1 and inspect

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	N
Package markings	G
Die placement	G
Die attach quality	G
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	N
Wirebond method	Thermosonic ball bonds using 1.3 mil gold wire.
Dicing method:	Sawn (full depth)
Die attach:	Silver-filled polyimide
Die surface integrity:	
Tool marks (absence):	NP (probe damage)
Particles (absence):	N
Contamination (absence):	N
Process defects (absence):	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP (cracks at contact edges)
Contact coverage	G
Contact registration	N
Contact defects	NP (some significant silicon mound growth)

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

Top

(National logo) 66AB
2672 M3.3

Bottom

none

WIREBOND STRENGTH

Wire material:	1.3 mil diameter gold
Die pad material:	Aluminum

sample 4

# of wires tested:	11
Bond lifts:	0
Force to break - high:	18g
- low:	17g
- avg.:	17.9g
- std. dev.:	0.28

DIE MATERIAL ANALYSIS

Passivation:	Nitride over silicon-dioxide.
Die metallization:	Aluminum.
Intermetal dielectric:	Silicon-dioxide.
Pre-metal glass:	Single layer of reflow glass. Grown and densified oxides were also present.

HORIZONTAL DIMENSIONS

Die size:	1.8 x 3.5 mm (73.5 x 140.5 mils)
Die area:	6.3 mm^2 (10,326 $mils^2$)
Min pad size:	0.13 mm x 0.13 mm (5.1 x 5.1 mils)
Min pad window:	0.11 mm x 0.11 mm (4.4 x 4.4 mils)
Min metal 2 width:	7.3 microns
Min metal 2 space:	7.7 microns
Min metal 2 pitch:	15 microns
Min via:	5.3 microns
Min metal 1 width:	3.4 microns
Min metal 1 space:	4.3 microns
Min metal 1 pitch:	7.7 microns
Min contact:	3 microns
Min poly width:	3.7 microns
Min poly space:	4.7 microns
Min gate length*	
- (N-channel)	3.7 microns
- (P-channel)	5.0 microns
Min N+ emitter:	16 microns (round)
Min P+ emitter:	12 microns (round)
Min P+ isolation:	10 microns
Min edge of base to P+ iso:	12 microns
Min emitter to edge of base:	8 microns

* *Physical gate length*

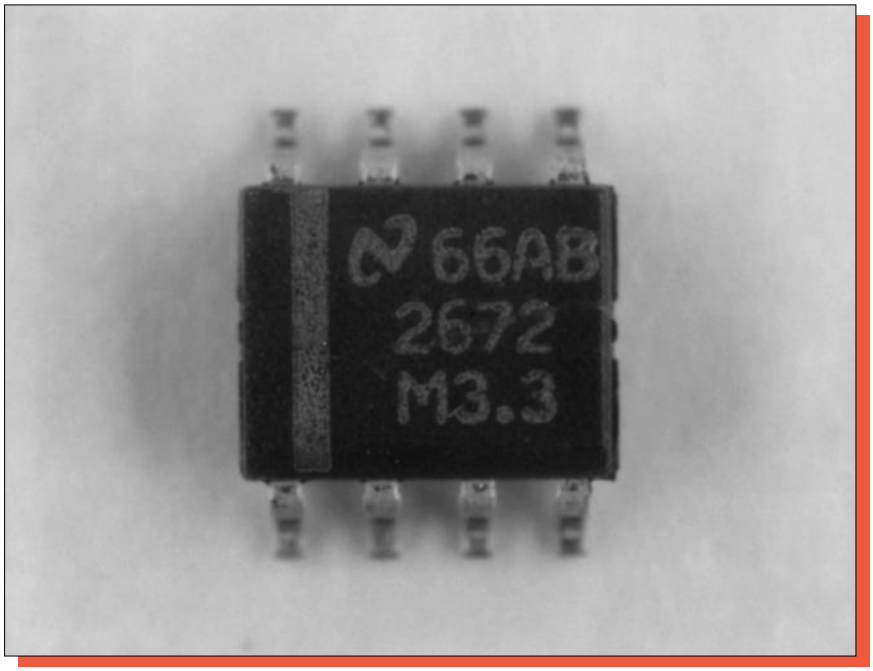
VERTICAL DIMENSIONS

Die thickness:	0.35 mm (14 mils)

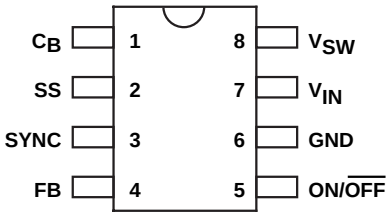
Layers

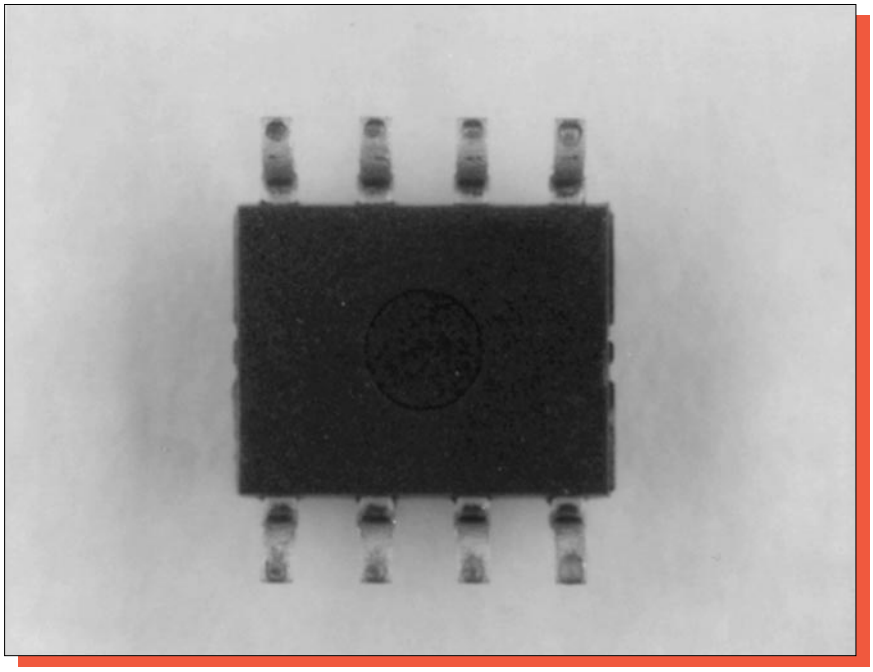
Passivation 2:	1.0 micron
Passivation 1:	0.45 micron
Aluminum 2:	2 microns
Intermetal dielectric (IMD):	0.95 micron
Aluminum 1:	0.75 micron
Pre-metal glass:	0.65 micron
Poly:	0.4 micron
Local oxide:	1 micron
N+ S/D diffusion:	0.6 micron
P+ S/D diffusion:	0.45 micron
P DMOS body:	5.5 microns
P+ base (NPN):	2.8 microns
N+ (DMOS):	10 microns
N+ emitter and collector (NPN):	0.6 micron
N- epi:	4.5 microns
P-well:	5.5 microns
N+ buried layer:	24 microns (from surface)

INDEX TO FIGURES



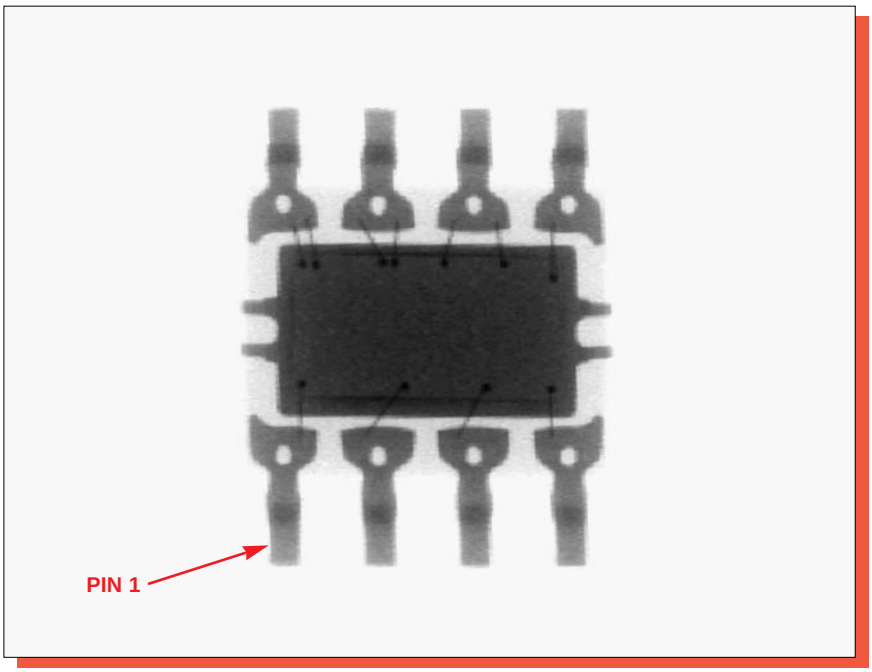
top





bottom

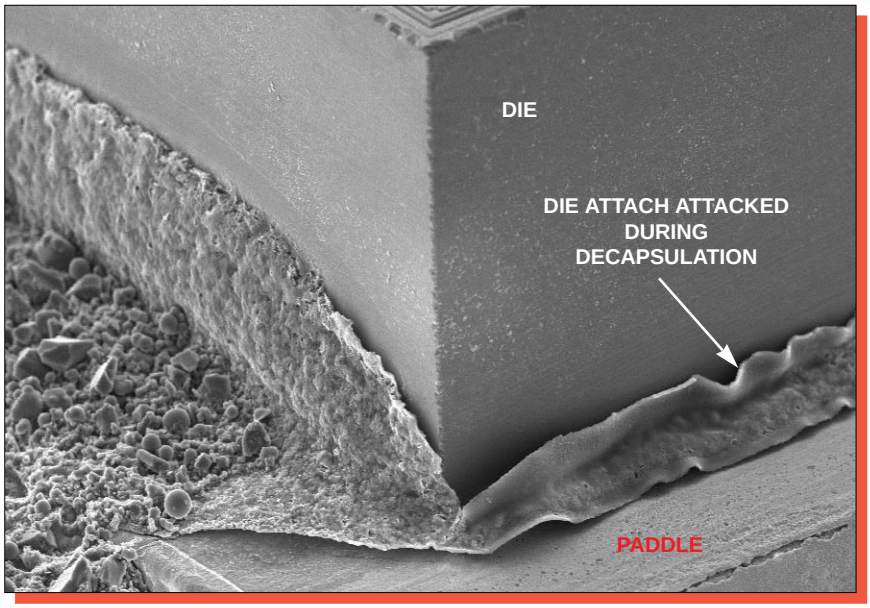
Figure 1. Package photographs and pinout of the National LM2672 device. Mag. 10x.



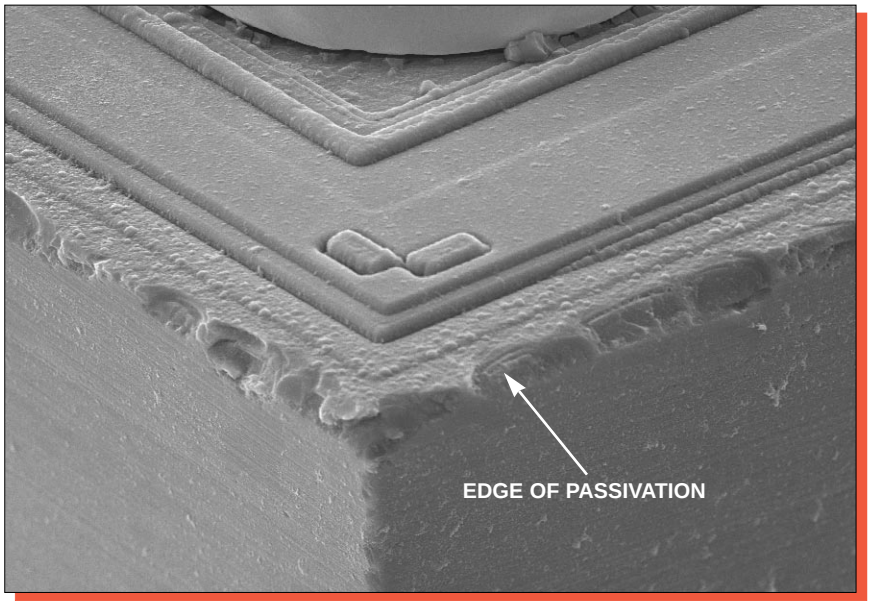
top

side

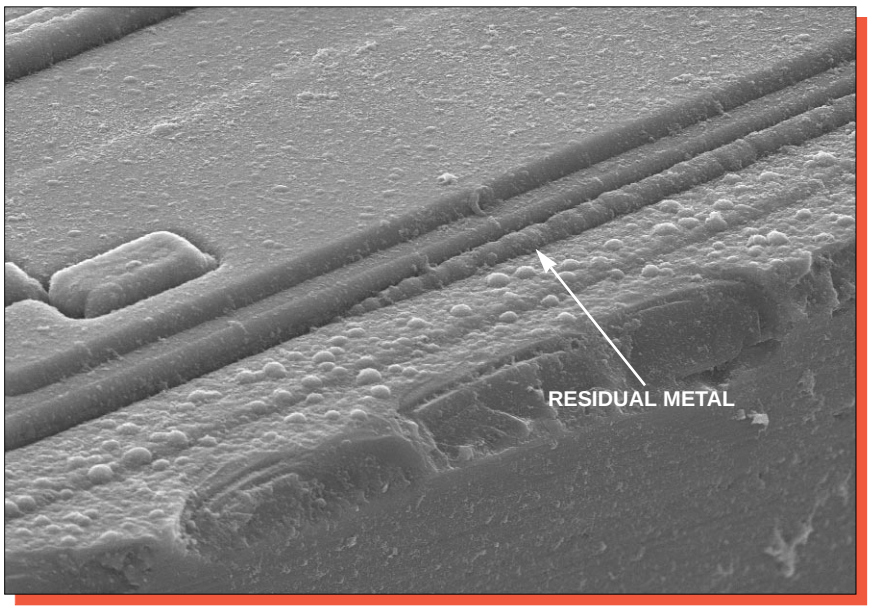
Figure 2. X-ray views of the package. Mag. 10x.



Mag. 200x

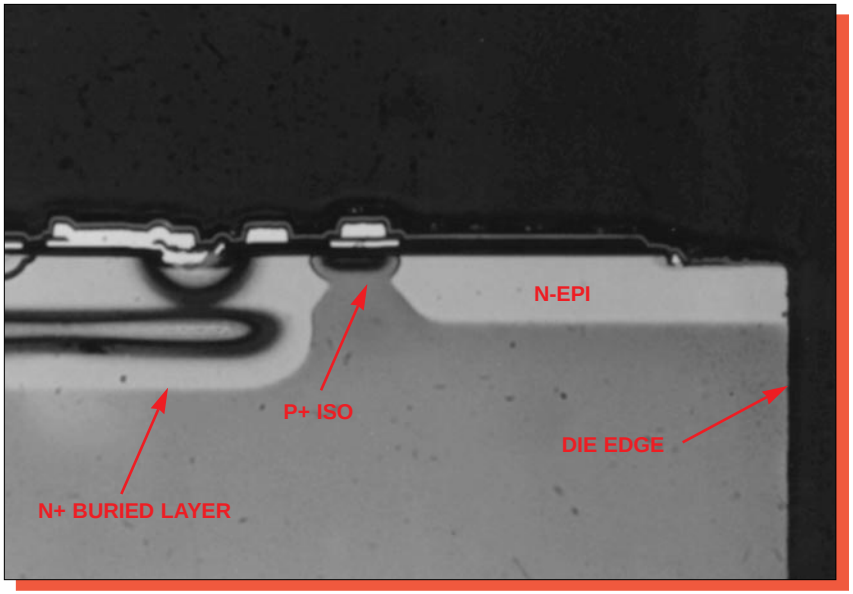


Mag. 750x

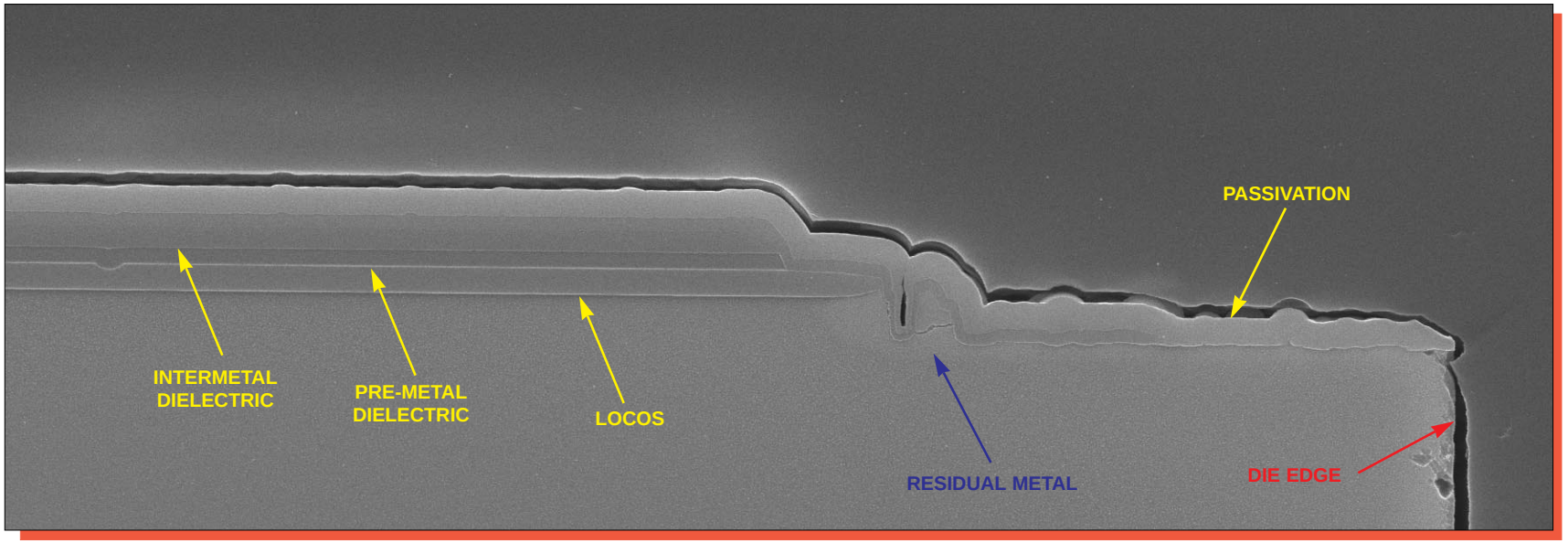


Mag. 1500x

Figure 3. SEM views of dicing and edge seal. 60°.

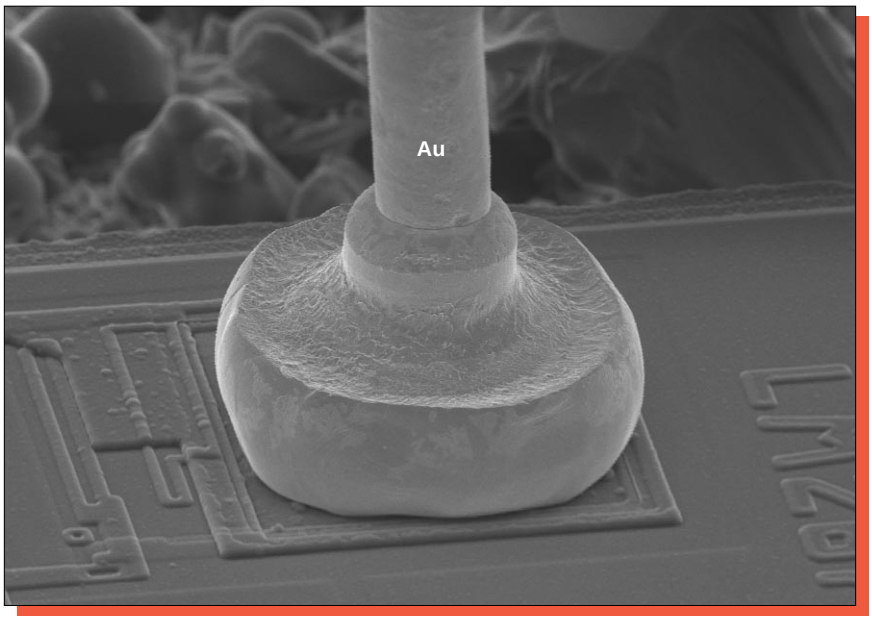


Mag. 800x



Mag. 4000x

Figure 3a. Optical and SEM section views of the die edge seal.



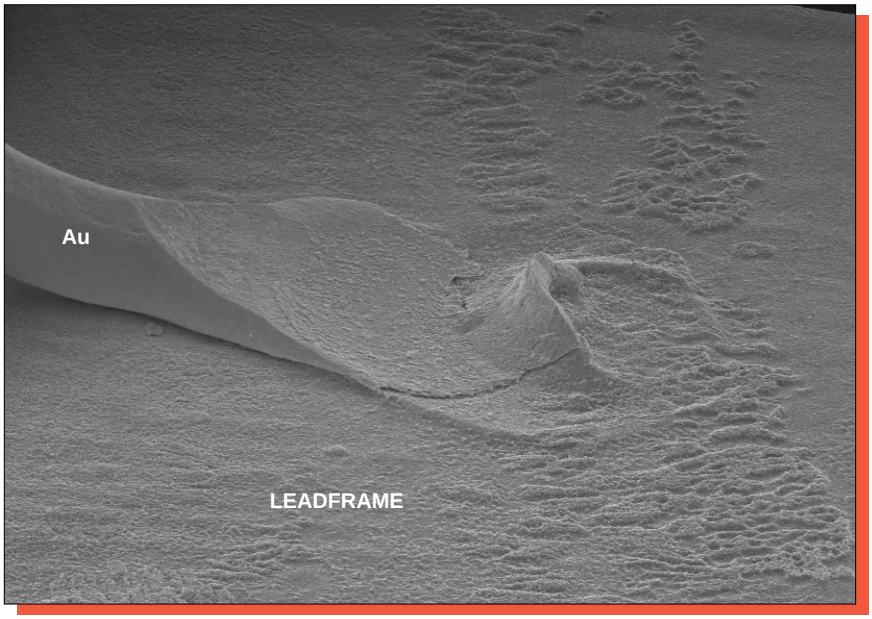
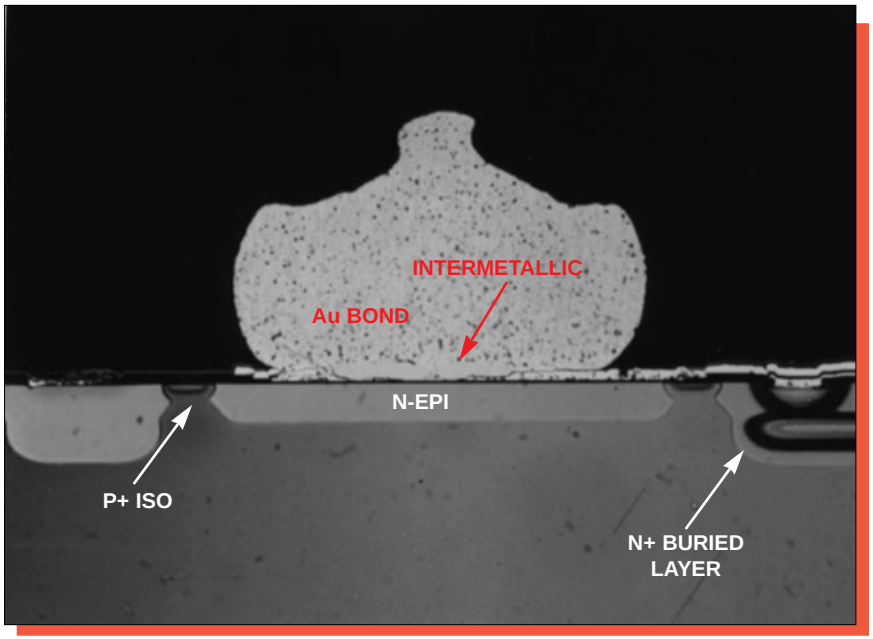
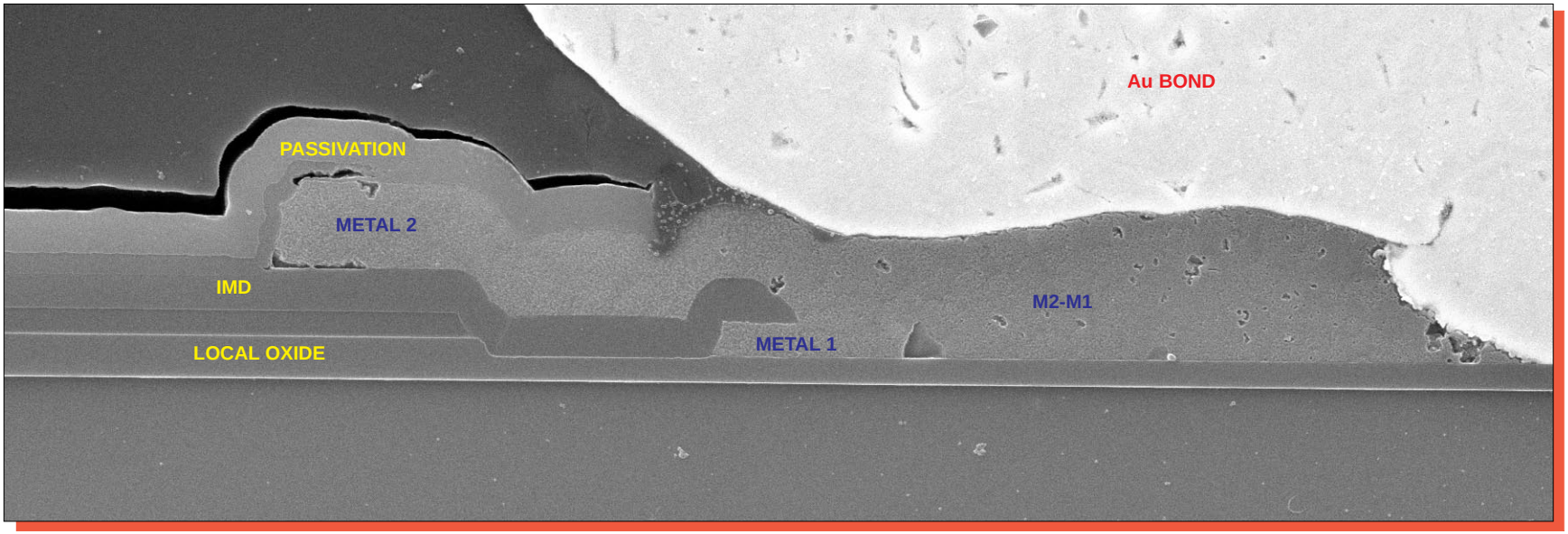


Figure 4. SEM views of typical wirebonds. Mag. 500x, 60°.



Mag. 500x



Mag. 6500x

Figure 4a. Optical and SEM section views of the bond pad structure.

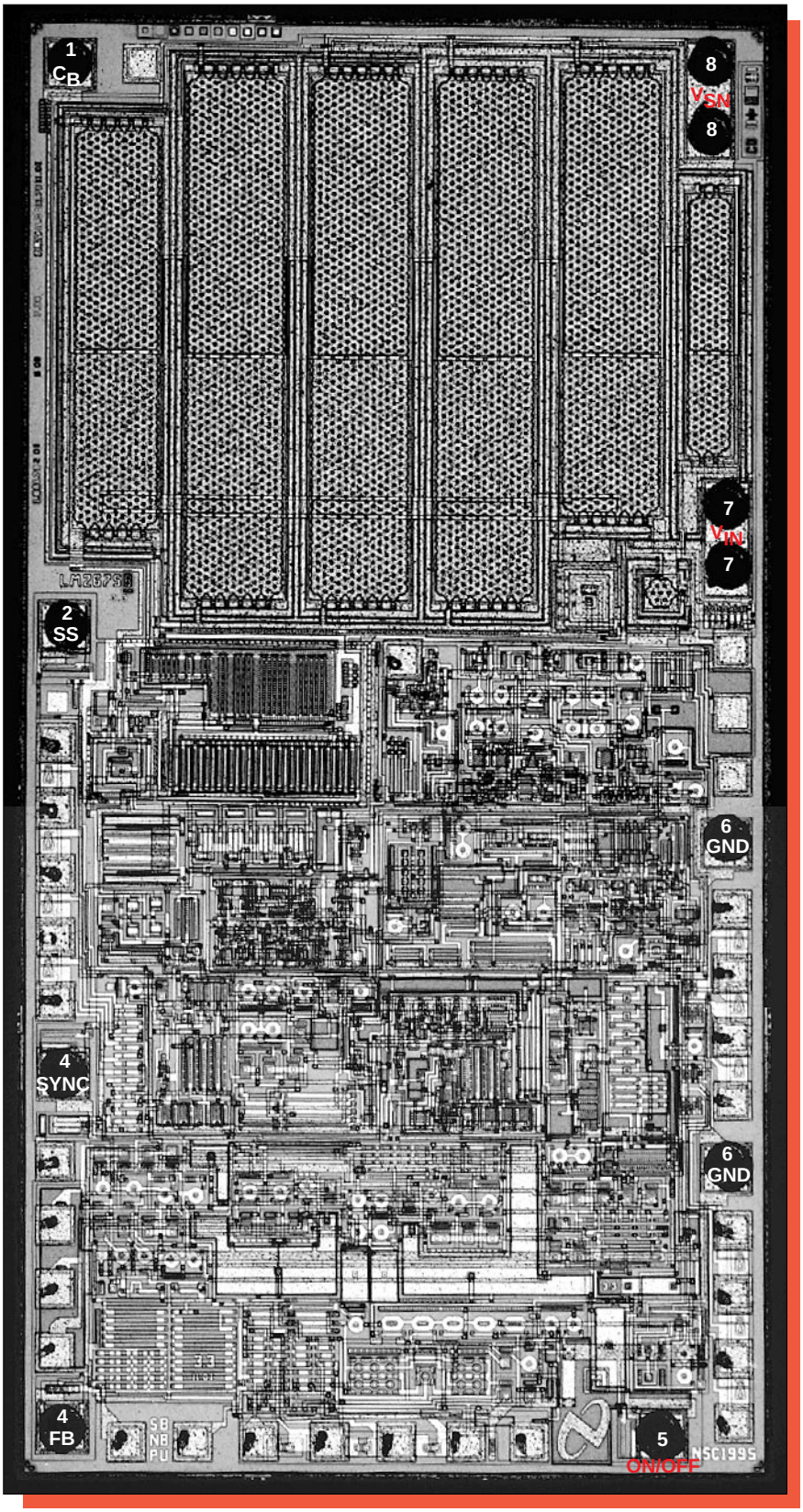


Figure 5. Whole die photograph of the National LM2672 device. Mag. 60x.

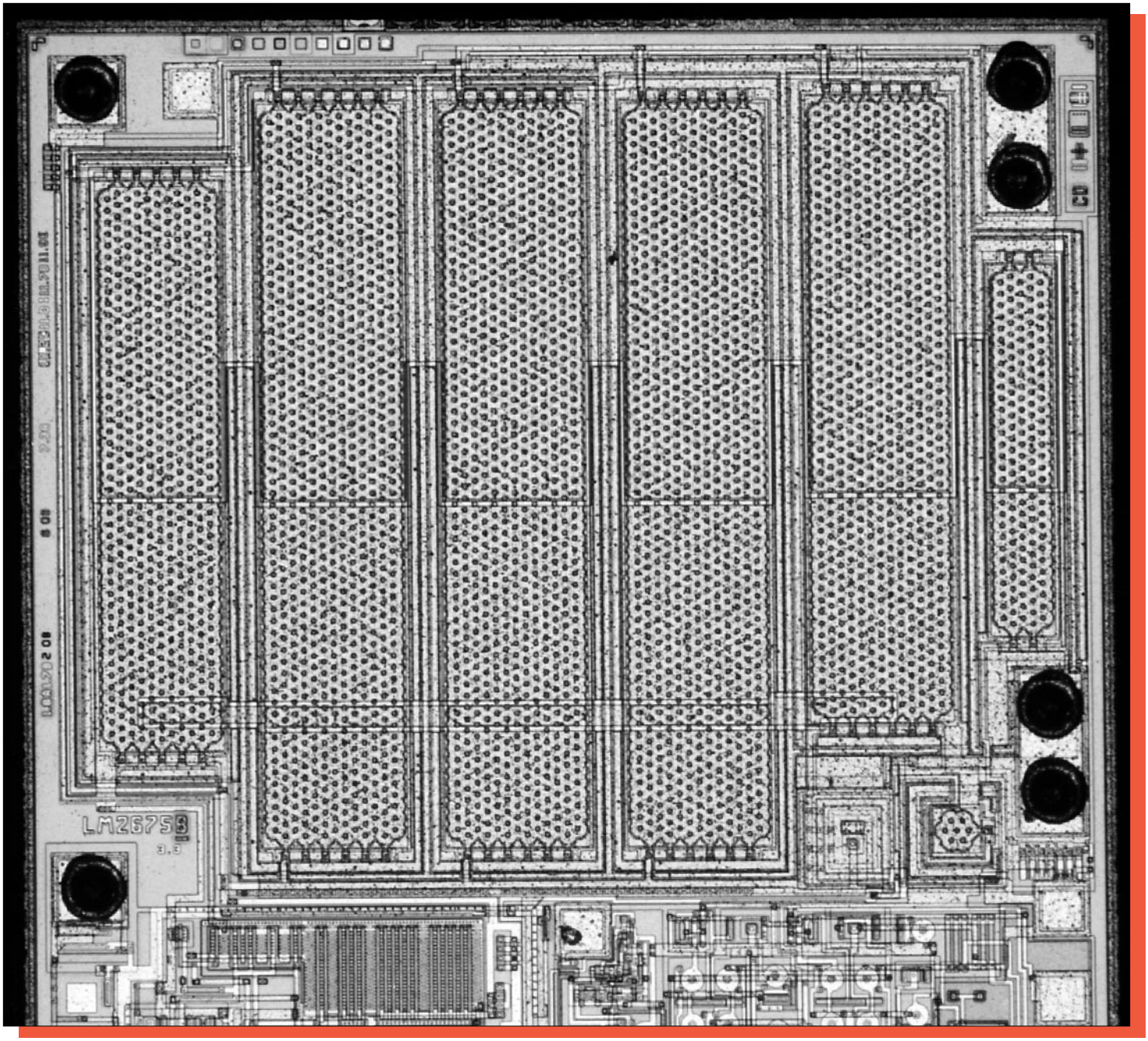


Figure 5a. Detailed optical view of the DMOS area. Mag. 100x.

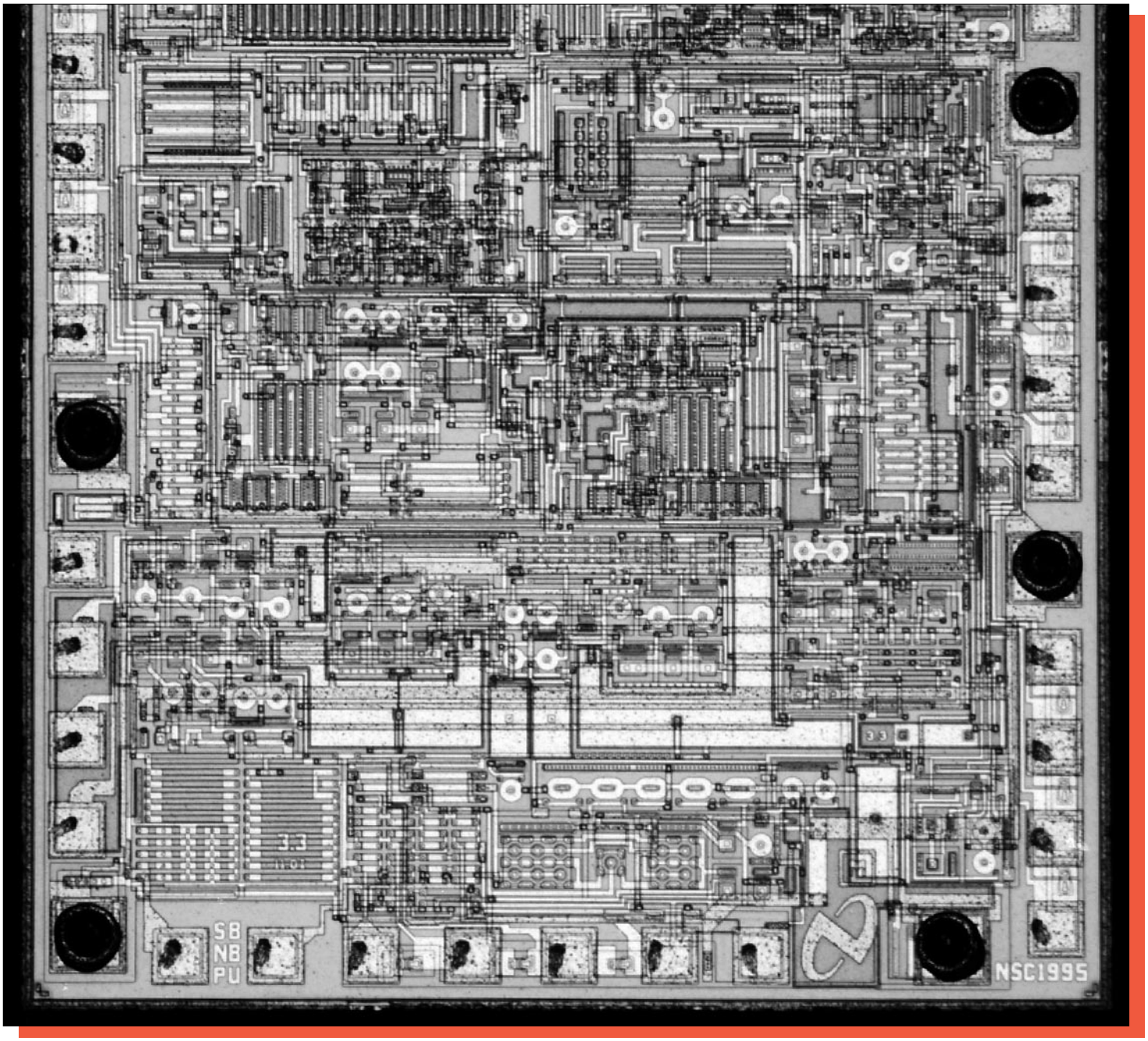
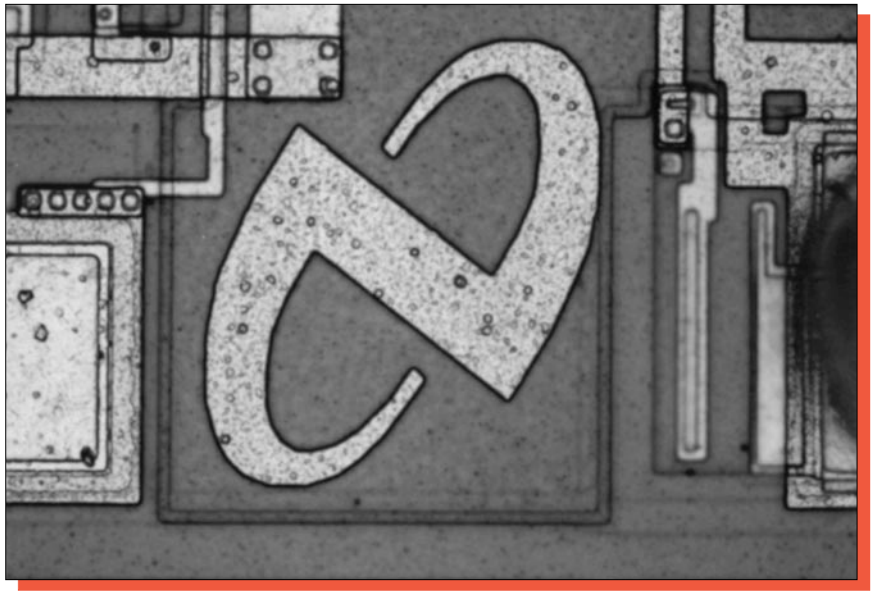
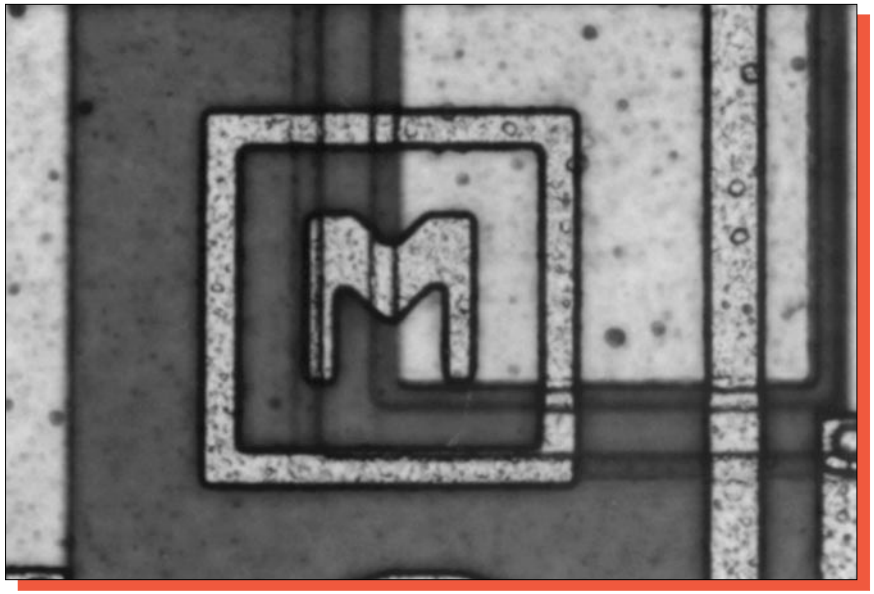


Figure 5b. Detailed optical view of the linear device area. Mag. 100x.



Mag. 400x

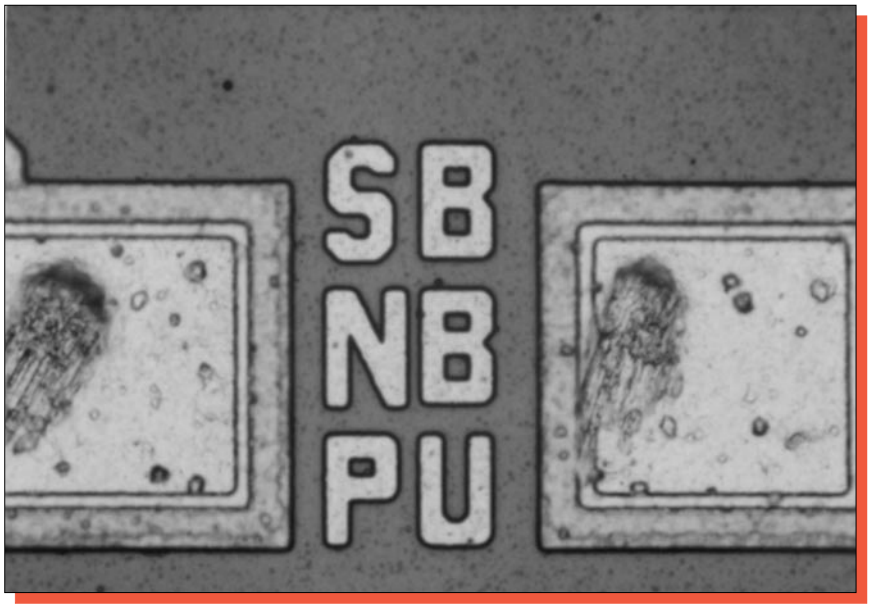


Mag. 800x

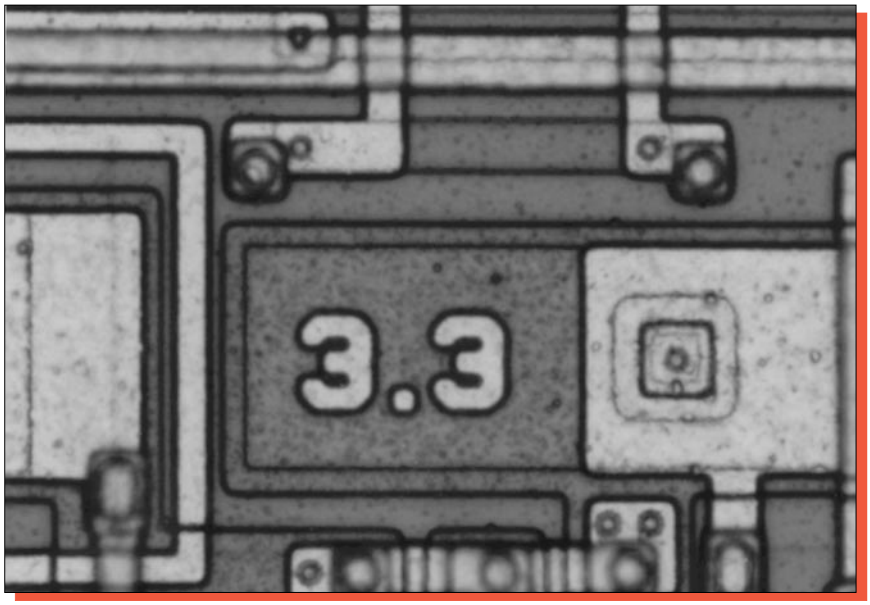
Mag. 500x

Mag. 500x

Figure 6. Die identification markings from the surface.



Mag. 500x



Mag. 800x

Mag. 800x

Figure 6a. Additional die markings from the surface.

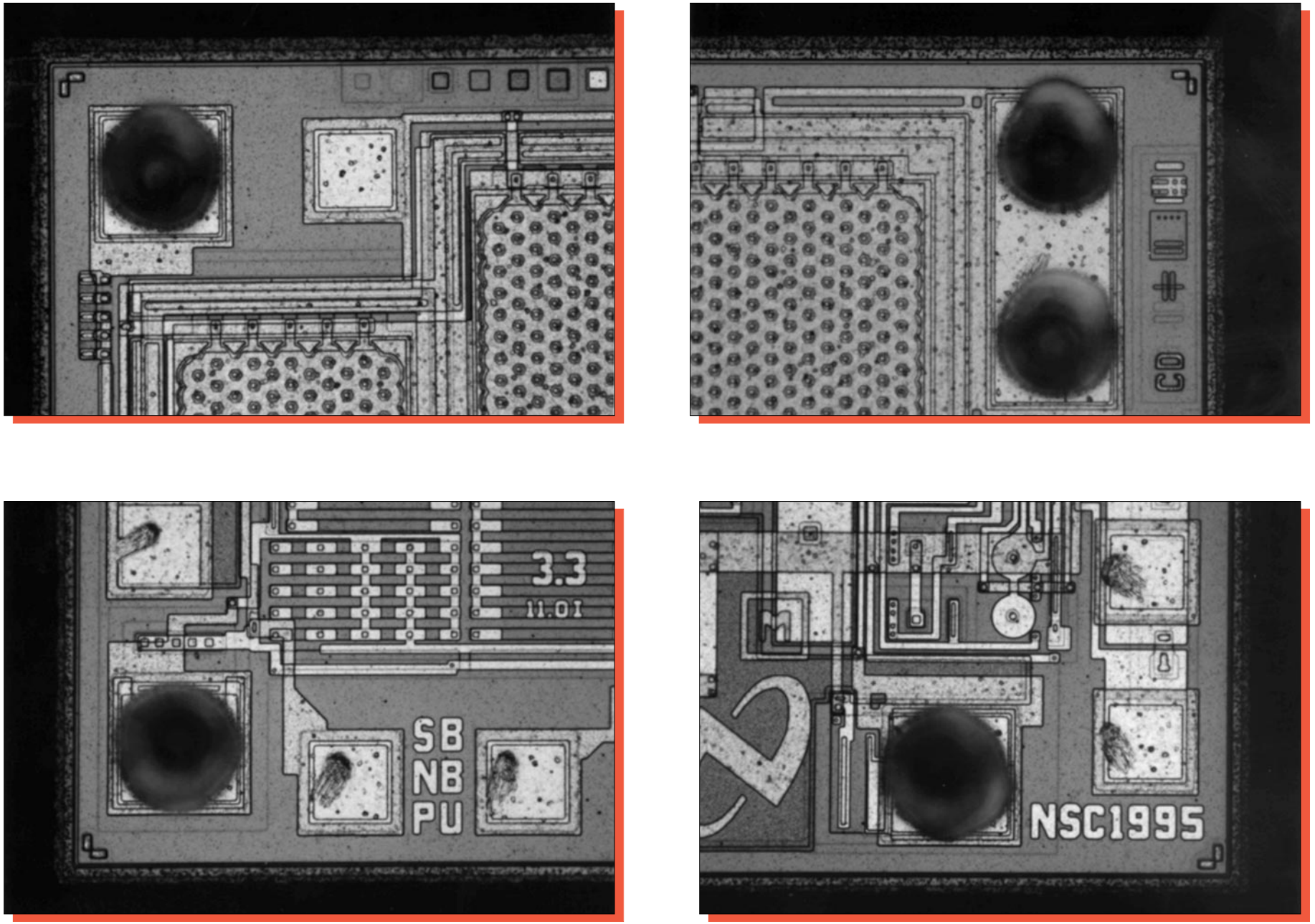
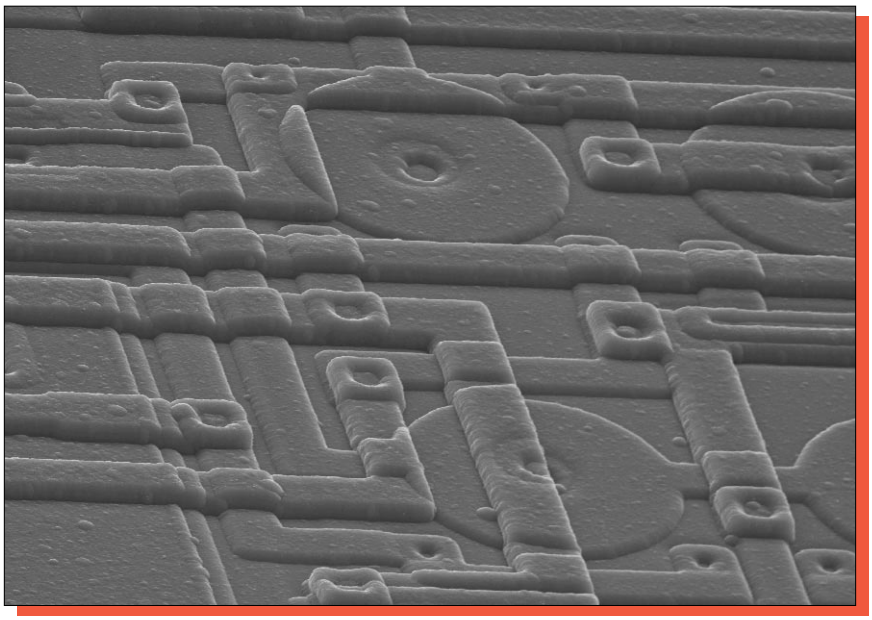
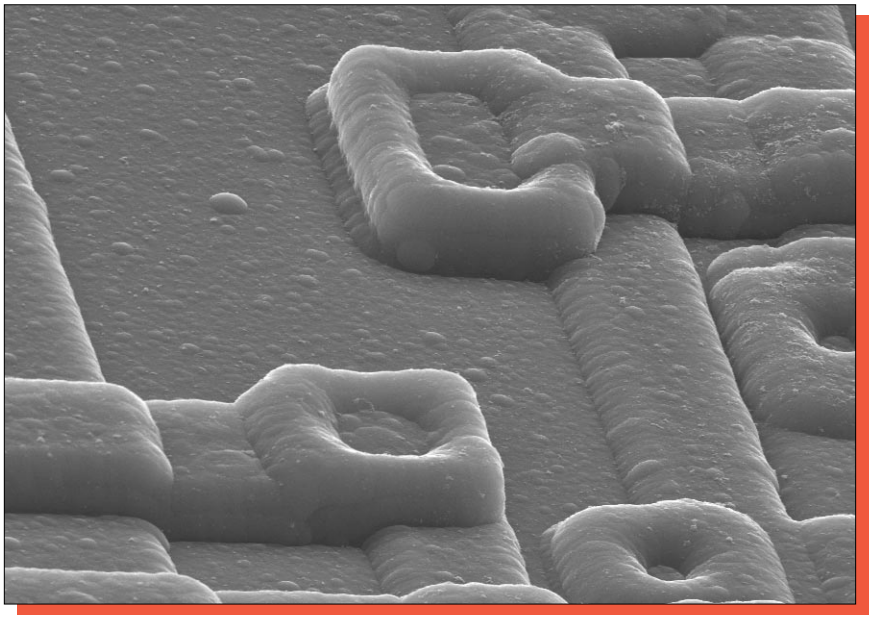


Figure 7. Optical views of the die corners on the National LM2672 device. Mag. 200x.

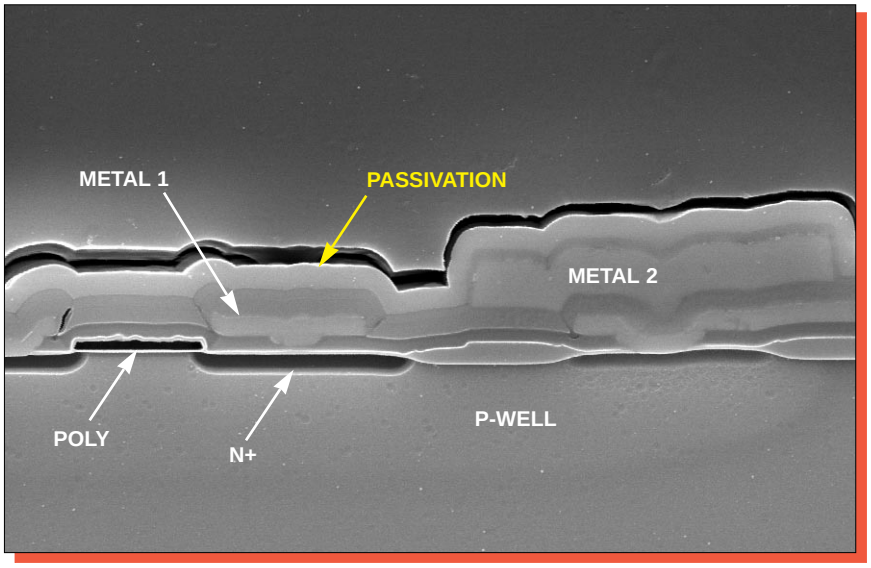


Mag. 1000x

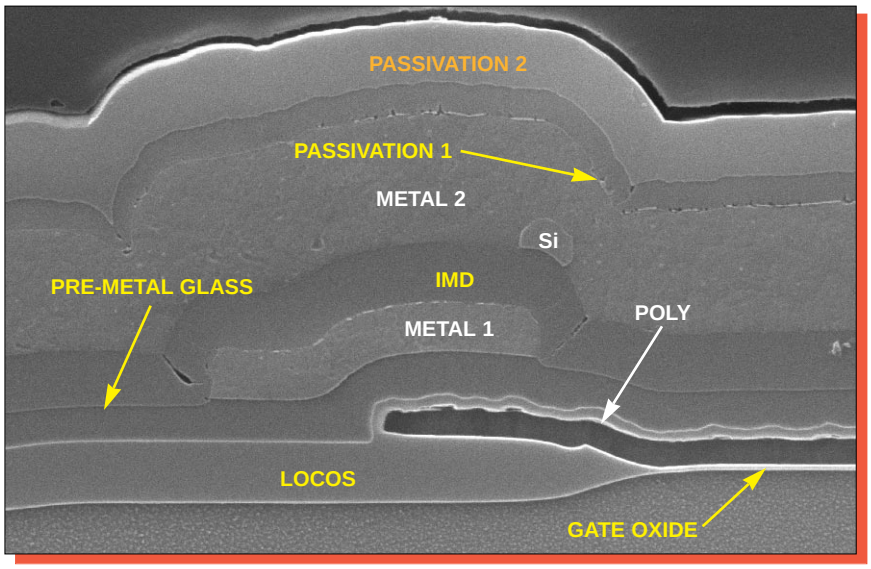


Mag. 3100x

Figure 8. SEM views illustrating passivation coverage. 60°.



Mag. 3000x



Mag. 8000x

Figure 8a. SEM section views illustrating general construction.

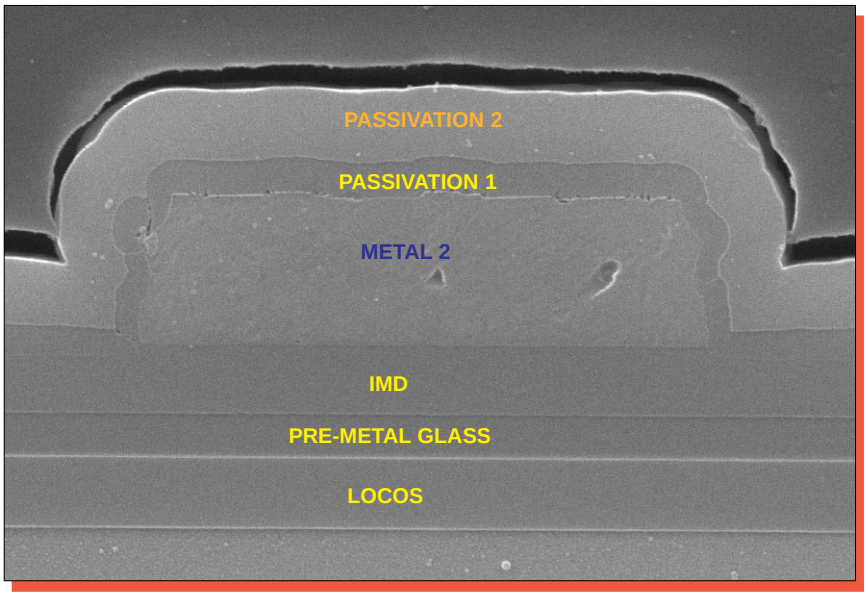
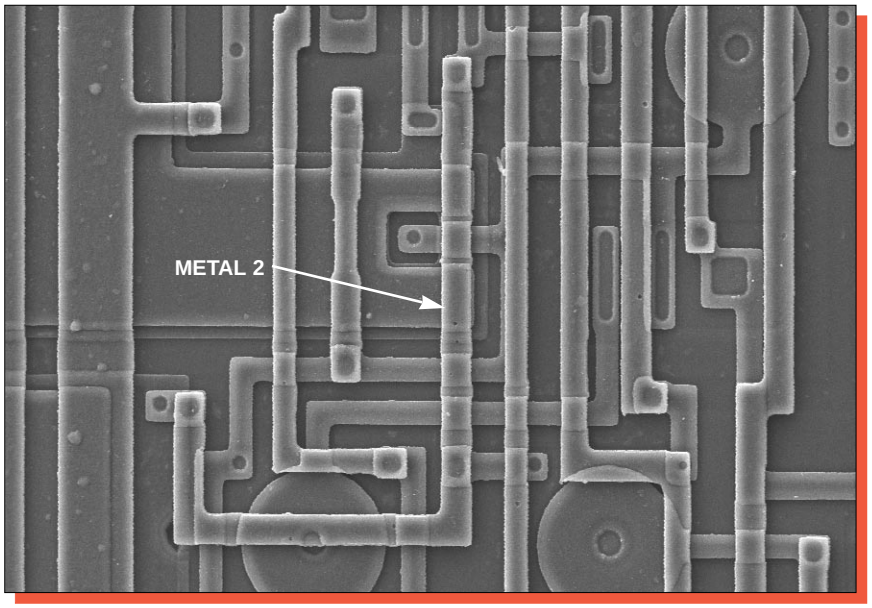
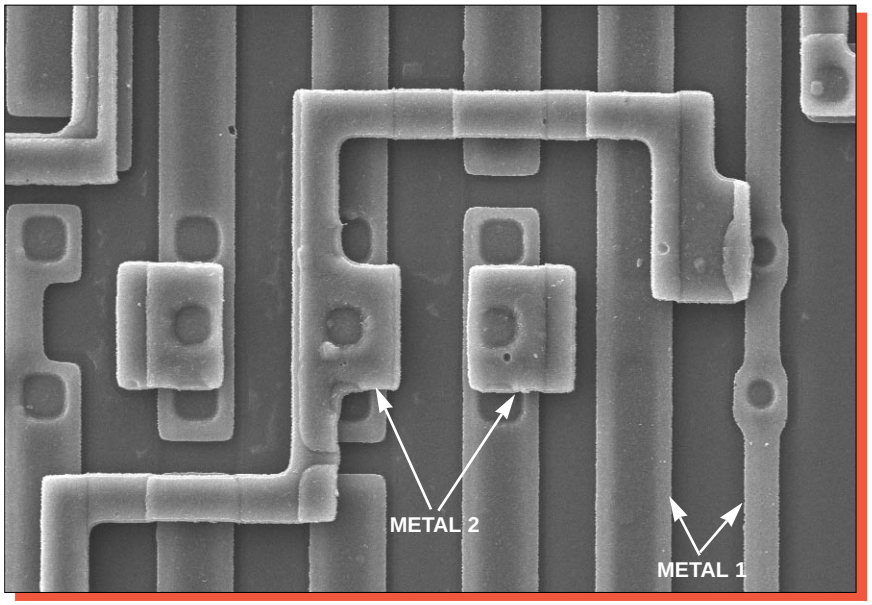


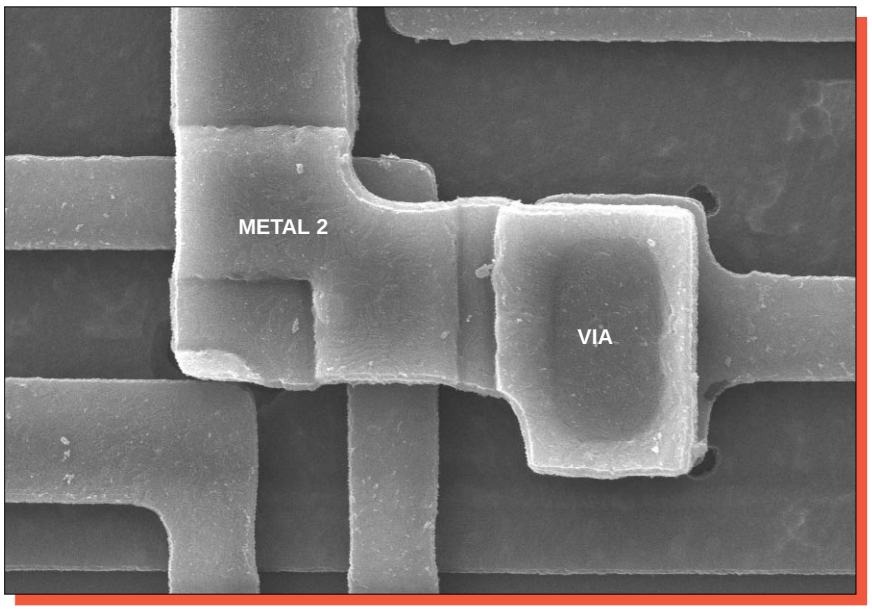
Figure 9. SEM section view of a metal 2 line profile. Mag. 10,000x.



Mag. 500x

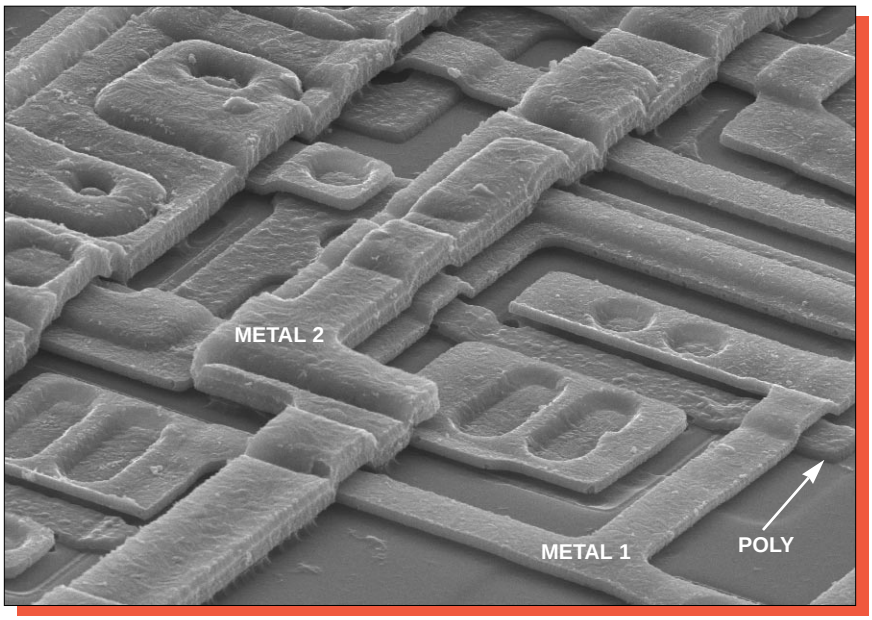


Mag. 1000x

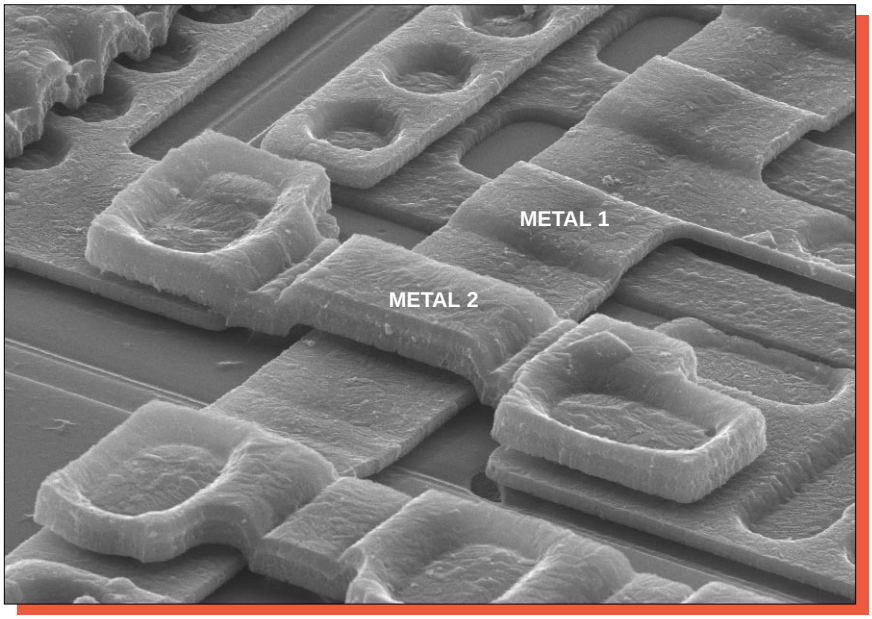


Mag. 3250x

Figure 10. Topological SEM views illustrating metal 2 patterning. 0°.



Mag. 2000x



Mag. 2700x

Figure 11. Perspective SEM views of metal 2 coverage. 60°.

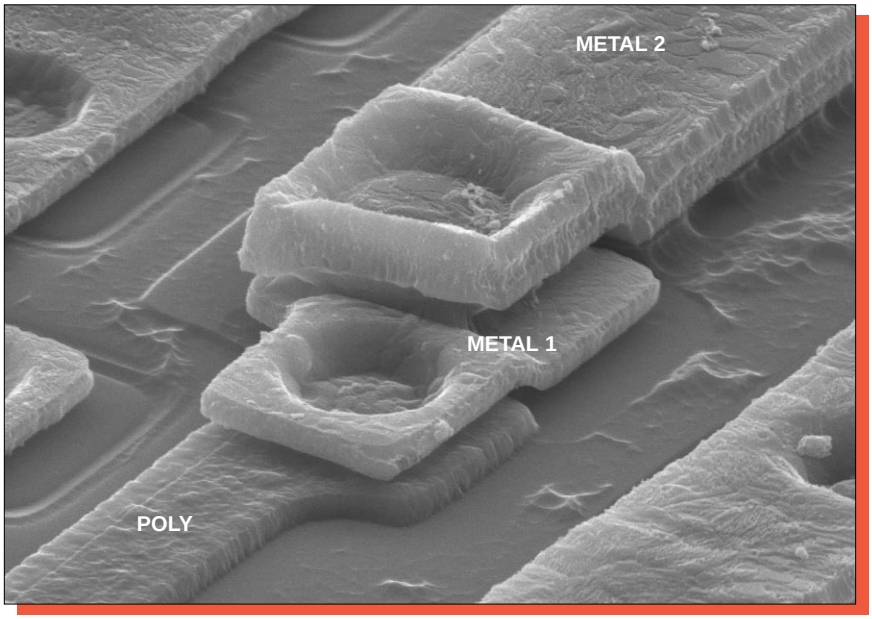


Figure 11a. Detailed SEM view of a metal 2-to-metal 1 via. Mag. 5000x, 60°.

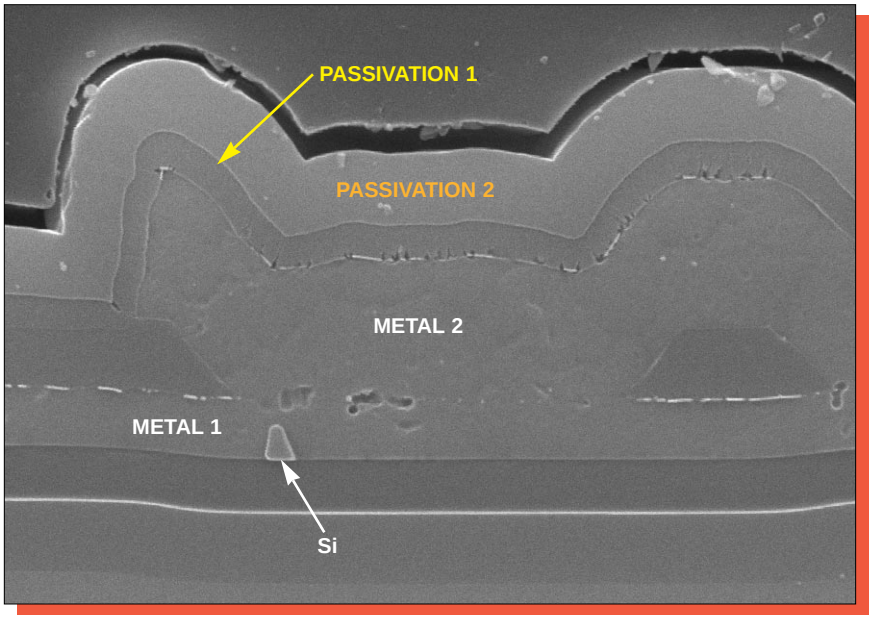
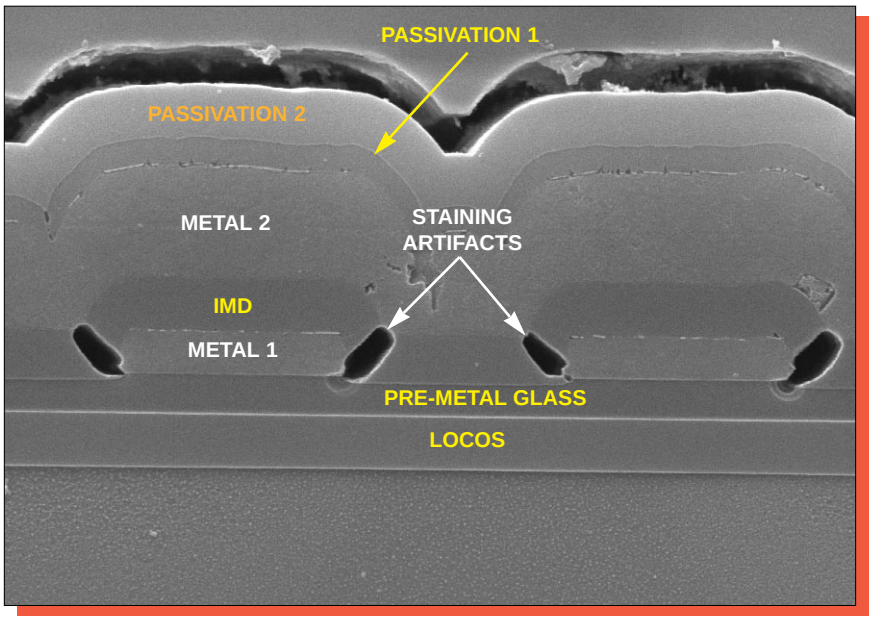
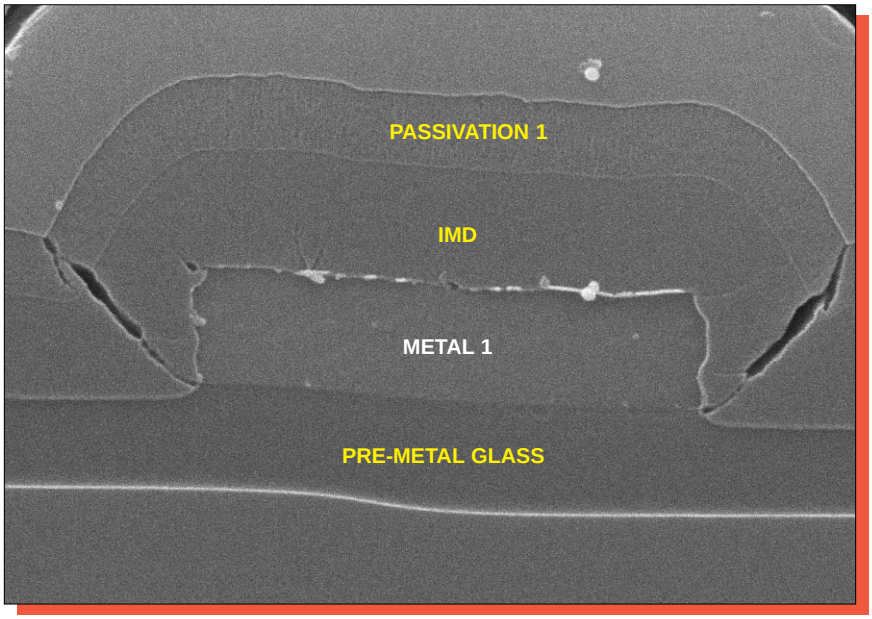


Figure 11b. SEM section view of a metal 2-to-metal 1 via. Mag. 10,000x.

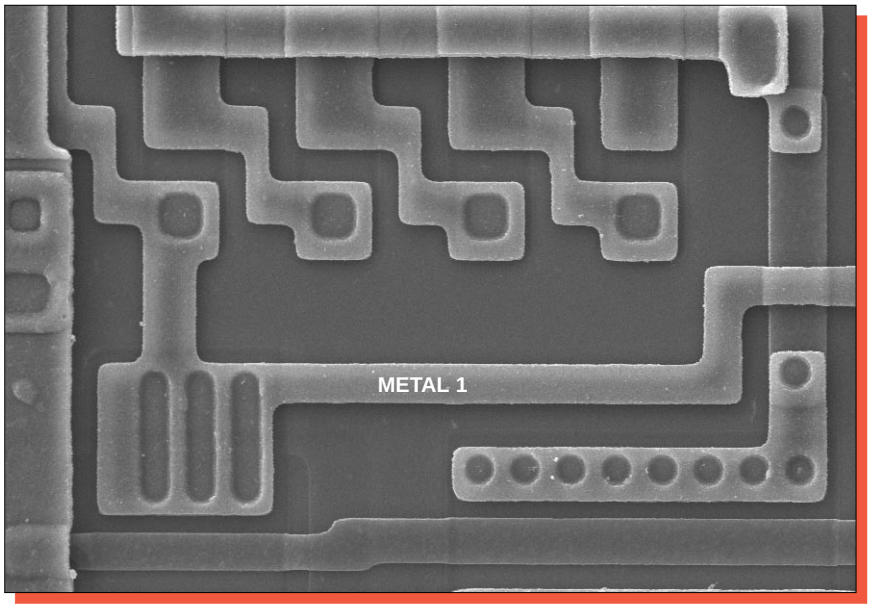


Mag. 7000x

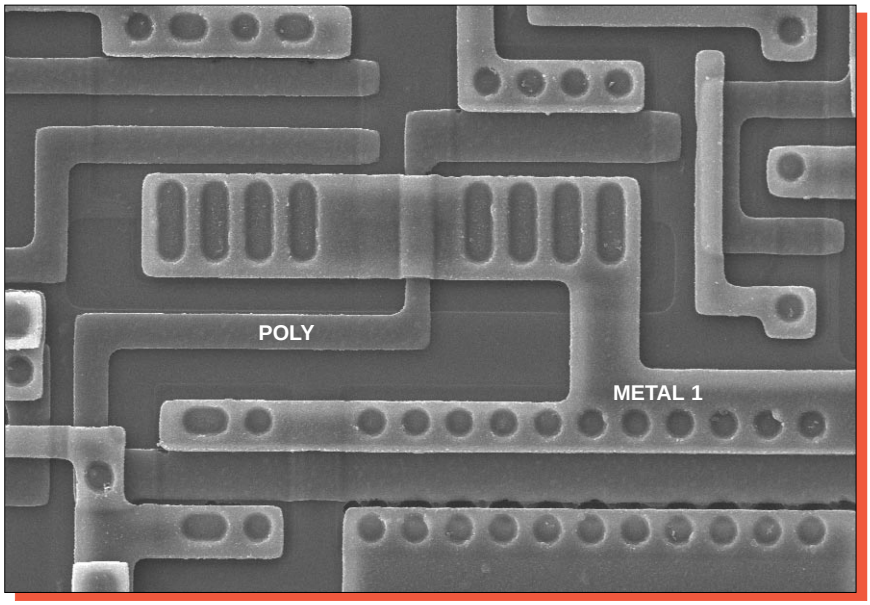


Mag. 20,000x

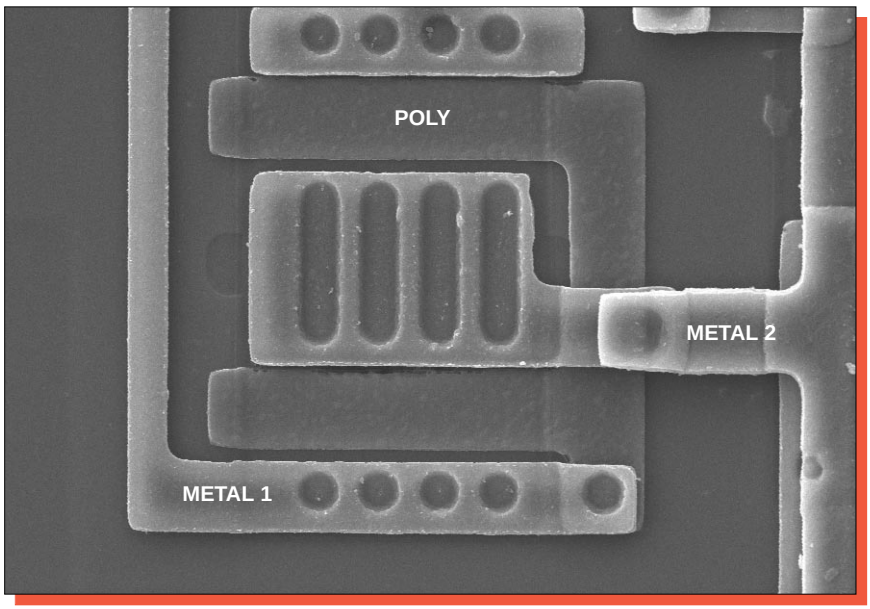
Figure 12. SEM section views of metal 1 line profiles.



Mag. 1000x

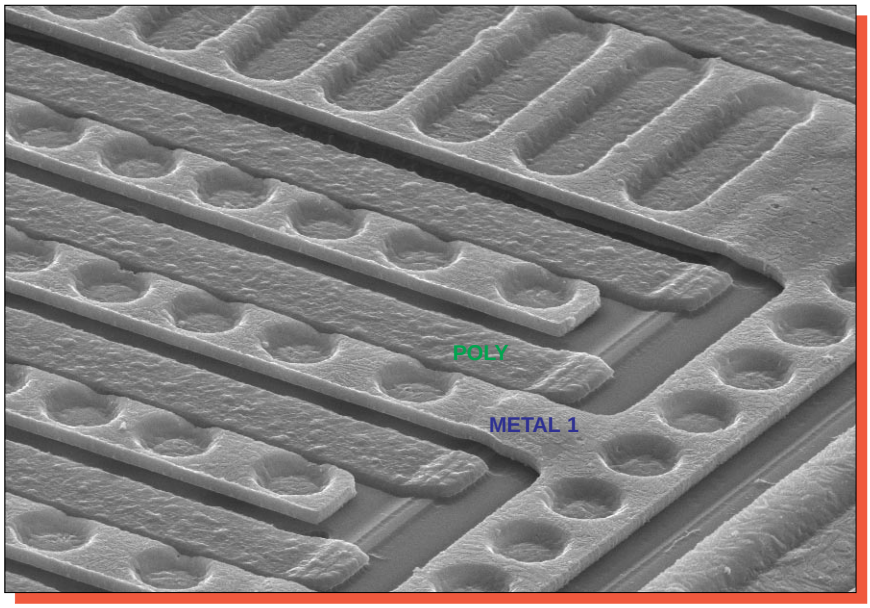


Mag. 1000x

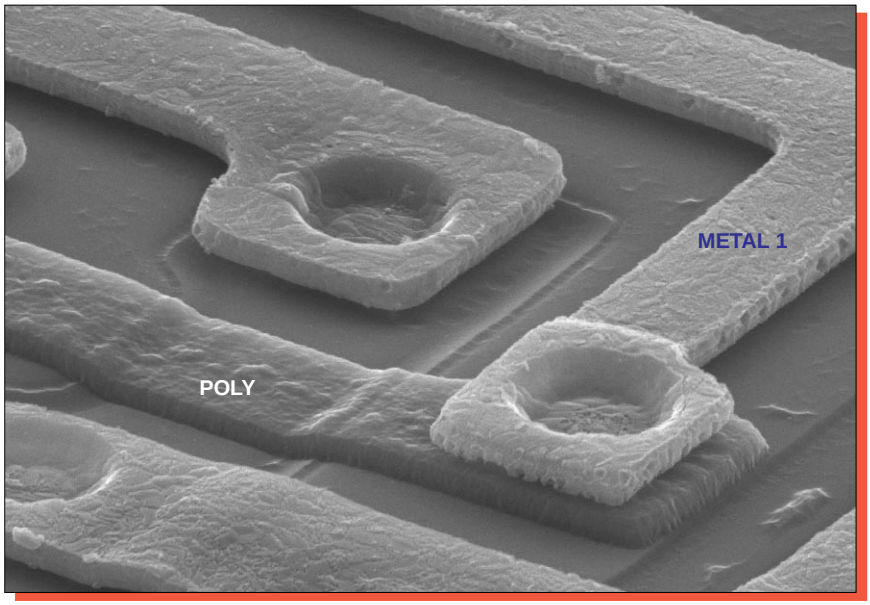


Mag. 1300x

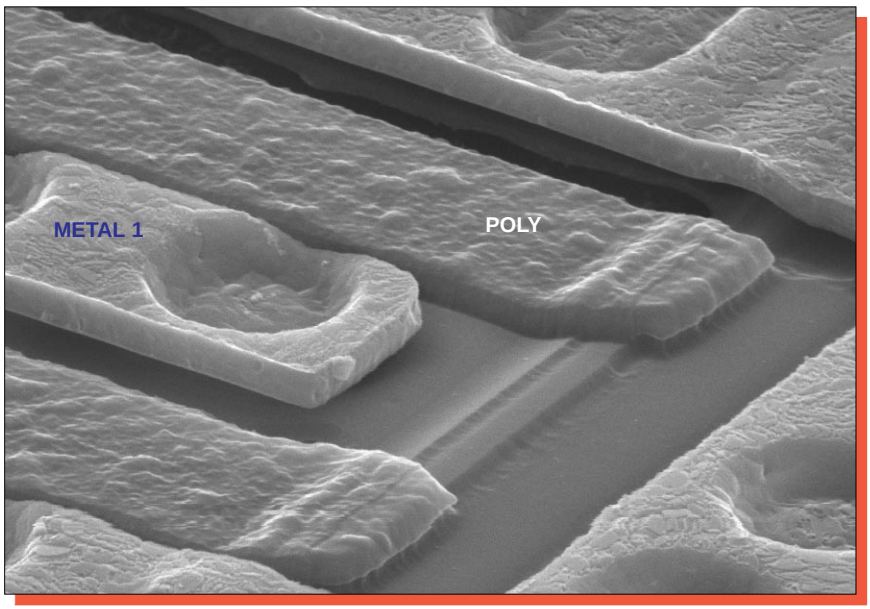
Figure 13. Topological SEM views illustrating metal 1 patterning. 0°.



Mag. 2400x

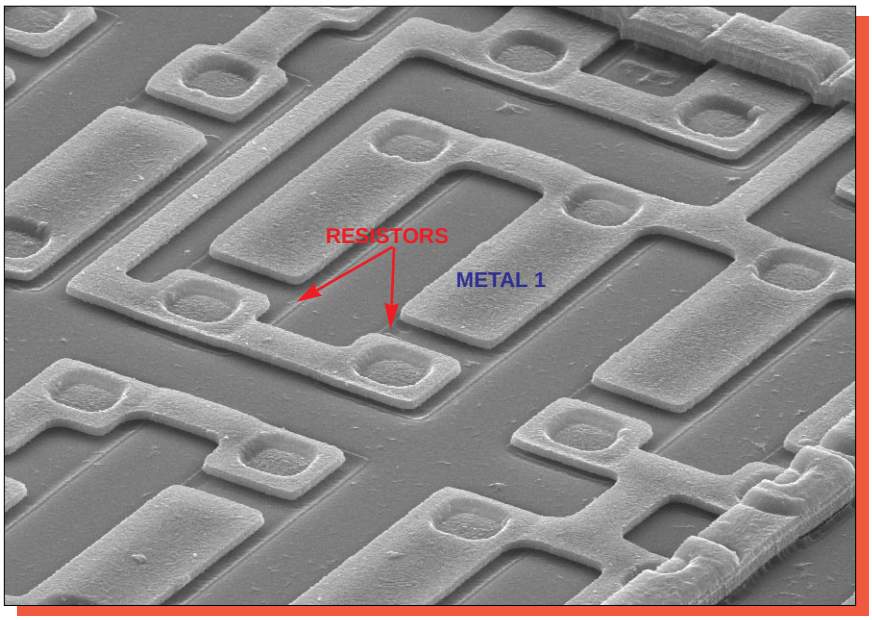


Mag. 5000x

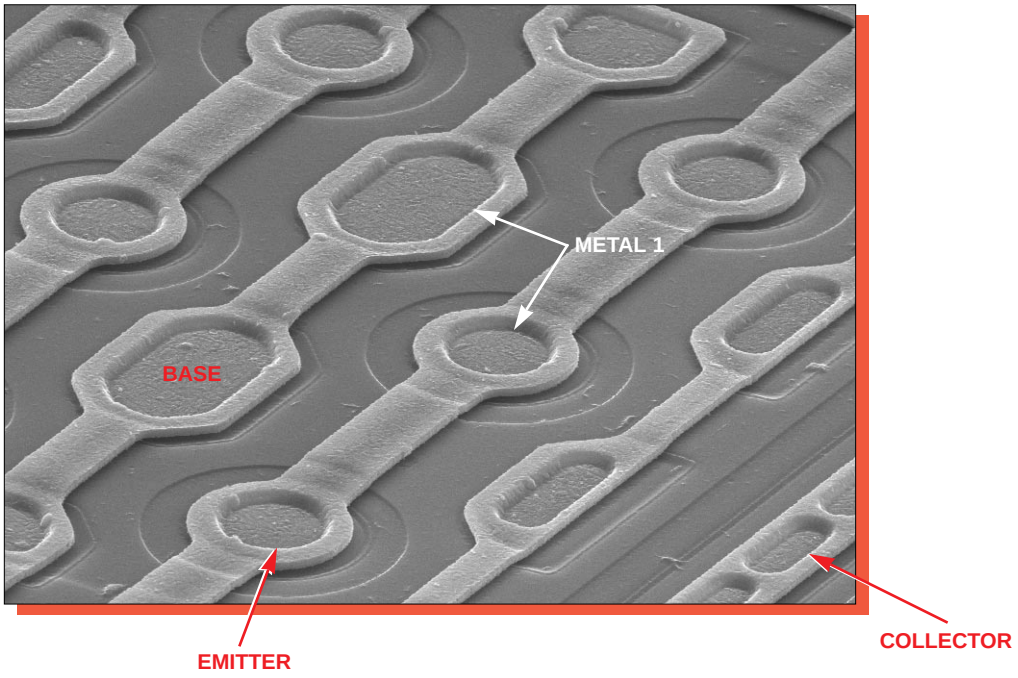


Mag. 6500x

Figure 14. Perspective SEM views of metal 1 coverage. 60°.

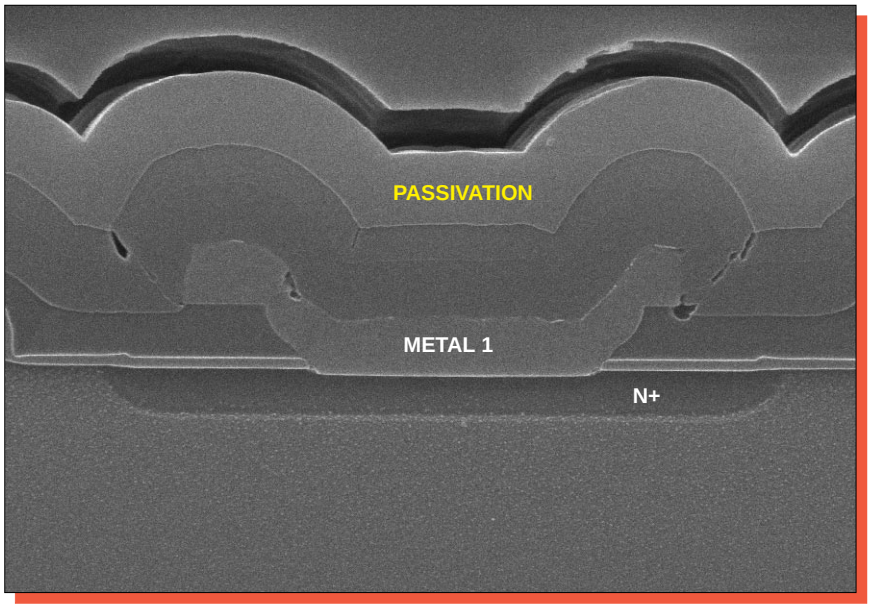


resistors

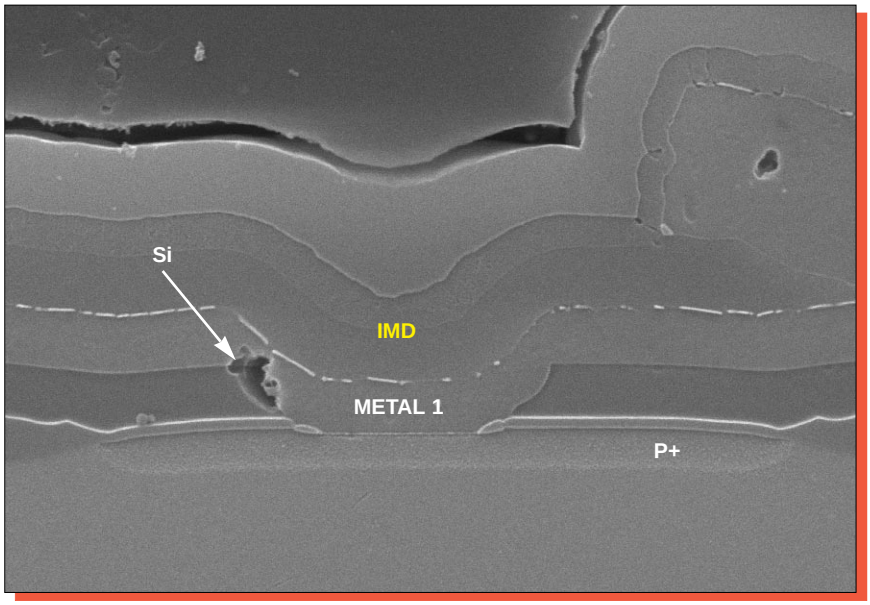


NPN transistor

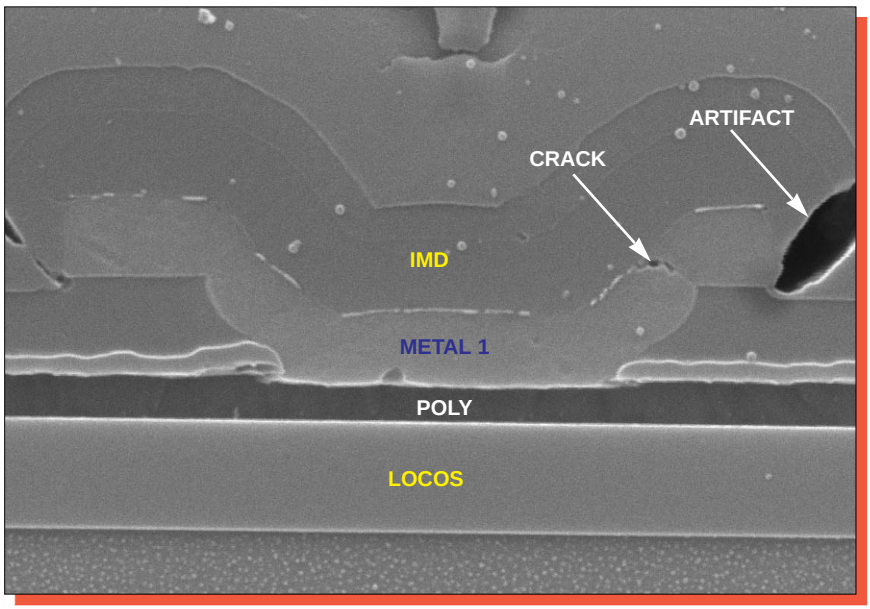
Figure 14a. Additional SEM views of metal 1 coverage. Mag. 1600x, 60°.



metal 1-to-N+,
Mag. 10,000x

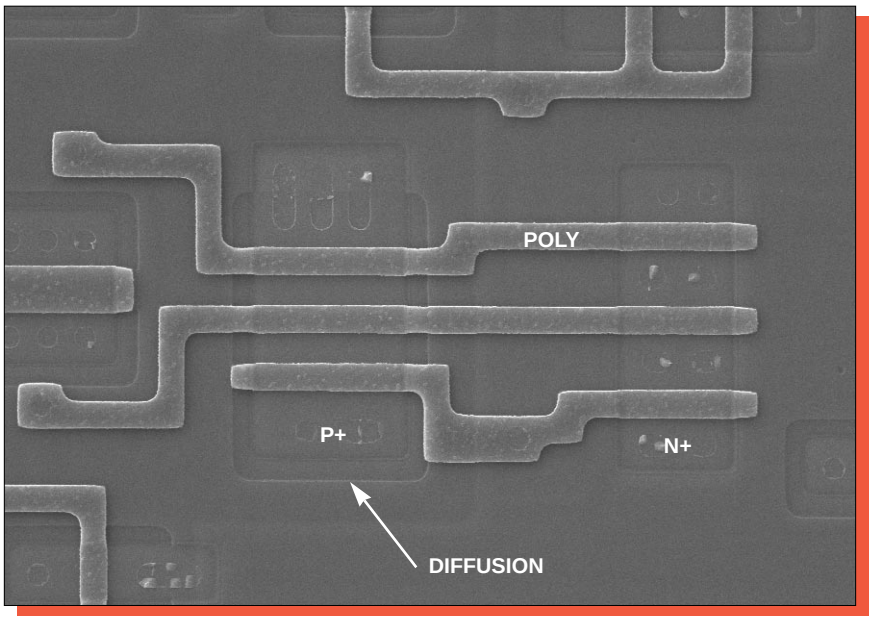


metal 1-to-P+,
Mag. 10,000x

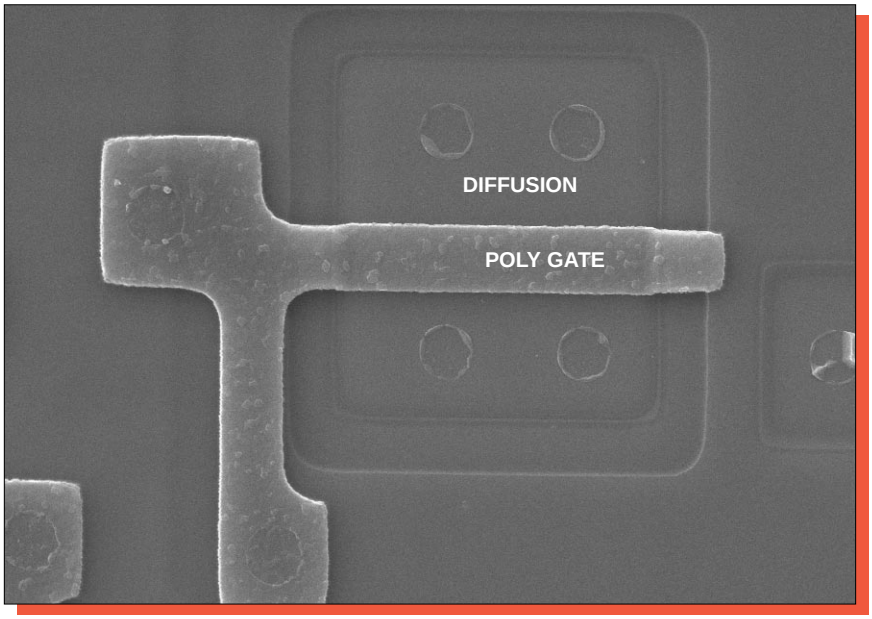


metal 1-to-poly,
Mag. 14,000x

Figure 15. SEM section views of typical contacts.

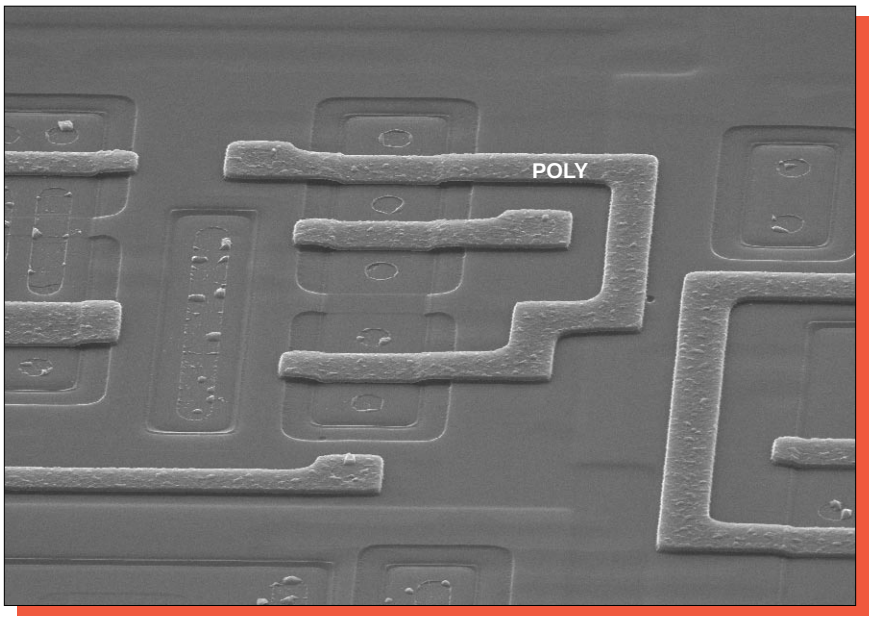


Mag. 800x

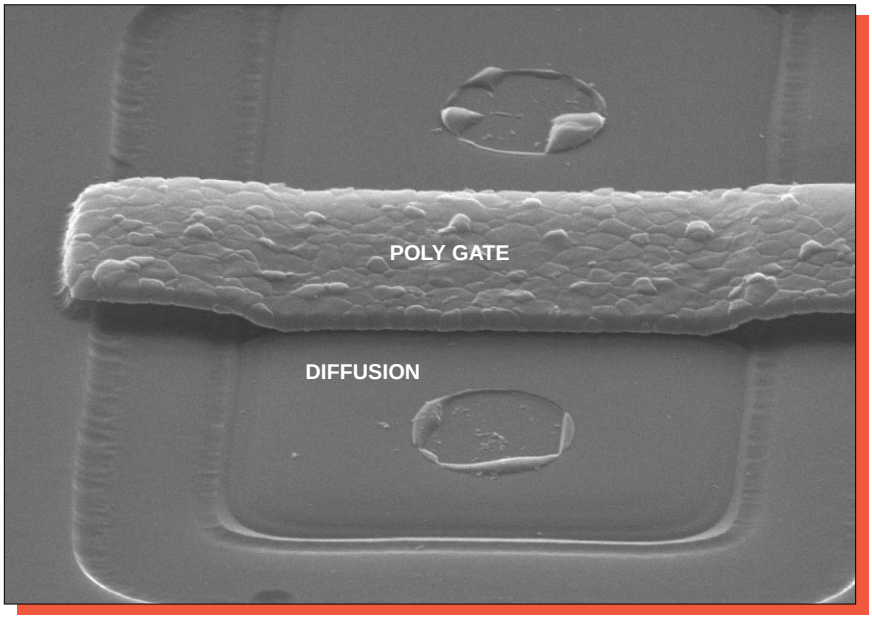


Mag. 2000x

Figure 16. Topological SEM views illustrating poly patterning. 0°.

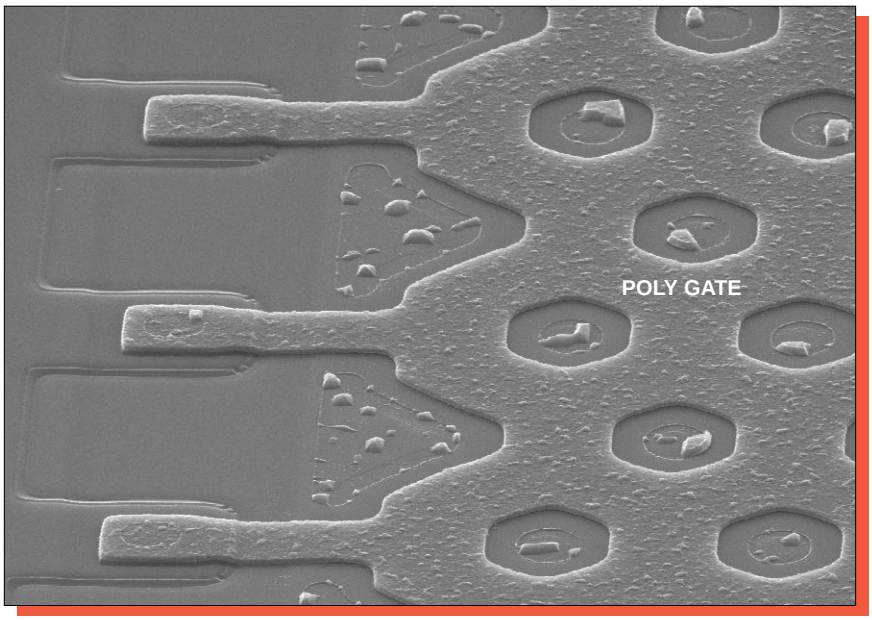


Mag. 1300x

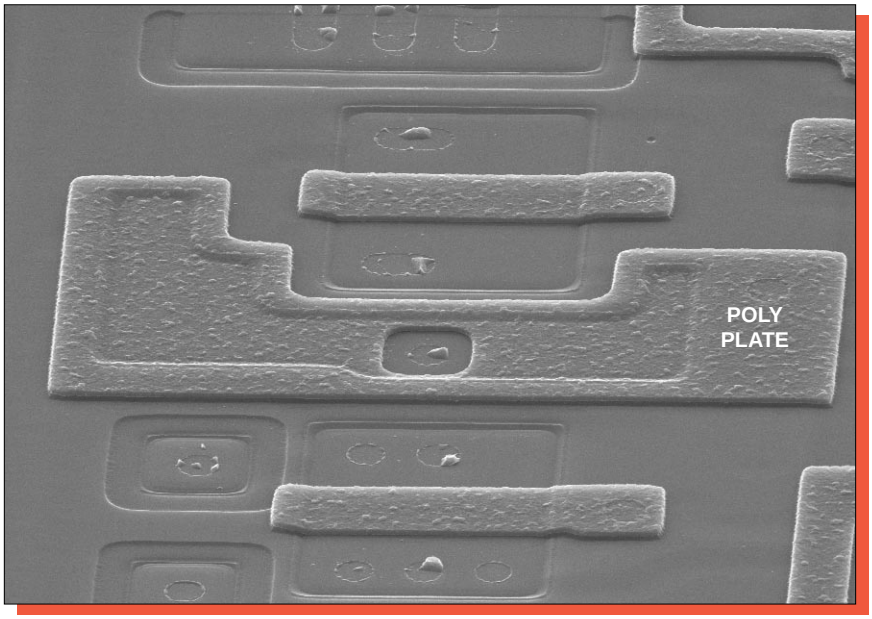


Mag. 6500x

Figure 17. Perspective SEM views of poly coverage. 60°.

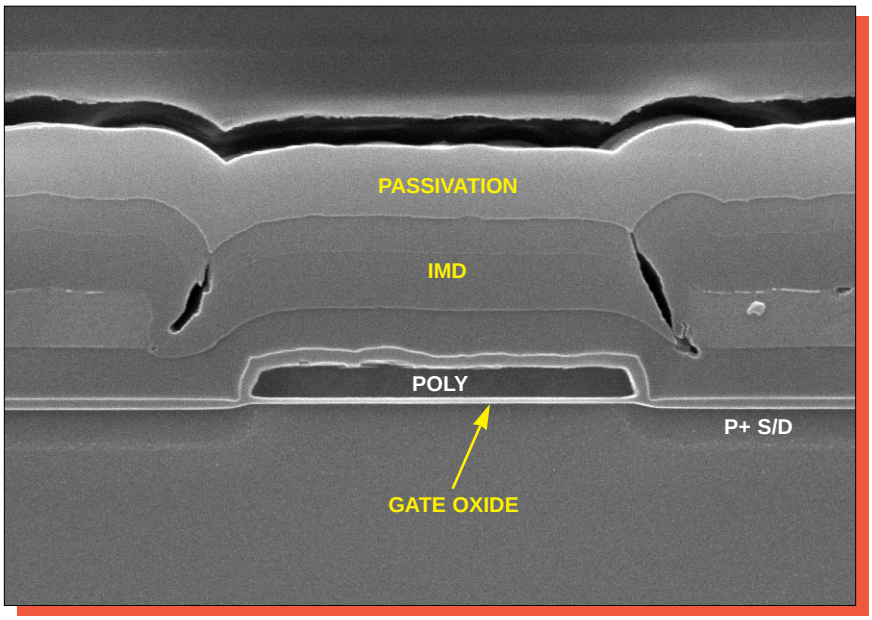


power HEXFET

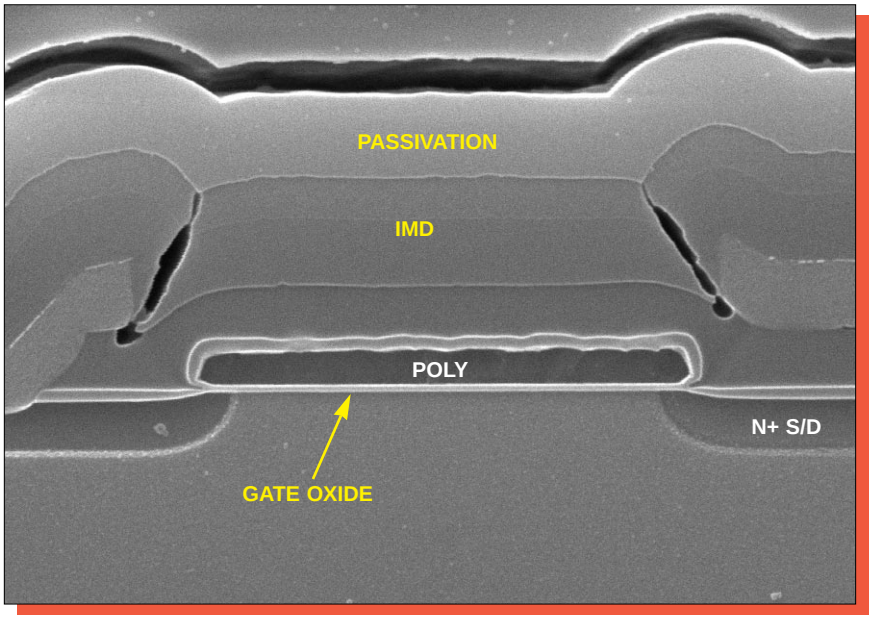


poly capacitor

Figure 17a. Additional SEM views of poly structures. Mag. 1600x, 60°.

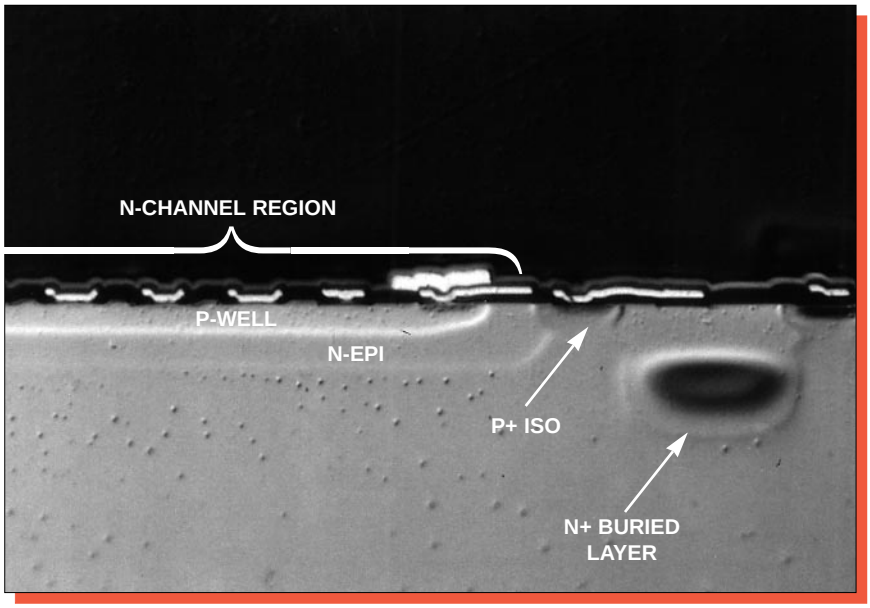


Mag. 10,000x

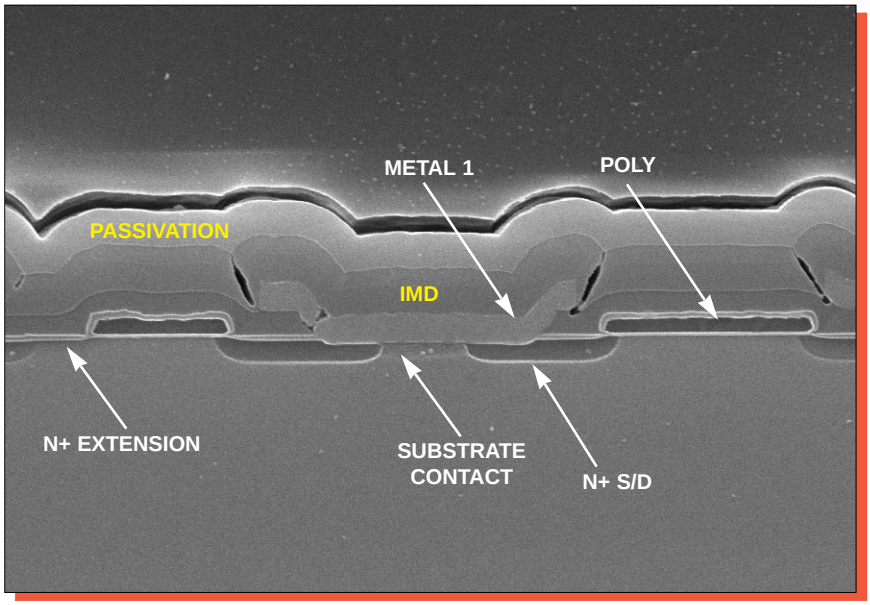


Mag. 12,000x

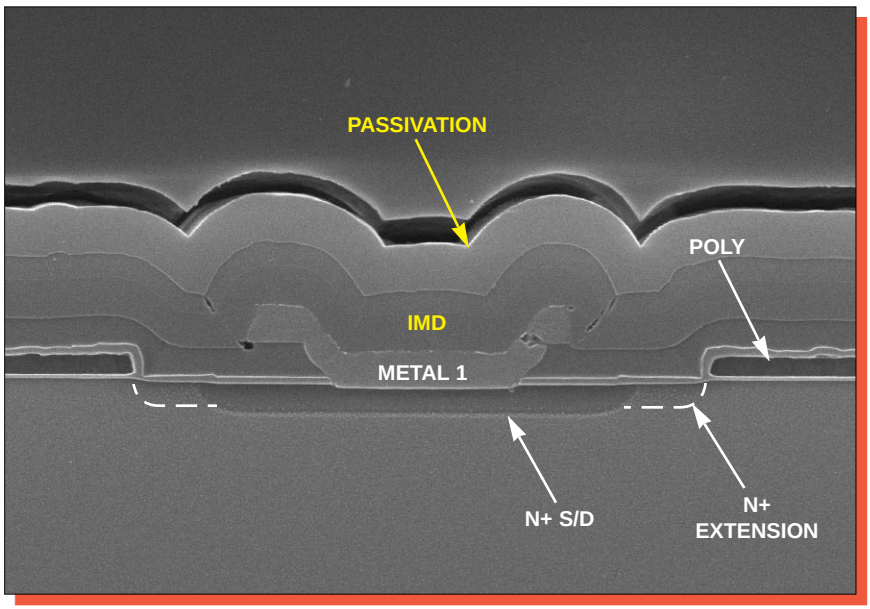
Figure 18. SEM section views of typical MOS transistors.



Mag. 800x

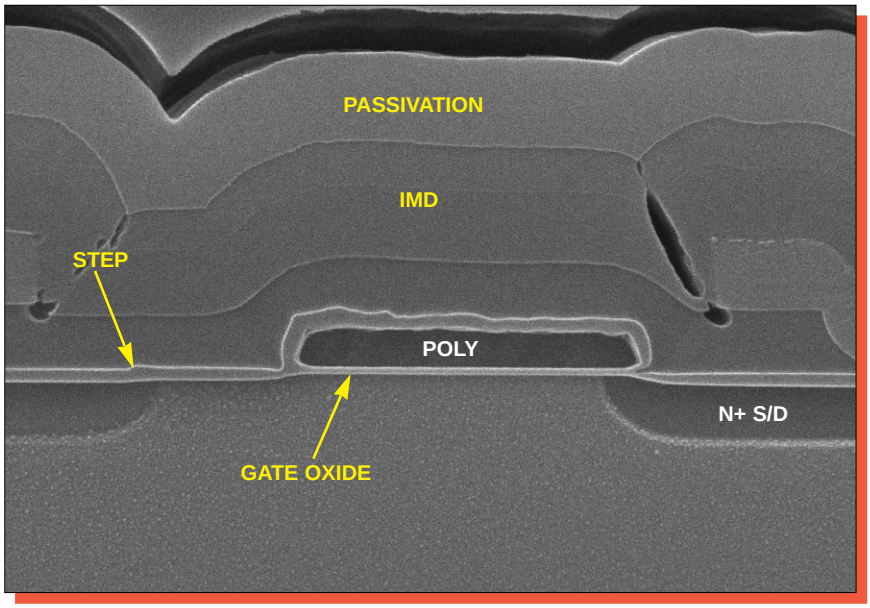


Mag. 6500x

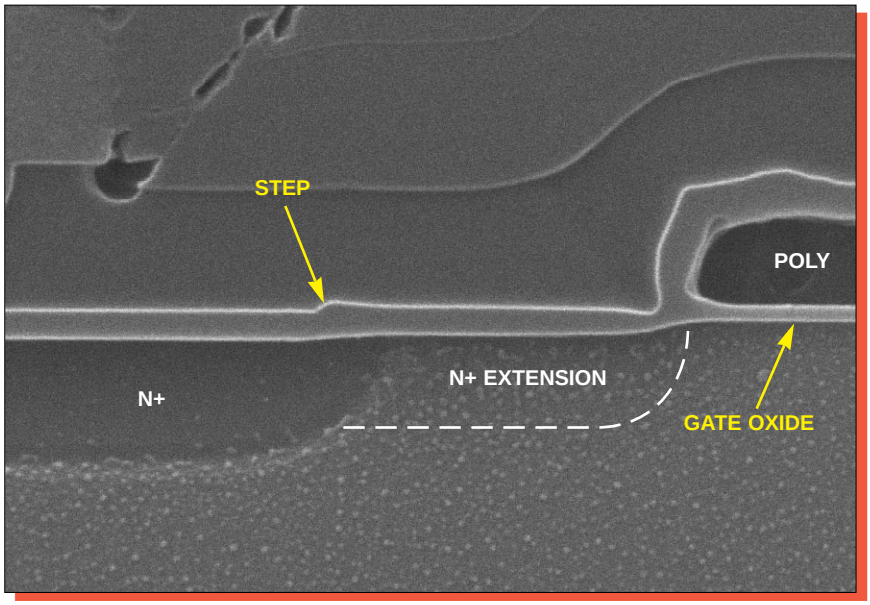


Mag. 8000x

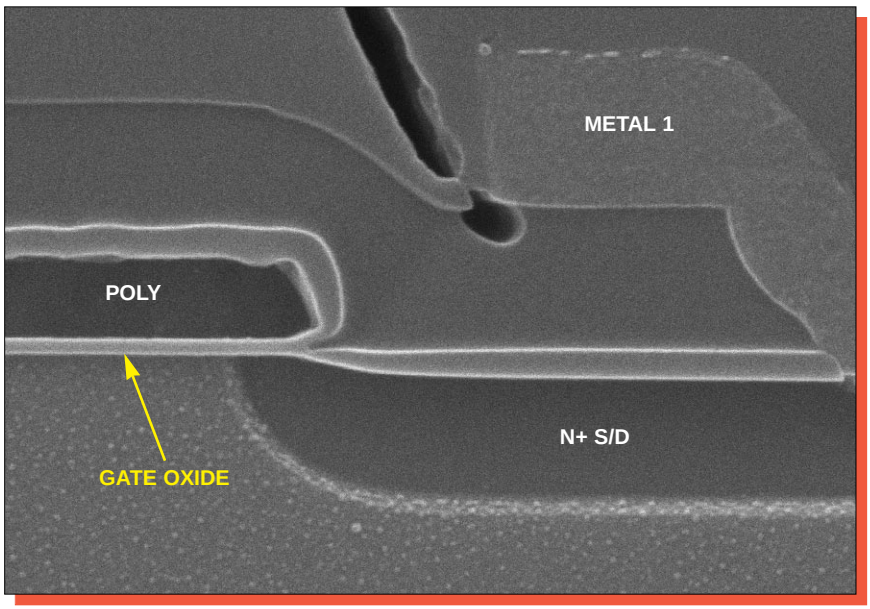
Figure 19. SEM section views of various N-channel structures.



Mag. 12,000x

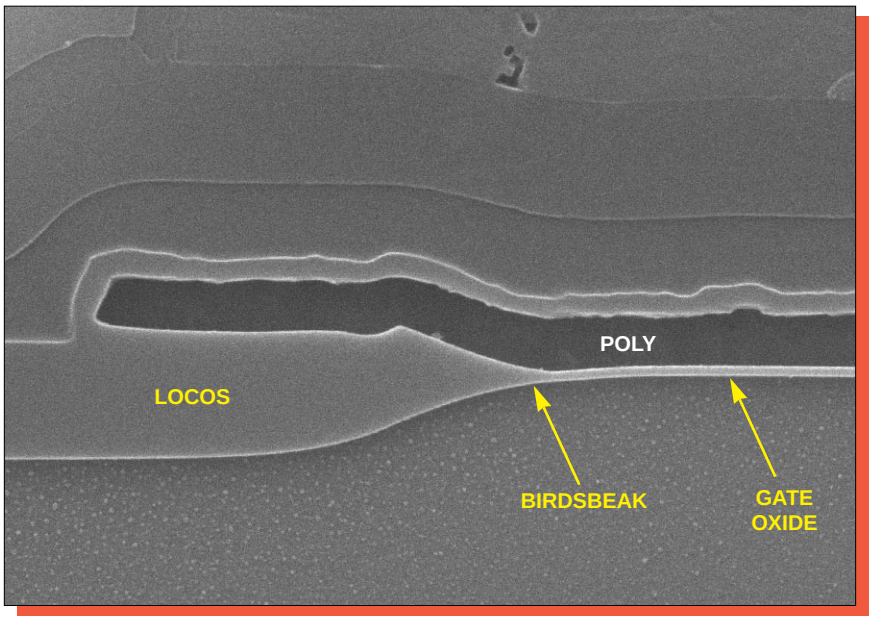


Mag. 26,000x



Mag. 26,000x

Figure 20. Detailed SEM section views of extended shallow source transistor structure.



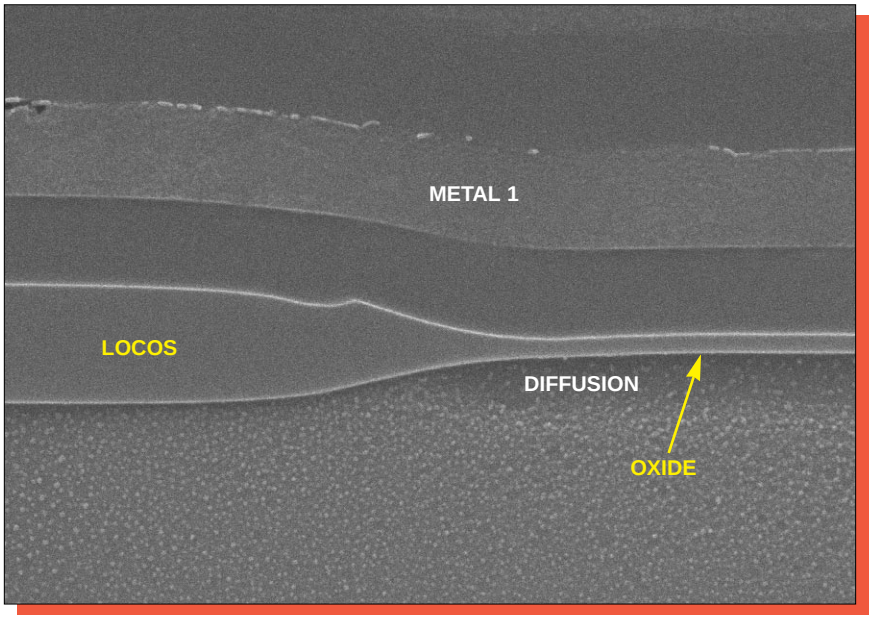
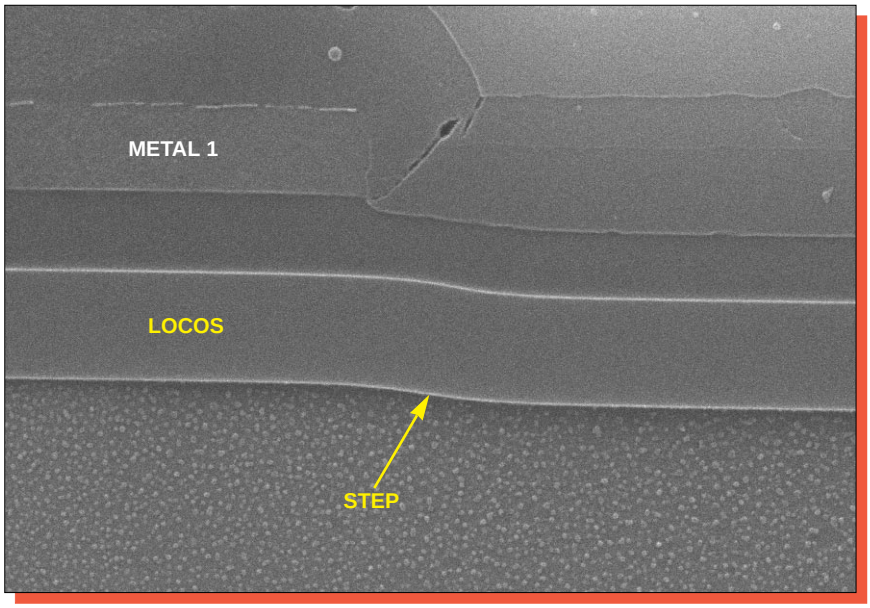
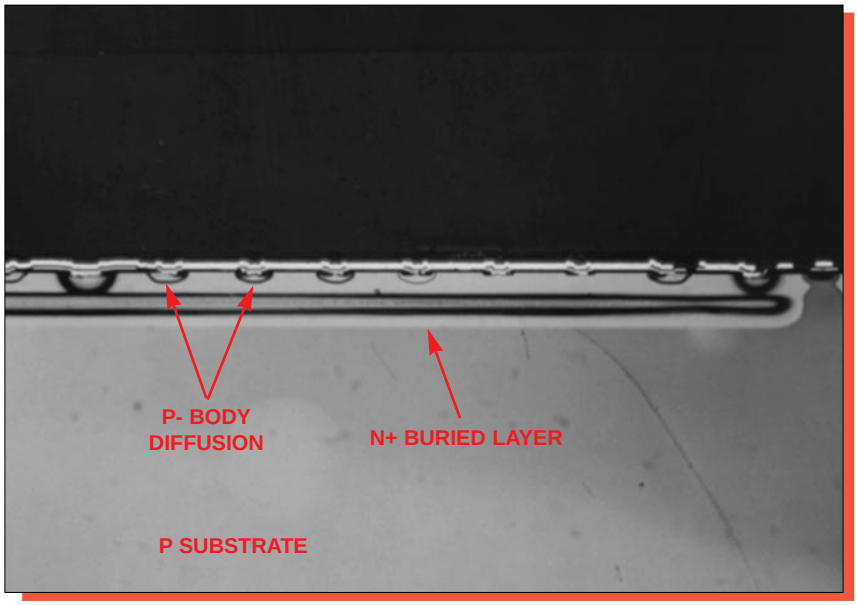


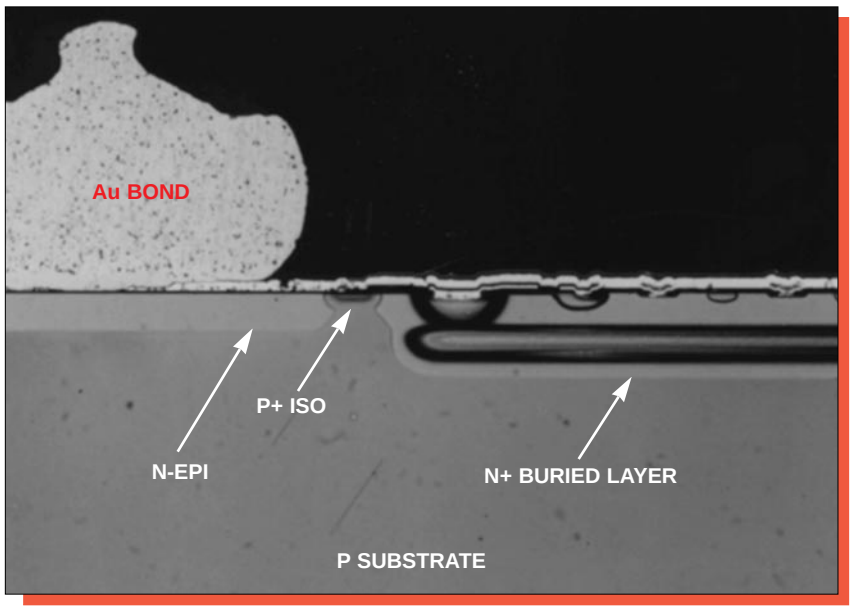
Figure 21. SEM section views of local oxide birdbeak profiles. Mag. 16,000x.



Mag. 14,000x

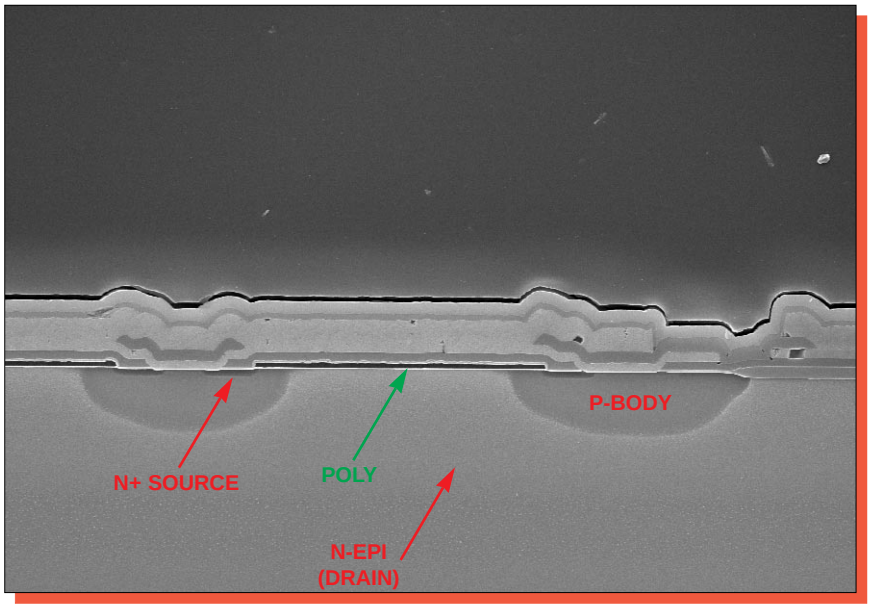


DMOS,
Mag. 320x

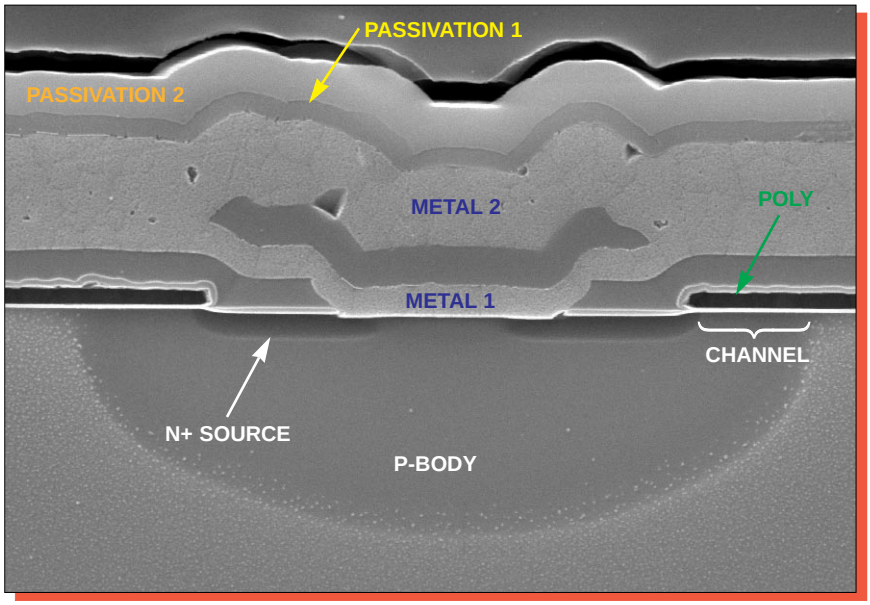


Mag. 500x

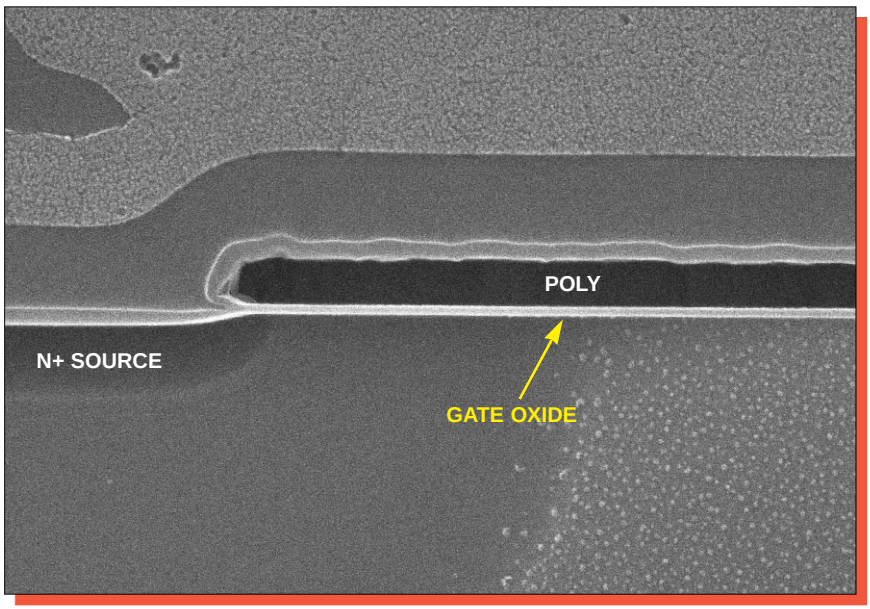
Figure 22. Optical and SEM section views of the well structure.



Mag. 1500x

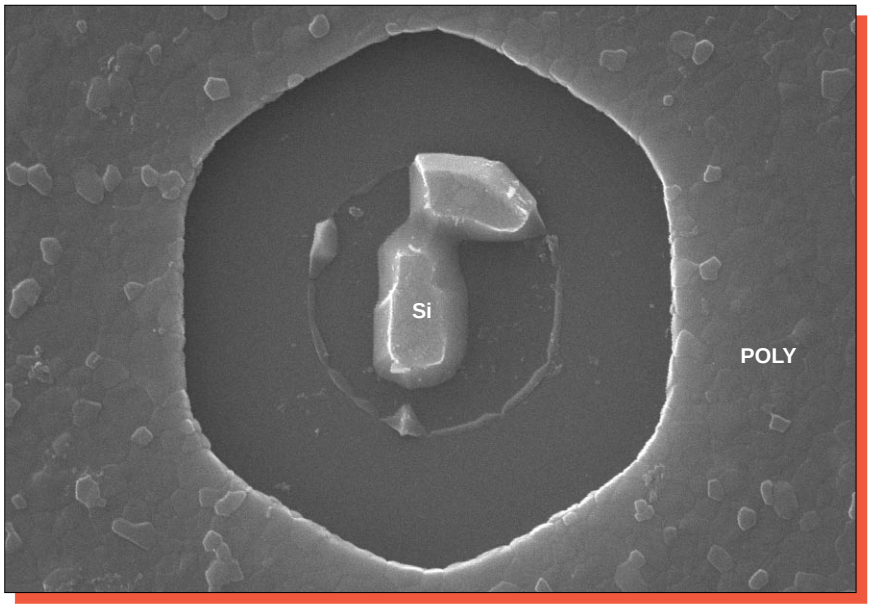


Mag. 6000x

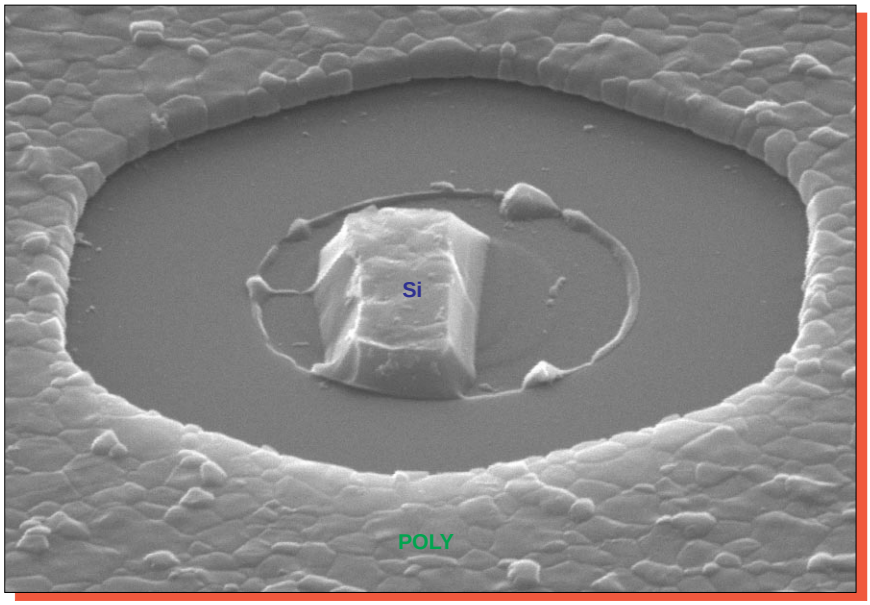


Mag. 16,000x

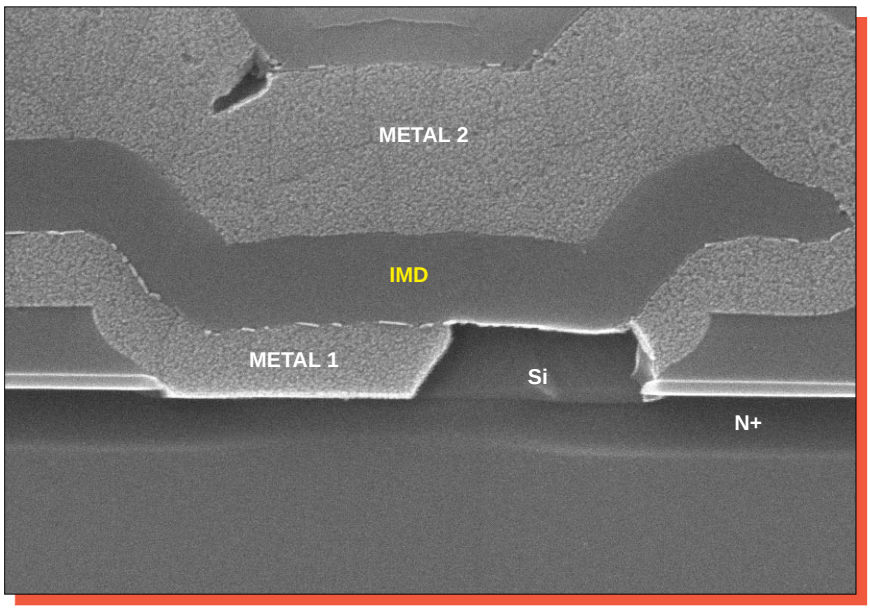
Figure 23. SEM section views of the DMOS Power HEXFET structure.



Mag. 10,000x, 0°



Mag. 10,000x, 60°



Mag. 13,000x

Figure 24. SEM views illustrating the silicon mound growth in the HEXFET structures.

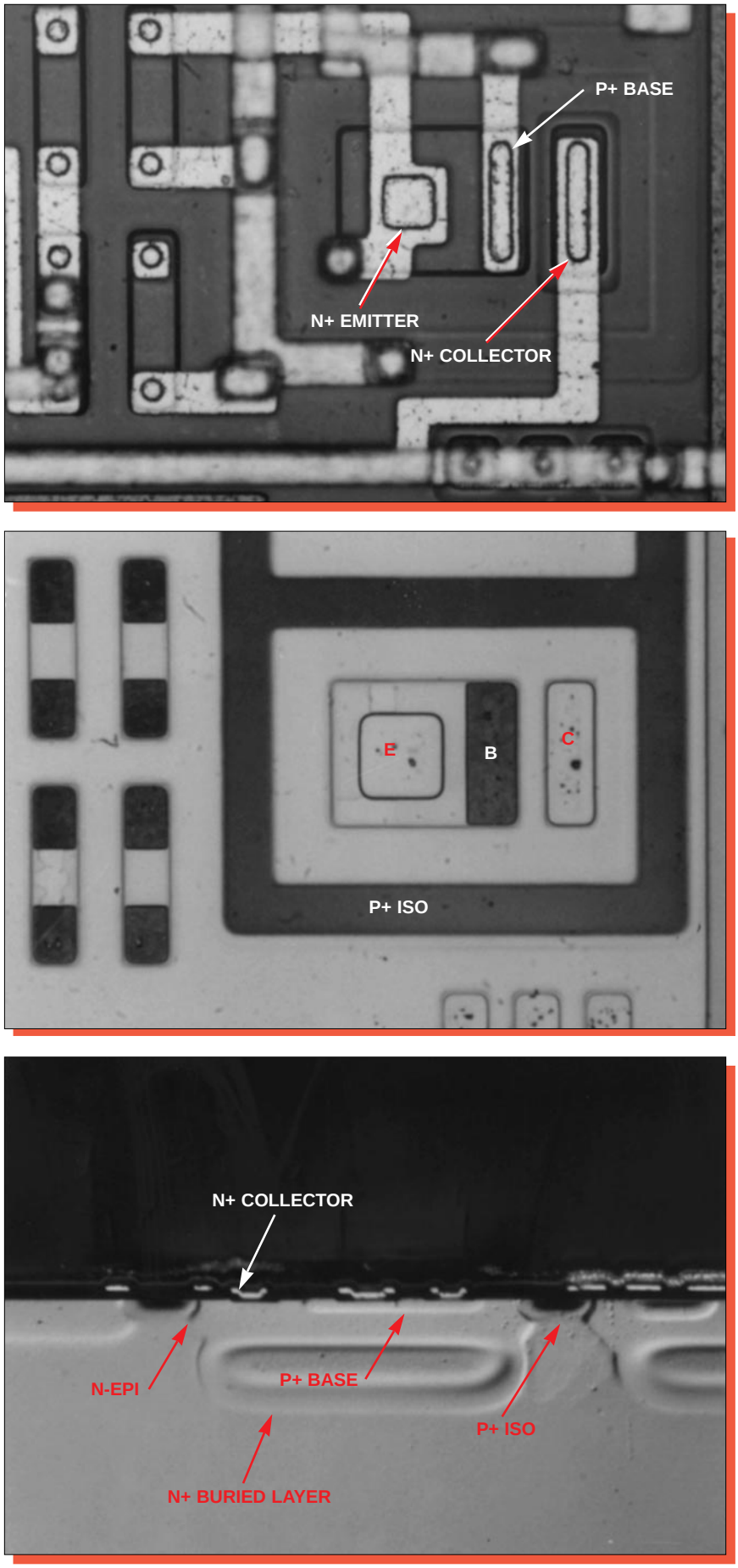


Figure 25. Optical views of an NPN transistor. Mag. 800x.

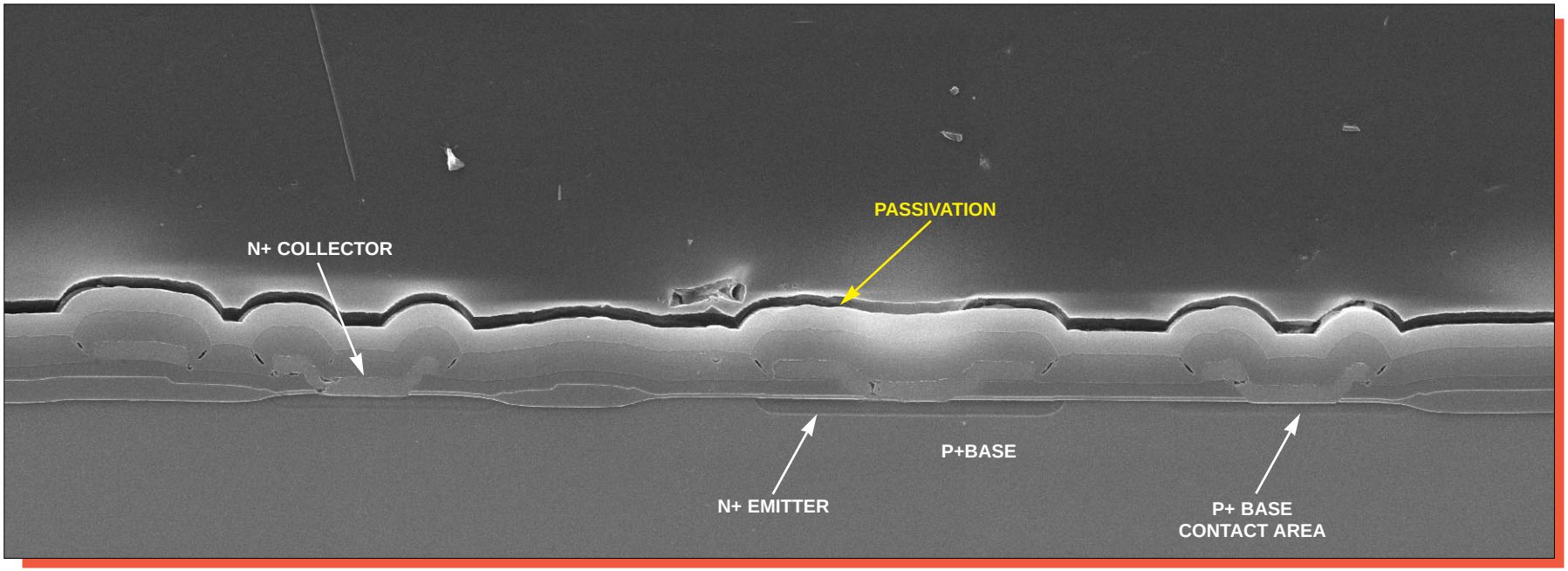
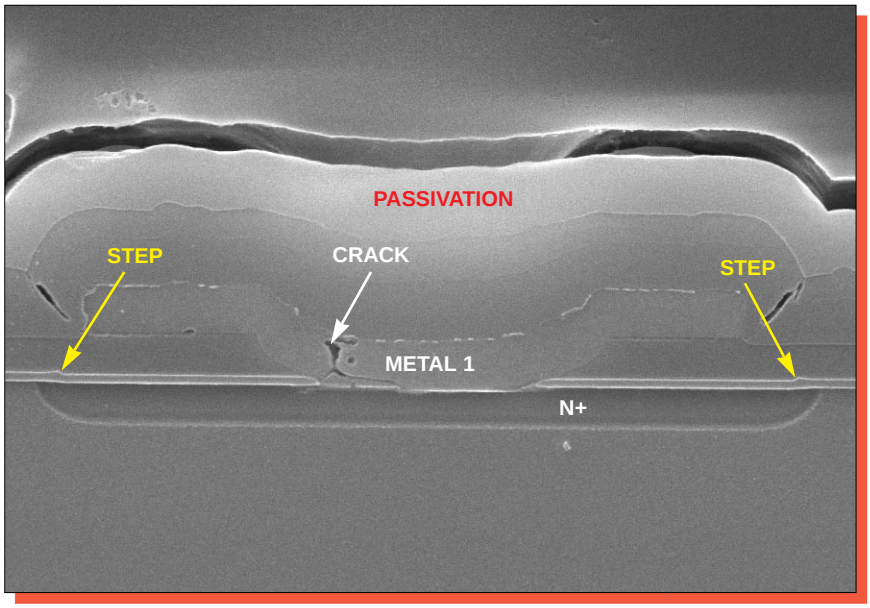
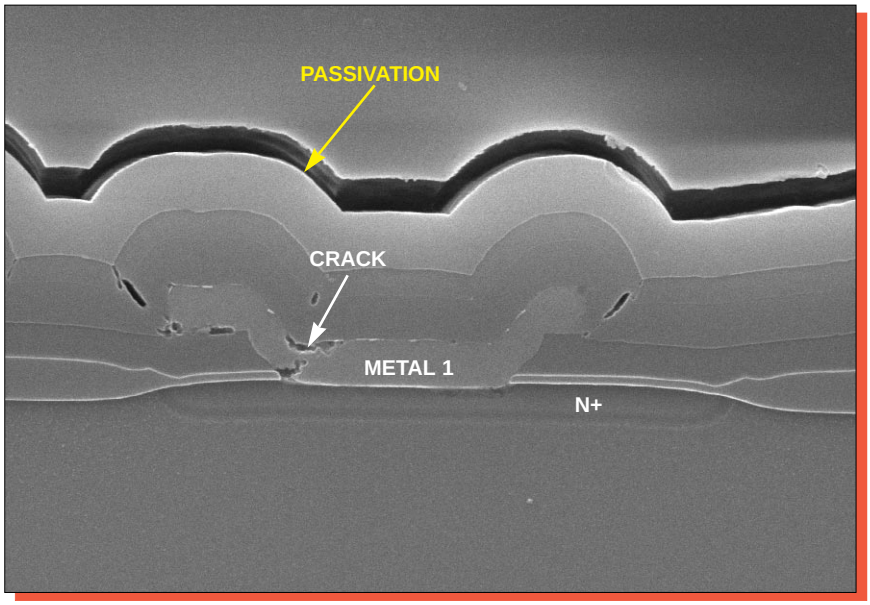


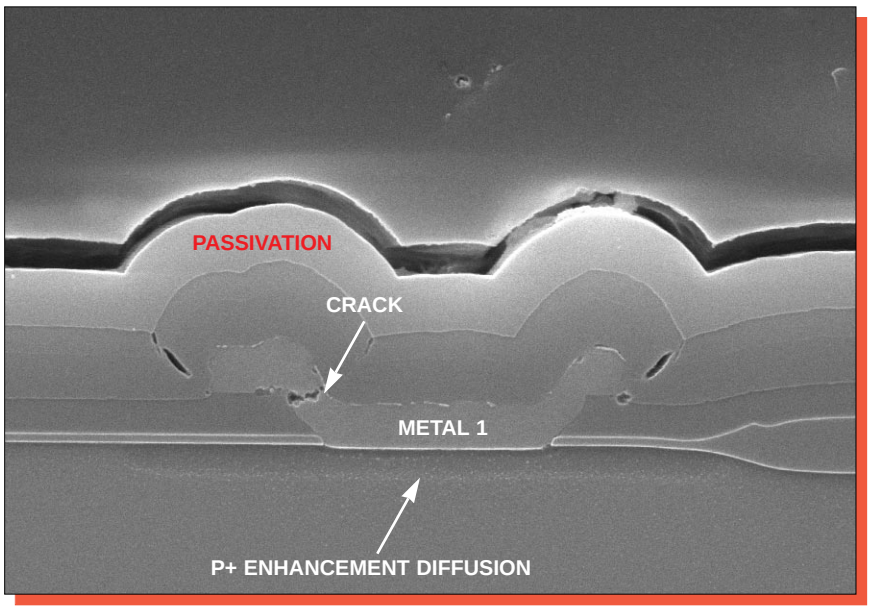
Figure 26. SEM section view of an NPN transistor. Mag. 3500x.



emitter

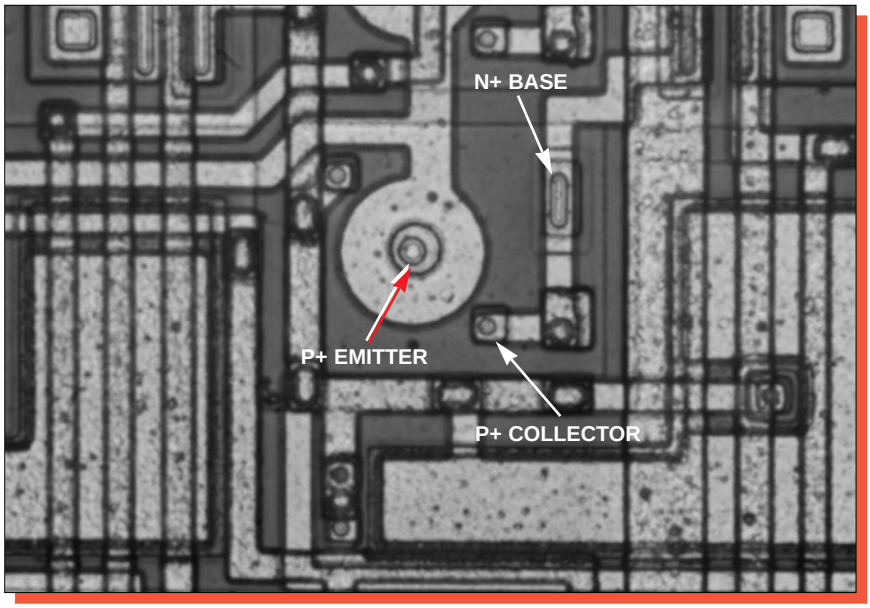


collector

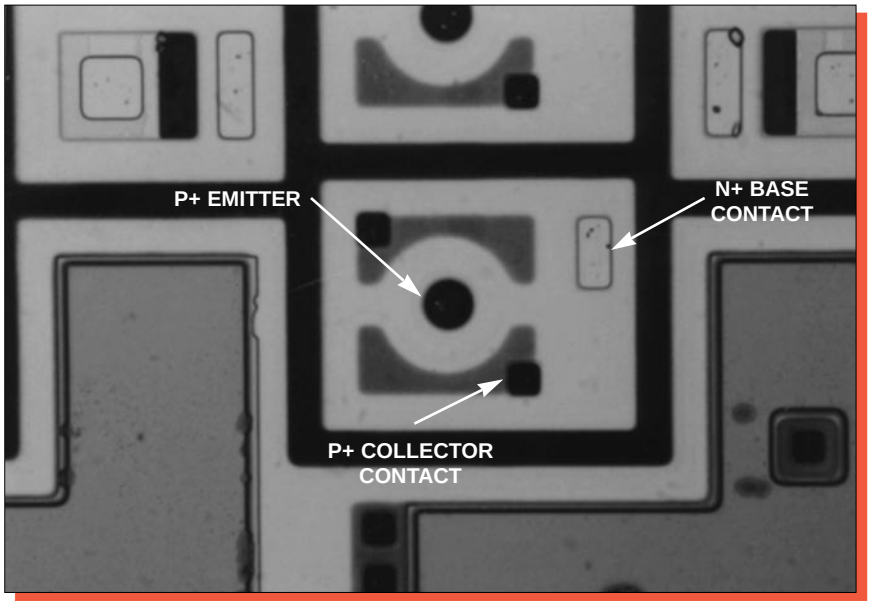


base

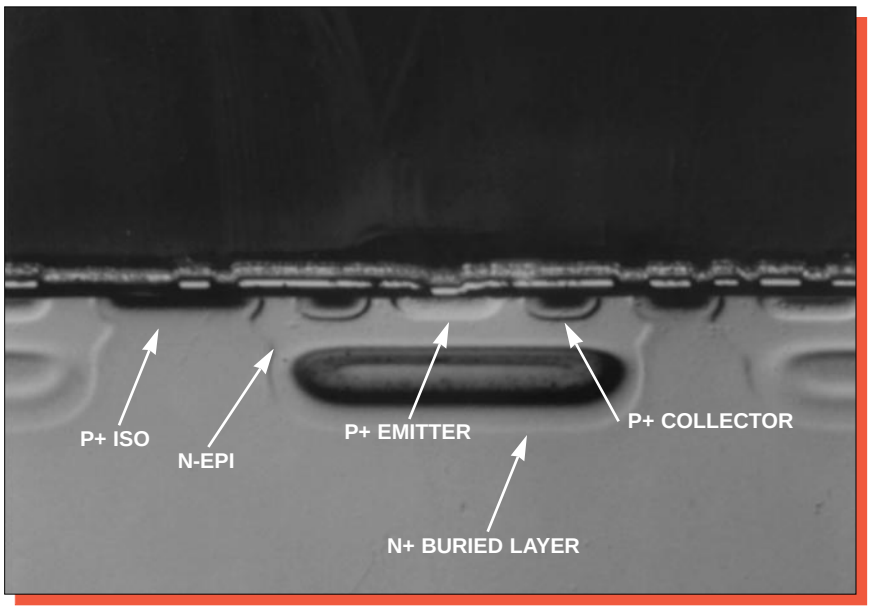
Figure 27. Detailed views of the NPN transistor. Mag. 8000x.



Mag. 500x

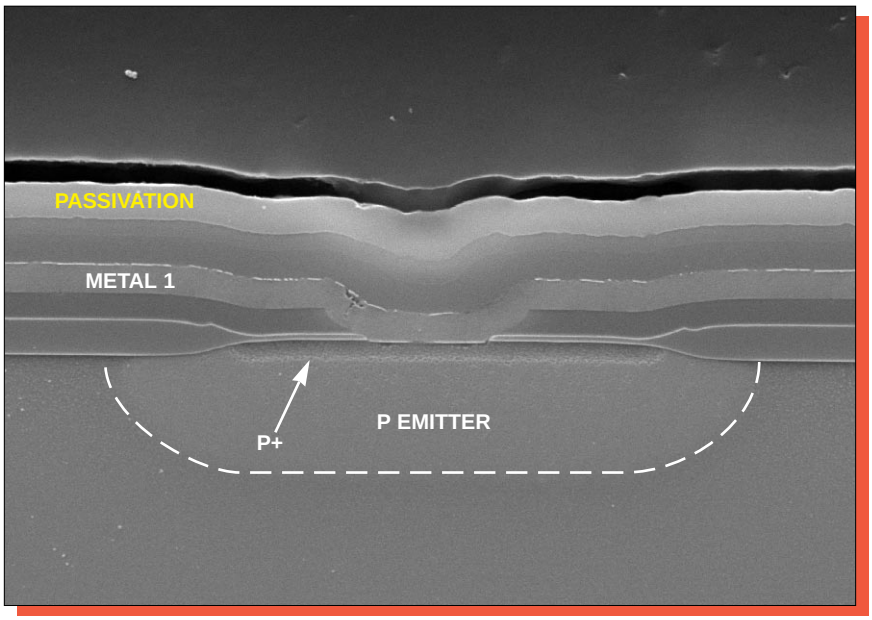


Mag. 500x

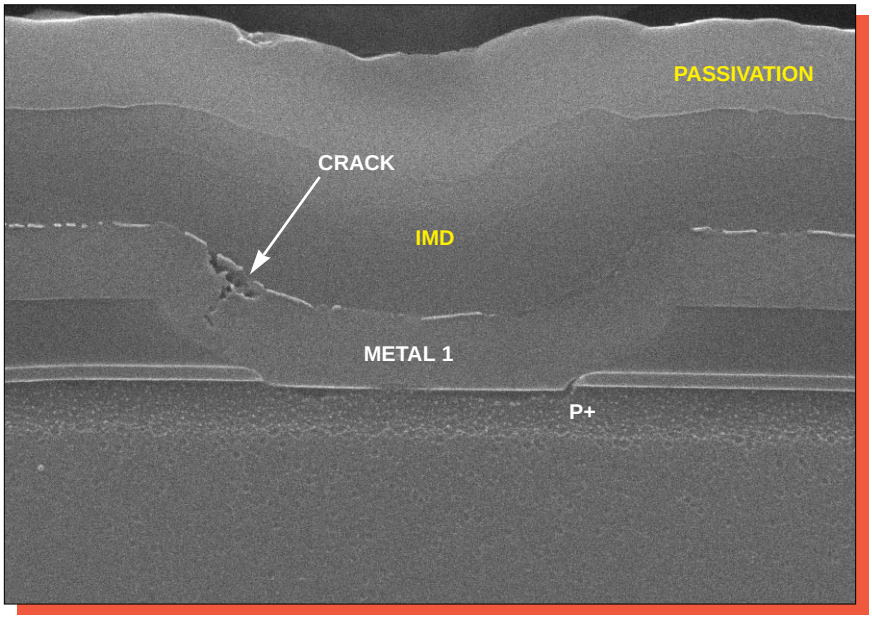


Mag. 800x

Figure 28. Optical views of a PNP transistor layout (diode connected).

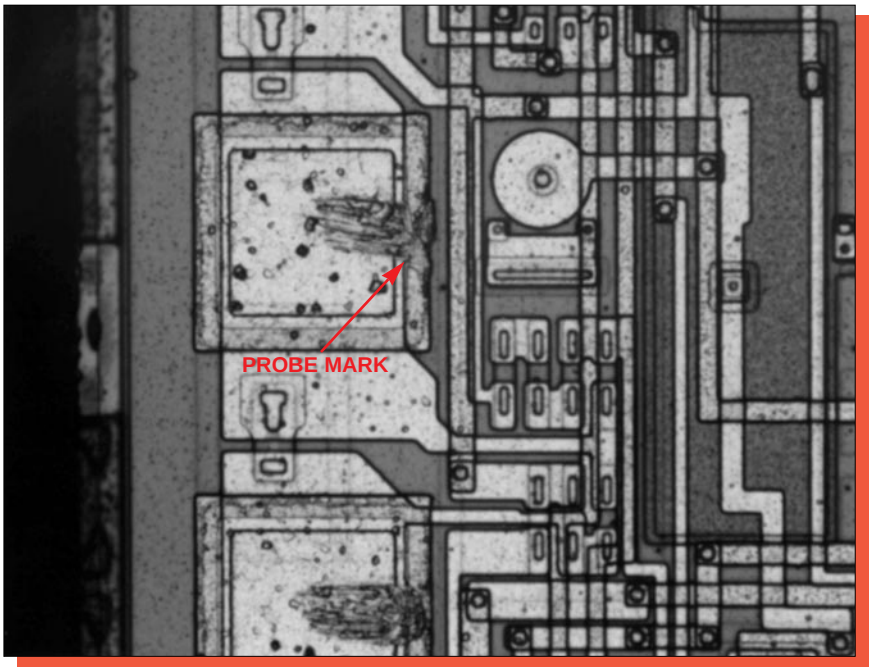


Mag. 5000x



Mag. 13,000x

Figure 29. SEM section views of a P+ emitter on a PNP device.



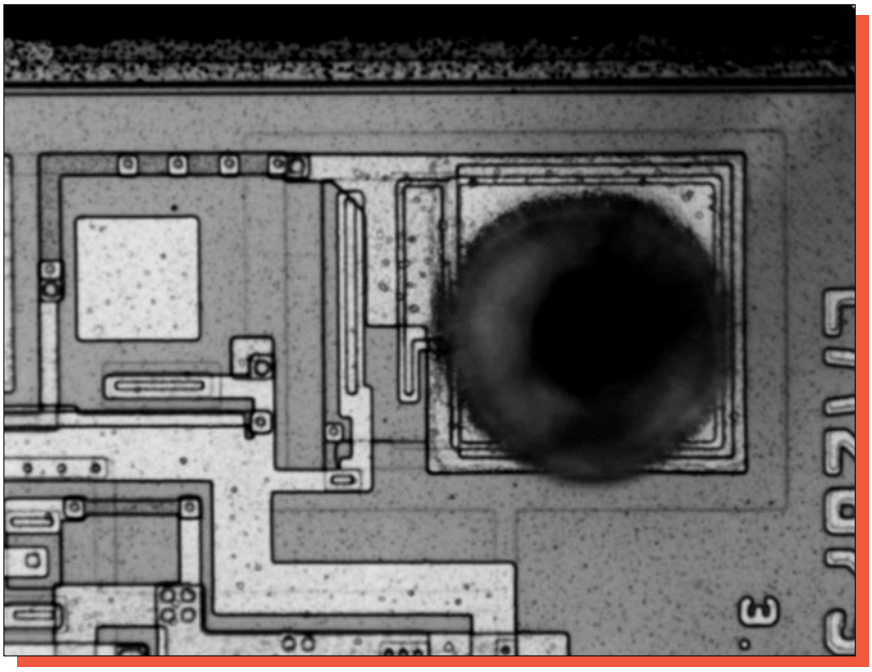
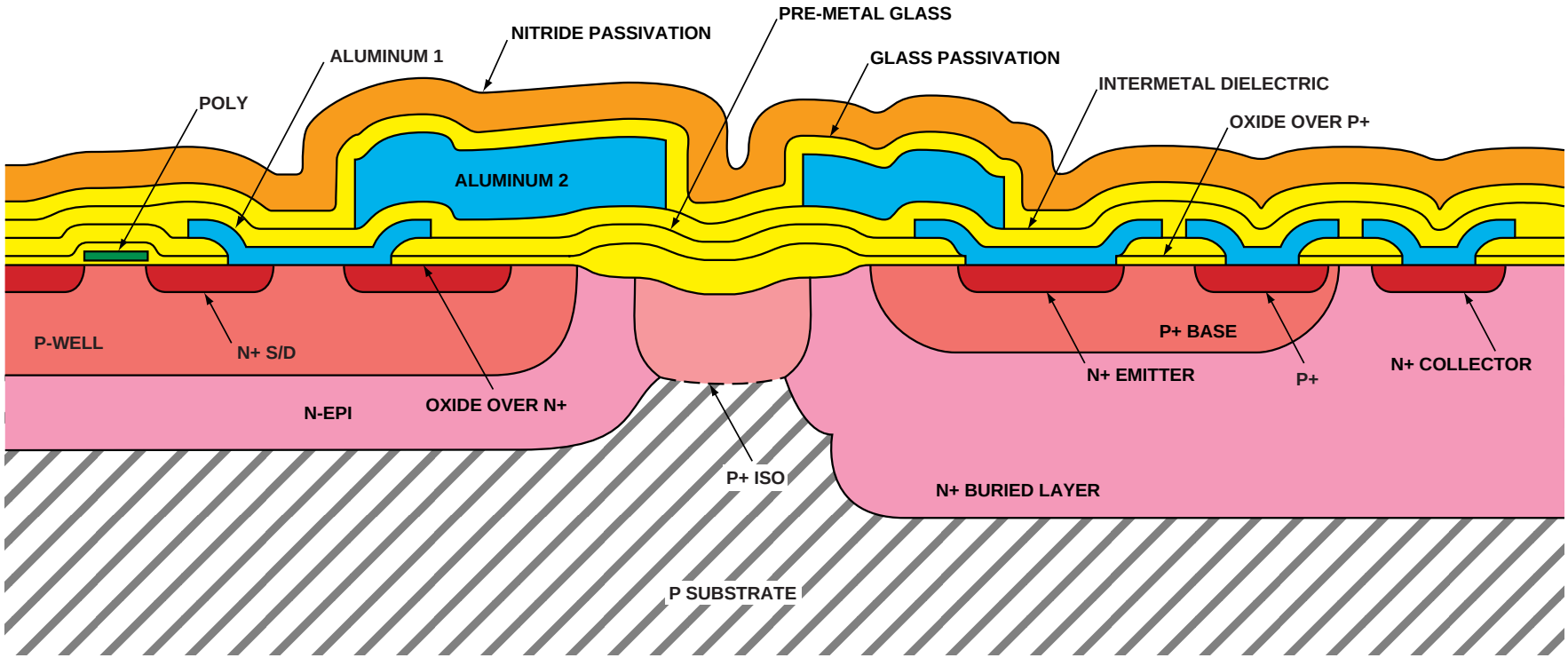


Figure 30. Optical views of probe damage and input layout (Pin 2, SS). Mag. 320x.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 31. Color cross section drawing illustrating device structure.