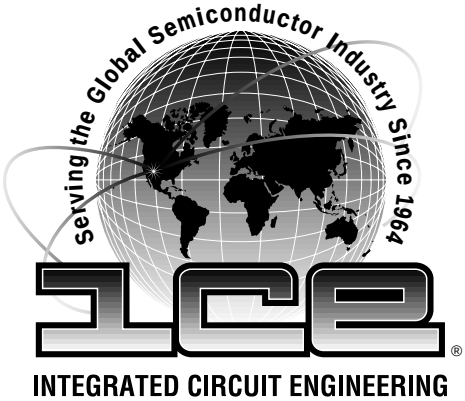
Construction Analysis

Xilinx XC9536
CPLD

Report Number: SCA 9212-568



INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Xilinx XC9536 CPLD. One device packaged in a 44-pin VQFP (very small quad flat pack) with gull wing leads for surface mount applications was provided. The part was date coded 9633.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 2 aluminum thinned up to 100 percent[2] at some vias (Figure 15) and metal 1 aluminum thinned up to 100 percent[2] at some contacts (Figures 21 and 22). Barrier metal maintained continuity.

Special Features:

- Fast FLASH technology.

- Sub-micron gates (0.45 micron N-channel, 0.5 micron P-channel).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Packaging/Assembly:

- The device was encapsulated in a 44-pin very small quad flat pack with gull wing leads.
- Lead locking provisions (anchors) at all pins.
- Thermosonic ball bond method using gold wire.
- Sawn dicing (full depth).
- Silver (Ag) epoxy die attach.

Die Process:

- Fabrication: Twin-well CMOS, selective oxidation process. P substrate and no epi.
- Final passivation: A layer of silicon-nitride over silicon-dioxide.
- Metallization: Two levels of aluminum interconnect patterned by dry-etch techniques. A titanium-nitride (TiN) cap and barrier metal were employed with both metal levels. Standard vias and contacts were employed (no plugs).
- Interlevel dielectric: Two layers of silicon-dioxide. A spin-on-glass (SOG) was used between these layers for planarization purposes. No evidence of chemical mechanical planarization (CMP) was present.
- Pre-metal glass: A thick reflow glass over various densified oxides. It appeared to have been reflowed prior to contact cuts only.
- Polysilicon: Two layers of polysilicon were present. Poly 1 was used exclusively in the array for floating gates and poly 2 (poly and tungsten silicide) was used for all standard gates on the die and word and program lines in the array.

TECHNOLOGY DESCRIPTION (continued)

- Diffusions: Transistors were formed using an LDD process in which the oxide sidewall spacers were left in place. Implanted N+ and P+ sources/drains. No silicide was used at diffusions.

- Twin-wells were used in a P substrate. No epi was present. A step was present in the oxide at the well boundaries.

- No buried contacts were employed on this device.

- Memory cells: The programmable array consisted of EEPROM cells (Fast FLASH technology). Metal 2 was used to form "piggyback" word and program lines. Metal 1 distributed the bit lines and GND. Poly 2 formed the word and program lines and poly 1 formed the floating gates. The interpoly dielectric consisted of ONO (oxide-nitride-oxide).

- Design features: Metal 2 bus lines were slotted for stress relief. Some isolated vias were present on the die which may be used for probing purposes (see Figure 4).

ANALYSIS RESULTS I

Assembly: **Figures 1 and 6**

Questionable Items: None.

General Items:

- 44-pin VQFP plastic packages with gull wing leads.
- Overall package quality: Normal. No defects were found on the external portions of the package.
- Leadframe: Lead-locking provisions (anchors) were present at all pins.
- Die attach: The die was attached to the header with silver-epoxy of normal quality.
- Die dicing: Die separation was by sawing with normal quality workmanship. No cracks or large chipouts were found in the die.
- Wirebonding: Thermosonic ball bond method using gold wire. Bonds were well formed and placement was good. Bond pad pitch was tight (117 microns); however, no problems were noted and wire spacing was good. Bond pad structure employed both metals.

ANALYSIS RESULTS II

Die Process: **Figures 2 - 37**

Questionable Items:[1]

- Metal 2 aluminum thinned up to 100 percent[2] at some vias (Figure 15) and metal 1 aluminum thinned up to 100 percent[2] at some contacts (Figures 21 and 22). Barrier metal maintained continuity.

Special Features:

- Fast FLASH technology.

- Sub-micron gates (0.45 micron N-channel, 0.5 micron P-channel).

General Items:

- Fabrication process: Selective oxidation CMOS process using twin-wells in a P substrate. No epi was present.

- Process Implementation: Die layout was clean and efficient. Alignment/registration was good at all levels and no damage or contamination was found.

- Final passivation: A layer of silicon-nitride over silicon-dioxide. Passivation extended into the scribe lane covering all metallization. A cutout was present in the passivation around the die perimeter in the scribe lane. This was probably employed to prevent cracks from radiating inward.

- Metallization: Two levels of aluminum interconnect. A titanium-nitride (TiN) cap and barrier metal were employed with each metal level. Standard vias and contacts were employed (no plugs).

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metal patterning: Both layers were defined by dry-etch techniques. Definition was normal for both layers. Some neckdown of metal 2 lines was noted where they crossed over metal 1 lines. Metal lines were widened at vias and contacts.

- Metal defects: No voiding or notching of the metals was found. No silicon nodules were found following the removal of the aluminum layers. No problems were noted.

- Metal step coverage: Metal 2 aluminum thinned up to 100 percent at some via edges. Metal 1 aluminum also thinned up to 100 percent at some contact edges. Barrier metal maintained continuity. The excessive thinning appears to be due to the metal deposition method employed.

- Vias and contacts: Metal 2 vias were overetched into the metal 1 cap; however, no problems are foreseen. No overetching of metal 1 contacts was noted.

- Interlevel dielectric: The dielectric between the two metal levels consisted of two layers of silicon-dioxide with a spin-on-glass (SOG) employed between for planarization purposes. No problems were noted.

- Pre-metal glass: The glass under metal 1 consisted of a thick reflow glass which was apparently reflowed prior to contact cuts only. This deposited glass was located over various densified oxides. No problems were found in any of the glass layers.

- Polysilicon: Two layers of poly were used. Polycide (tungsten silicide on poly 2) formed all standard gates on the die. Poly 1 was used exclusively for floating gates in the array. No poly stringers or spurs were present. Definition was by a dry etch of good quality.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeak. A step was present in the field oxide indicating a twin-well process was used.

ANALYSIS RESULTS II (continued)

- Diffusions: Transistors were formed using an LDD process in which the oxide sidewall spacers were left in place. Implanted N+ and P+ sources/drains were employed. Definition was normal and no problems were present. Diffusions were not silicided.

- Wells: Twin-wells in a P substrate. No problems were apparent.

- Epi: No epi was used. No substrate defects were found.

- Buried contacts: No buried contacts were used on this device.

- Memory cells: The programmable array consisted of EEPROM cells (Fast FLASH technology). Metal 2 was used to form "piggyback" word and program lines. Metal 1 formed the bit lines and distributed GND. Poly 2 formed the word and program lines and poly 1 formed the floating gates. The interpoly dielectric consisted of ONO (oxide-nitride-oxide). Cell size was 5.2 x 6 microns and cell area was 31 microns^2.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

Passivation removal and inspect metal 2

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Aluminum 1 removal and inspect barrier

Delayer to poly/substrate and inspect poly structures and die surface

Die material analysis

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal/Poor

DETAIL OF EVALUATION

Package integrity	N
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	N
Dicing quality	G
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	P*
Metal registration	G
Contact coverage	G
Contact registration	G

**Metal 2 and metal 1 aluminum thinning up to 100 percent.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP	BOTTOM (molded)
(logo) XILINX® XC9536™ VQ44ASJ9633 A63042A 7C B(penciled)	KOREA 23

DIE MATERIAL ANALYSIS

Final passivation:	Silicon-nitride over silicon-dioxide.
Metallization 2:	Aluminum with a titanium-nitride cap and barrier metal.
Interlevel dielectric:	Two layers of silicon-dioxide with a spin-on glass.
Metallization 1:	Aluminum with a titanium-nitride cap and barrier metal.
Intermediate glass:	Reflow glass.
Polycide:	Tungsten on poly 2.

HORIZONTAL DIMENSIONS

Die size:	3.4 x 5.6 mm (134 x 222 mils)
Die area:	19.2 mm^2 (29,748 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.3 x 4.3 mils)
Min pad window:	0.09 x 0.09 mm (3.7 x 3.7 mils)
Min pad space:	8 microns
Min metal 2 width:	0.8 micron
Min metal 2 space:	1.0 micron
Min metal 2 pitch (uncontacted):	1.9 micron
Min metal 2 pitch (contacted):	2.6 microns
Min via:	1.0 micron (round)
Min via pitch:	2.0 microns
Min metal 1 width:	0.55 micron
Min metal 1 space:	0.9 micron
Min metal 1 pitch (uncontacted):	1.6 micron
Min metal 1 pitch (contacted):	2.5 microns
Min contact:	1.0 micron
Min contact pitch:	1.7 micron
Min contact-to-gate:	0.6 micron
Min poly 2 width:	0.45 micron
Min poly 2 space:	0.85 micron
Min poly 1 width:	0.65 micron
Min gate length* (N-ch):	0.45 micron
(P-ch):	0.5 micron
Cell pitch:	5.2 x 6 microns
Cell size:	31 $microns^2$

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.4 mm (16 mils)

Layers:

Passivation 2:	0.45 micron
Passivation 1:	0.25 micron
Metallization 2 - cap:	0.05 micron (approx.)
- aluminum:	0.75 micron
- barrier:	0.1 micron
Interlevel dielectric:	0.65 - 1.9 micron
Metallization 1 - cap:	0.07 micron
- aluminum:	0.5 micron
- barrier:	0.1 micron
Pre-metal glass:	0.35 - 0.9 micron
Polycide - silicide:	0.13 micron
- poly 2:	0.1 micron
Poly 1:	0.1 micron
Local oxide:	0.5 micron
N+ S/D:	0.17 micron
P+ S/D:	0.2 micron
N-well:	4.0 microns

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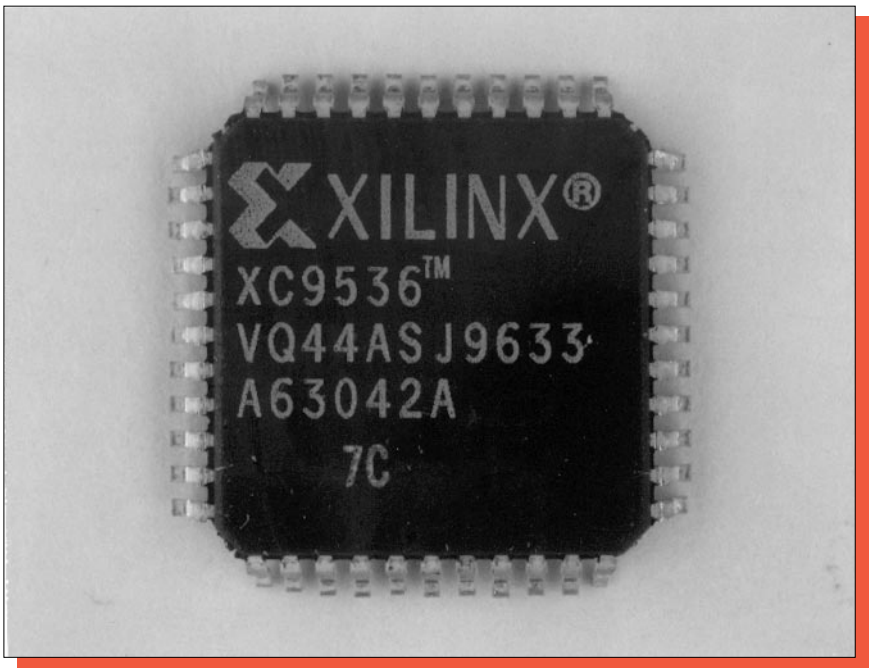


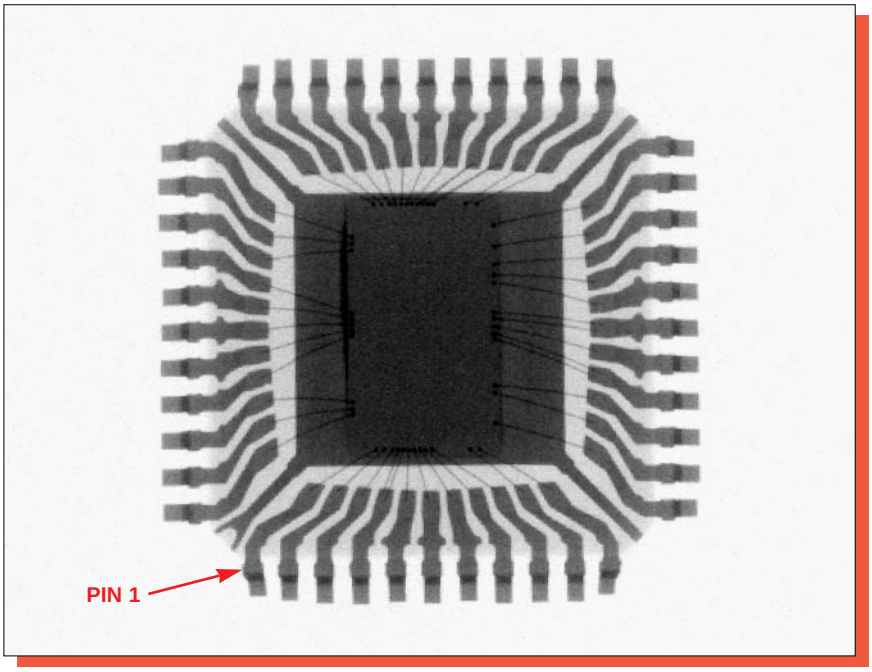


Figure 1. Package photograph and x-ray view of the Xilinx XC9536. Mag. 6x.

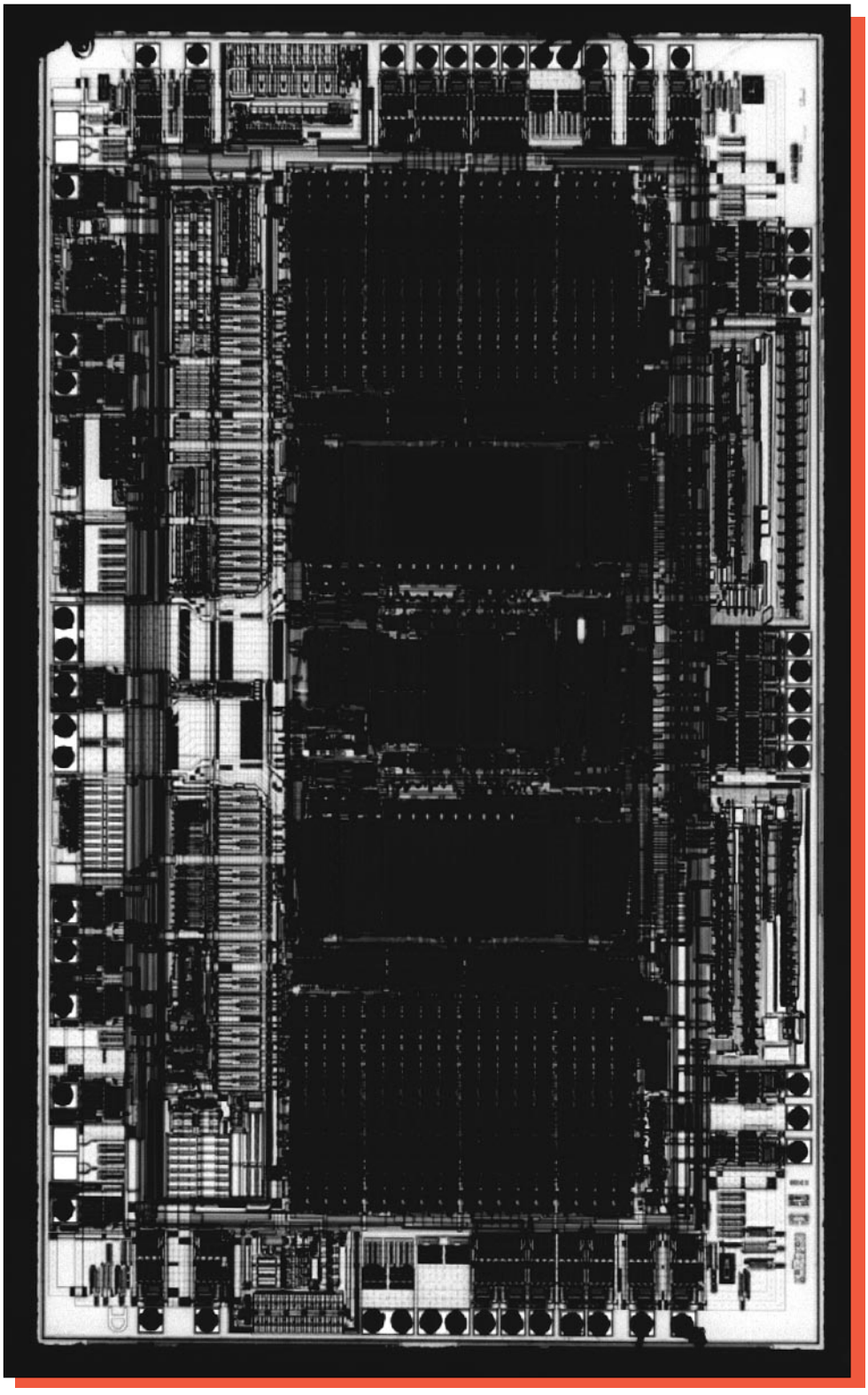


Figure 2. Whole die photograph of the Xilinx XC9536. Mag. 40x.

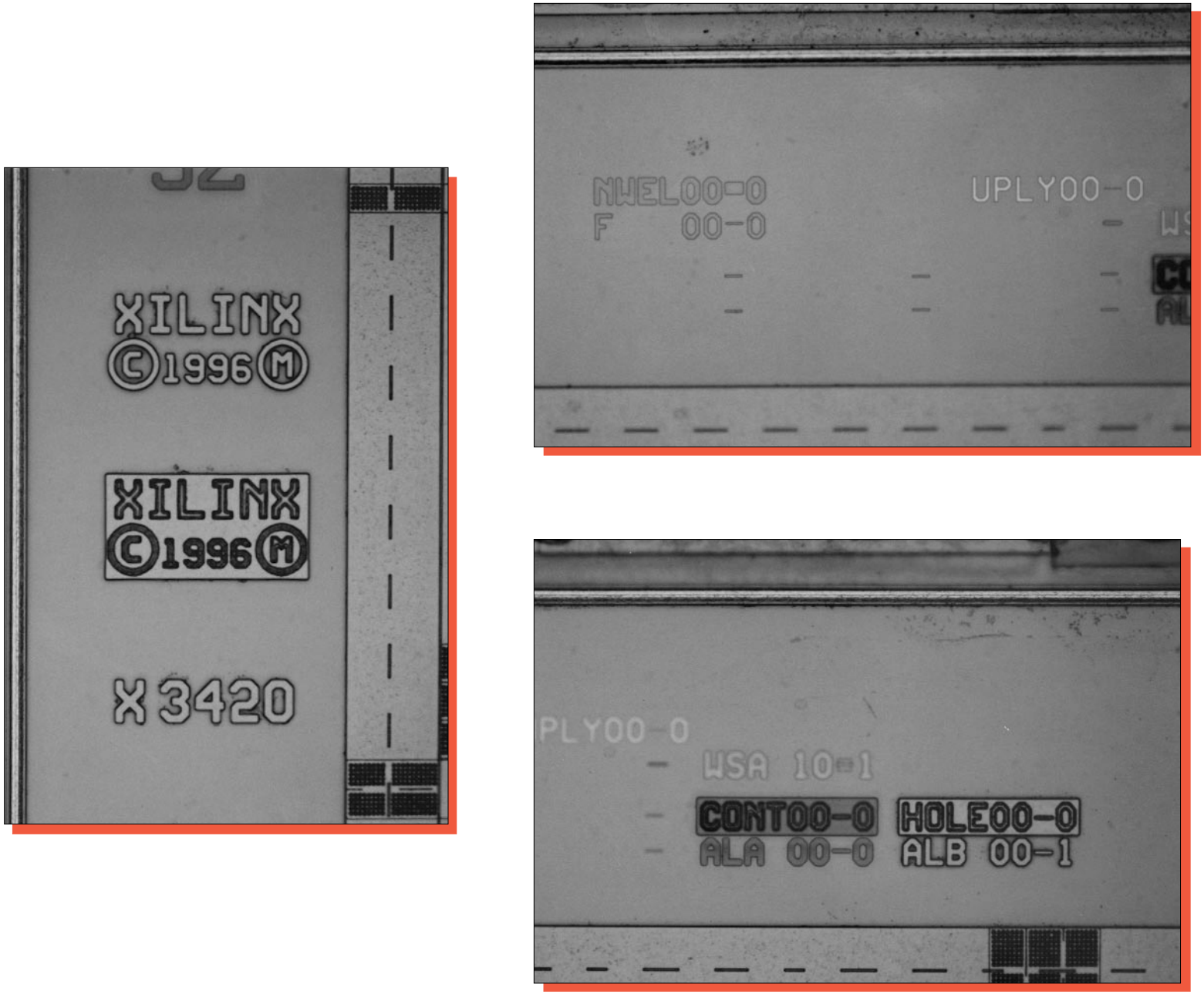
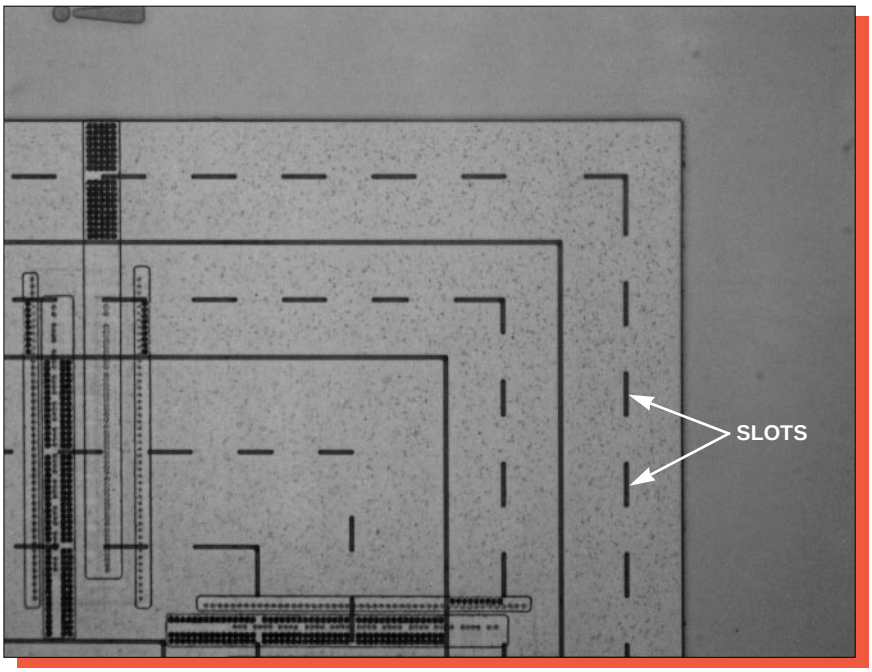
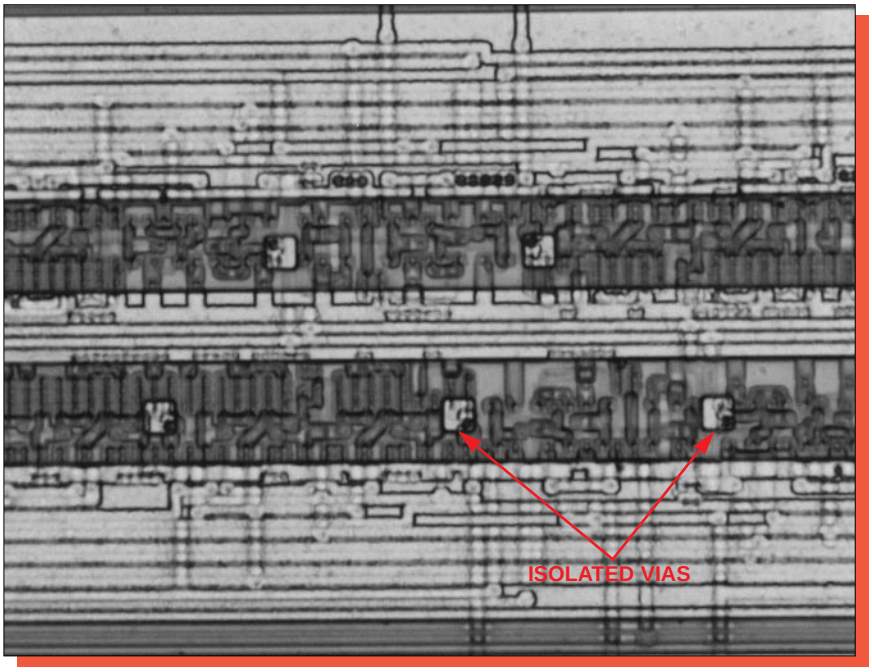


Figure 3. Die identification markings. Mag. 400x.



Mag. 400x



Mag. 800x

Figure 4. Optical views illustrating design features.

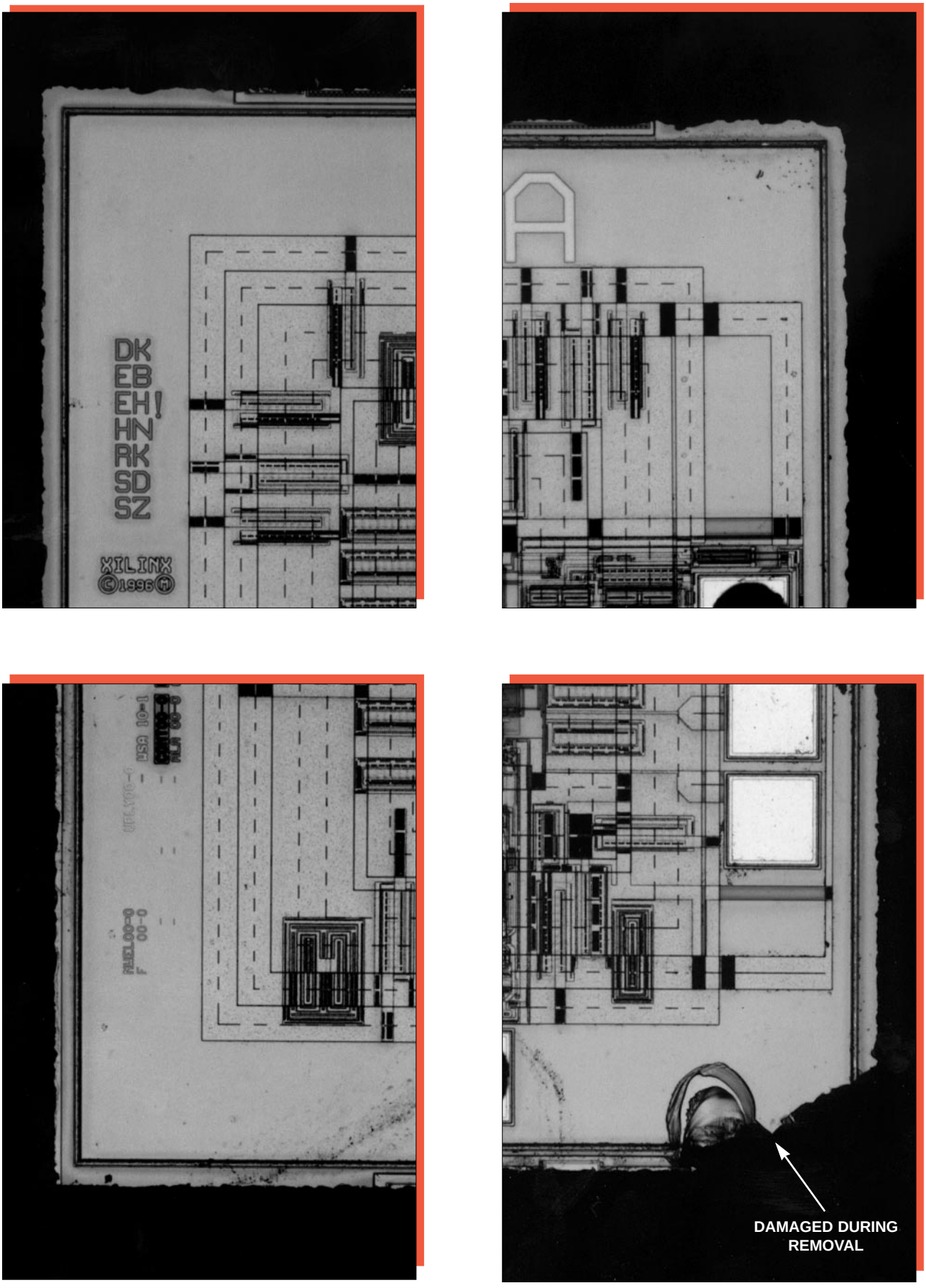
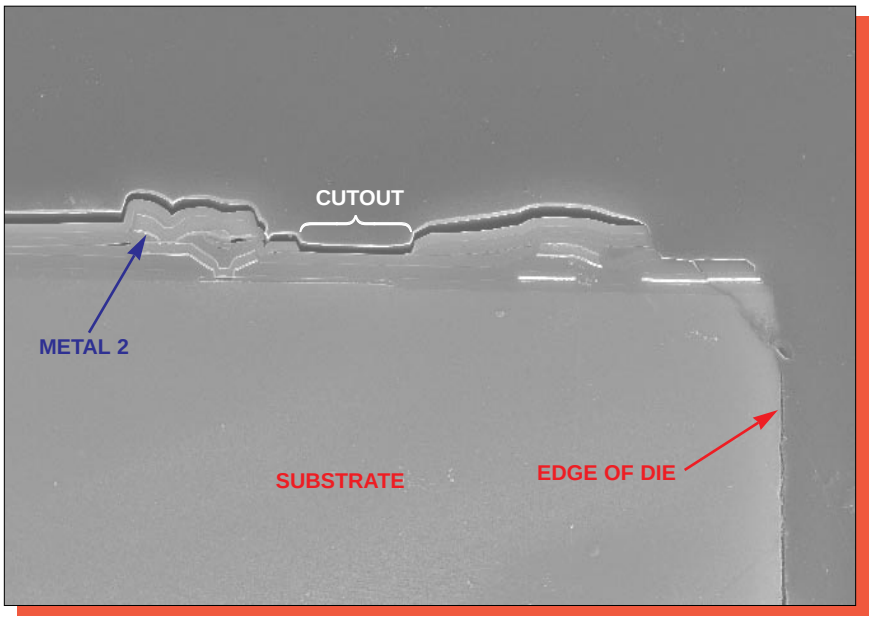
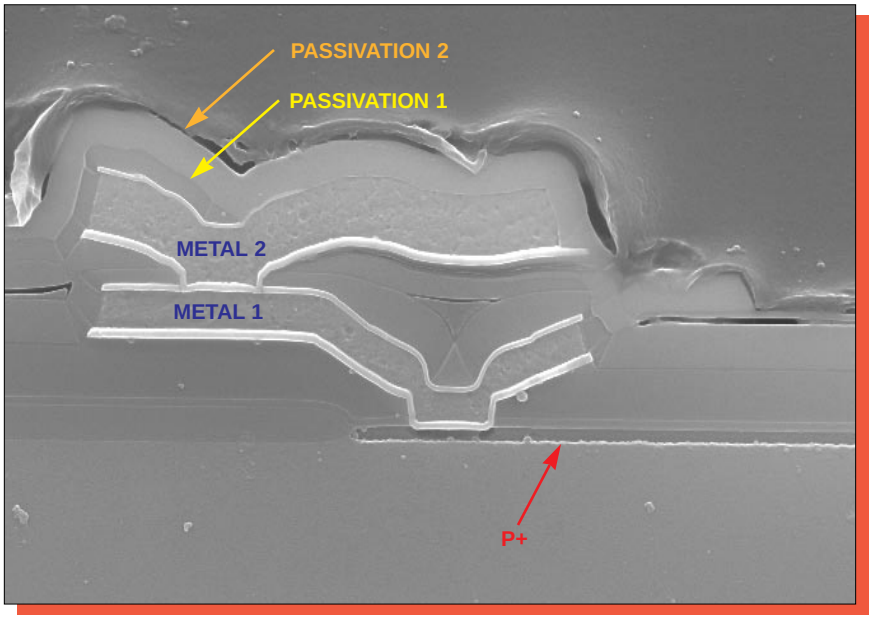


Figure 5. Optical views of die corners. Mag. 160x.

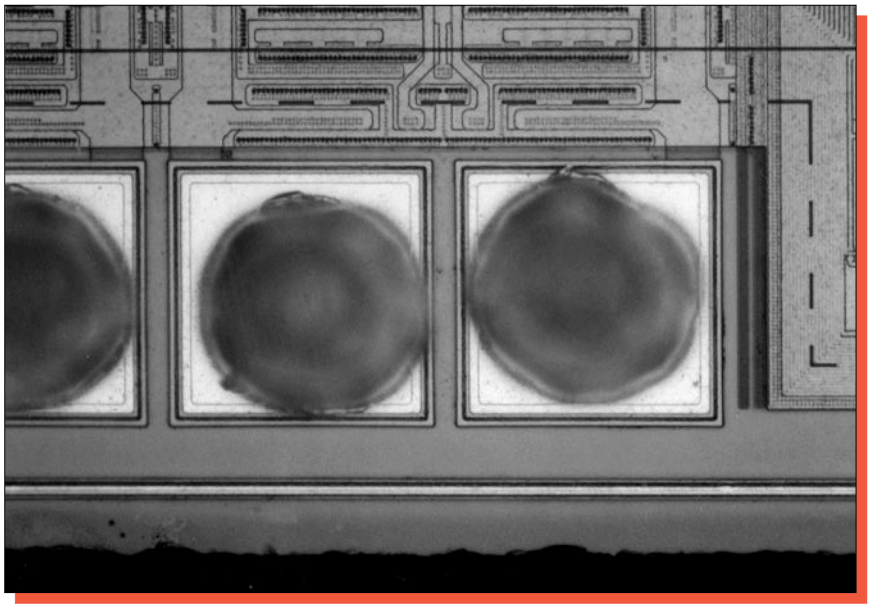


Mag. 2600x

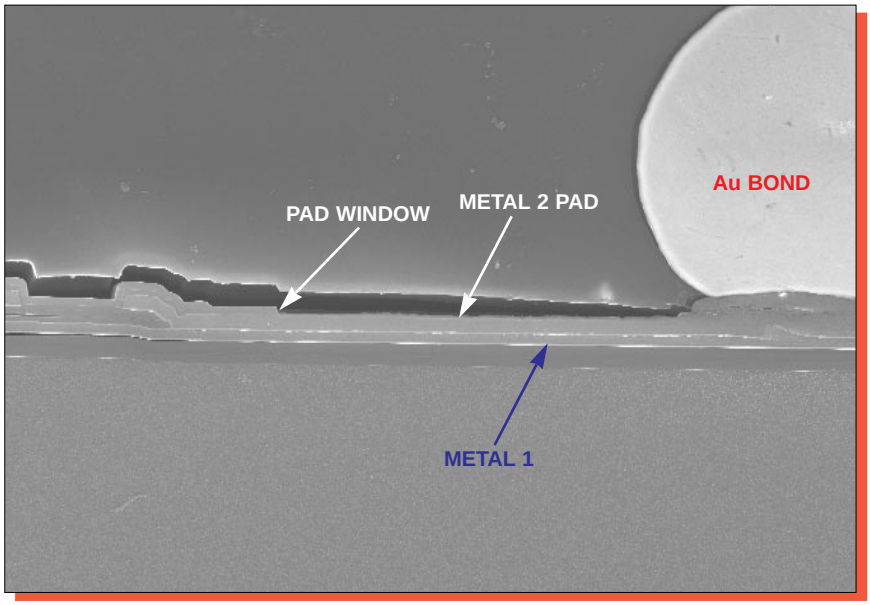


Mag. 10,300x

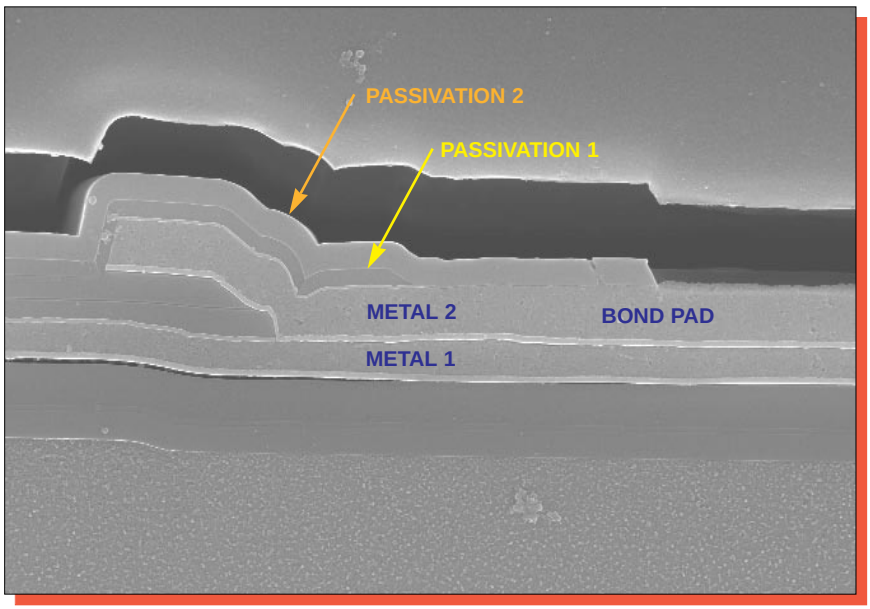
Figure 6. SEM section views of the edge seal structure.



Mag. 320x

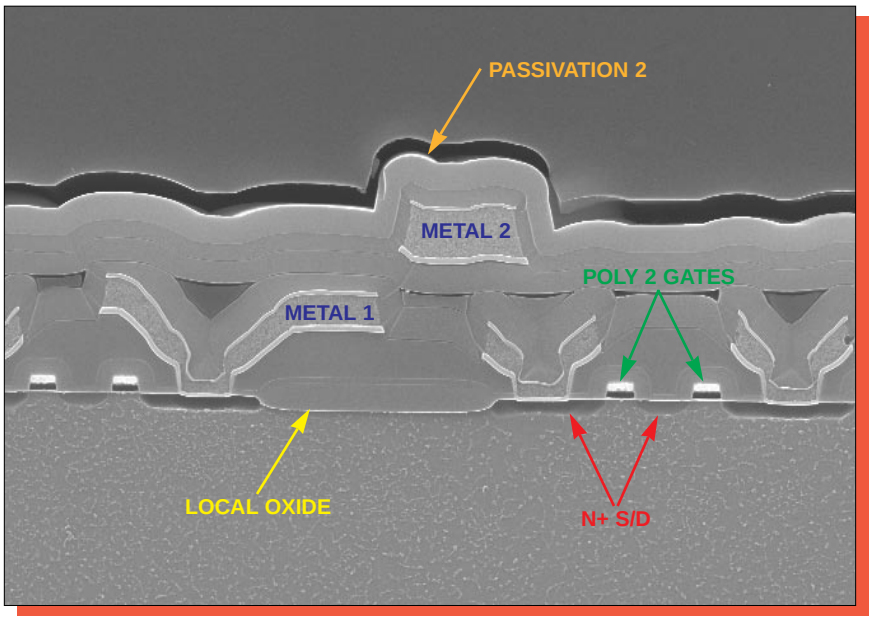


Mag. 2200x

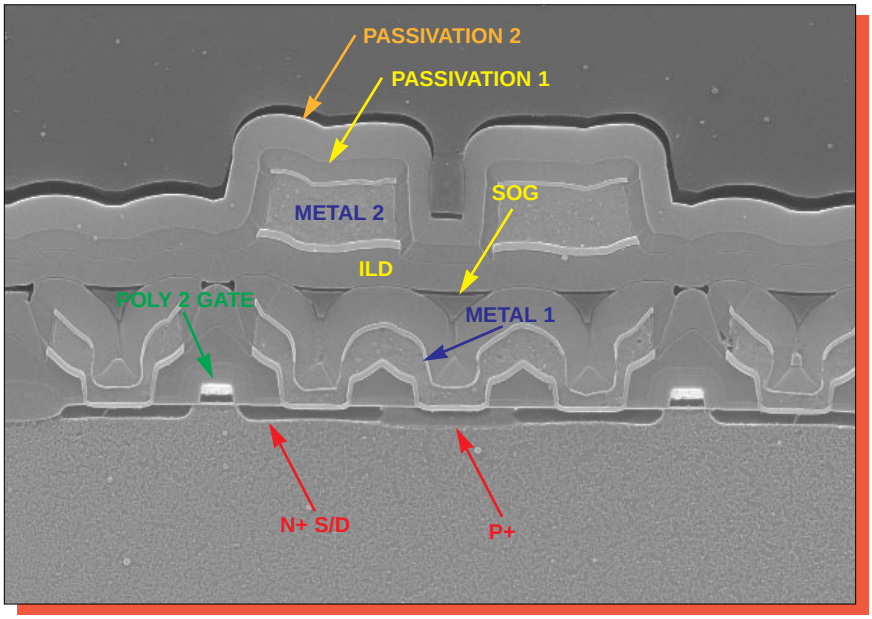


Mag. 7700x

Figure 7. Topological and section views of the bond pad layout and structure.

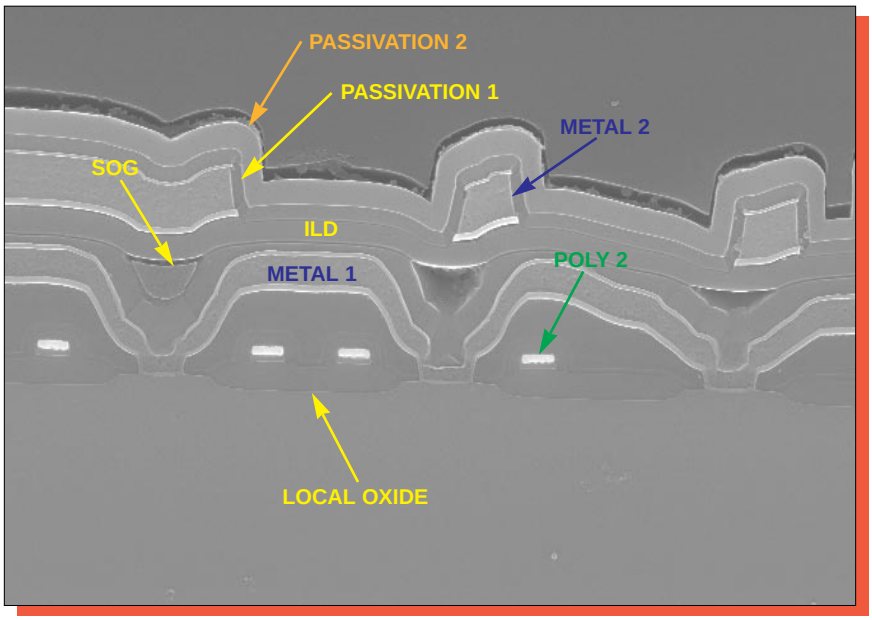


Mag. 7900x

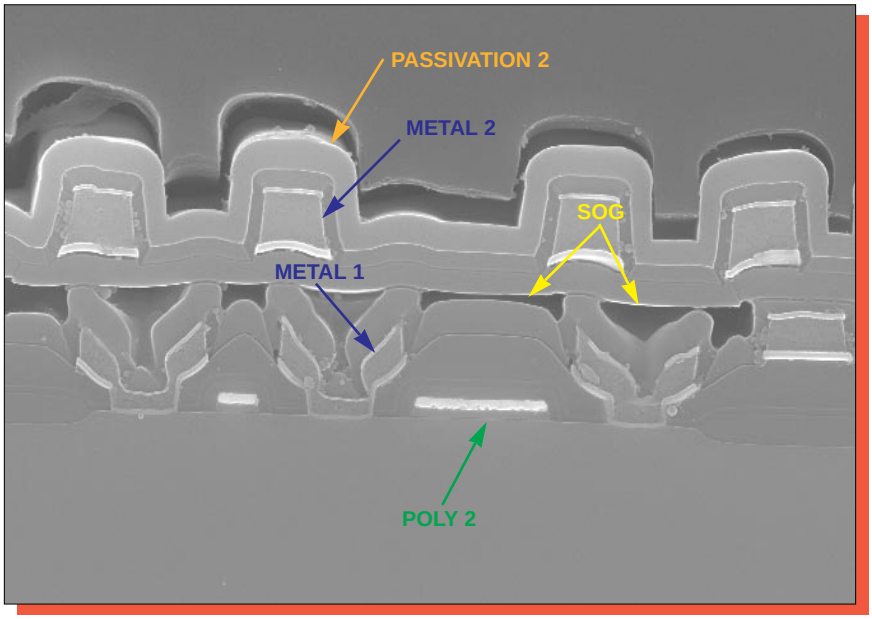


Mag. 9600x

Figure 8. SEM section views illustrating general device structure.

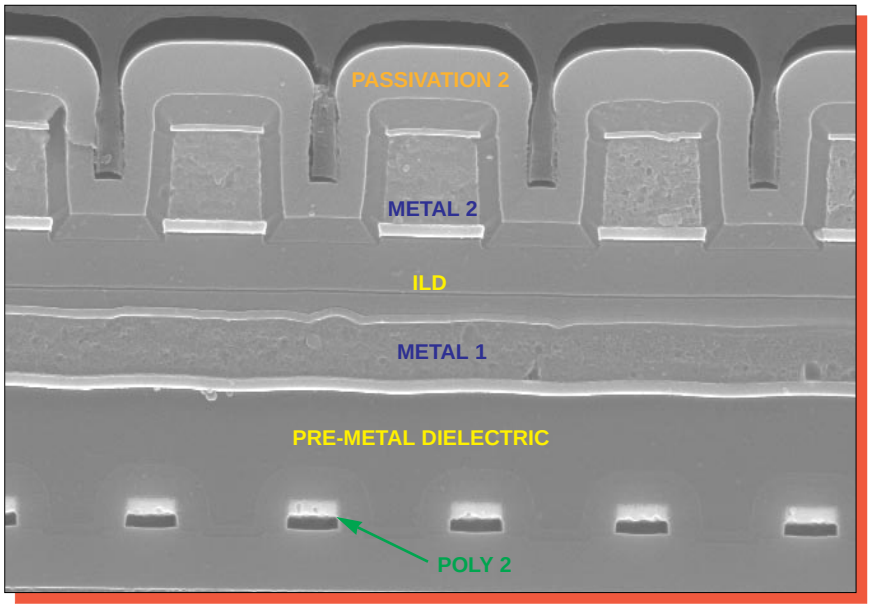


Mag. 7600x

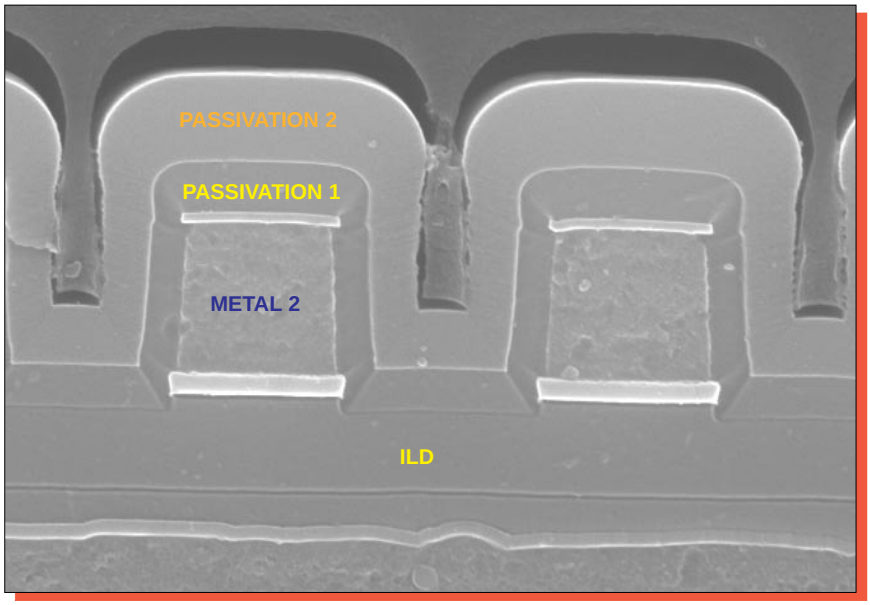


Mag. 9000x

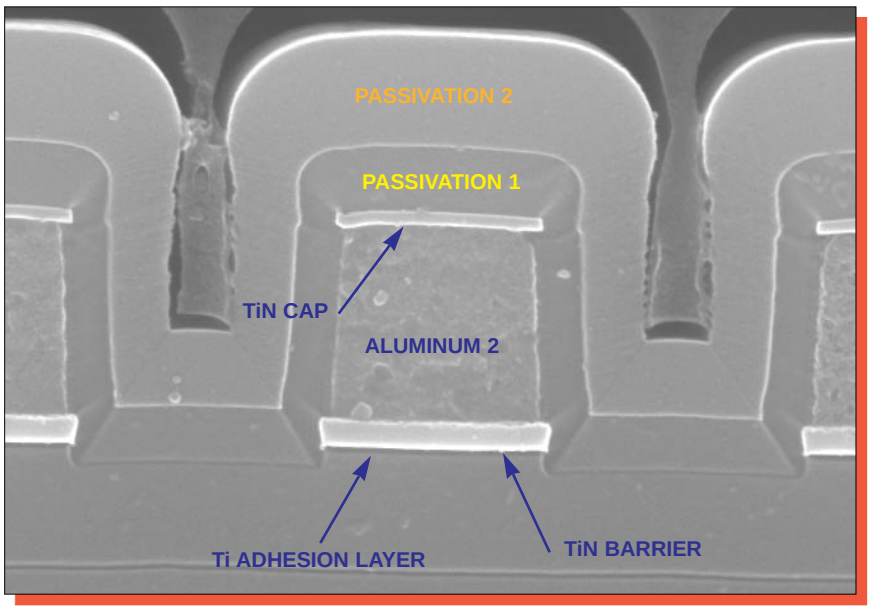
Figure 9. Glass etch section views illustrating general device structure.



Mag. 15,500x

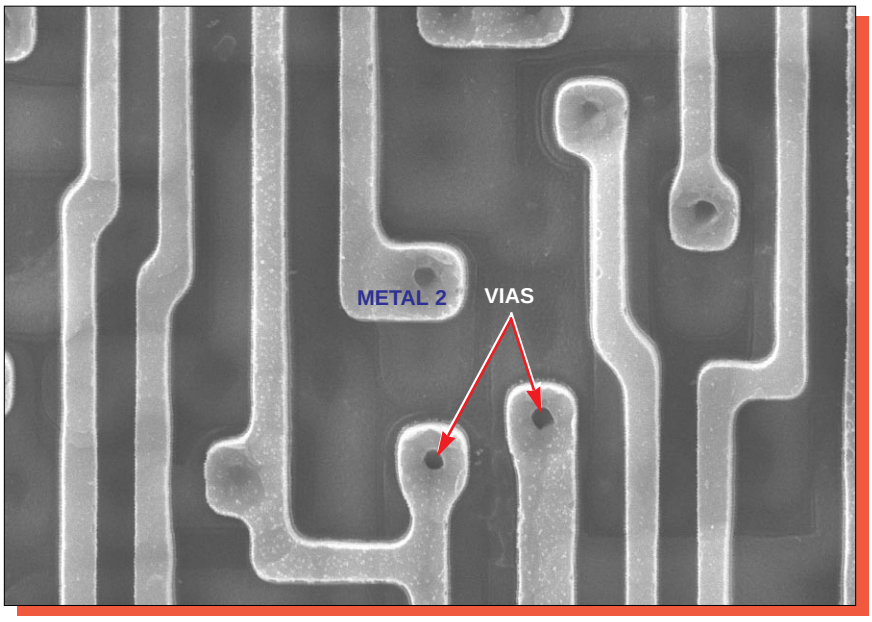


Mag. 26,250x



Mag. 34,000x

Figure 10. SEM section views of metal 2 line profiles.



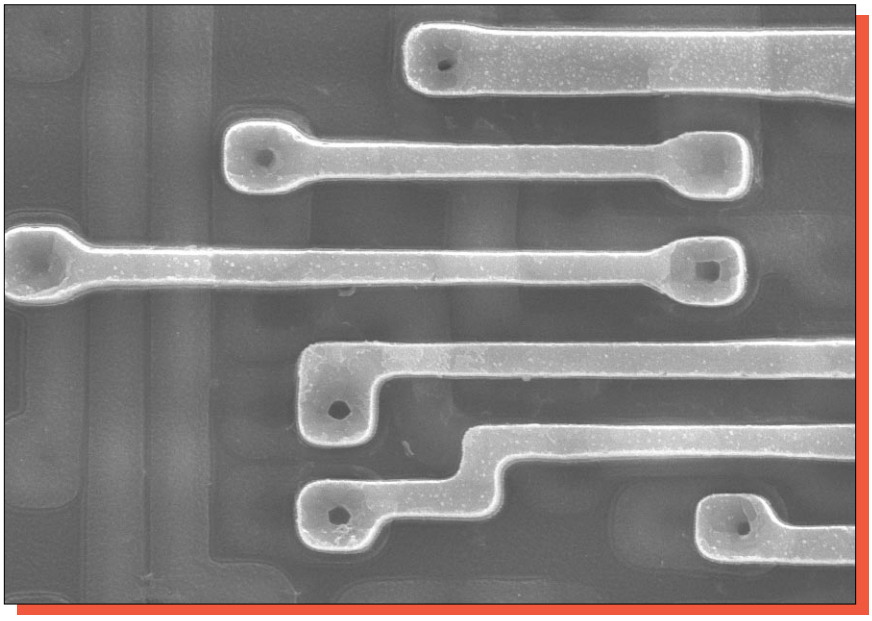
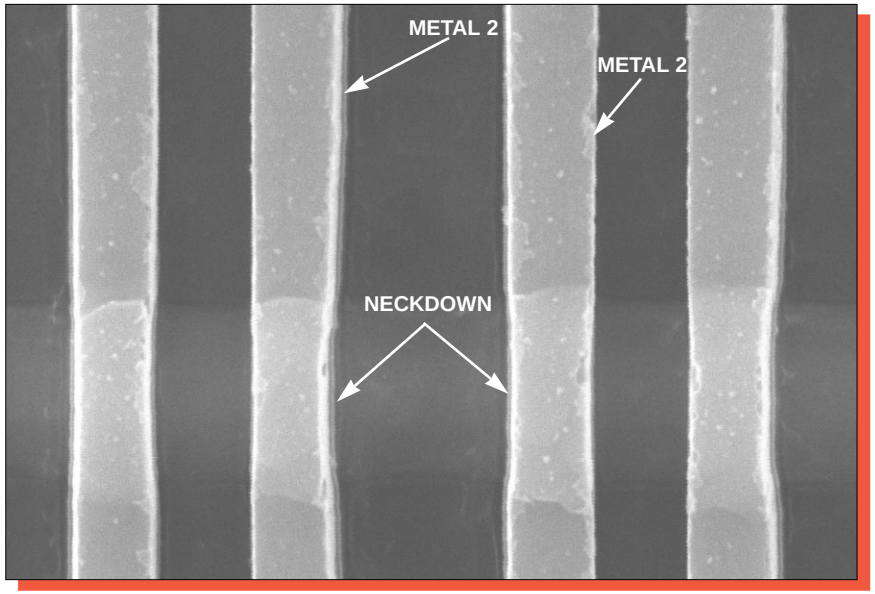
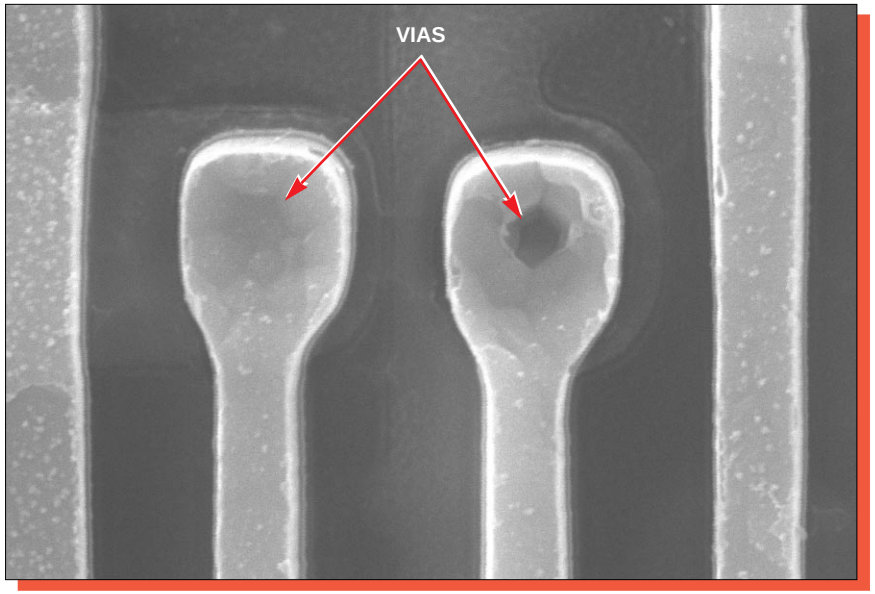
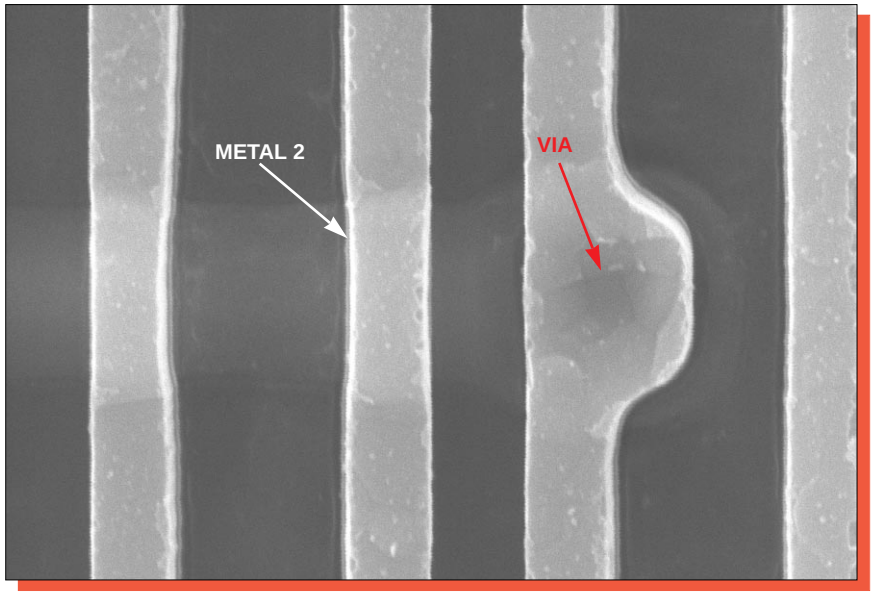


Figure 11. Topological SEM views of metal 2 patterning. Mag. 5500x, 0°.







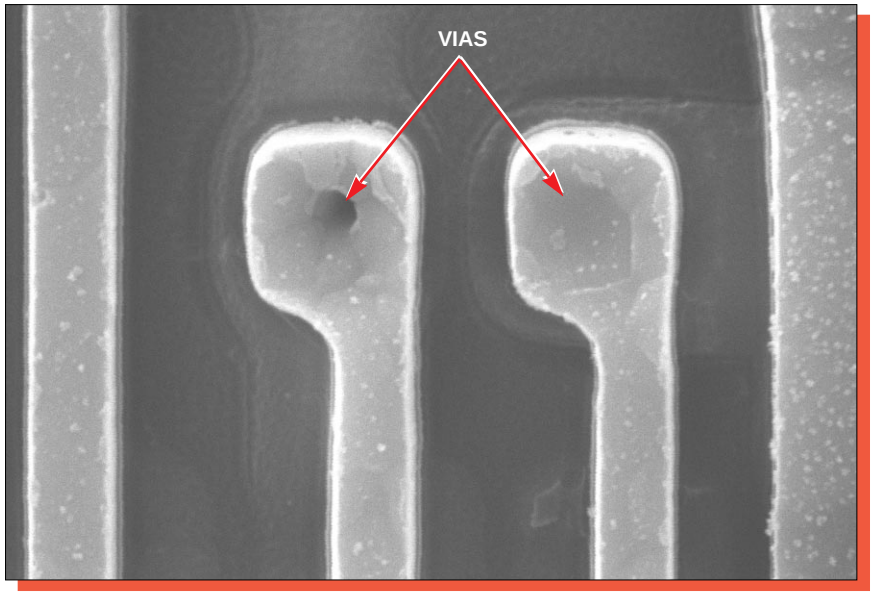
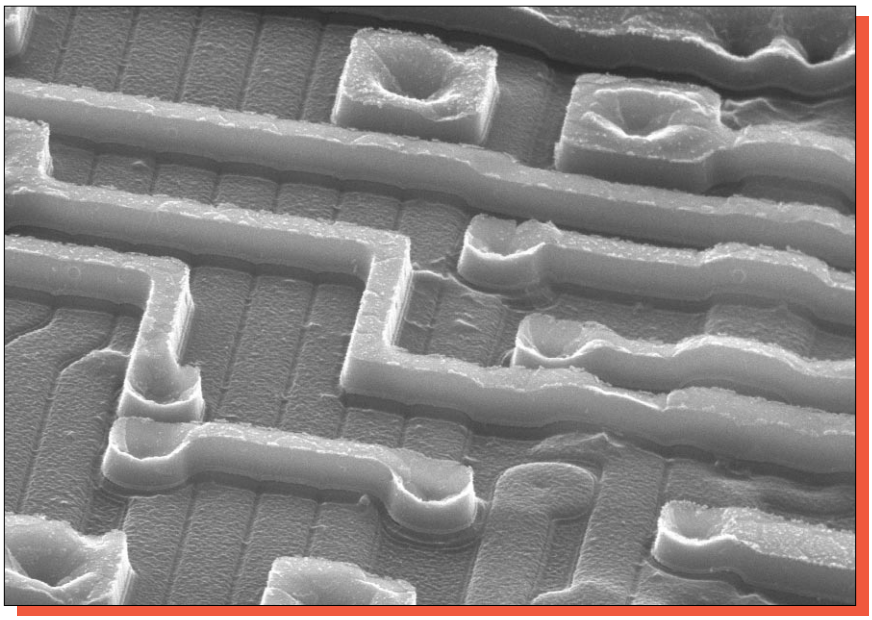
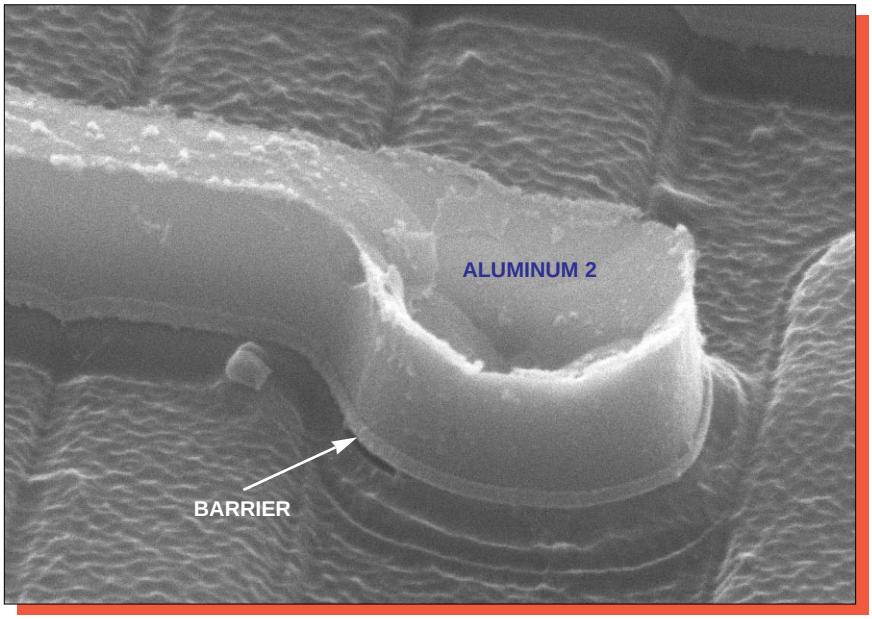


Figure 12. Topological SEM views of metal 2 design rule features. Mag. 13,000x, 0°.

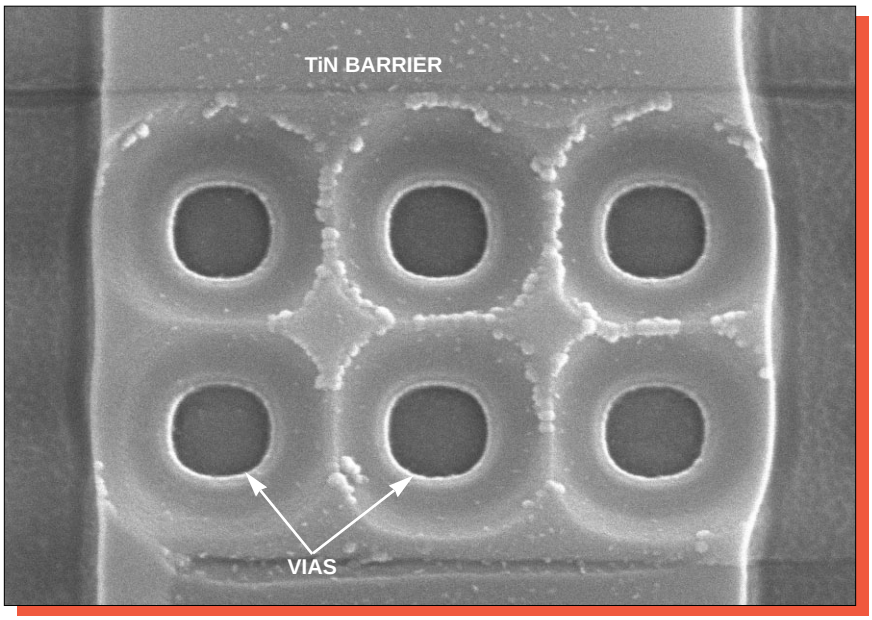


Mag. 6000x

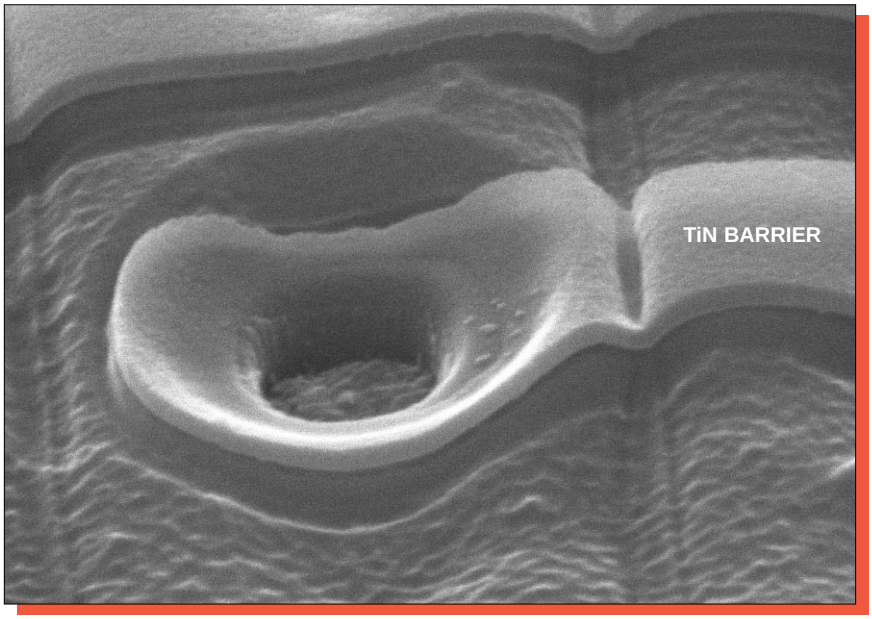


Mag. 25,000x

Figure 13. SEM views of general metal 2 integrity. 60°.

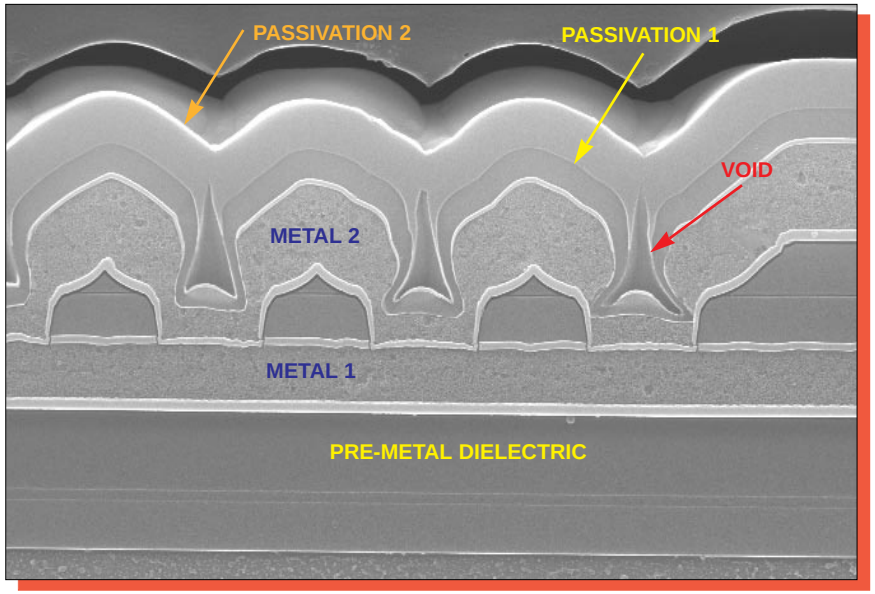


Mag. 15,000x, 0°

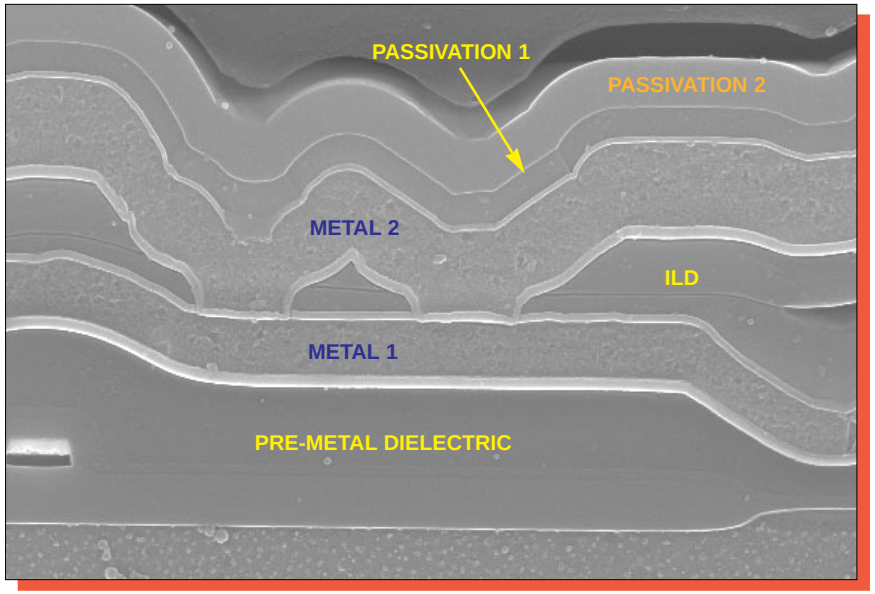


Mag. 31,000x, 55°

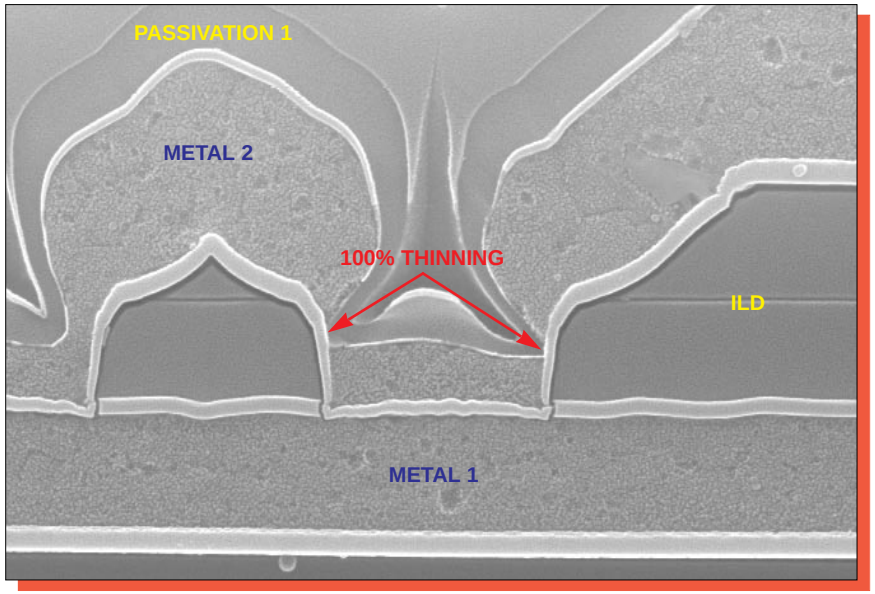
Figure 14. SEM views of metal 2 barrier.



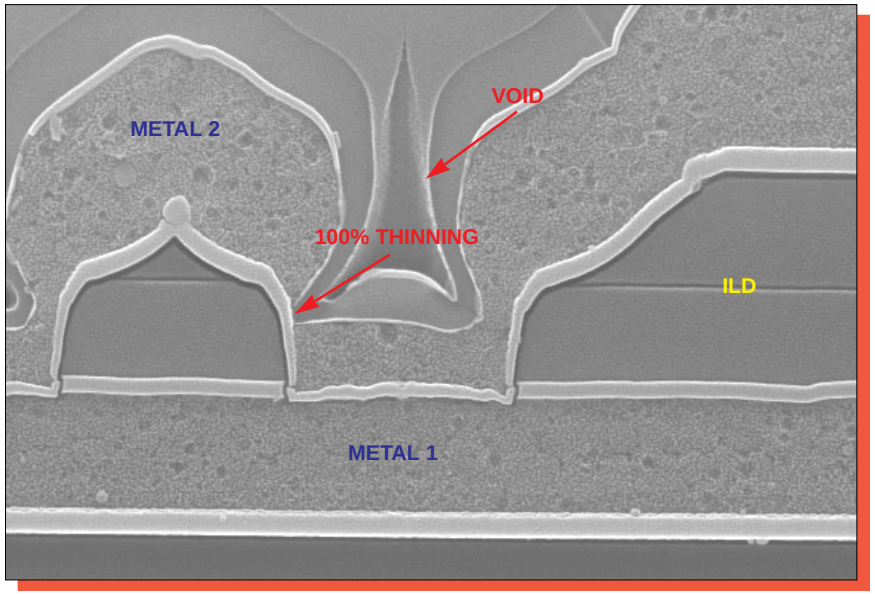
Mag. 14,000x



Mag. 14,600x

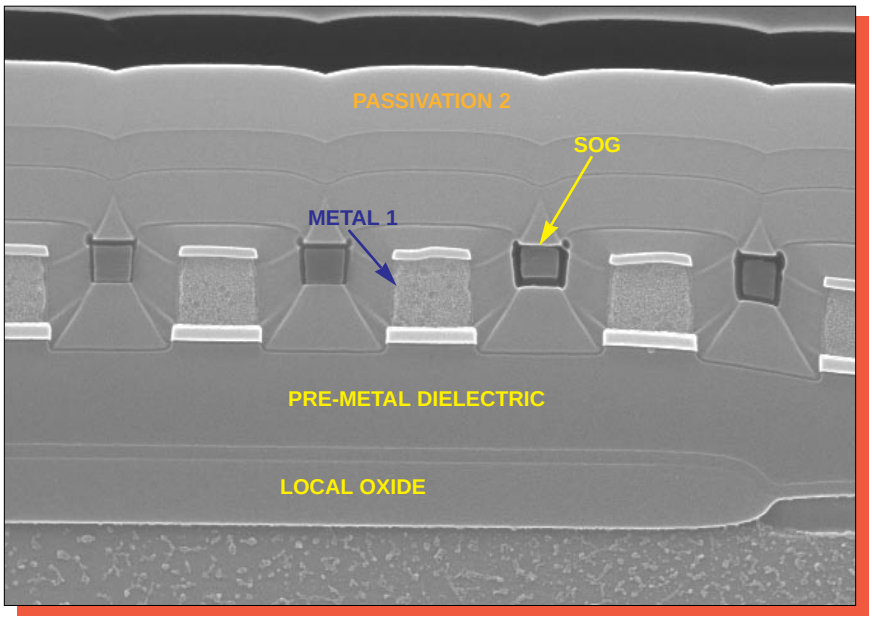


Mag. 30,000x

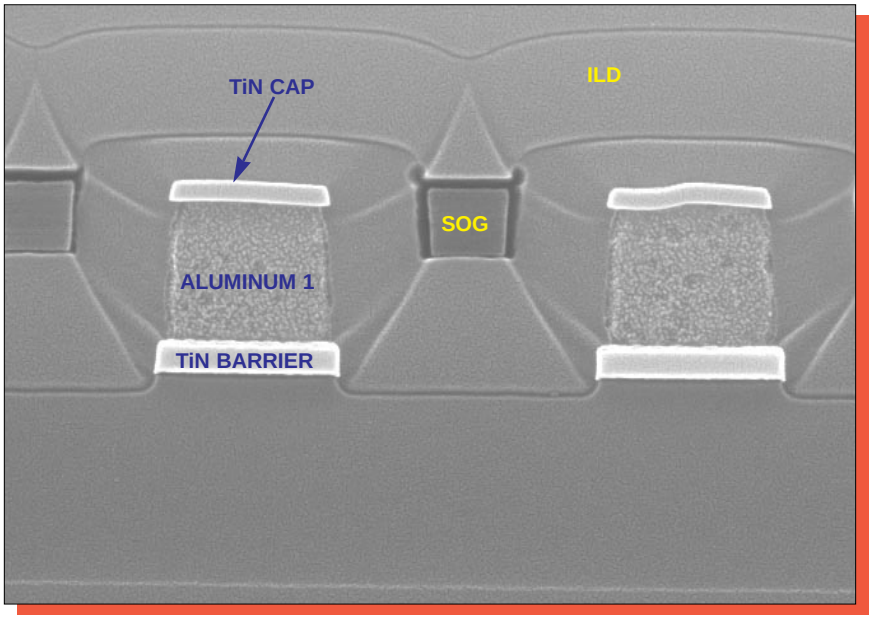


Mag. 30,000x

Figure 15. SEM section views of metal 2-to-metal 1 vias.

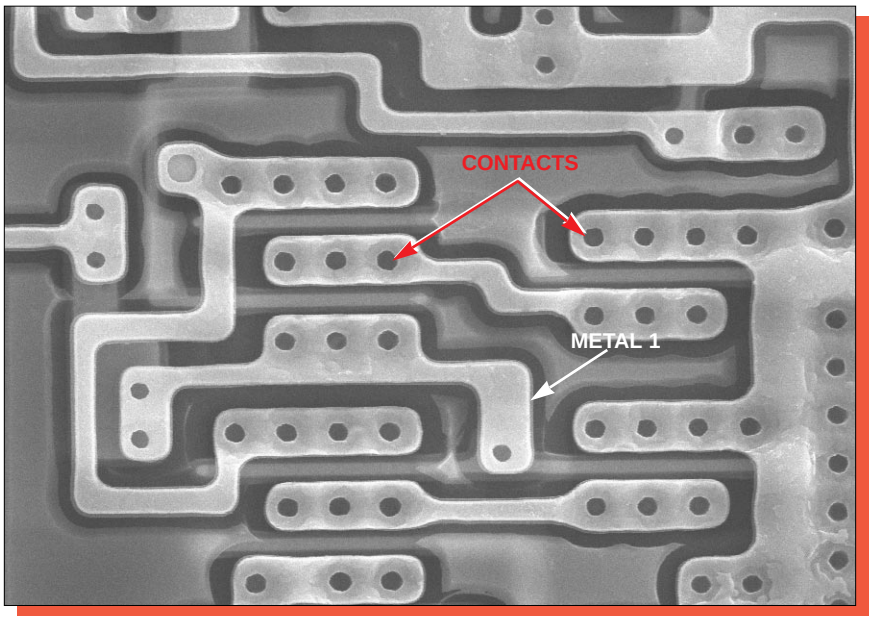


Mag. 18,300x

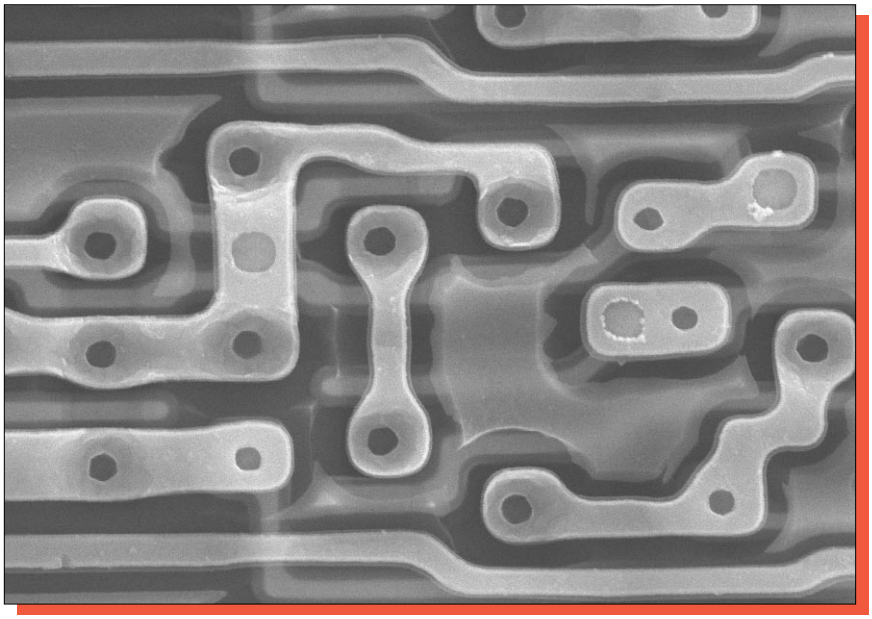


Mag. 37,300x

Figure 16. SEM section views of metal 1 line profiles.

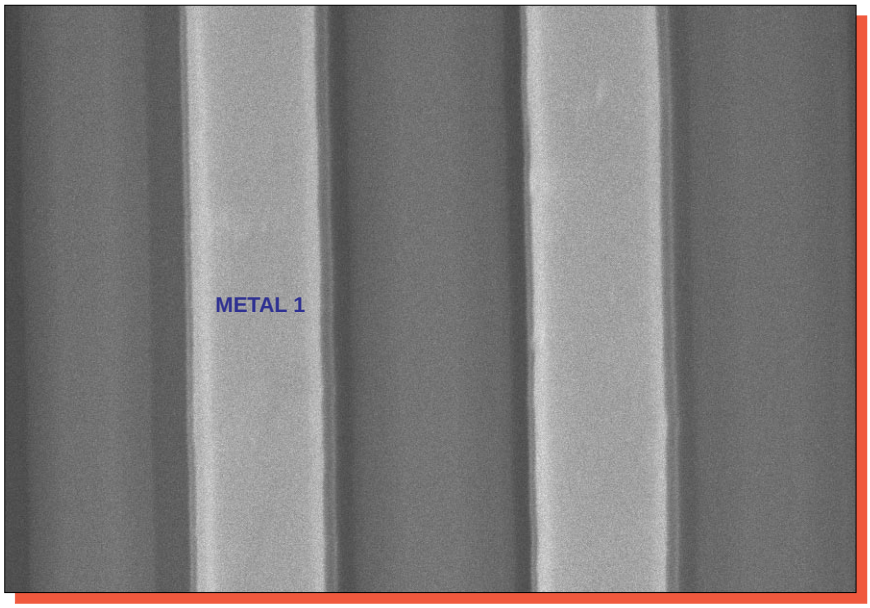


Mag. 4000x

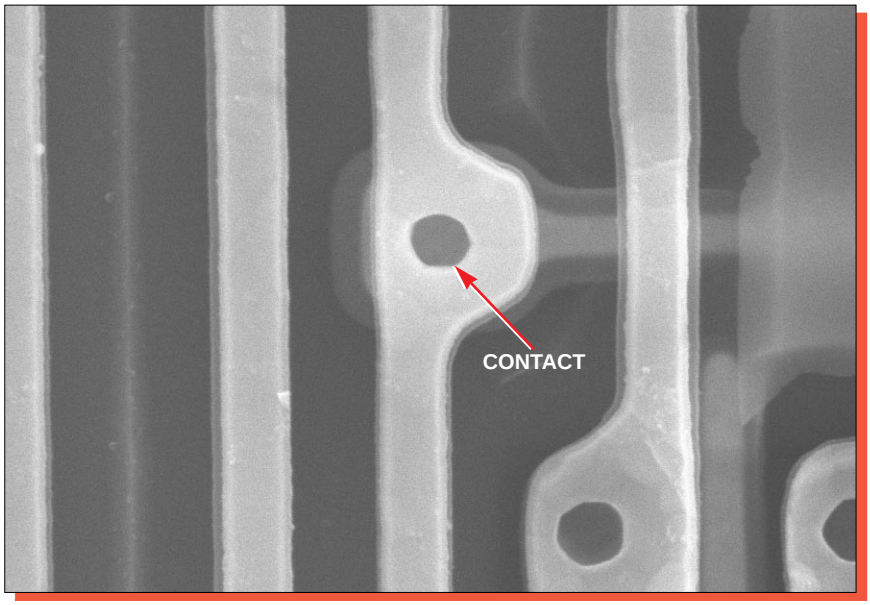


Mag. 6000x

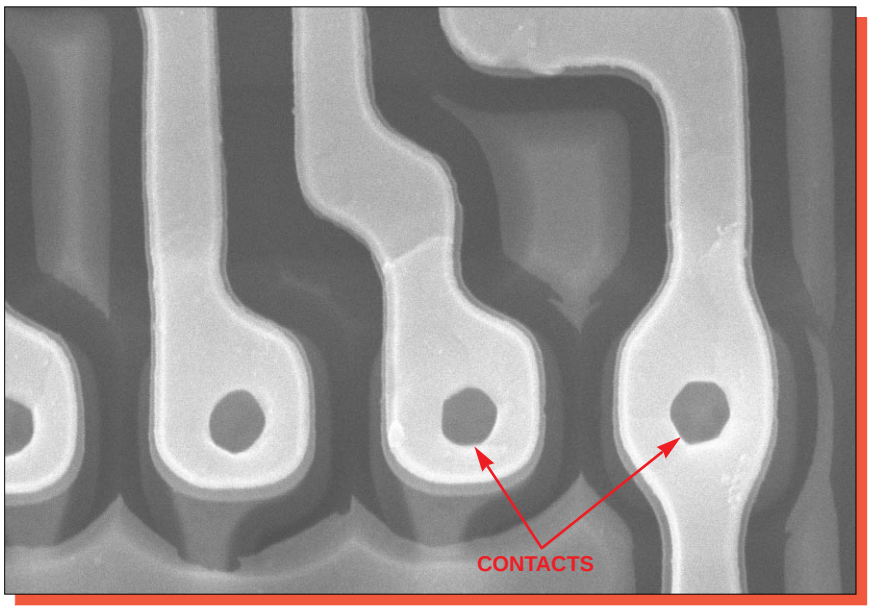
Figure 17. Topological SEM views of metal 1 patterning. 0°.



Mag. 26,000x

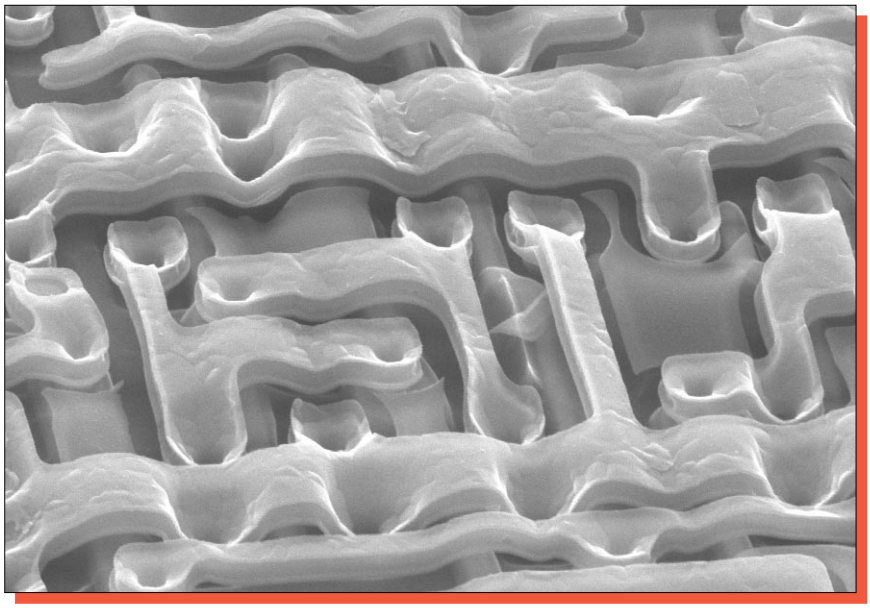


Mag. 13,000x

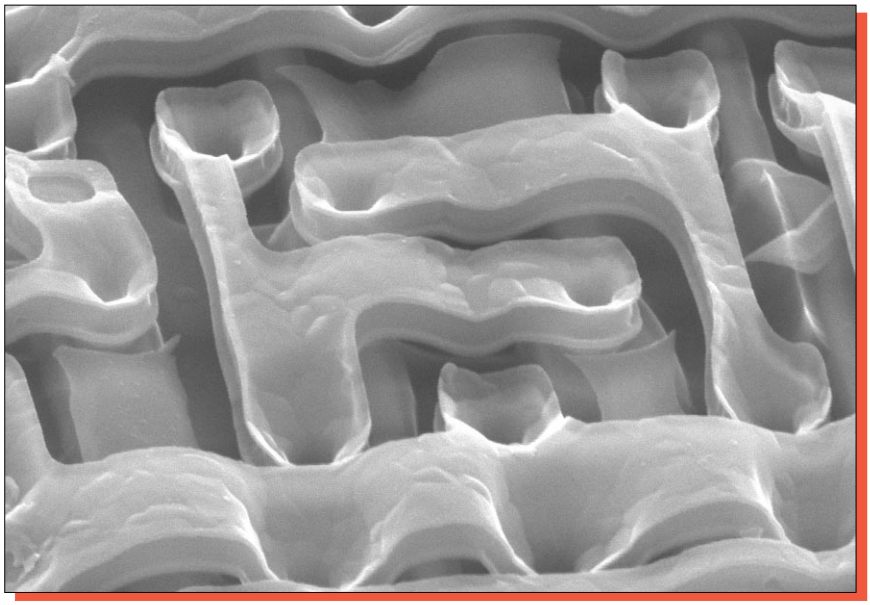


Mag. 13,000x

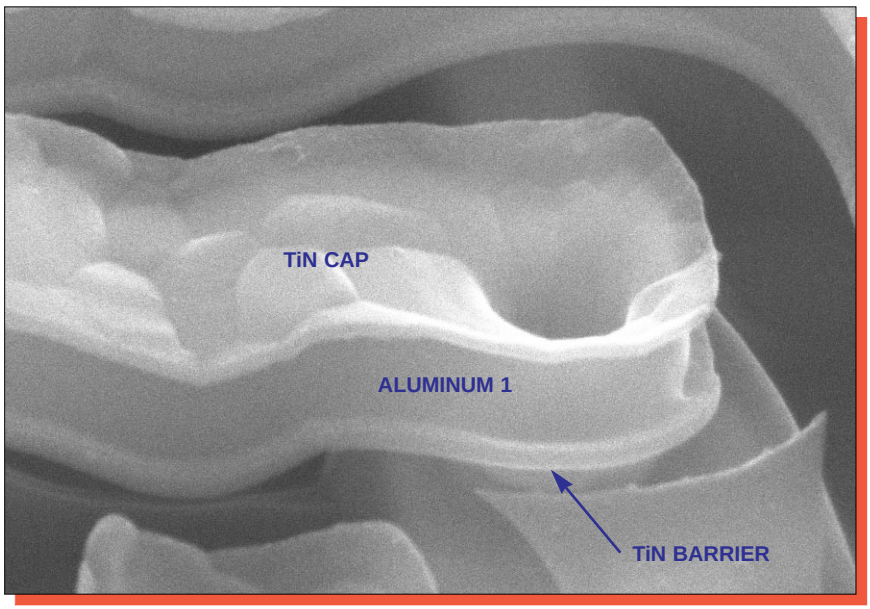
Figure 18. Topological SEM views of metal 1 design rule features. 0°.



Mag. 5500x

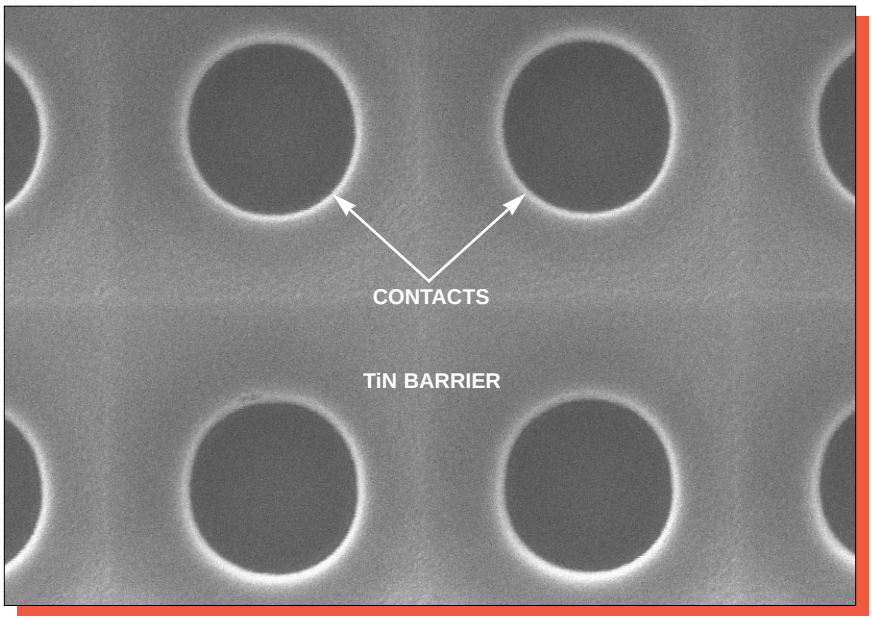


Mag. 9000x

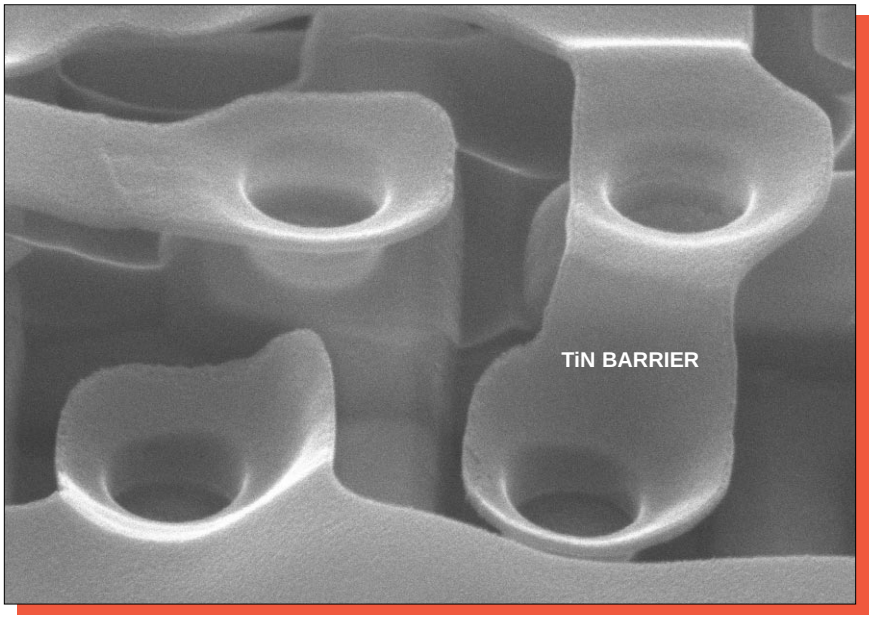


Mag. 27,000x

Figure 19. SEM views of general metal 1 integrity. 55°.

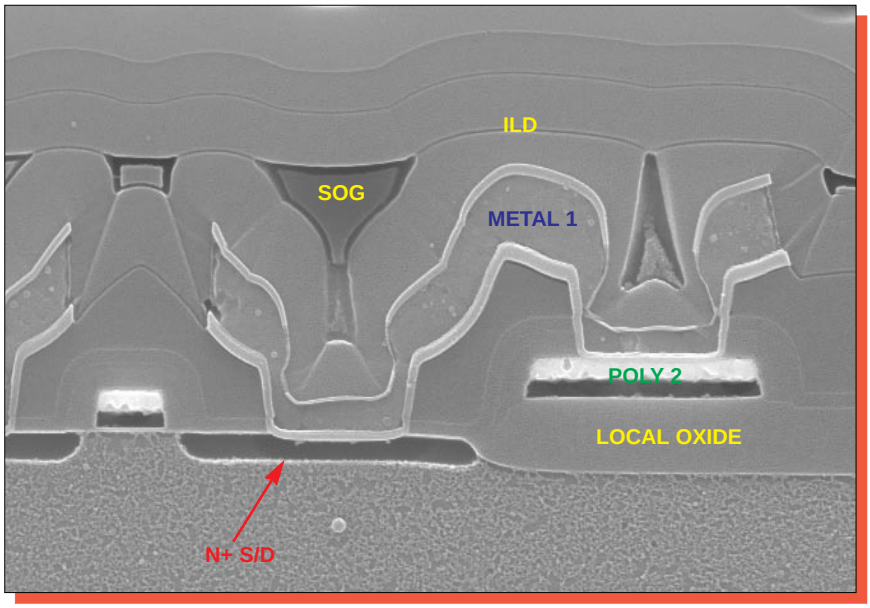


Mag. 26,000x, 0°

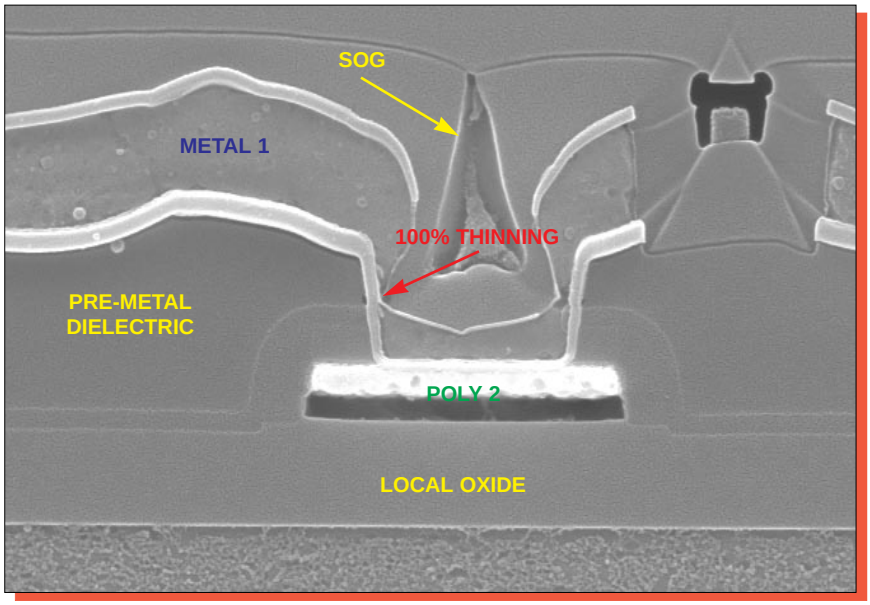


Mag. 20,000x, 55°

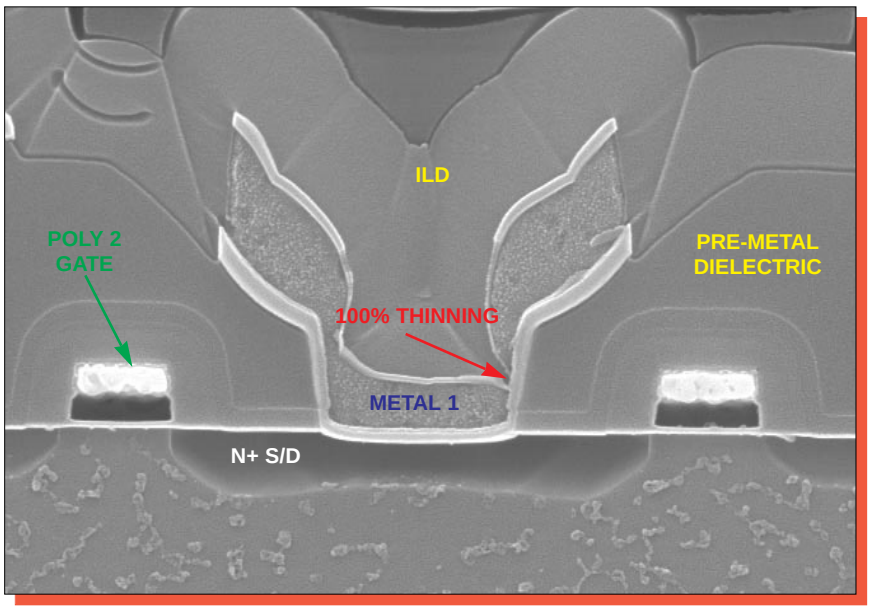
Figure 20. SEM views of metal 1 barrier.



Mag. 19,500x

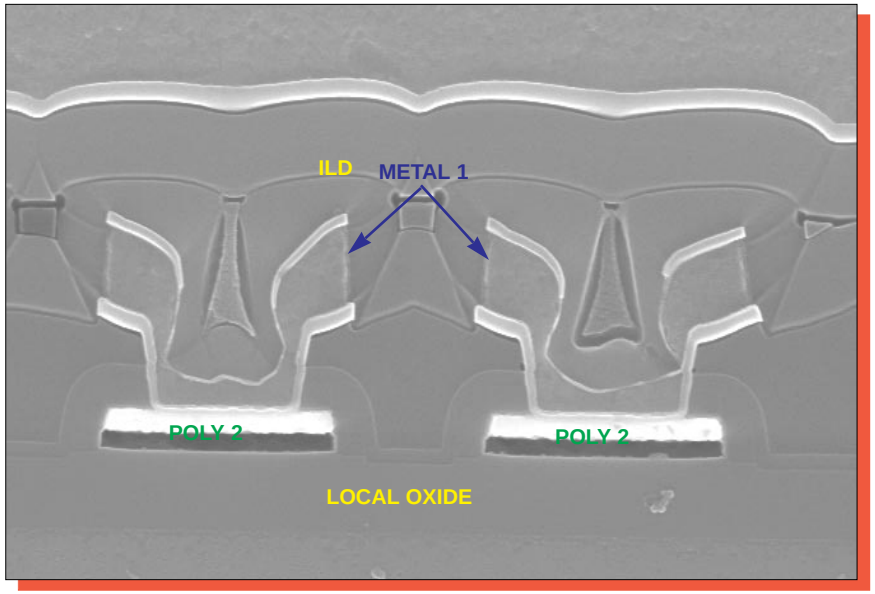


Mag. 27,400x

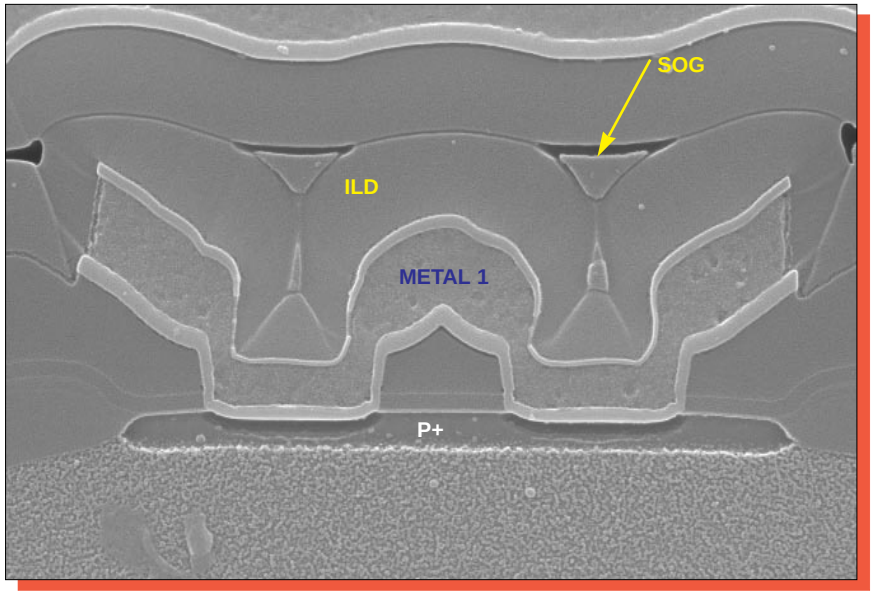


Mag. 29,300x

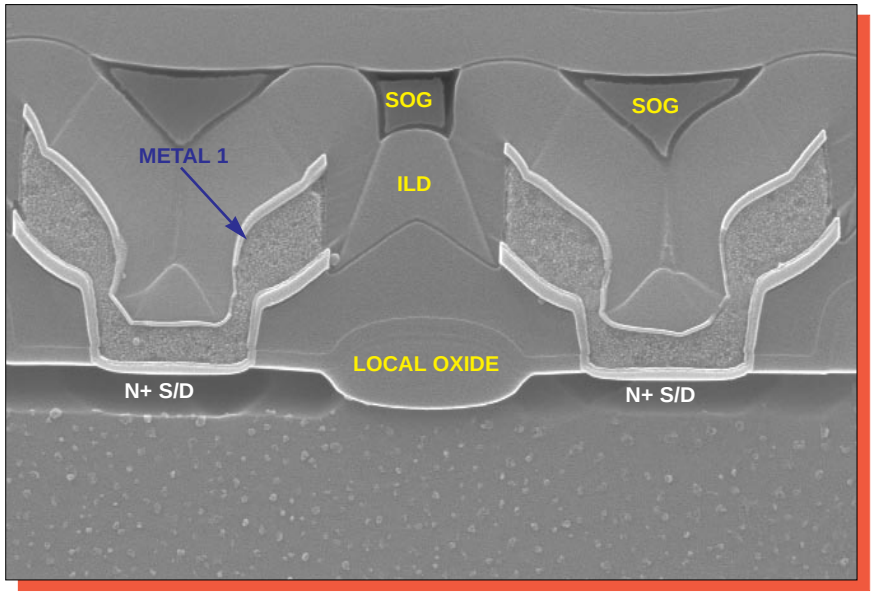
Figure 21. SEM section views of metal 1 contacts.



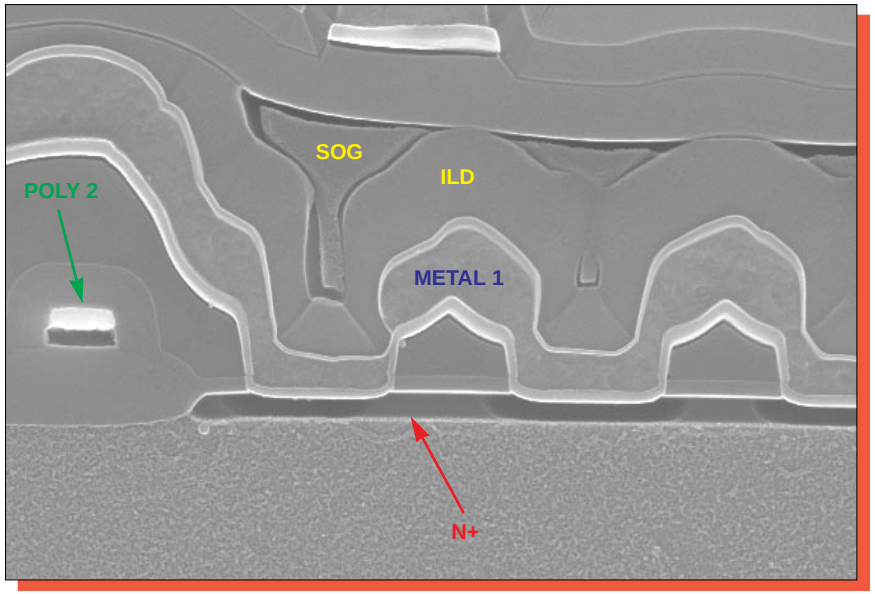
Mag. 20,500x



Mag. 23,300x

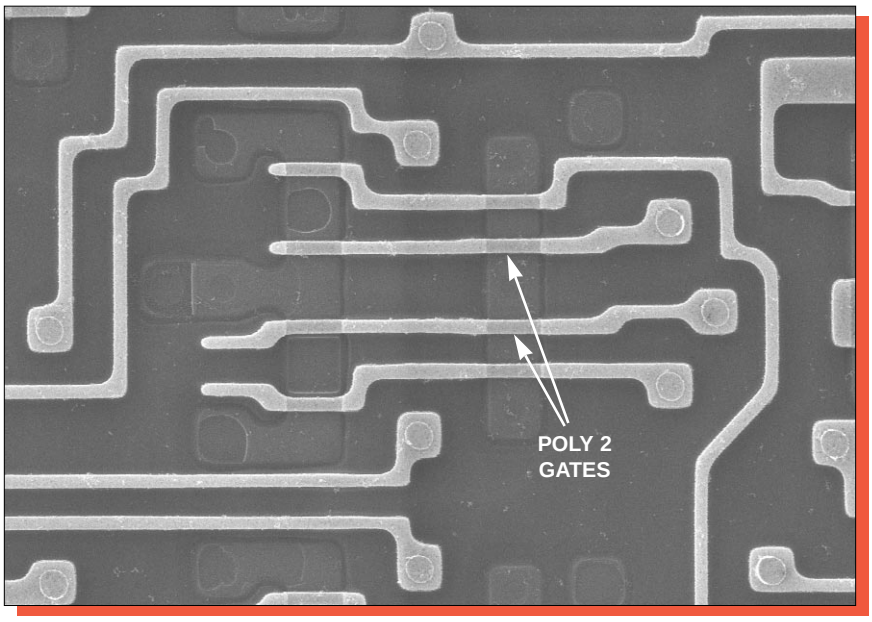


Mag. 23,000x



Mag. 20,500x

Figure 22. SEM section views illustrating metal 1 contact spacings.



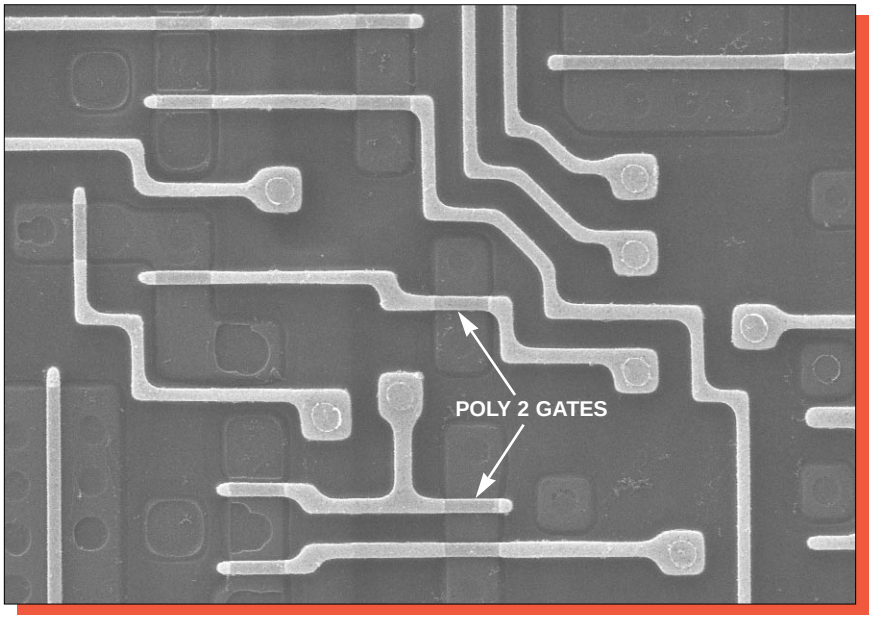
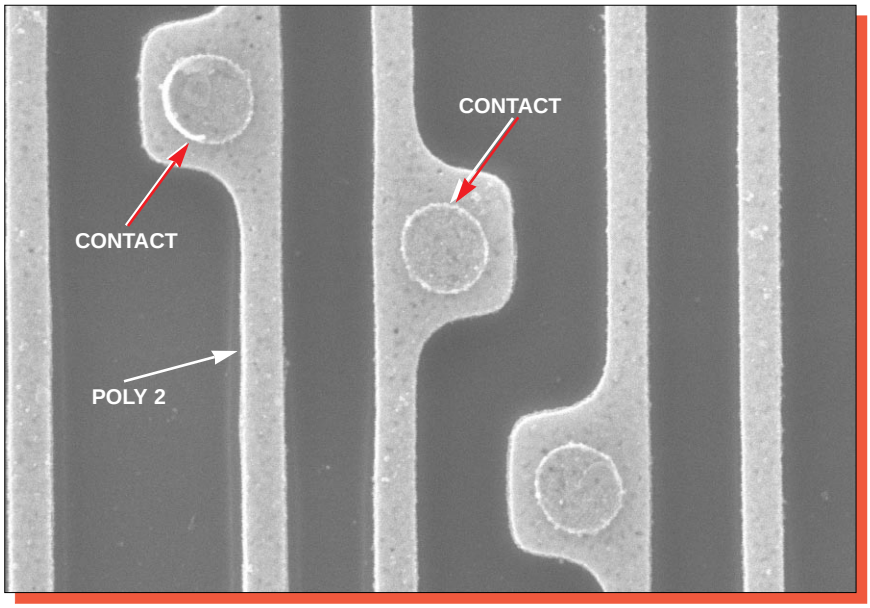
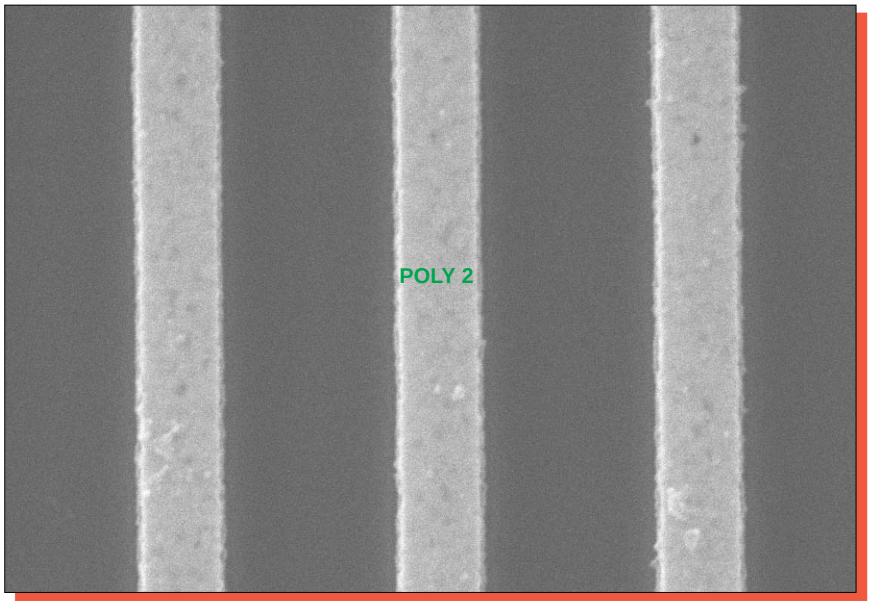


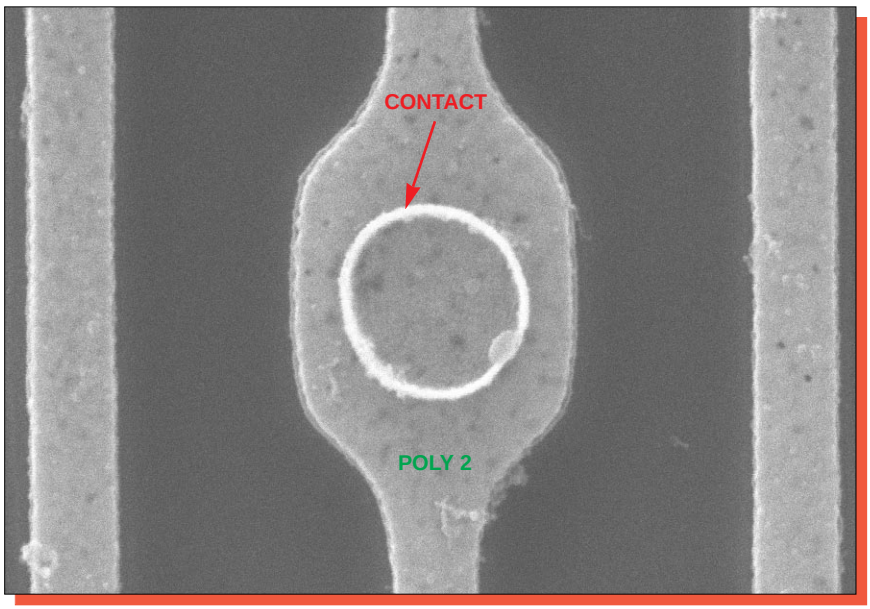
Figure 23. Topological SEM views of poly patterning. Mag. 4000x, 0°.



Mag. 13,000x

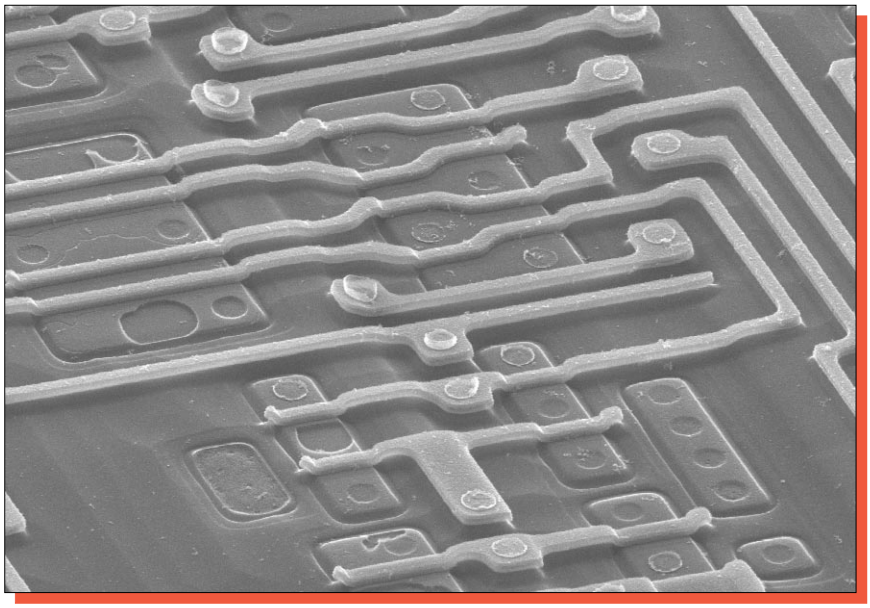


Mag. 26,000x

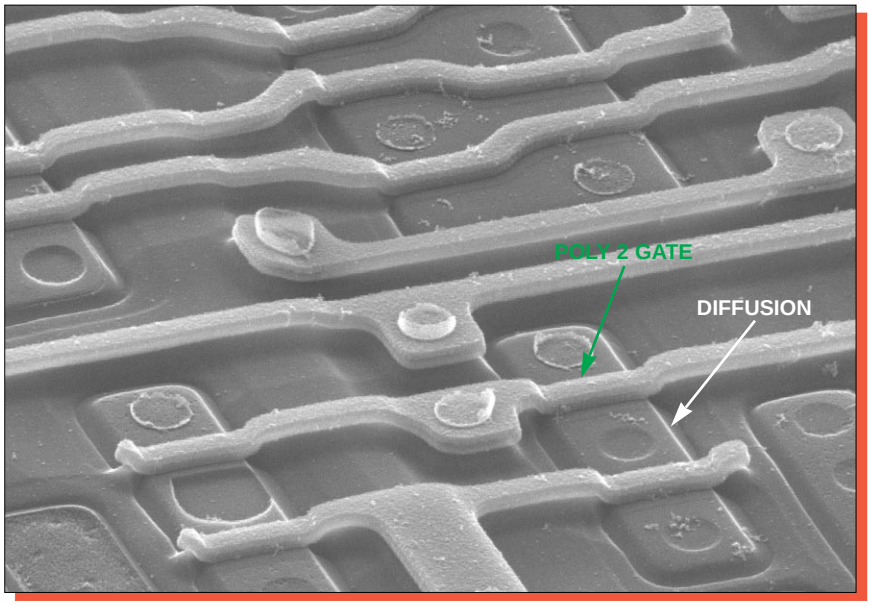


Mag. 26,000x

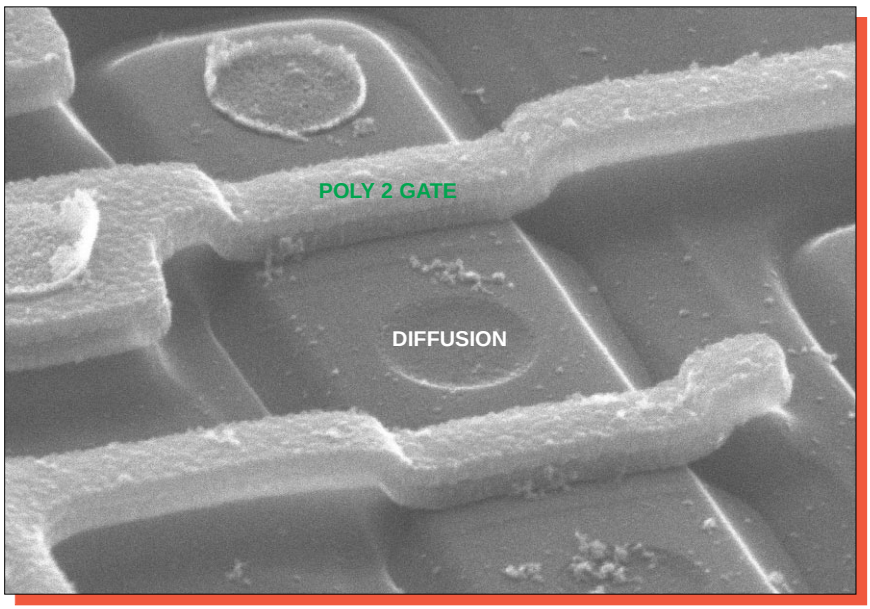
Figure 24. Topological SEM views of poly design rule features.



Mag. 5000x

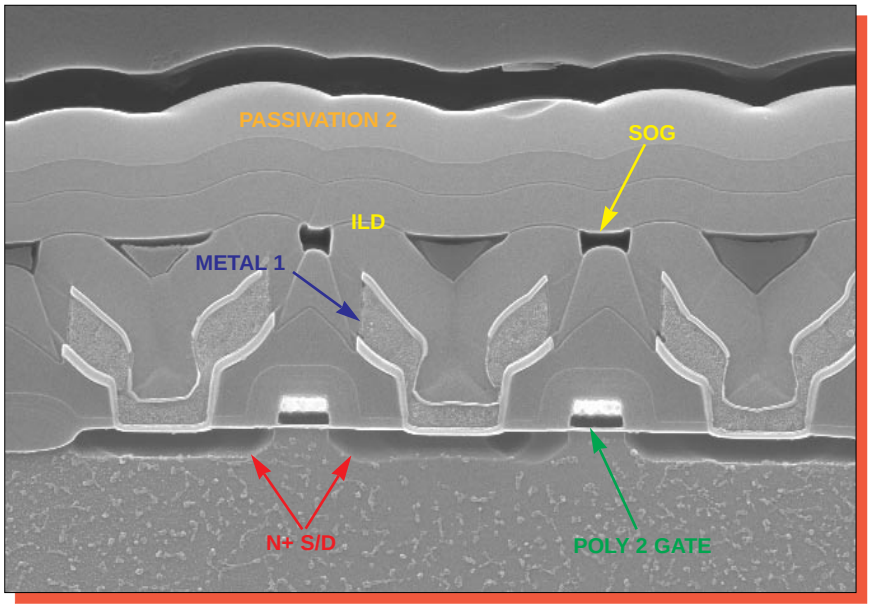


Mag. 9000x

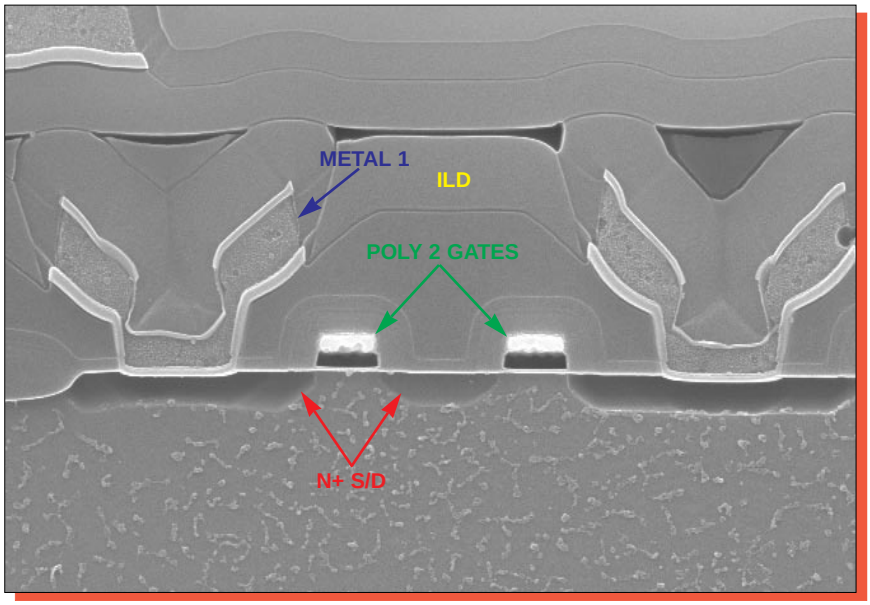


Mag. 25,000x

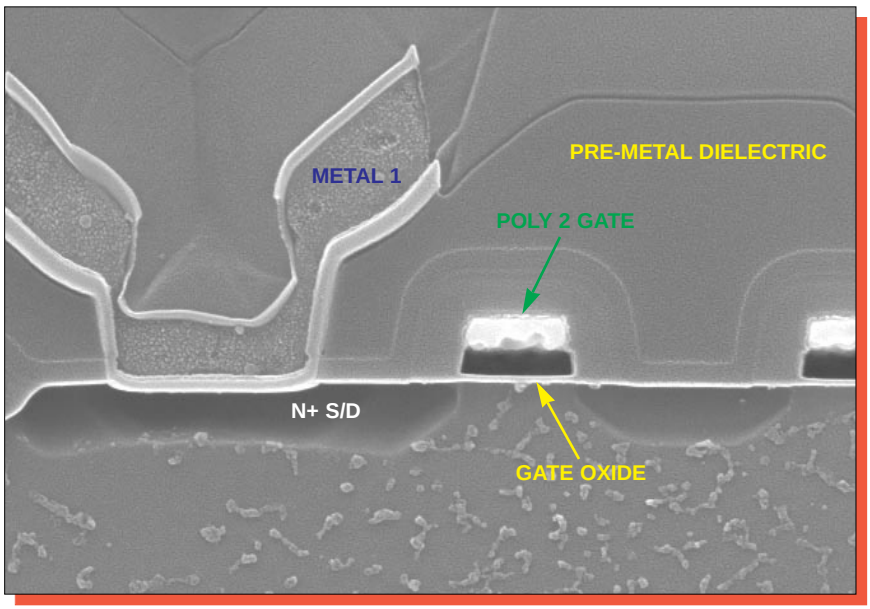
Figure 25. Perspective SEM views of poly coverage. 55°.



Mag. 14,600x

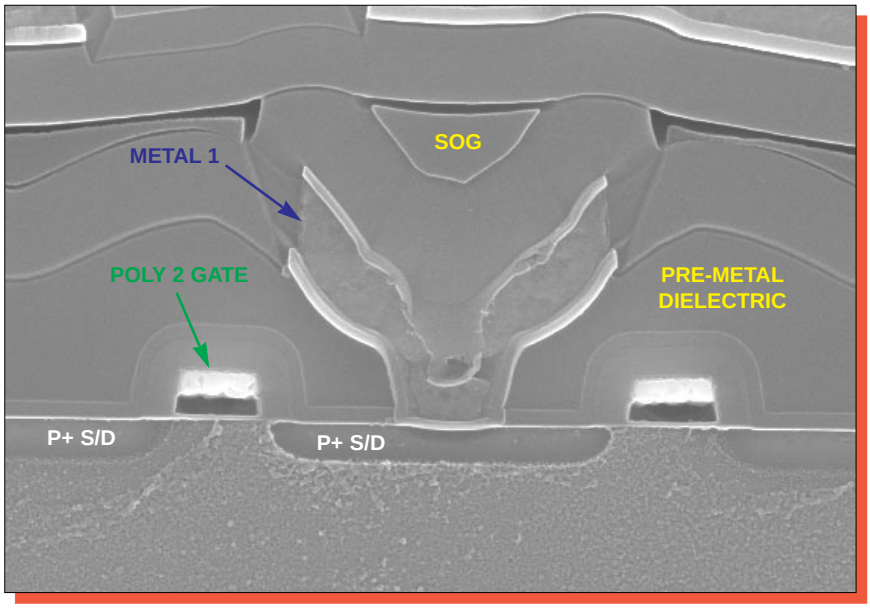


Mag. 17,700x

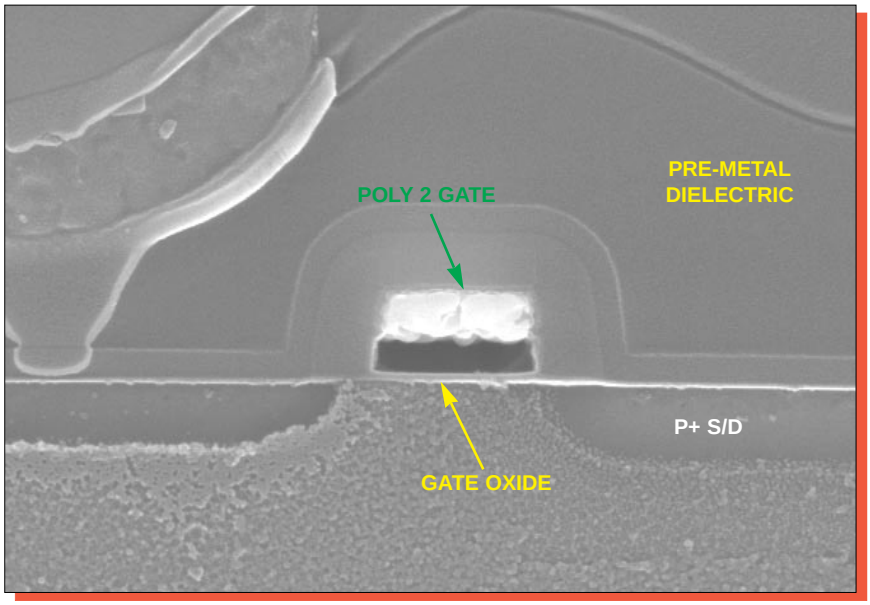


Mag. 31,500x

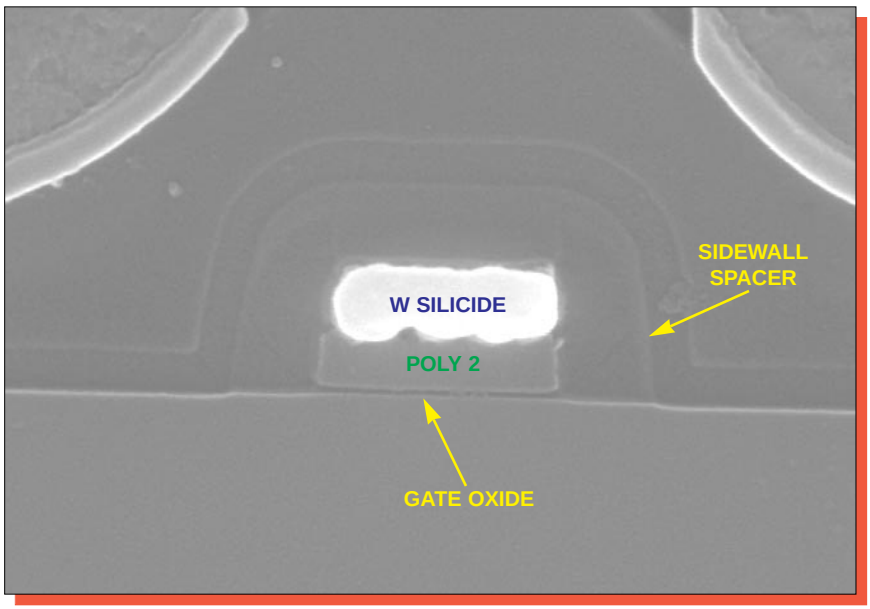
Figure 26. SEM section views of N-channel transistors.



Mag. 22,200x

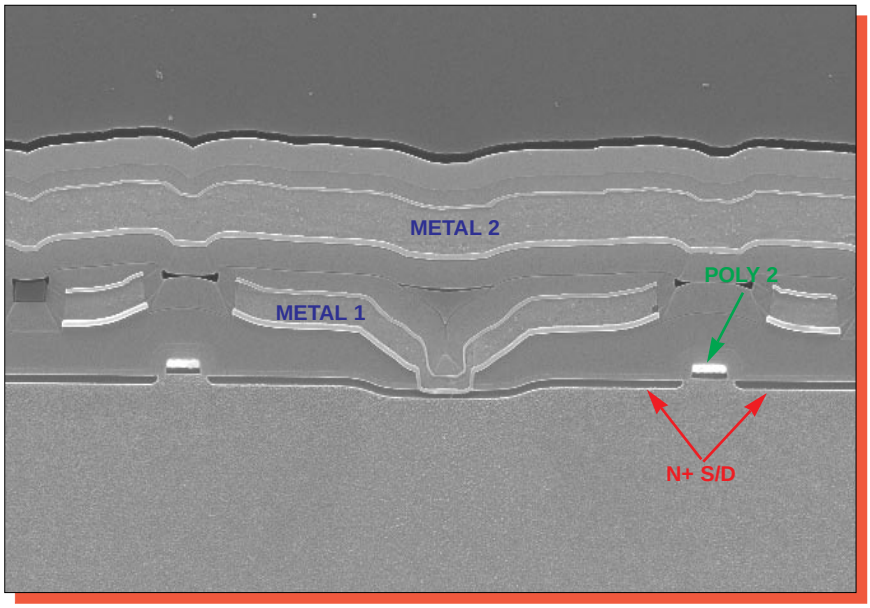


Mag. 42,000x

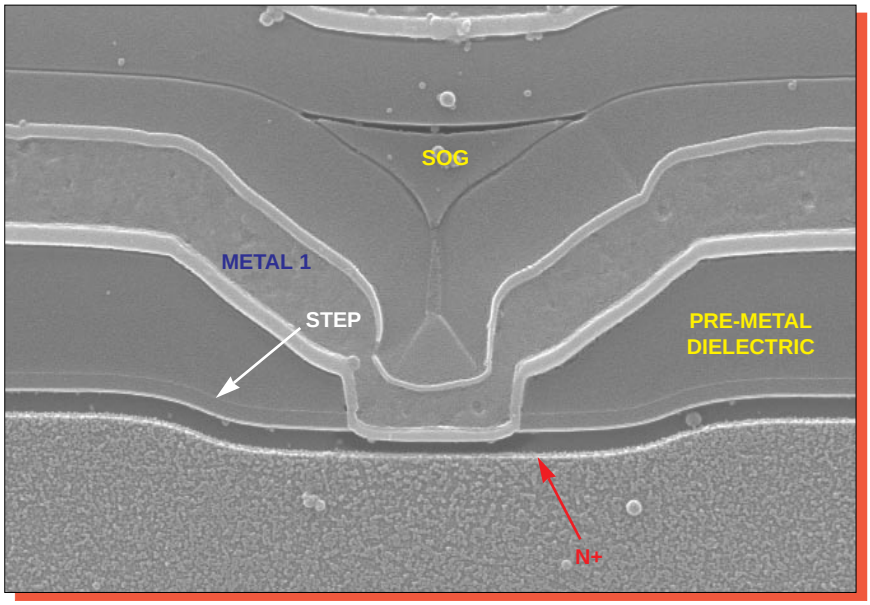


Mag. 61,000x

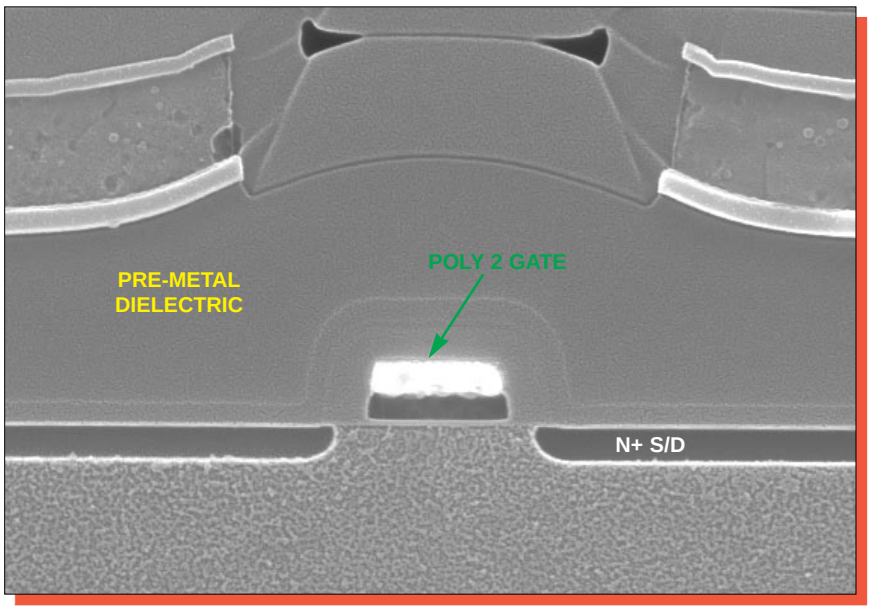
Figure 27. SEM section views of P-channel transistors.



Mag. 7500x

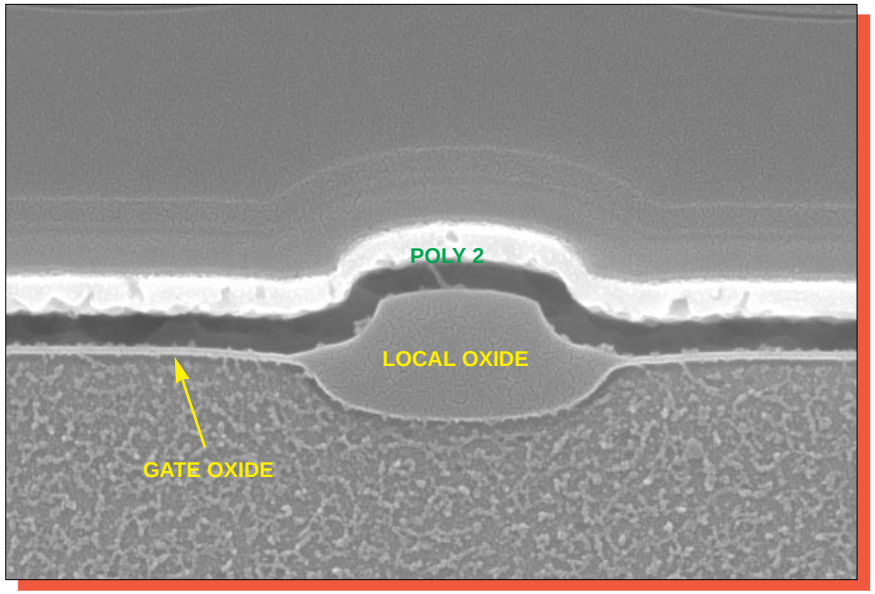


Mag. 23,200x

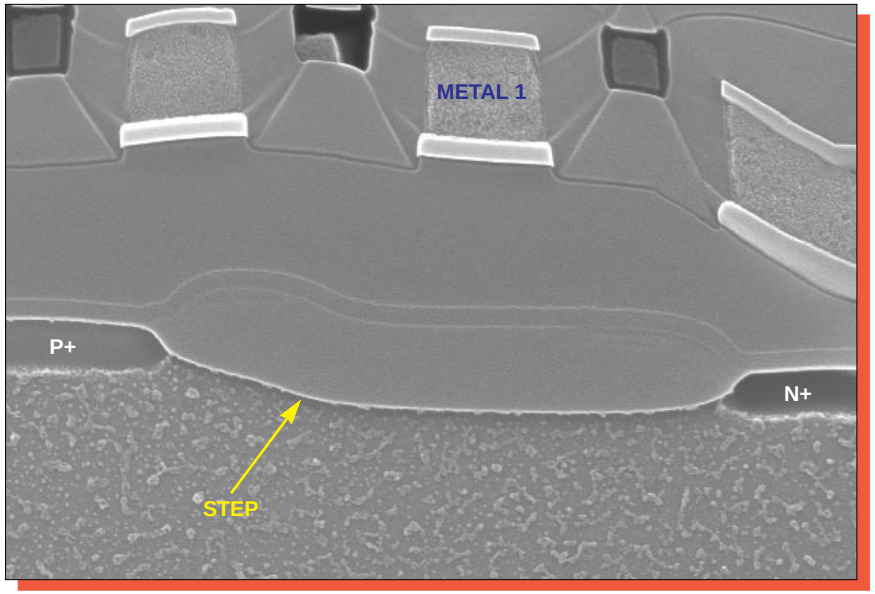


Mag. 30,000x

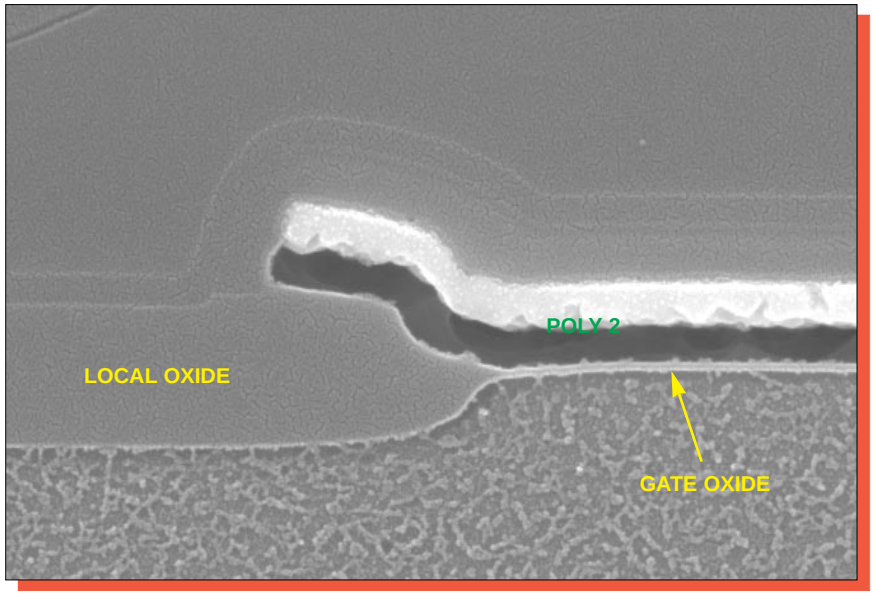
Figure 28. SEM section views of the I/O structure.



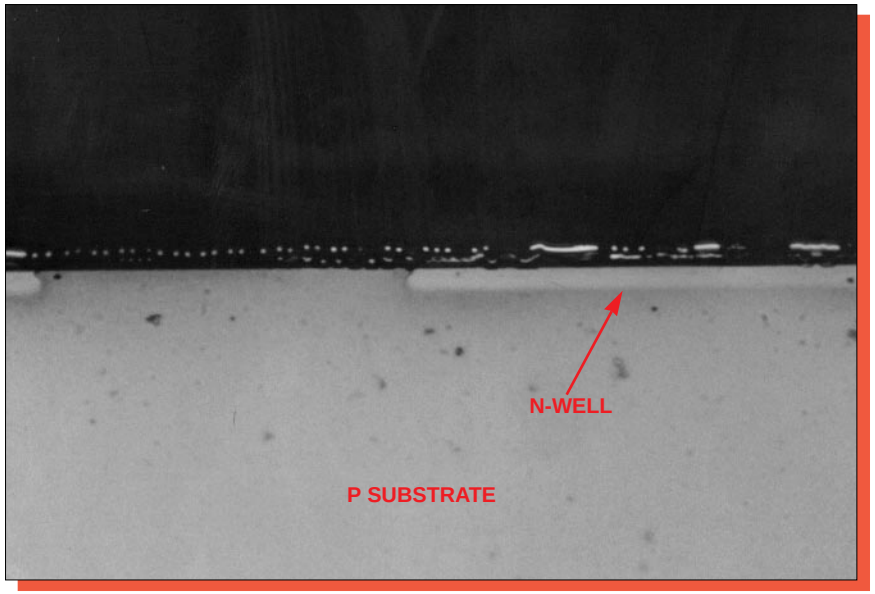
Mag. 36,400x



Mag. 25,300x

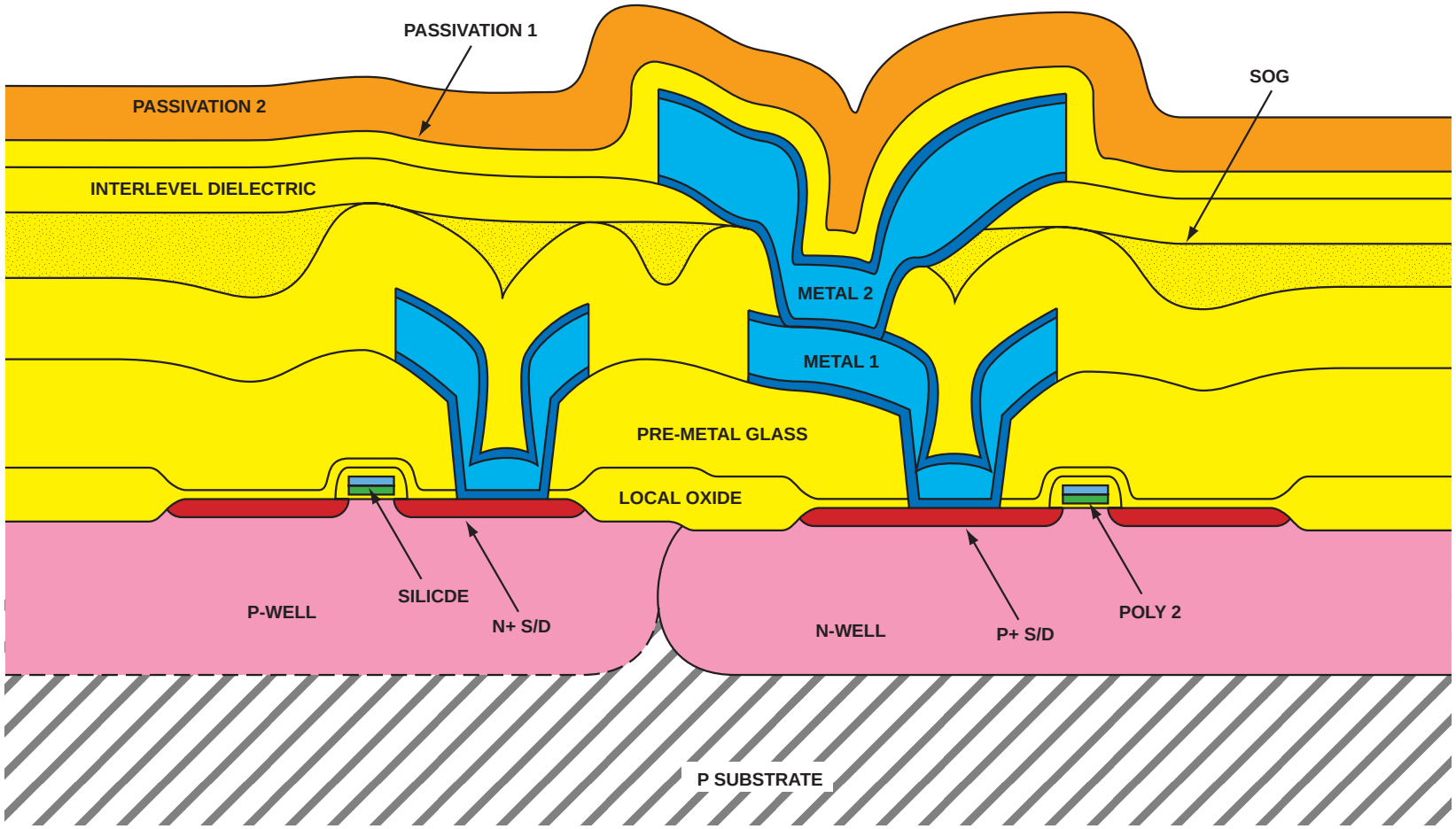


Mag. 41,200x



Mag. 800x

Figure 29. SEM section views of local oxide and well structure.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 30. Color cross section drawing illustrating device structure.

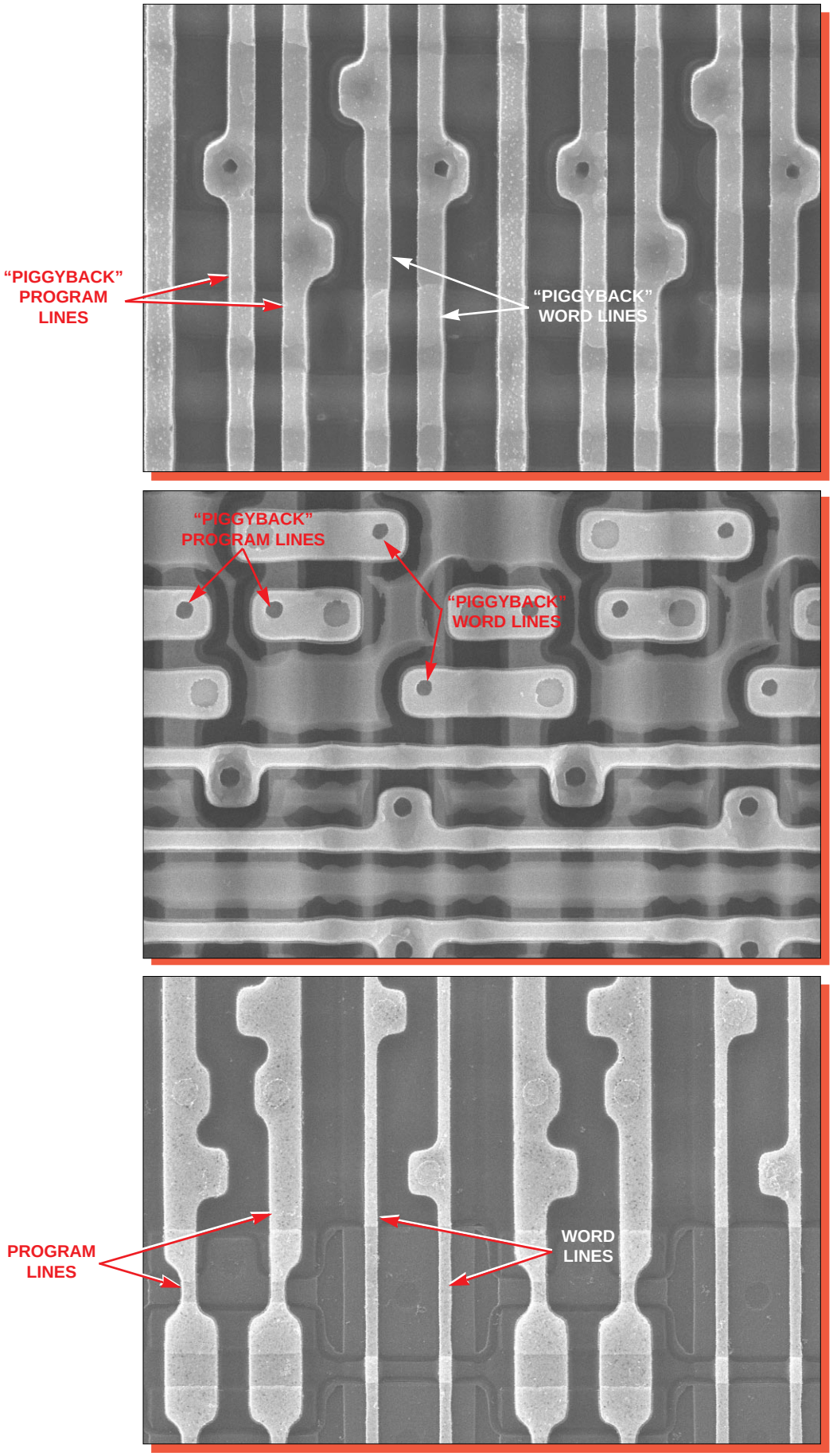


Figure 31. Topological SEM views of the EEPROM array illustrating "piggyback" word line connections. Mag. 5000x, 0°.

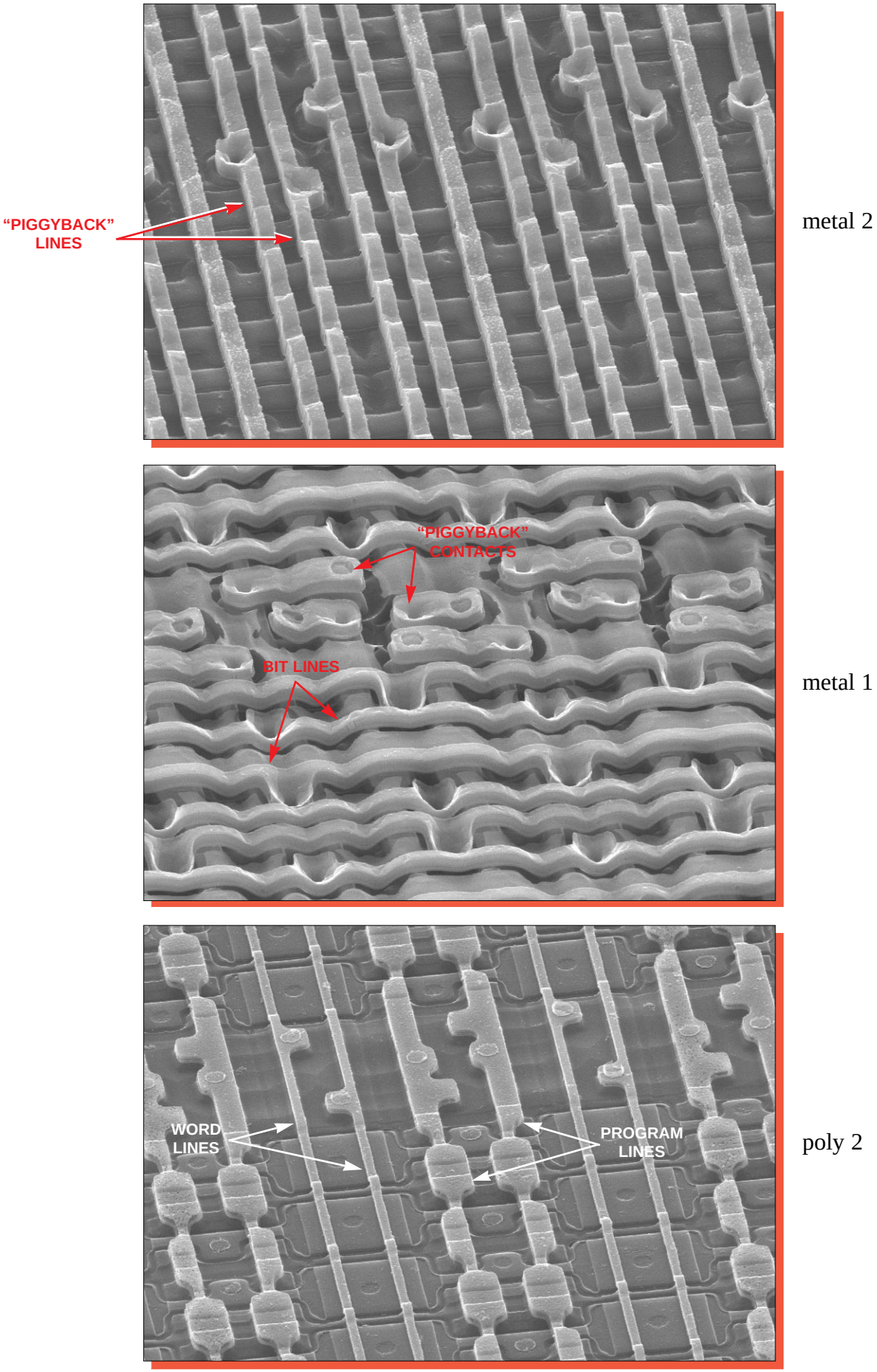
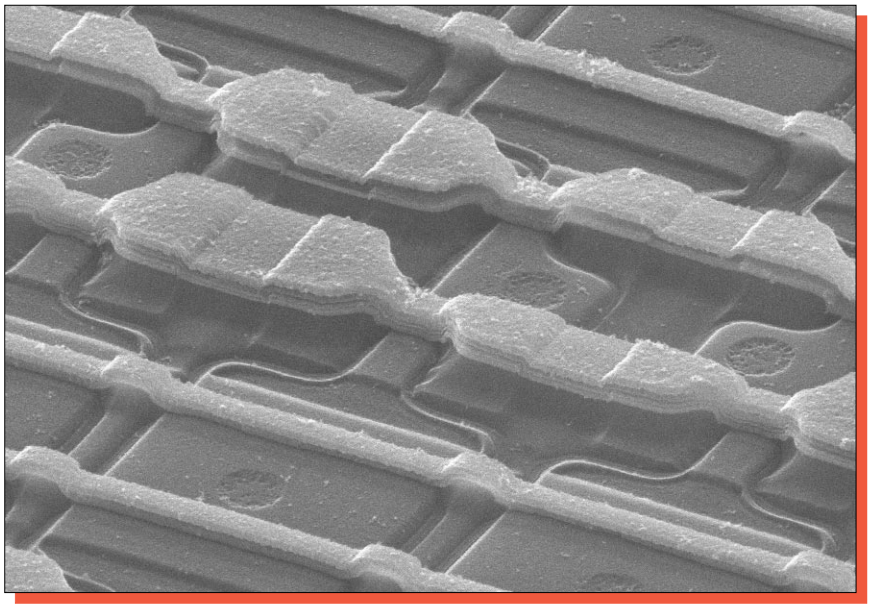
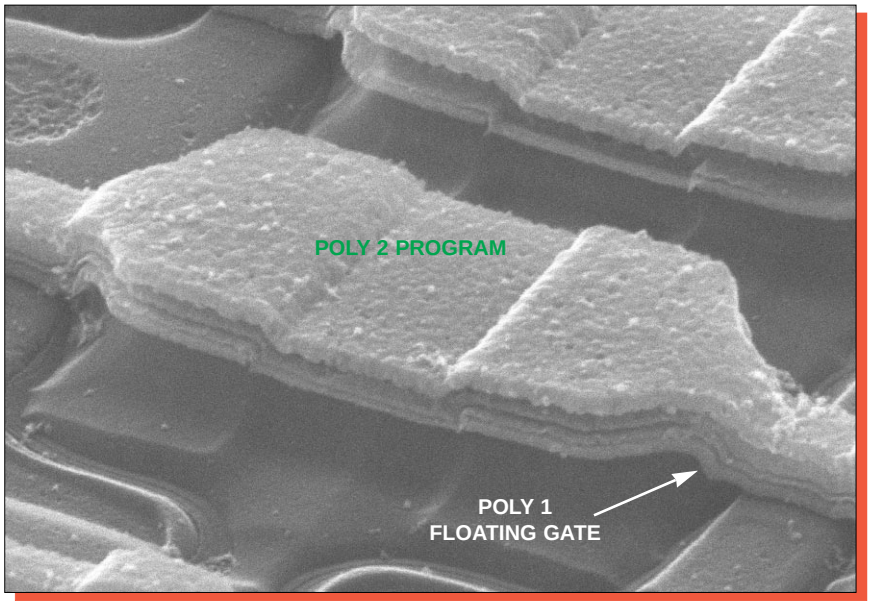


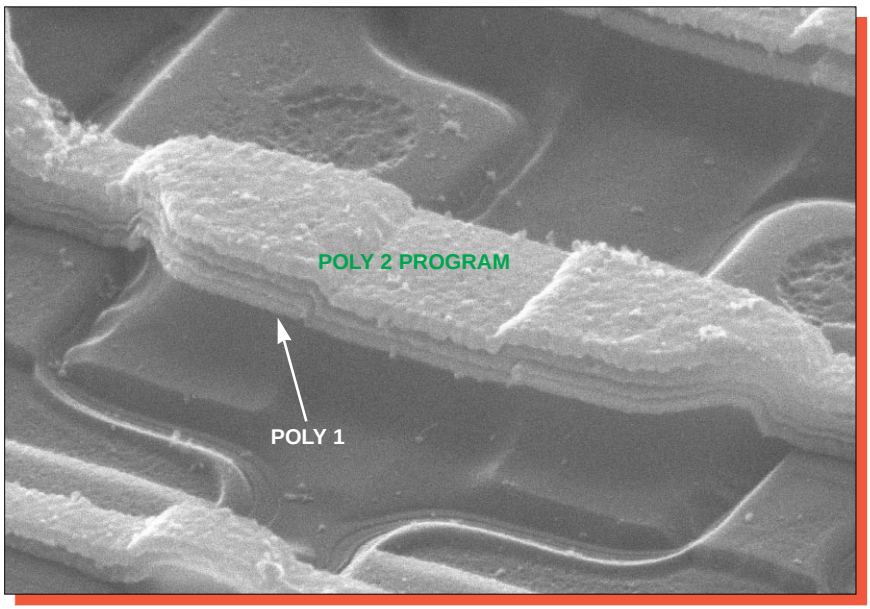
Figure 32. Perspective SEM views of the EEPROM array. Mag. 4000x, 55°.



Mag. 10,000x

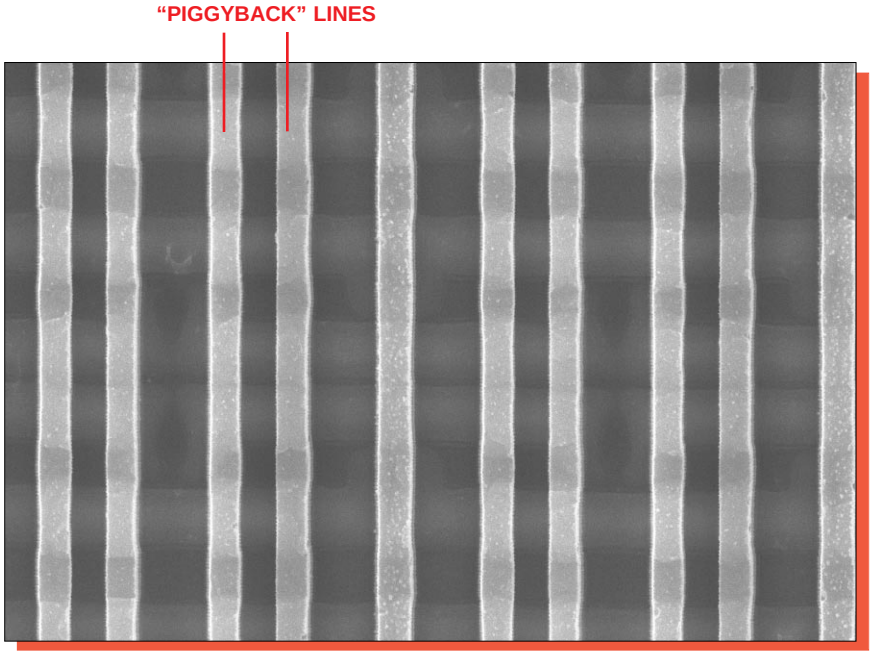


Mag. 24,000x

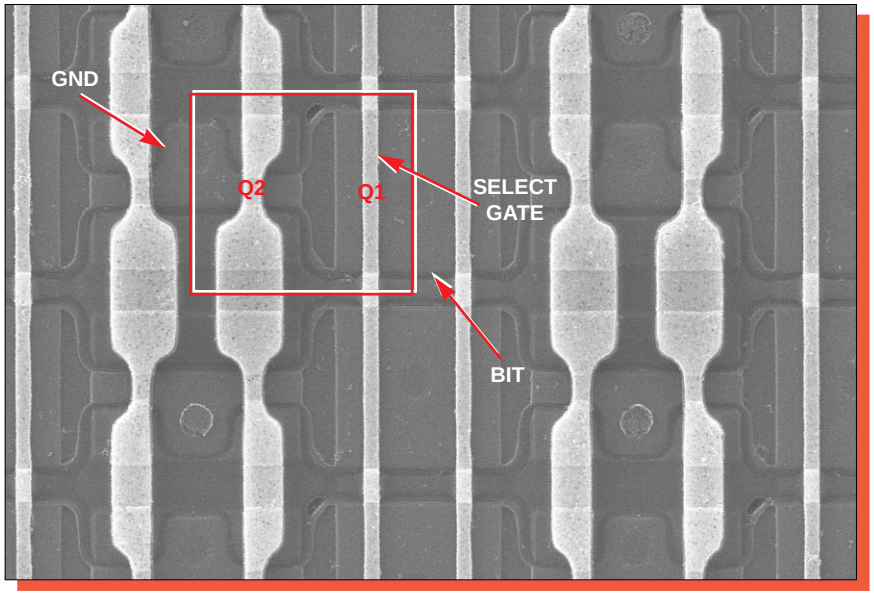


Mag. 24,000x

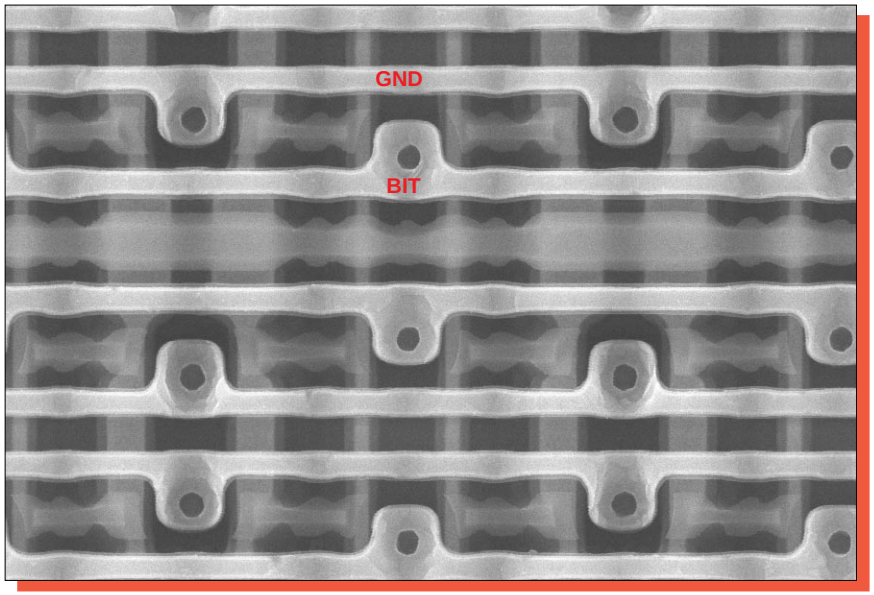
Figure 33. SEM detail views of EEPROM cells. 55°.



metal 2



poly



metal 1

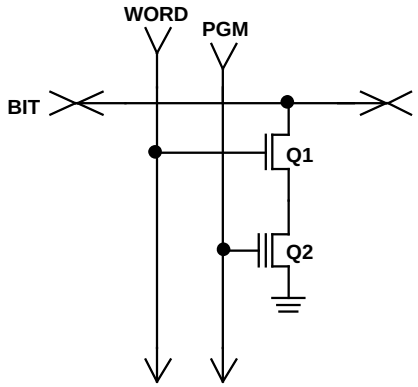
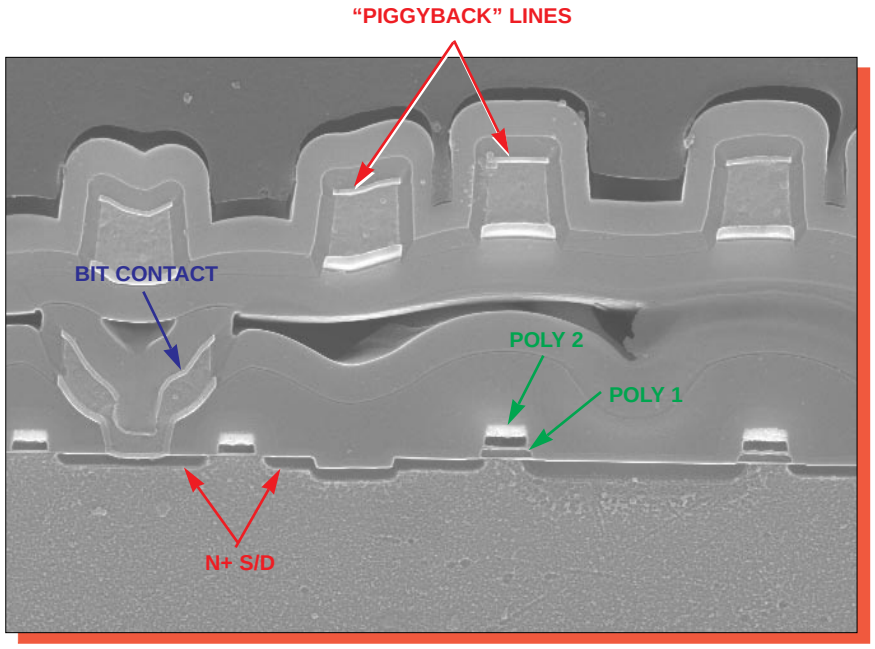
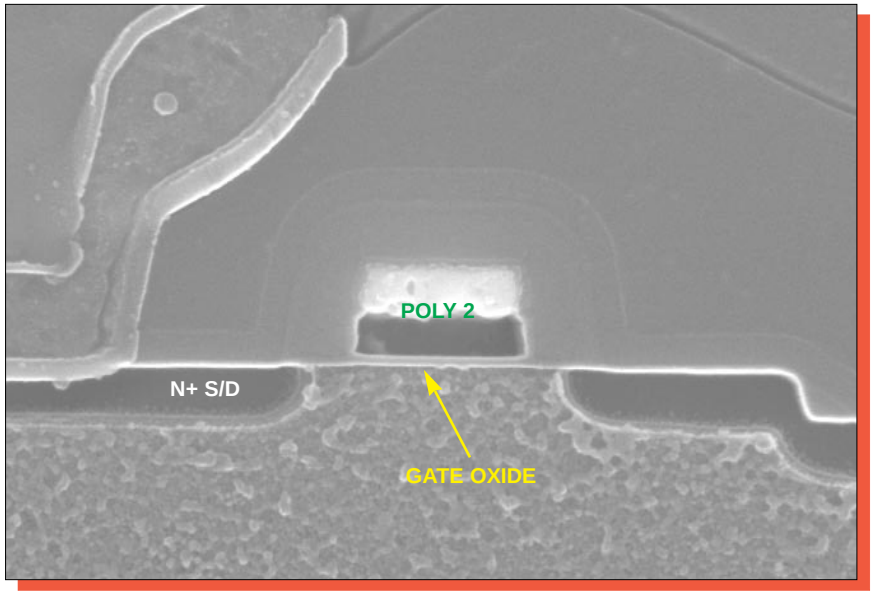


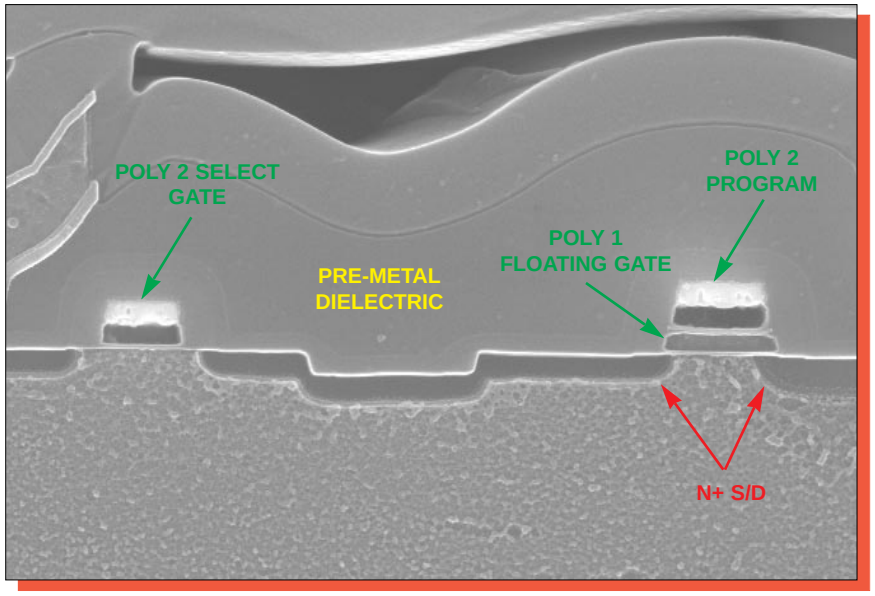
Figure 34. Topological SEM views of EEPROM cells and schematic. Mag. 5000x, 0°.



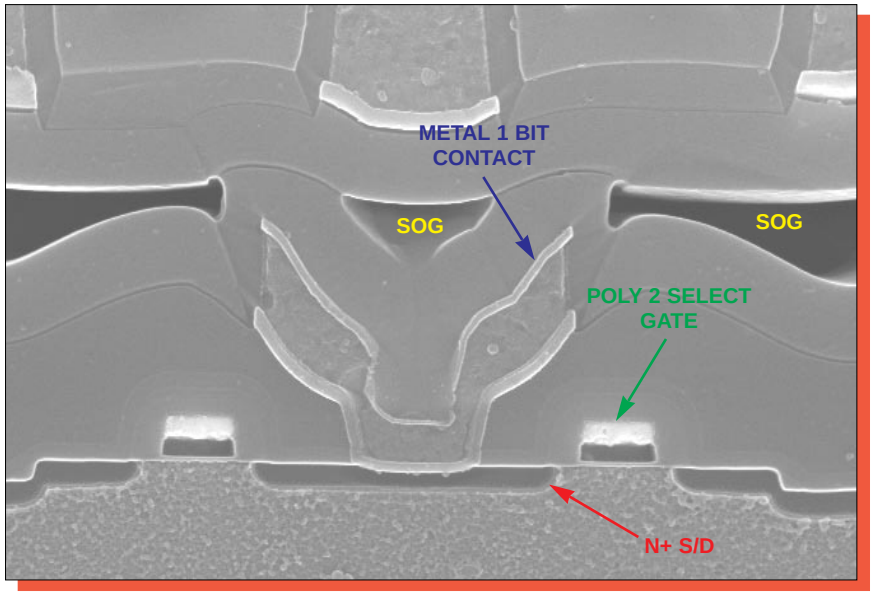
10,500x



Mag. 47,000x

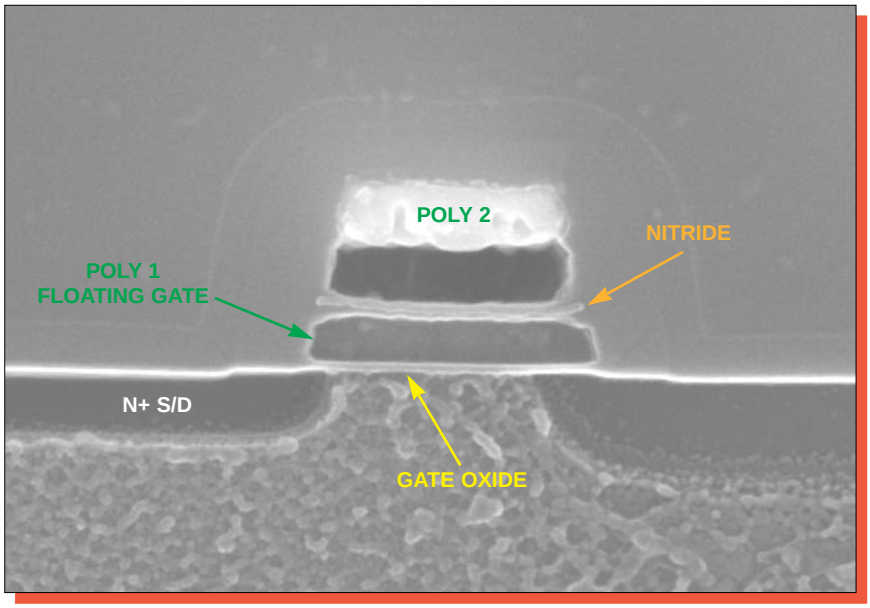


Mag. 22,500x

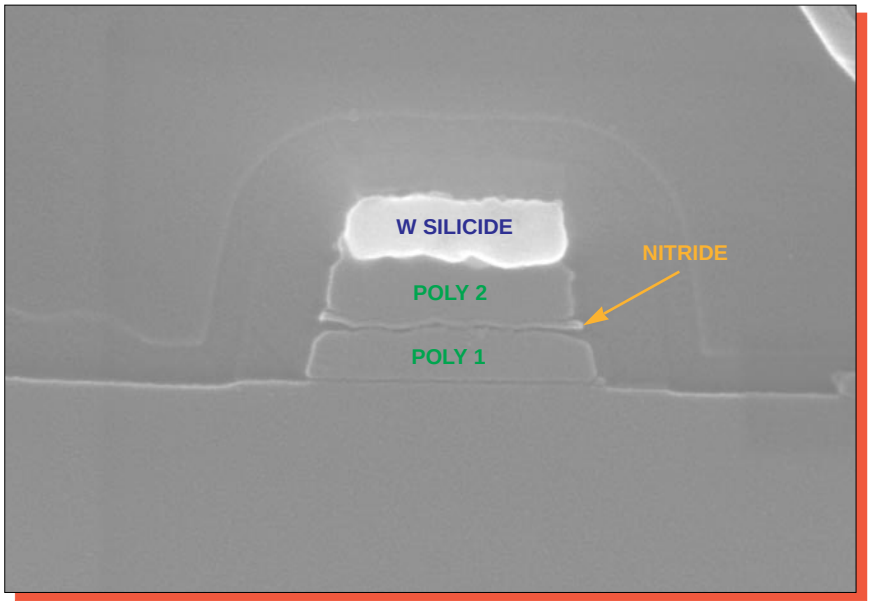


Mag. 21,000x

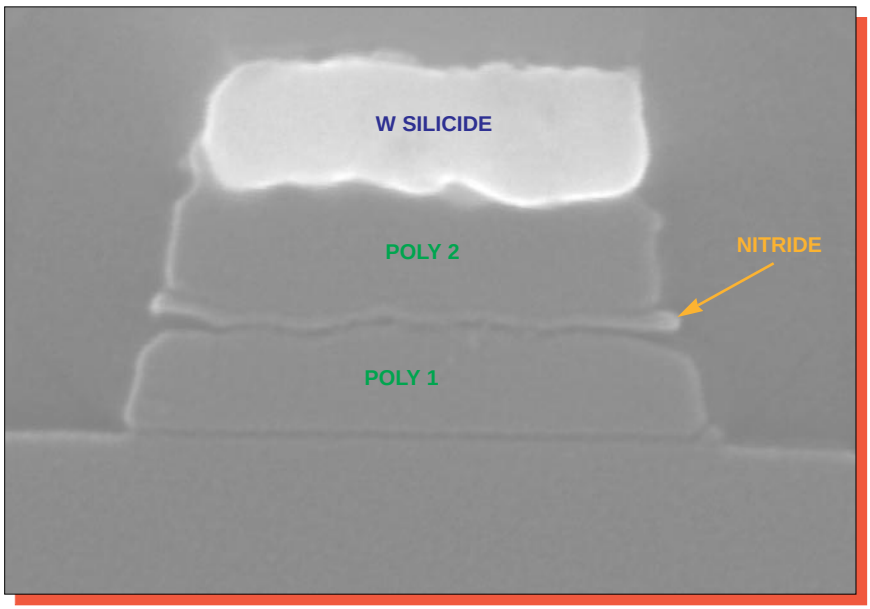
Figure 35. SEM section views of an EEPROM cell (perpendicular to word line).



Mag. 59,000x

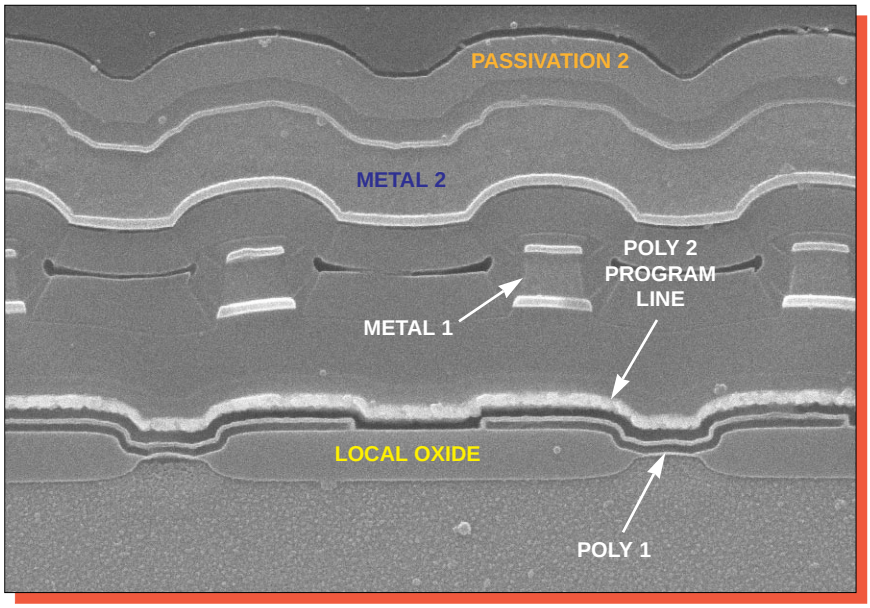


glass etch,
Mag. 59,000x

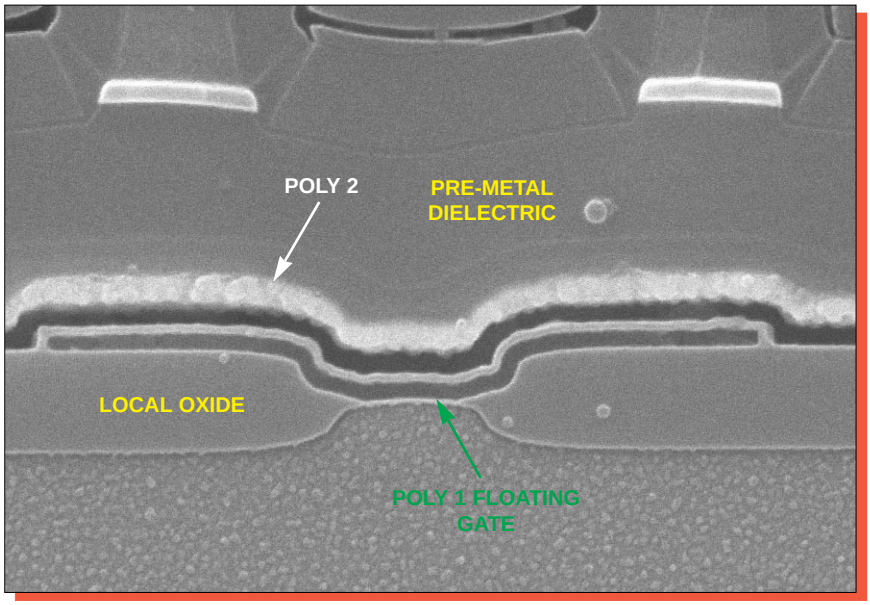


glass etch,
Mag. 117,500x

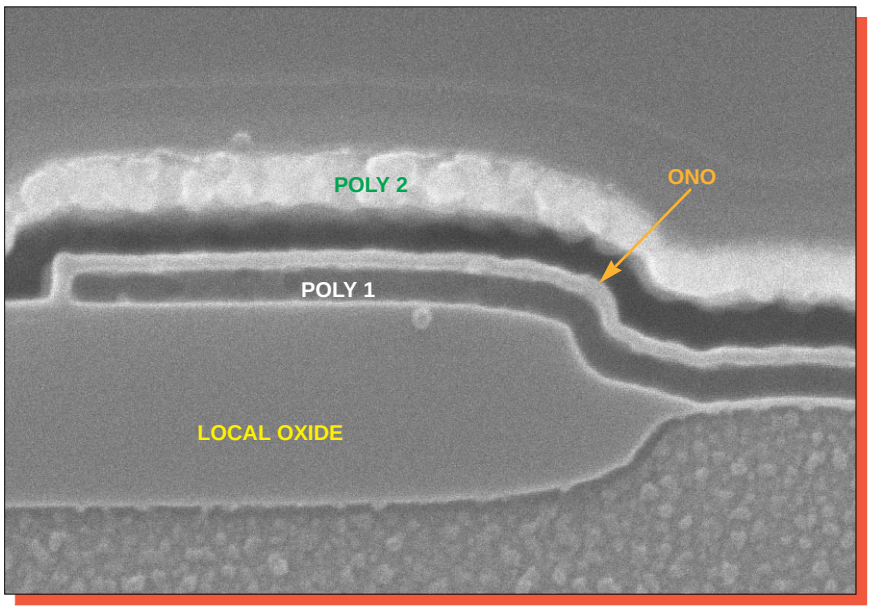
Figure 36. Detail views of EEPROM floating gate structure (perpendicular to word lines).



Mag. 13,000x



Mag. 26,000x



Mag. 52,000x

Figure 37. SEM section views of EEPROM cells (parallel to word line).