Construction Analysis

IBM/Motorola MPC750 RISC Microprocessor

Report Number: SCA 9711-563

INTEGRATED CIRCUIT ENGINEERING

17350 N. Hartford Drive
Scottsdale, AZ 85255
Phone: 602-515-9780
Fax: 602-515-9781
e-mail: ice@ice-corp.com
Internet: http://www.ice-corp.com

INDEX TO TEXT

INTRODUCTION

This report describes a construction analysis of the IBM/Motorola MPC750 RISC Microprocessor. Two engineering samples (275 MHz) were used for the analysis. The devices were received in 361-pin (360 actual) ceramic BGA packages. Although no date code was present on the devices, they are believed to have been fabbed in the second half of 1997.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Six metal, P-epi, CMOS process.
- Very aggressive feature size: 0.17 micron gates (0.15 micron effective?).
- Metal 1 (tungsten) was defined by a damascene process. Stacked vias were employed.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium silicided diffusion structures.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 361-pin (360 actual) ceramic ball grid arrays (BGAs). The die was mounted surface down on the ceramic substrate (C4 flip-chip assembly).

- A blue colored underfill was present between the die surface and the ceramic substrate.

- External package solder balls were employed for package to board connections.

- Solder balls were employed for all connections to die metallization (C4 flip-chip process). Copper-tin bond pads were employed with a chromium barrier.

- Sawn dicing (full depth).

Die Process:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process employing twin-wells in an apparent P-epi on a P substrate.

- Die coat: A thin patterned polyimide die coat was present over the entire die.

- Final passivation: A layer of nitride over a layer of glass.

- Metallization: Six levels of metal defined by dry-etch techniques. Metal 1 (tungsten) was defined by a damascene process. Metals 2 - 6 consisted of aluminum with titanium-nitride caps. Metal 6 employed a titanium barrier which was also probably used under metals 2 - 5, but was too thin to delineate clearly. Tungsten plugs were employed for vias under metals 2 - 6. All tungsten plugs and tungsten metal 1 were lined with titanium-nitride. Stacked vias were employed at all levels.

TECHNOLOGY DESCRIPTION (continued)

- Intermetal dielectrics: Intermetal dielectrics 2 - 5 used the same dielectric structure. Two layers of glass were deposited. The first layer was subjected to an etchback and the second layer was planarized by chemical-mechanical-planarization (CMP). Intermetal dielectric 1 (between M1 and M2) consisted of a single thick layer of glass which had also been subjected to CMP (after M1 deposition).

- Pre-metal glass: A thick layer of glass over a thin nitride. This dielectric was also planarized by CMP (after metal 1 deposition).

- Polysilicon: A single layer of dry-etched polycide (poly and titanium-silicide). This layer was used to form all gates on the die. Oxide sidewall spacers were used to provide the LDD spacing.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Titanium was sintered into the diffusions (salicide process).

- Isolation: Field oxide isolation consisted of oxide-filled shallow-trench isolation. It was very planar with the diffused silicon surfaces.

- Wells: Twin-wells in a P-epi on a P substrate.

- Memory cells: On-chip Level 1 data and instruction Cache memory cell arrays (32KByte each) were employed. On-chip Level 2 Cache was also employed. Both Cache memory cells used a 6T CMOS SRAM cell design although the layout differed. It is not apparent which cells were Level 1 or 2 Cache memory, so they are referred to as Array A and Array B (see Figures 40 - 43). On Array A metal 3 distributed GND and bit lines (via metals 1 - 3). Metal 2 distributed Vcc and formed “piggyback” word lines throughout the cells and was used as cell interconnect. Metal 1 also provided cell interconnect. Poly formed the select and storage gates. On Array B metal 3 formed the bit lines, metal 2 distributed GND and Vcc and formed “piggyback” word line. Metal 1 formed cell interconnect and poly formed the gates. Cell size on Array A was 4 x 6.7 microns and on Array B was 3.3 x 4.8 microns.

- Metal 5 redundancy fuses were present. Metal 5 aluminum fuse links were connected to the tungsten below. No blown fuse links were present. Passivation cutouts were present over the fuse blocks.

ANALYSIS RESULTS I

Assembly: **Figures 1 and 5**

Questionable Items:[1] None.

Special Features: None.

General items:

- The devices were packaged in 361-pin ceramic BGA packages. The die was mounted surface down on the ceramic (flip-chip assembly).

- Overall package quality: Good. No defects were found on the external portions of the packages. External solder balls were well formed and placed.

- Die connections: Solder balls were used for connections to the die (C4 process). A separate metal layer (copper-tin over a chromium barrier) formed the bond pads. Pads were connected to the metal 6 through cutouts in the passivation and die coat. Ball placement was good. Pad size was 4.5 mils (round) and ball pad pitch was 9.9 mils. A blue colored underfill was present between the die and the ceramic substrate. No voids were noted in this material.

- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process and Design: **Figures 2 - 43**

Questionable Items:[1]

- Misalignment of metal 3 to the underlying tungsten plugs (Figures 23 - 24).

Special Features:

- Six metal, P-epi, CMOS process.
- Aggressive gate sizes (0.17 micron).
- Metal 1 (tungsten) was defined by a damascene process. Stacked vias were employed.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium silicided diffusion structures.

General Items:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process employing twin-wells in an apparent P-epi on a P substrate. No problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels (except metal 3 to underlying plugs).
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Die coat: A patterned polyimide die coat was present over the entire die surface.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Final passivation: A layer of nitride over a layer of glass. Coverage was good. Edge seal was also good as the passivation extended to the scribe lane to seal the metallization.

- Metallization: Six levels of metal interconnect. Metals 2 - 6 consisted of aluminum with titanium-nitride caps. Metal 6 employed a titanium barrier which was also probably used under metals 2 - 5, but was too thin to delineate clearly. Tungsten plugs were employed with metals 2 - 6. All plugs were lined with titanium-nitride underneath. Metal 1 was used as a local interconnect and consisted of tungsten defined by a damascene process. The metal 1 tungsten was also lined with titanium-nitride.

- Metal patterning: All aluminum metal levels were defined by a dry etch of good quality. Metal 6 profiles were somewhat unusual (see Figure 10). Some metal lines were widened slightly at via connections.

- Metal defects: None. No voiding, notching or cracking of the metal layers was found. No silicon nodules were found following removal of the metal layers.

- Metal step coverage: No metal thinning was present at the connections to the tungsten via plugs or metal 1. The absence of thinning is due to the good control of plug height and the planarization technique employed.

- Vias and contacts: All via and contact cuts were defined by a dry etch of good quality. Again, alignment of the metals and plugs was good (except metal 3). Metal 3 was misaligned to the metal 3 plugs below (see Figures 23 and 24). This misalignment decreased contact area by approximately 50 percent and decreased adjacent metal-to-tungsten plug spacing. This does not appear to be a serious concern. Vias and contacts were placed directly over one another (stacked vias). No problems were noted.

ANALYSIS RESULTS II (continued)

- Intermetal dielectrics: Intermetal dielectrics 2 - 5 consisted of the same type of oxide structure. Two layers of glass were deposited, the first layer was subjected to a sputter etchback and the second layer of glass was subjected to CMP which left the surface very planar. Intermetal dielectric 1 consisted of a single thick layer of glass which had also been subjected to CMP. No problems were found with any of these layers.

- Pre-metal glass: A thick layer of silicon-dioxide over a thin nitride. This layer was also planarized by chemical-mechanical-planarization. No problems were found.

- Polysilicon: A single level of polycide (poly and titanium-silicide) was used. It formed all gates and word lines in the array. Definition was by dry etch of good quality. Oxide sidewall spacers were used throughout and left in place. No problems were found.

- Isolation: The device used oxide-filled shallow-trench isolation which was quite planar with the silicon surface. No problems were present.

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Titanium was sintered into the diffusions (salicide process) to reduce series resistance. An LDD process was used employing sidewall spacers.

- Wells: Twin-wells were used in what we believe to be a P-epi on a P substrate. Definition was normal, although we could not delineate the P-well.

- Buried contacts: Direct poly to diffusion contacts were not used.

- Memory cells: On-chip Level 1 data and instruction Cache memory cell arrays (32KByte each) were employed. On-chip Level 2 Cache was also employed. Both Cache memory cells used 6T CMOS SRAM cell design although the layout differed. It is not apparent which cells were Level 1 or 2 Cache memory, so they are referred to as Array A and Array B (see Figures 40 - 43). On Array A metal 3 distributed GND and bit lines (via metals 1 - 3). Metal 2 distributed Vcc and formed "piggyback" word lines throughout the cells and was used as cell interconnect. Metal 1 also provided cell interconnect. Poly formed the select and storage gates. On Array B metal 3 formed the bit lines, metal 2 distributed GND and Vcc and formed "piggyback" word lines. Metal 1 formed cell interconnect and poly formed the gates. Cell size on Array A was 4 x 6.7 microns and on Array B was 3.3 x 4.8 microns.

ANALYSIS RESULTS II (continued)

- Metal 5 redundancy fuses were present. Metal 5 aluminum formed the fuse links and were connected to tungsten plugs below. No blown fuse links were present. Passivation cutouts were present over the fuse blocks. No problems were seen.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Die optical inspection

Delayer to metal 6 and inspect

Aluminum removal (metal 6) and inspect plugs

Delayer to metal 5 and inspect

Aluminum removal (metal 5) and inspect tungsten plugs

Delayer to metal 4 and inspect

Aluminum removal (metal 4) and inspect tungsten plugs

Delayer to metal 3 and inspect

Aluminum removal (metal 3) and inspect tungsten plugs

Delayer to metal 2 and inspect

Aluminum removal (metal 2) and inspect tungsten plugs

Delayer to metal 1 and inspect

Tungsten removal (metal 1)

Delayer to polycide/substrate and inspect

Die sectioning (90° for SEM)

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

OVERALL QUALITY EVALUATION: Overall Rating: Normal to Good.

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Solder ball placement	G
Solder ball interconnect quality	G
Dicing quality	G
Die attach quality	G
Die attach method	C4 solder ball interconnect technique
Dicing method	Sawn
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	G
Metal registration	N*
Contact coverage	N*
Via/contact registration	N
Etch control (depth)	N

**Misalignment of metal 3 to underlying plugs.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP (lid)

IBM R25000PAP
Arthur 88H5811
A1M010
275 (handmarked)

DIE MATERIAL ANALYSIS

Final passivation:	Single layer of nitride over a glass layer.
Metallization 2 - 6:	Aluminum with titanium-nitride caps and apparent thin titanium adhesion layers.
Intermetal dielectrics 2 - 5:	A layer of glass followed by another layer of glass which was planarized by CMP.
Intermetal dielectric 1:	Thick layer of glass (CMP planarization).
Metallization 1:	Tungsten (damascene process) with titanium-nitride liner.
Vias (M2 - M5):	Tungsten (lined with titanium-nitride).
Pre-metal glass:	Thick layer of silicon-dioxide over a thin nitride.
Polycide:	Titanium-silicide on polysilicon.
Salicide on diffusions:	Titanium-silicide.

HORIZONTAL DIMENSIONS

Die size:	7.8 x 9 mm (308 x 356 mils)
Die area:	70.7 mm^2 (109,648 $mils^2$)
Min pad size:	0.11 mm (4.5 mils round)
Min pad space:	0.14 mm (5.6 mils)
Min metal 6 width:	2 microns (bottom portion of the line)
Min metal 6 space:	1.7 micron
Min metal 6 pitch:	3.8 microns
Min metal 5 width:	0.5 micron (bottom portion of the line)
Min metal 5 space:	0.6 micron
Min metal 5 pitch:	1.2 micron
Min metal 4 width:	0.55 micron
Min metal 4 space:	0.65 micron
Min metal 4 pitch:	1.2 micron
Min metal 3 width:	0.55 micron
Min metal 3 space:	0.5 micron
Min metal 3 pitch:	1.95 micron
Min metal 2 width:	0.45 micron
Min metal 2 space:	0.45 micron
Min metal 2 pitch:	1.0 micron
Min metal 1 width:	0.45 micron
Min metal 1 space:	0.4 micron
Min via (M6-to-M5):	1.2 micron
Min via (M5-to-M4):	0.7 micron
Min via (M4-to-M3):	0.65 micron
Min via (M3-to-M2):	0.7 micron
Min via (M2-to-M1):	0.5 micron
Min contact:	0.45 micron
Min polycide width:	0.17 micron
Min polycide space:	0.45 micron
Min gate length* - (N-channel):	0.17 micron
- (P-channel):	0.17 micron
SRAM cell size (array A):	27 $microns^2$
SRAM cell pitch (array A):	4 x 6.7 microns
SRAM cell size (array B):	16 $microns^2$
SRAM cell pitch (array B):	3.3 x 4.8 microns

**Physical gate length.*

VERTICAL DIMENSIONS

Layers:

Passivation 2:	0.4 micron
Passivation 1:	0.4 micron
Metal 6 - cap:	0.04 micron
- aluminum:	1.9 micron
- barrier:	0.1 micron
- plugs:	1.2 micron
Intermetal dielectric 5 - glass 2:	0.4 - 1 micron
- glass 1:	0.3 - 1 micron
Metal 5 - cap:	0.04 micron
- aluminum:	0.8 micron
- plugs:	1.2 micron
Intermetal dielectric 4 - glass 2:	0.15 - 0.95 micron
- glass 1:	0.5 - 1 micron
Metal 4 - cap:	0.06 micron
- aluminum:	0.8 micron
- plugs:	1.1 micron
Intermetal dielectric 3 - glass 2:	0.25 - 1 micron
- glass 1:	0.45 - 1 micron
Metal 3 - cap:	0.05 micron
- aluminum:	0.8 micron
- plugs:	1.2 micron
Interlevel dielectric 2 - glass 2:	0.5 - 1.2 micron
- glass 1:	0.4 - 0.7 micron
Metal 2 - cap:	0.05 micron
- aluminum:	0.6 micron
- plugs:	0.8 micron
Intermetal dielectric 1:	0.7 micron
Metal 1:	0.4 - 0.6 micron
Nitride layer:	0.06 micron
Pre-metal glass:	0.55 micron
Polycide - silicide:	0.03 micron
- poly:	0.1 micron
Gate oxide:	40Å (approximate)
Trench oxide:	0.4 micron
N+ S/D:	0.15 micron
P+ S/D:	0.13 micron
N-well:	0.8 micron (approximate)
P-epi:	1.7 micron

INDEX TO FIGURES

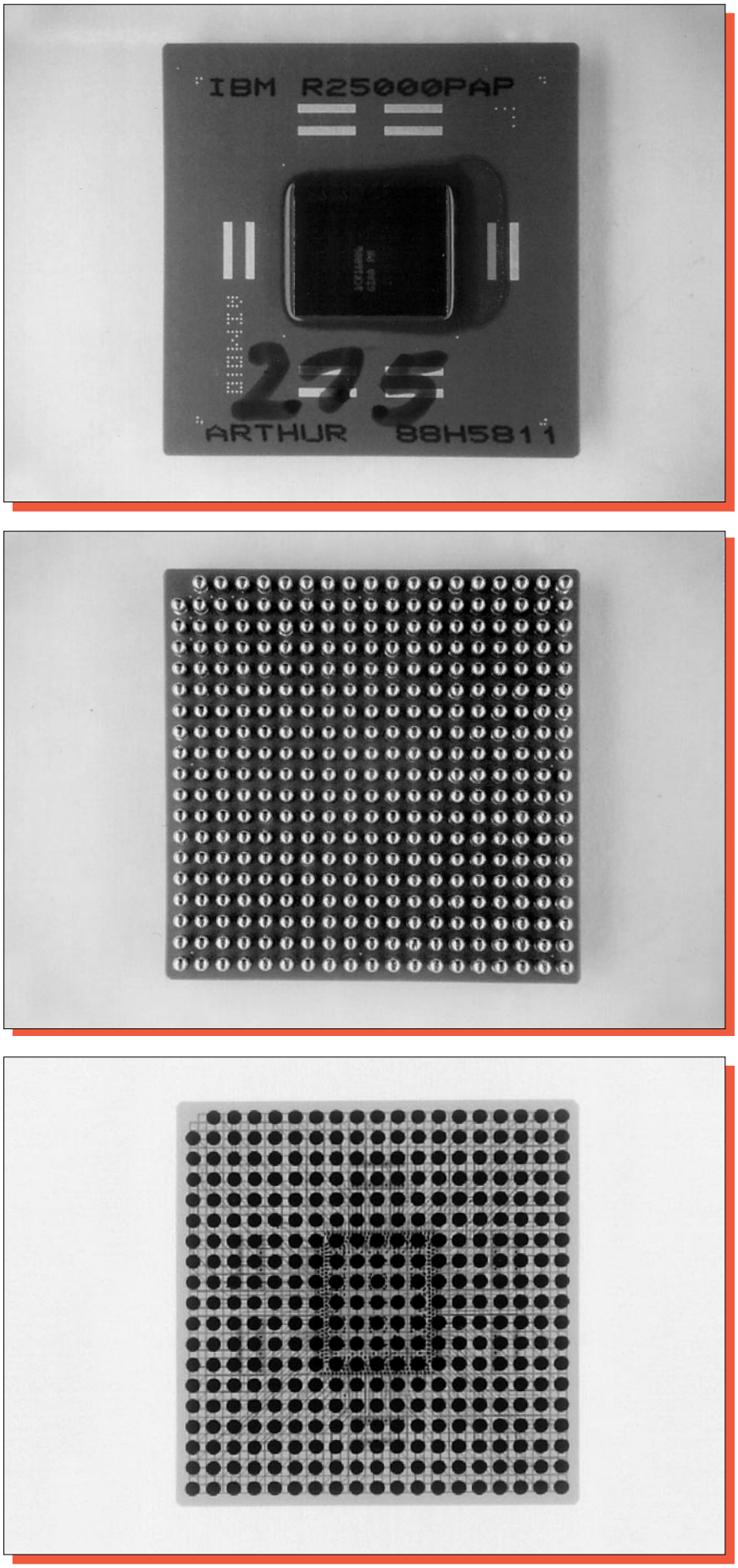


Figure 1. Package photographs and x-ray of the IBM/Motorola 750 RISC. Mag. 2.5x.

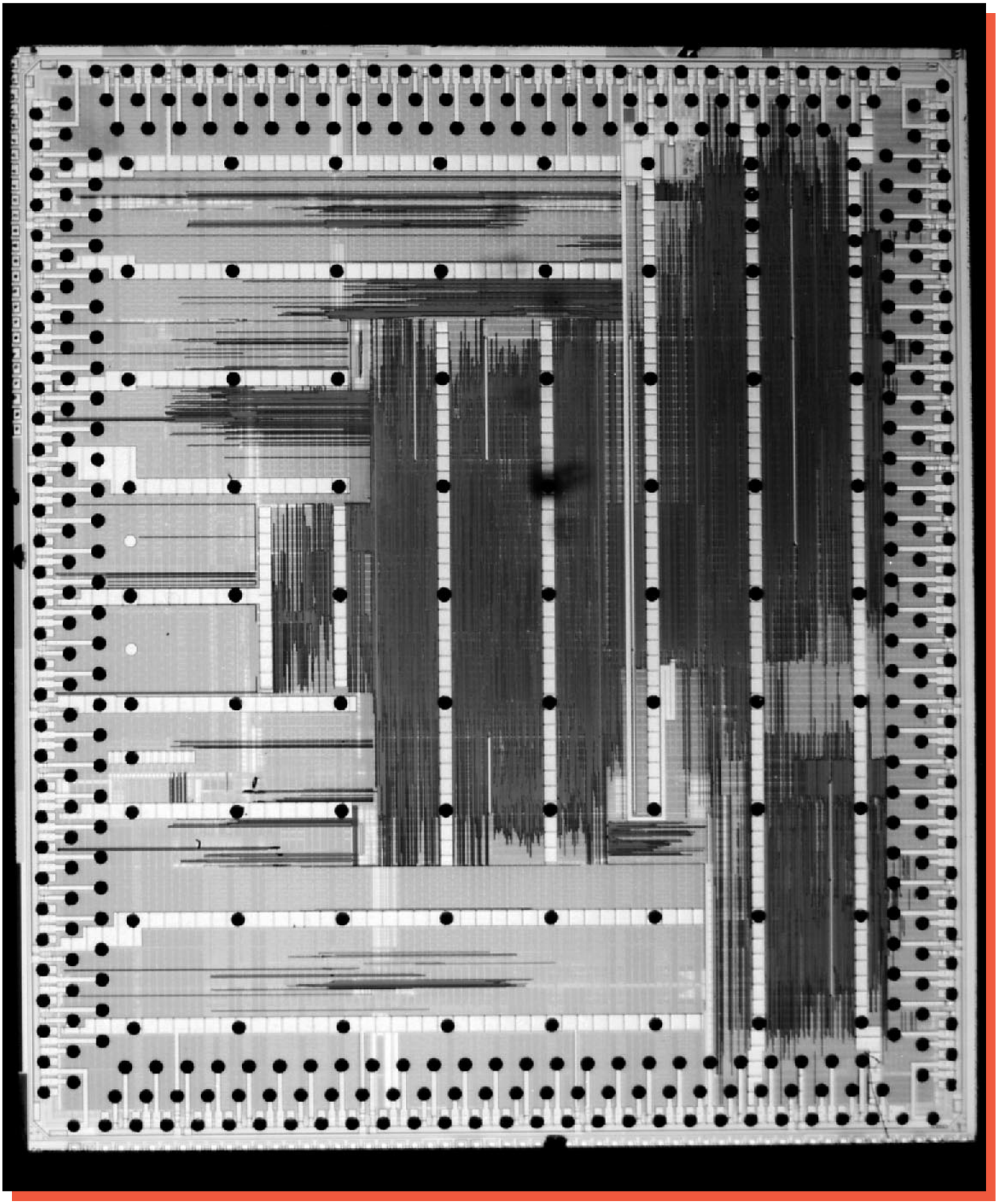
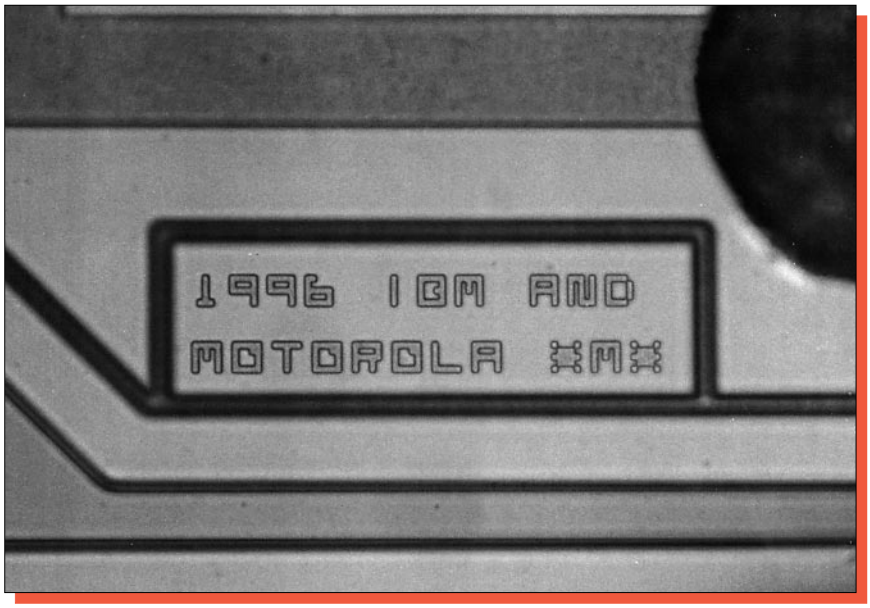
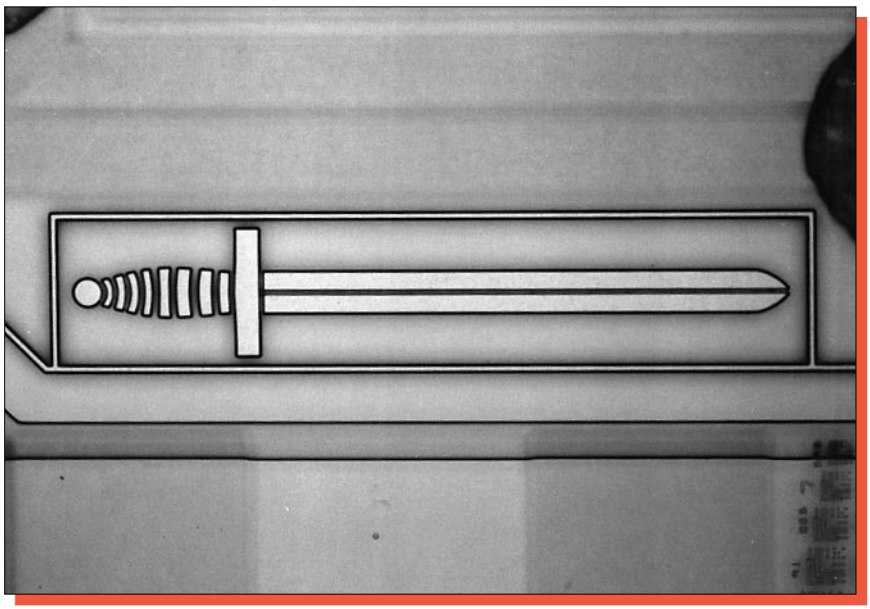


Figure 2. Whole die photograph of the IBM/Motorola 750 RISC microprocessor. Mag. 23x.



Mag. 500x

Mag. 500x



Mag. 320x

Figure 3. Optical views of die markings.

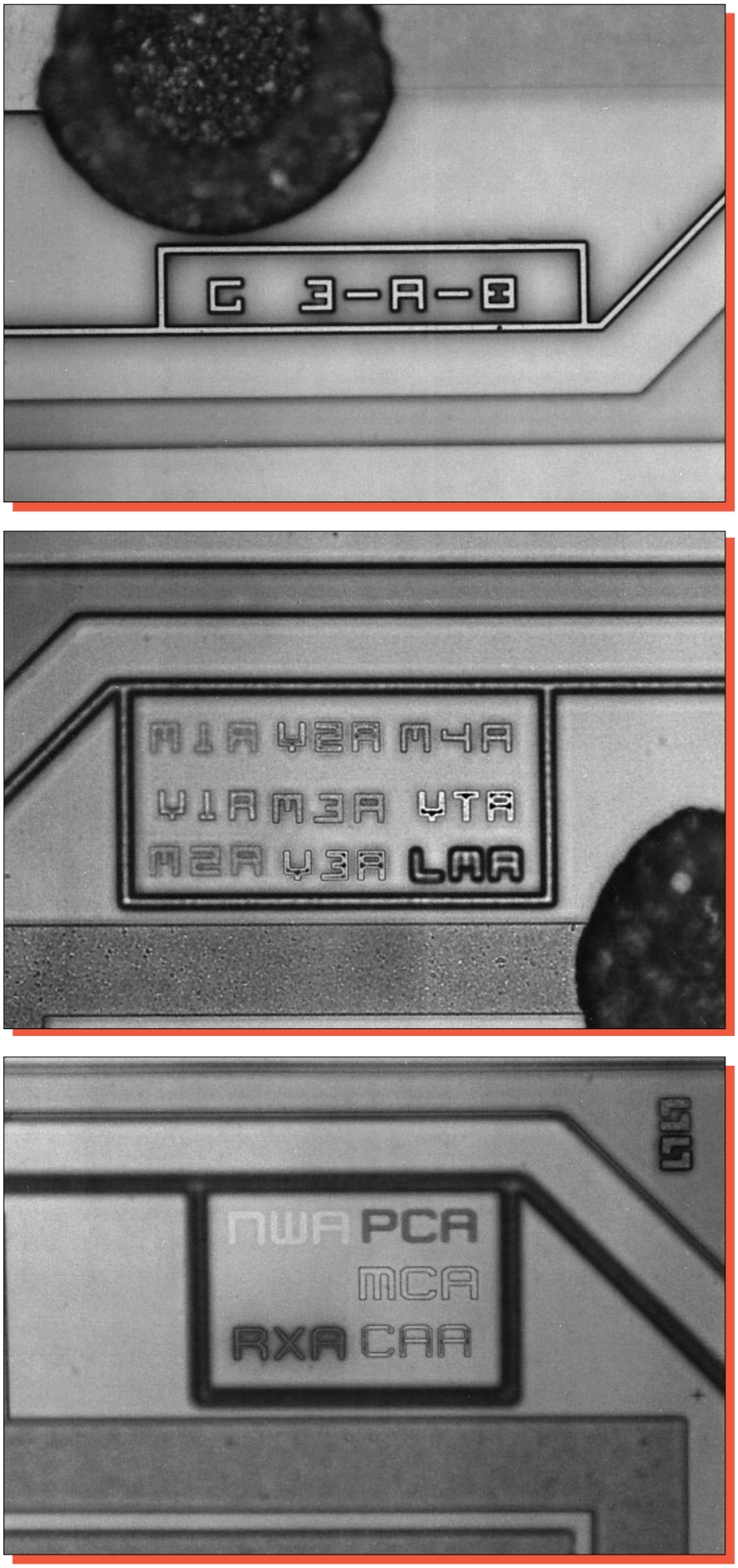


Figure 3a. Additional die and mask markings. Mag. 500x.

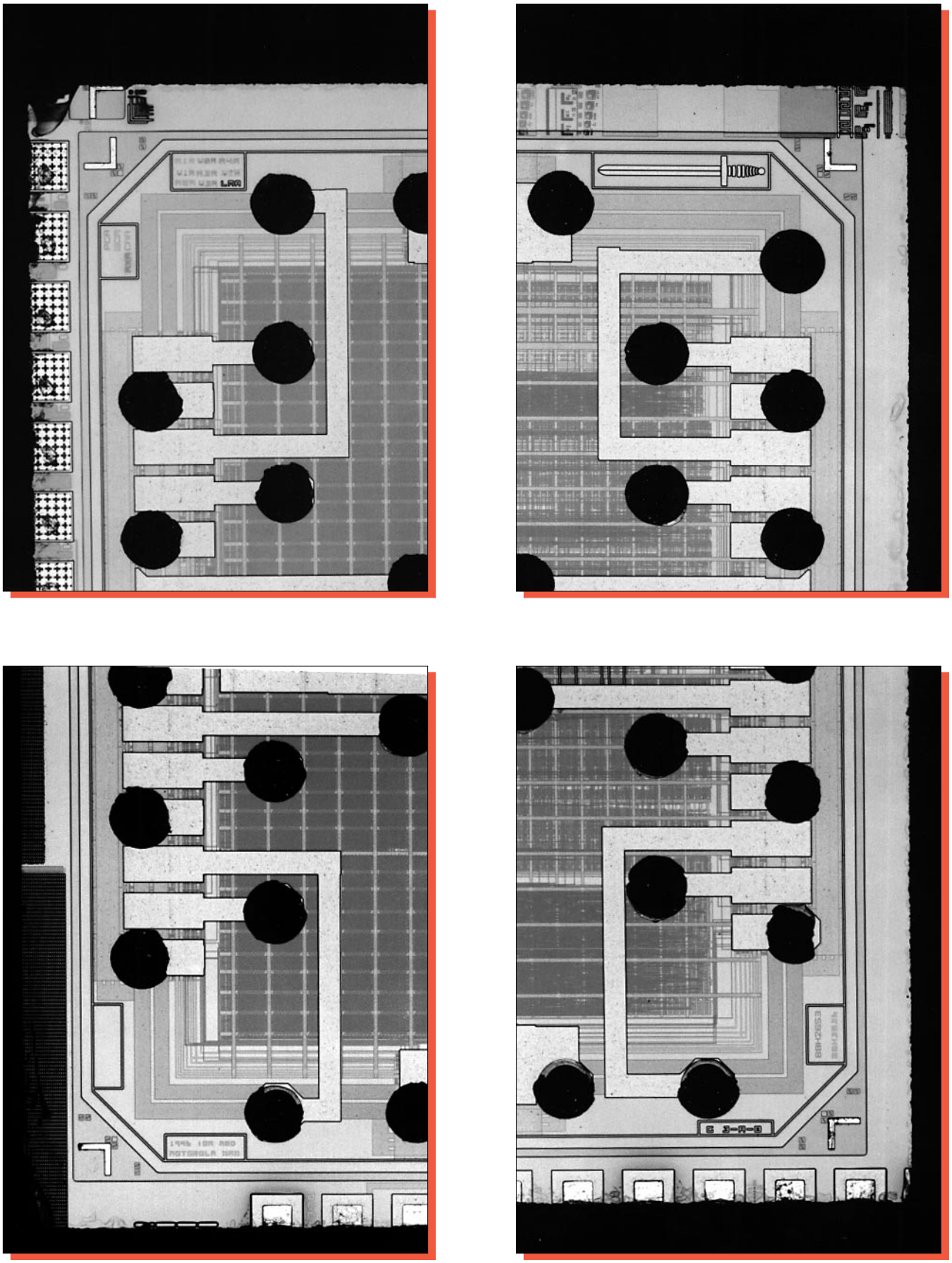
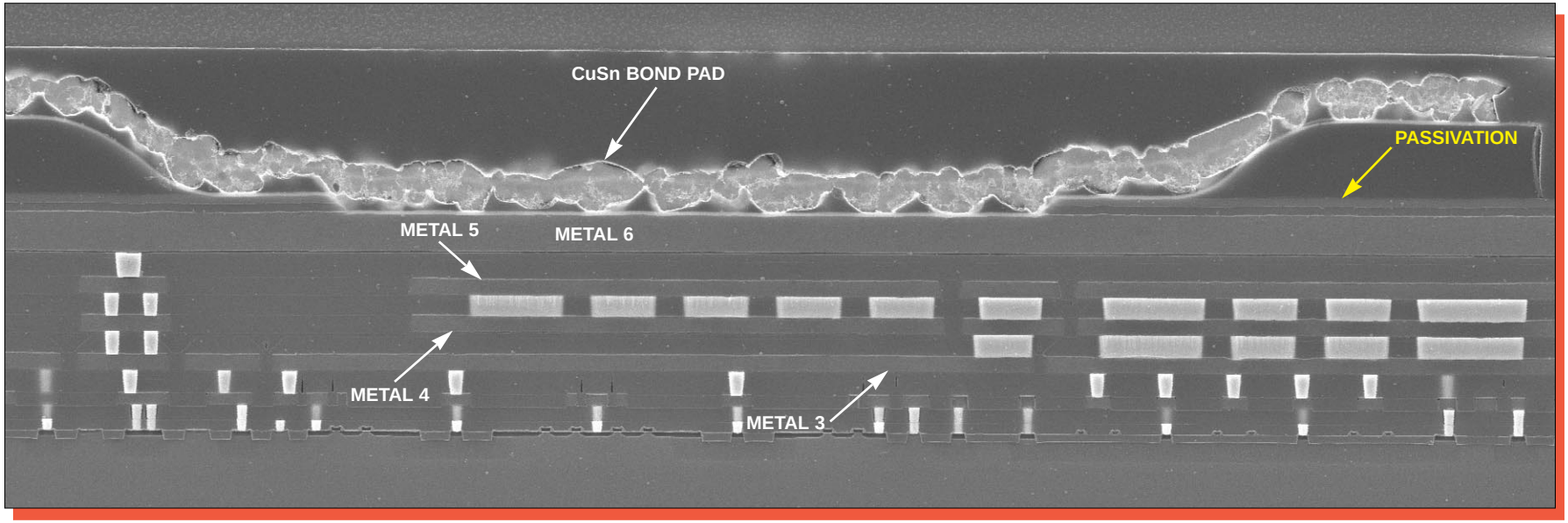
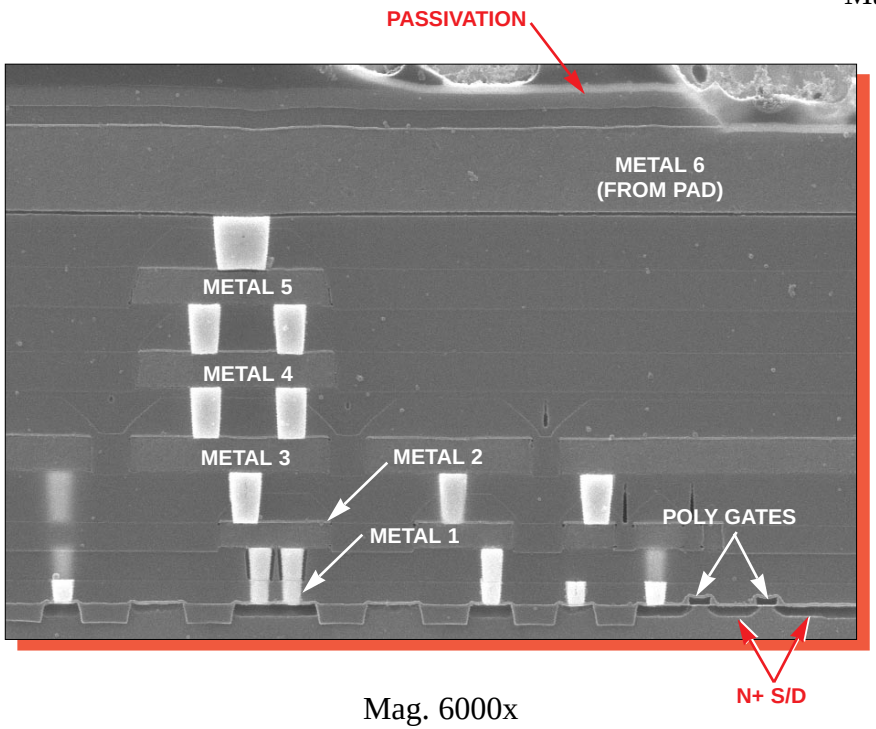


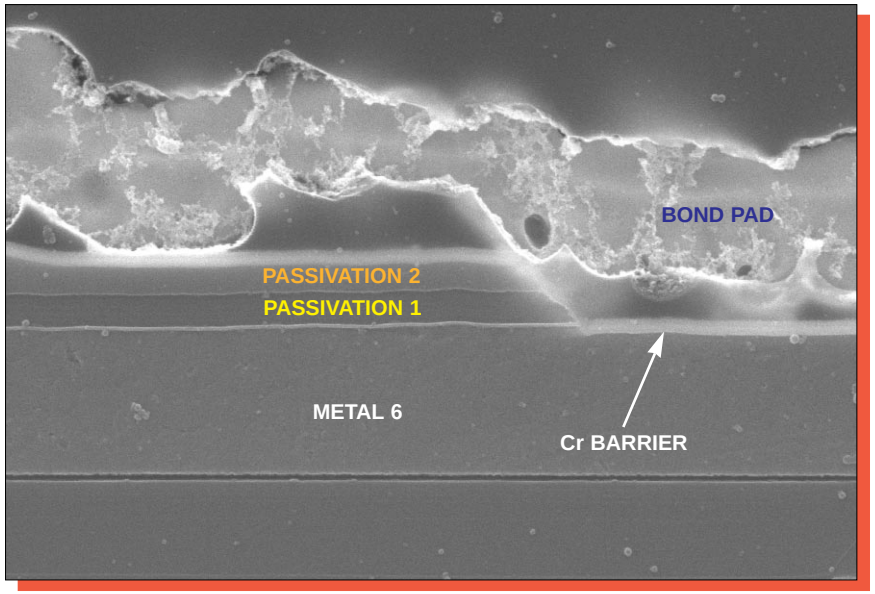
Figure 4. Optical views of die corners. Mag. 100x.



Mag. 3000x

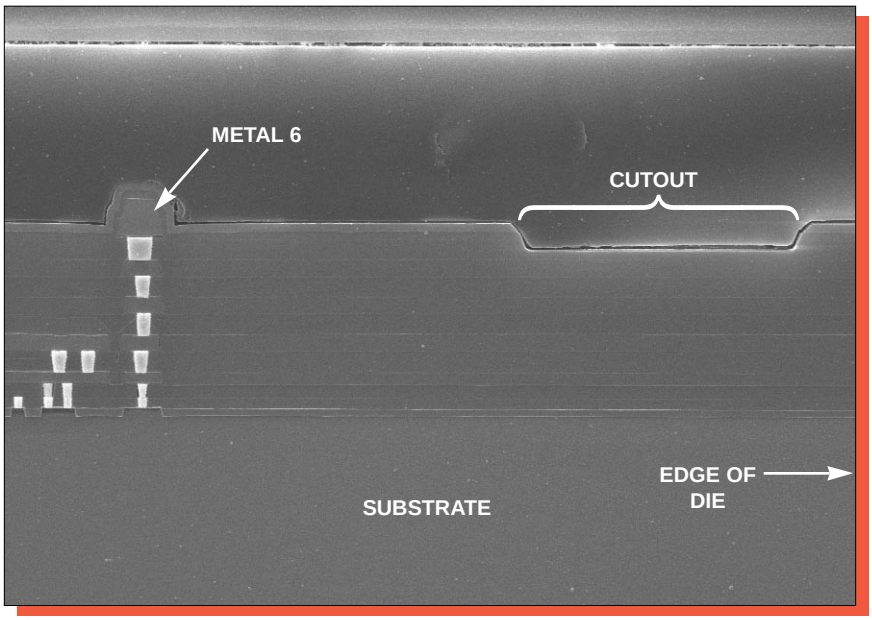


Mag. 6000x

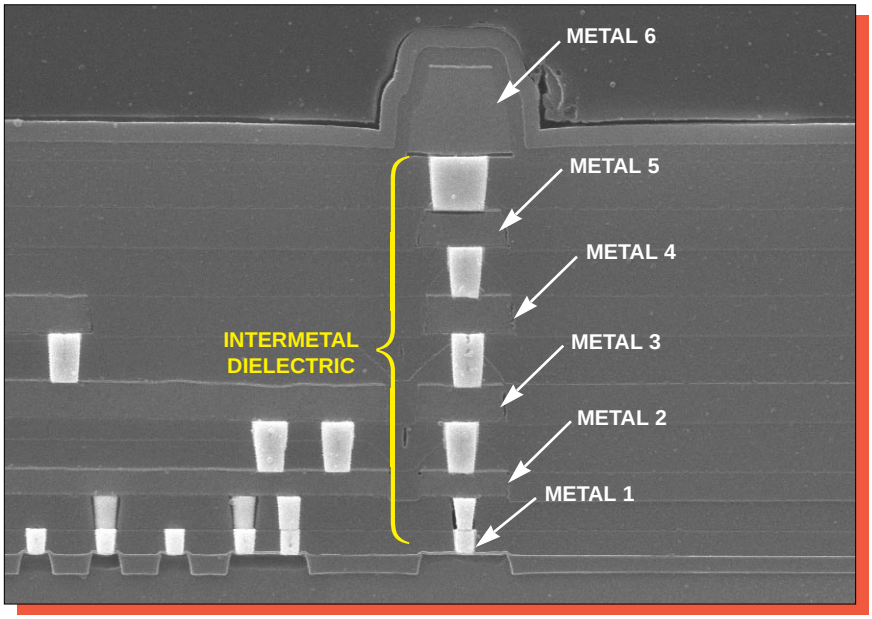


Mag. 10,000x

Figure 5. SEM section views of the bond pad structure.

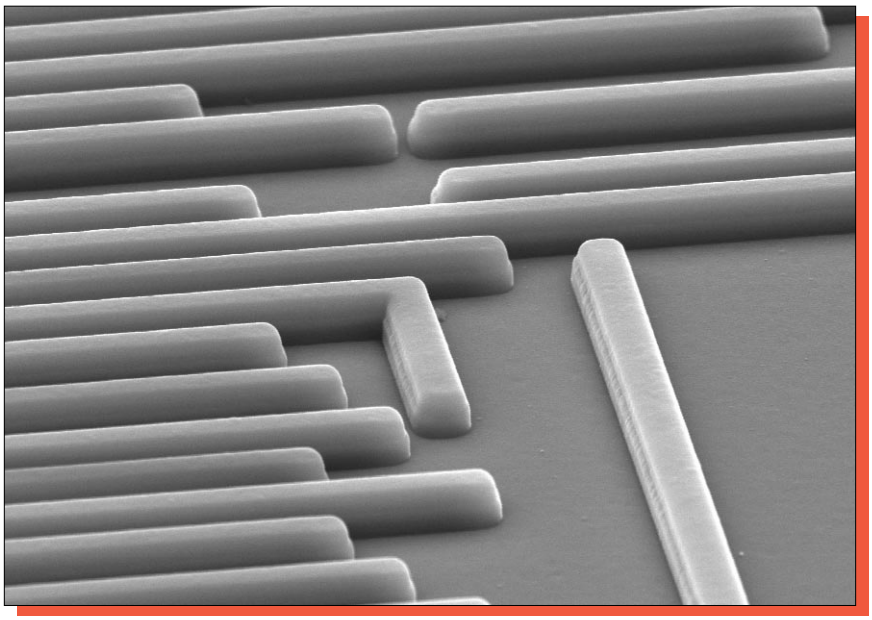


Mag. 2500x

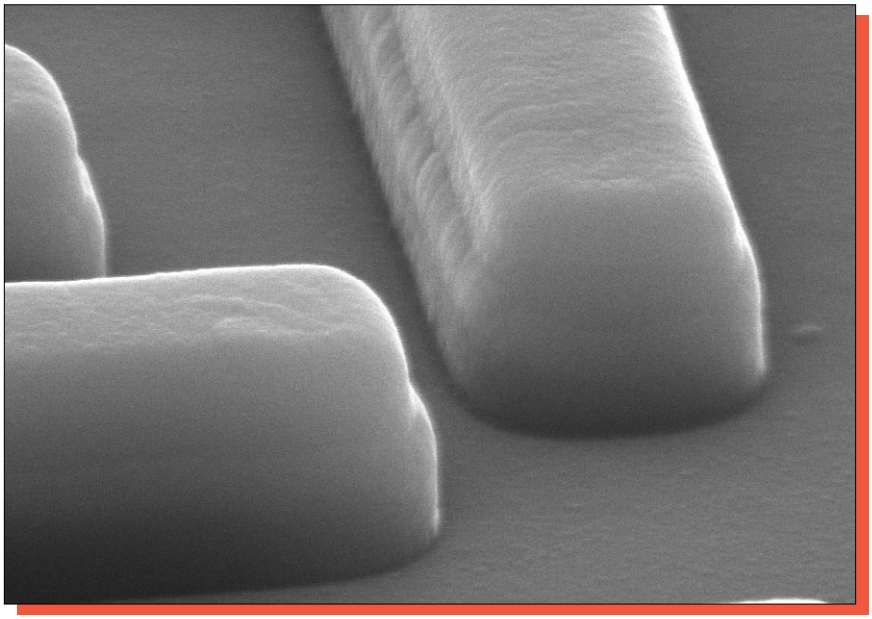


Mag. 6000x

Figure 6. SEM section views of the edge seal structure.



Mag. 2500x



Mag. 13,000x

Figure 7. SEM views of general passivation coverage. 60°.

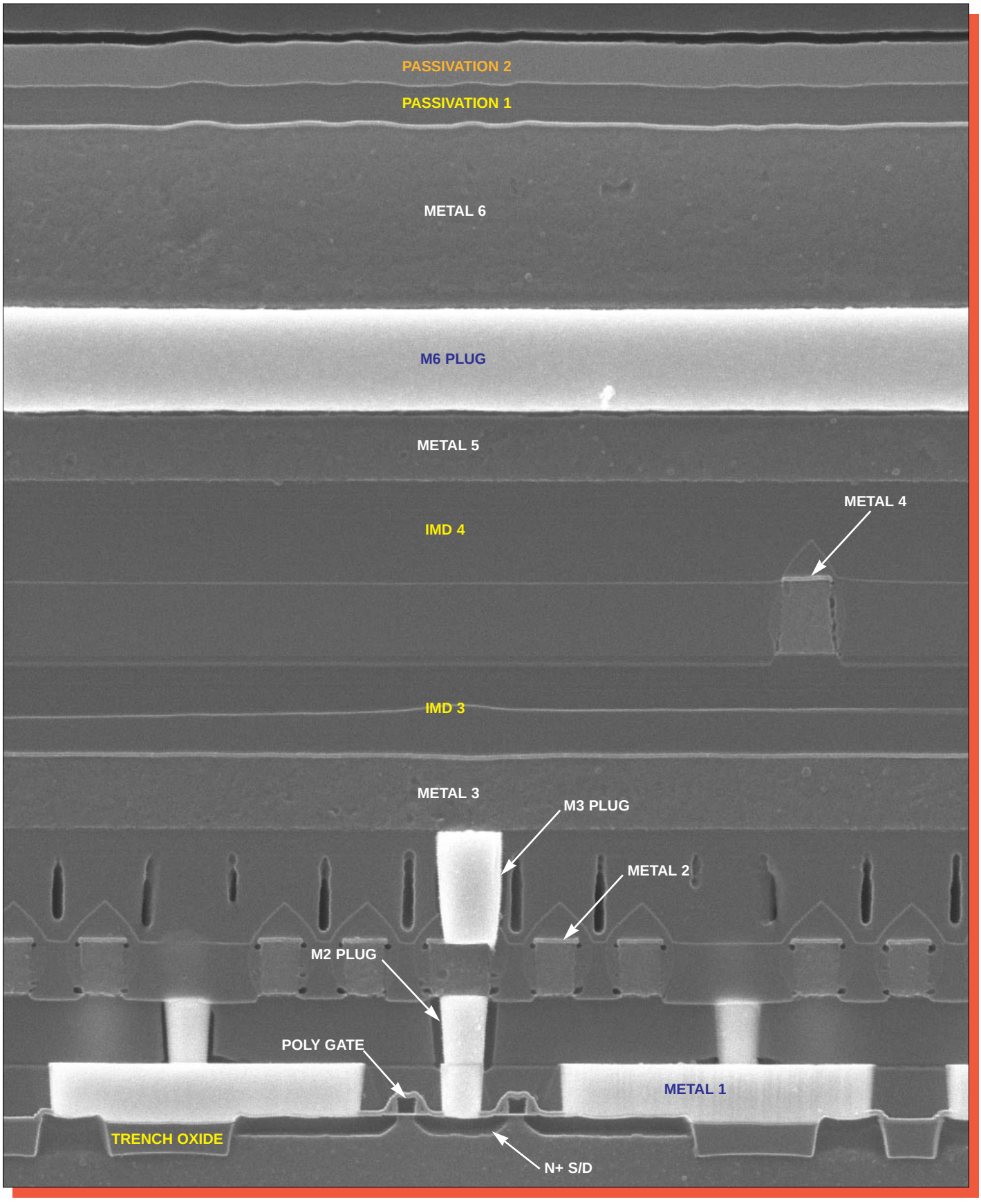
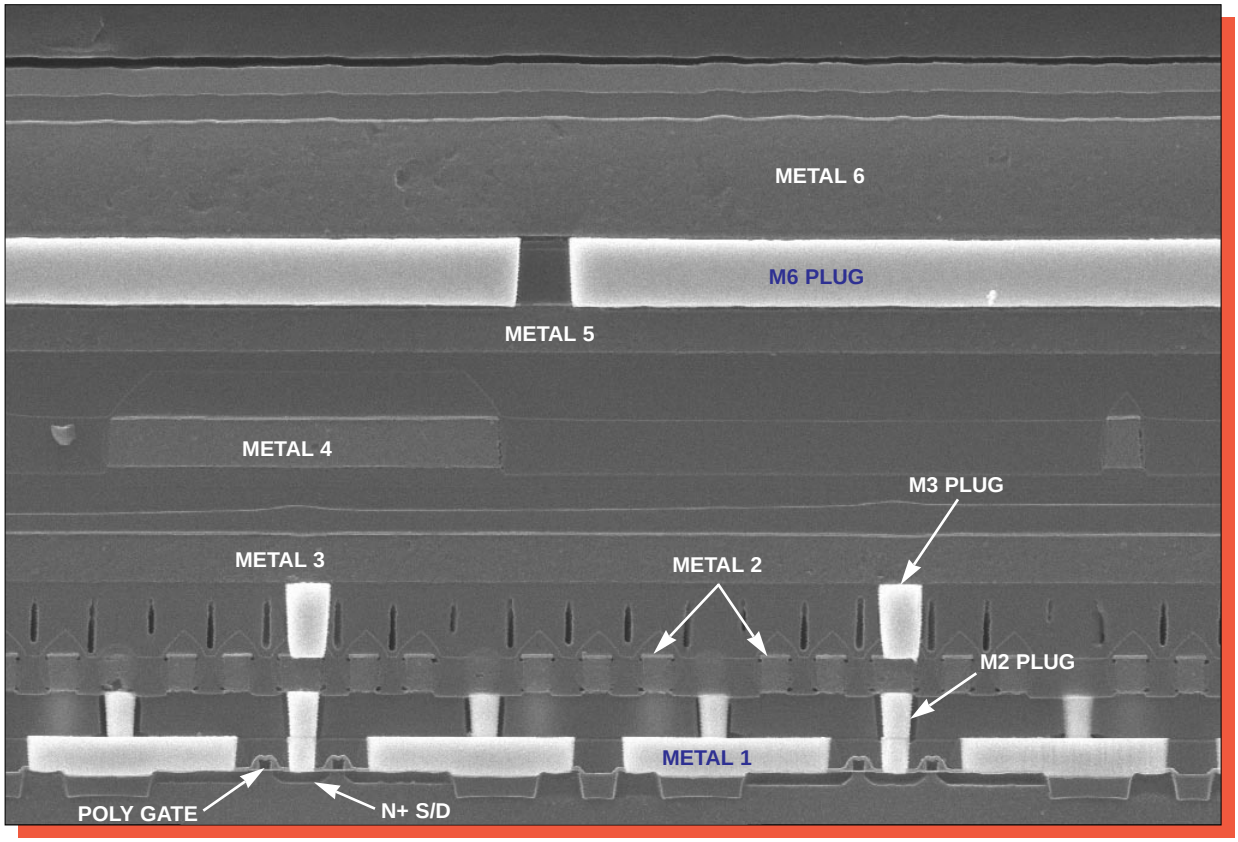
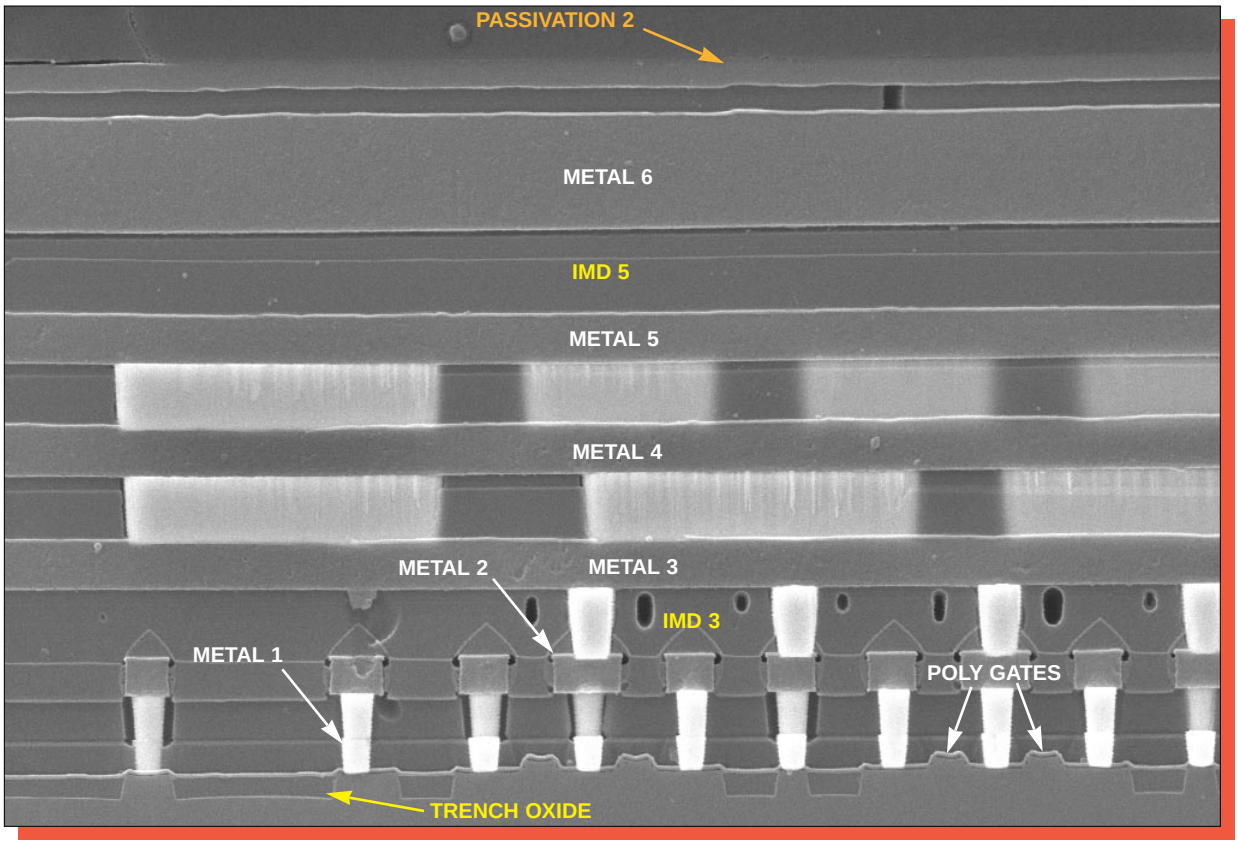


Figure 8. SEM section view illustrating general device structure. Mag. 17,400x.

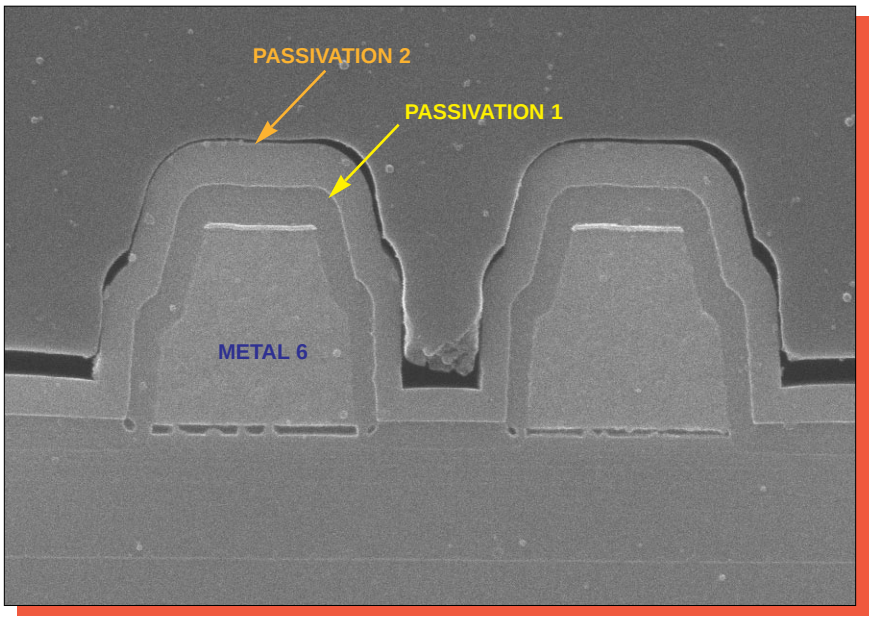


Mag. 7500x

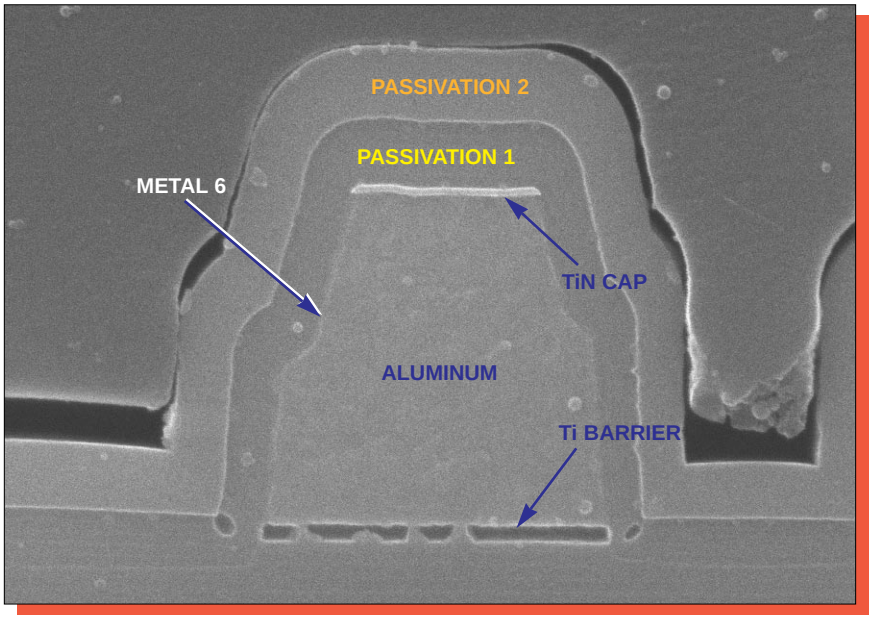


glass-etch, Mag. 8000x

Figure 9. Additional SEM section views illustrating general structure.

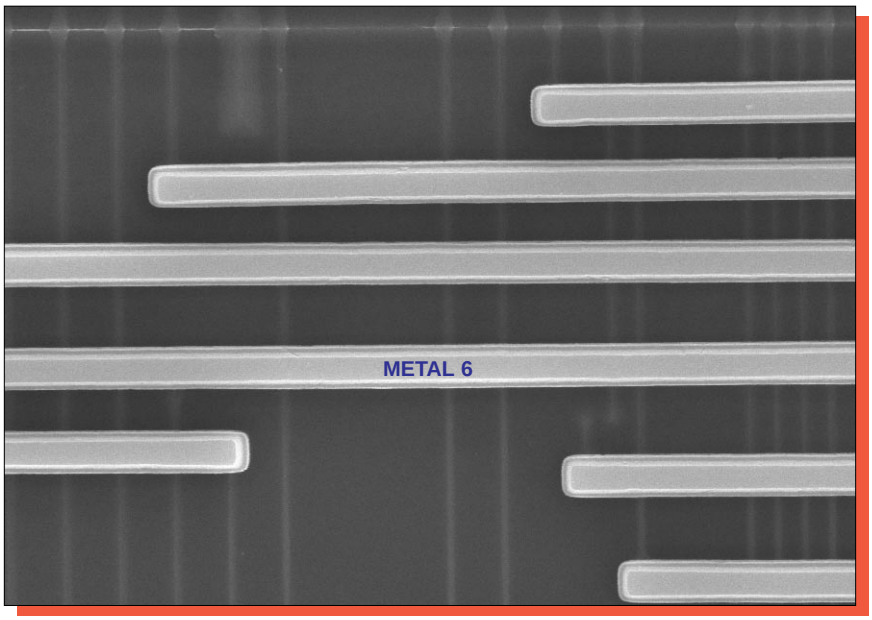


Mag. 13,000x

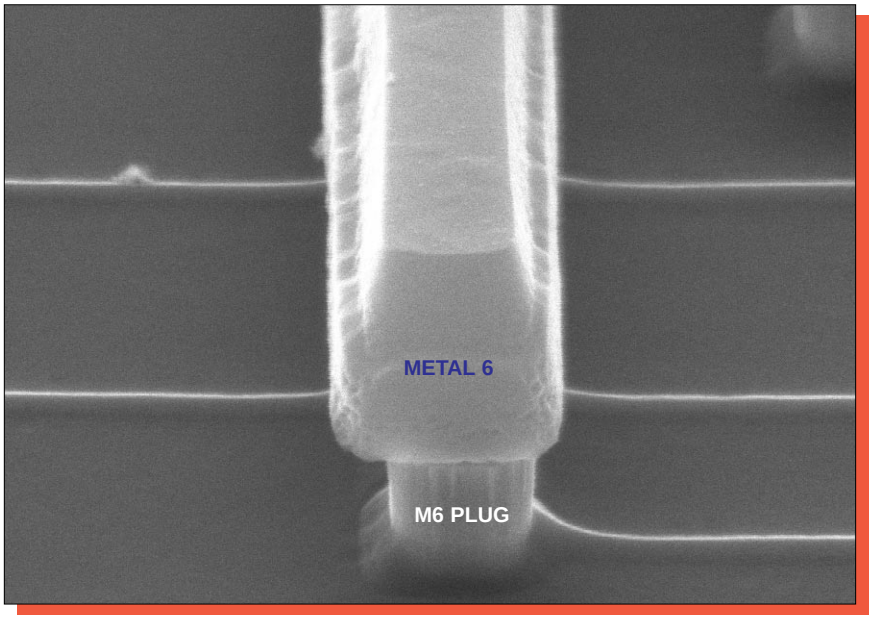


Mag. 23,000x

Figure 10. SEM section views of metal 6 line profiles.

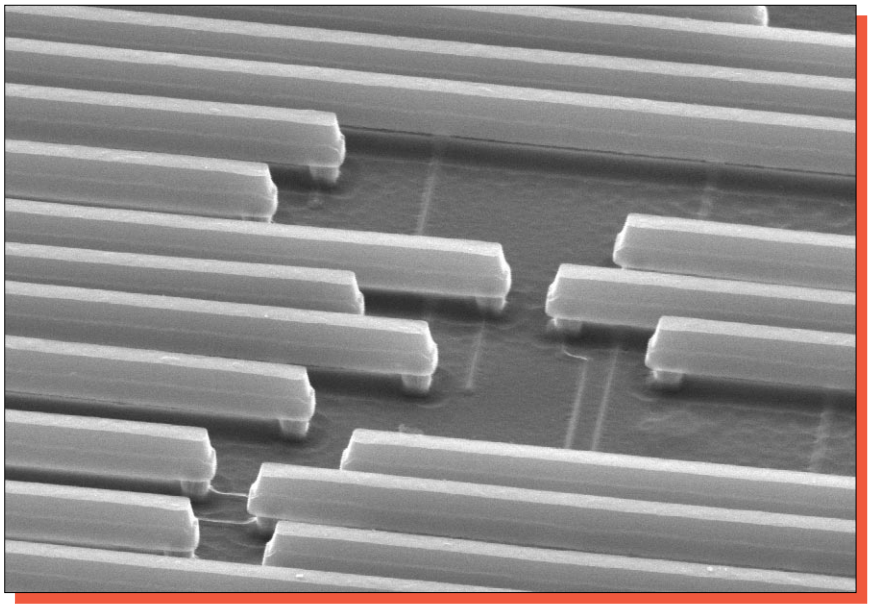


Mag. 2800x, 0°

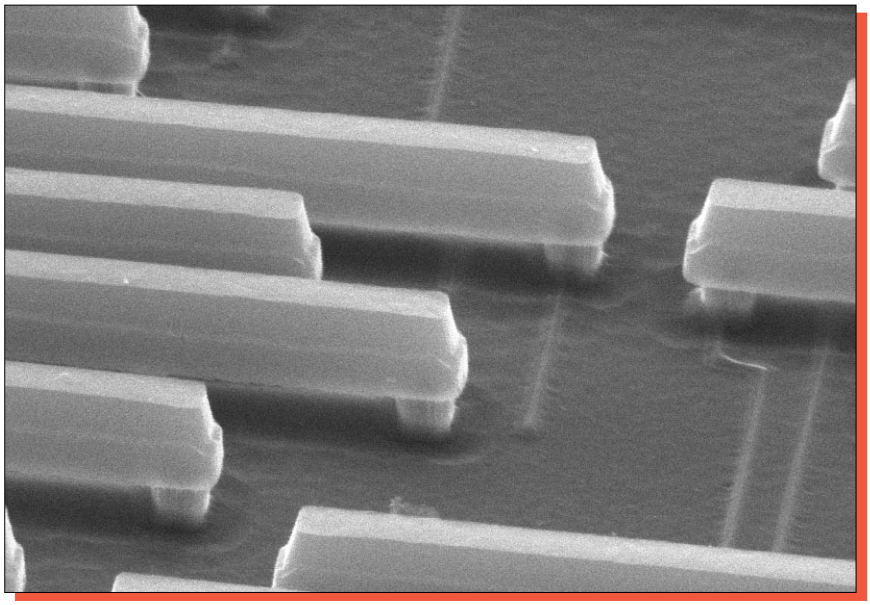


Mag. 15,000x, 60°

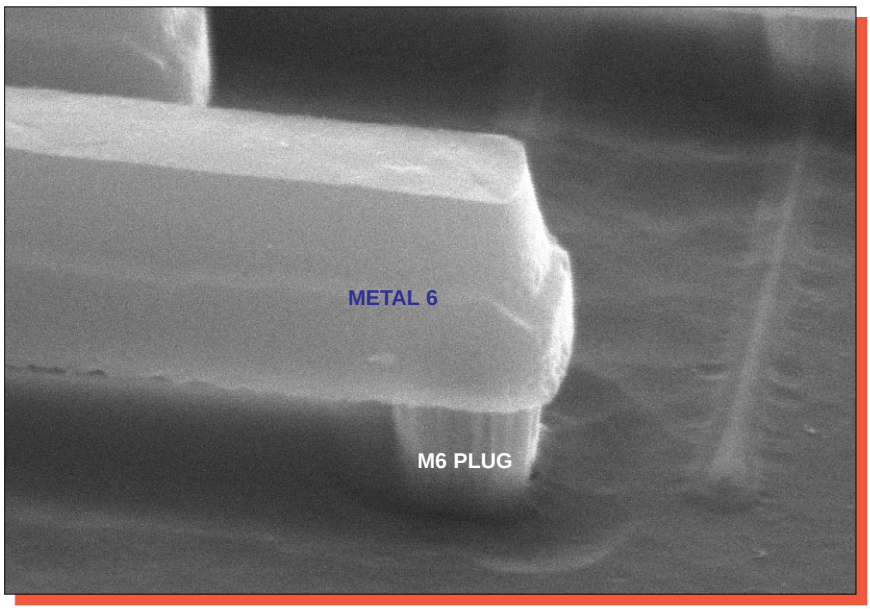
Figure 11. SEM views illustrating metal 6 patterning.



Mag. 3000x

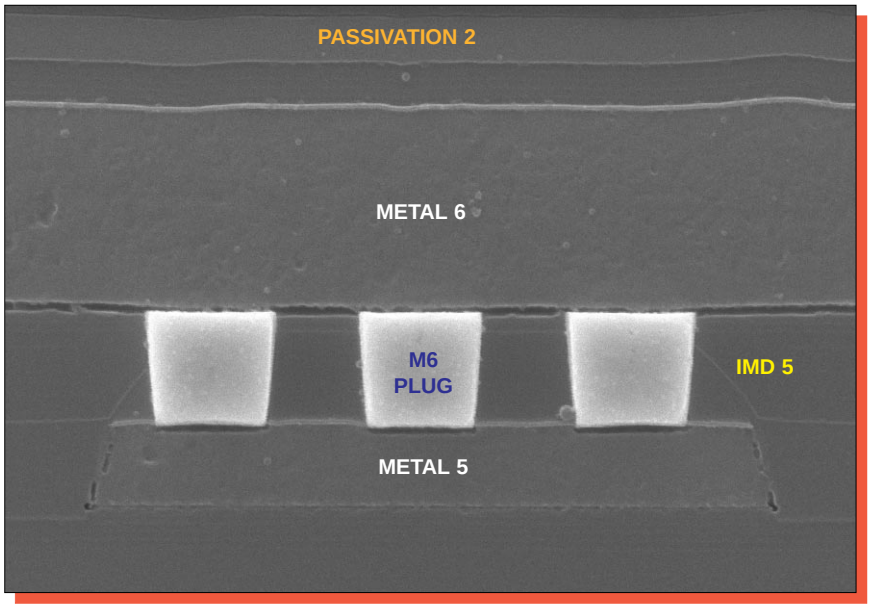


Mag. 6000x

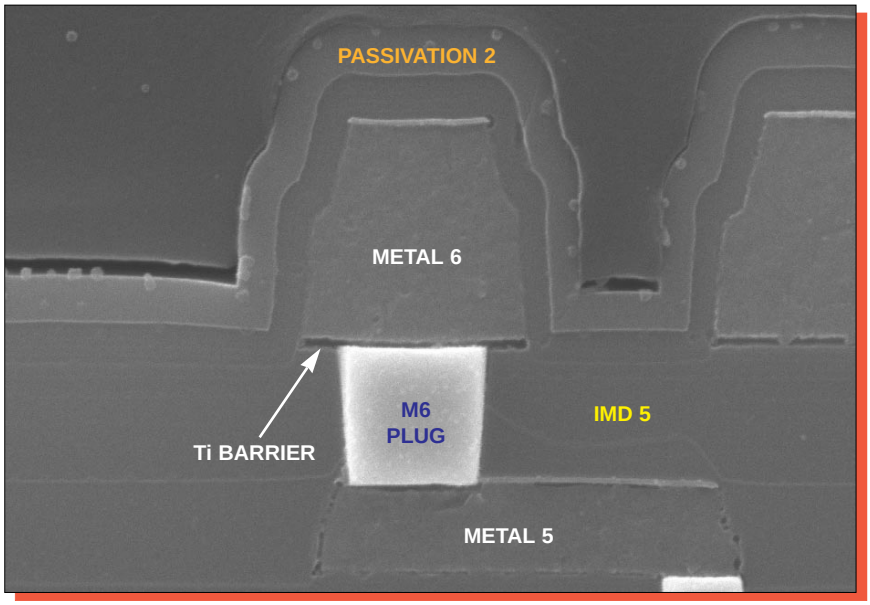


Mag. 15,000x

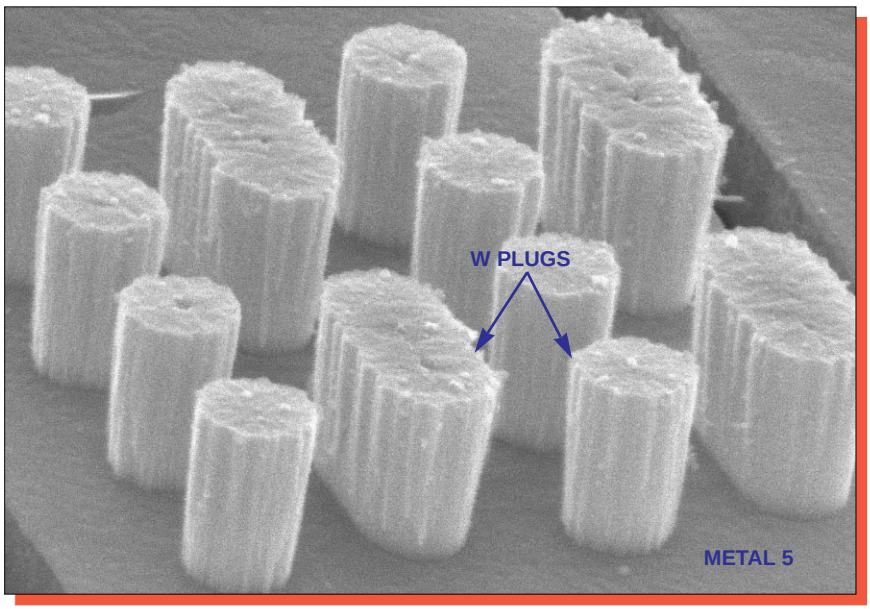
Figure 12. SEM views illustrating general metal 6 integrity. 60°.



Mag. 13,000x

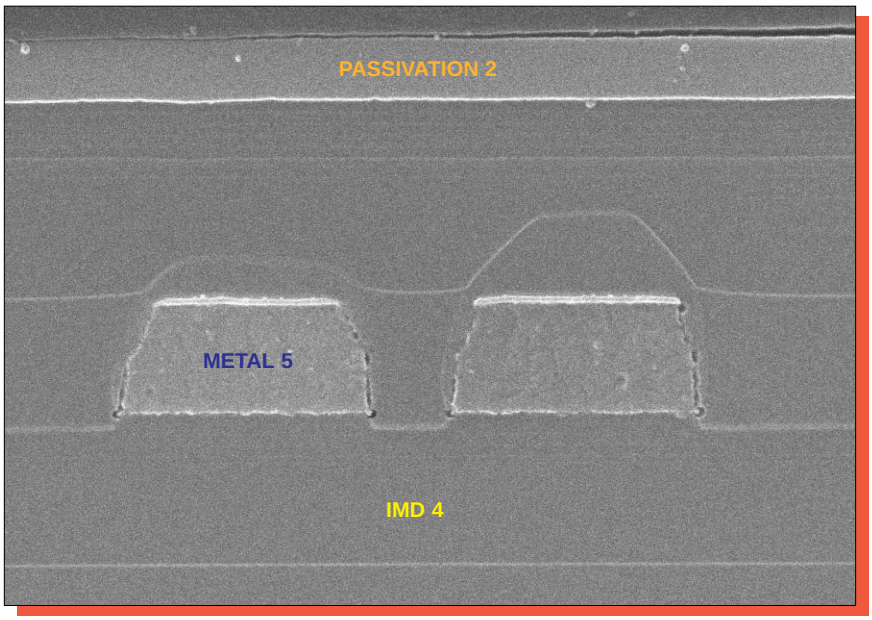


Mag. 15,000x

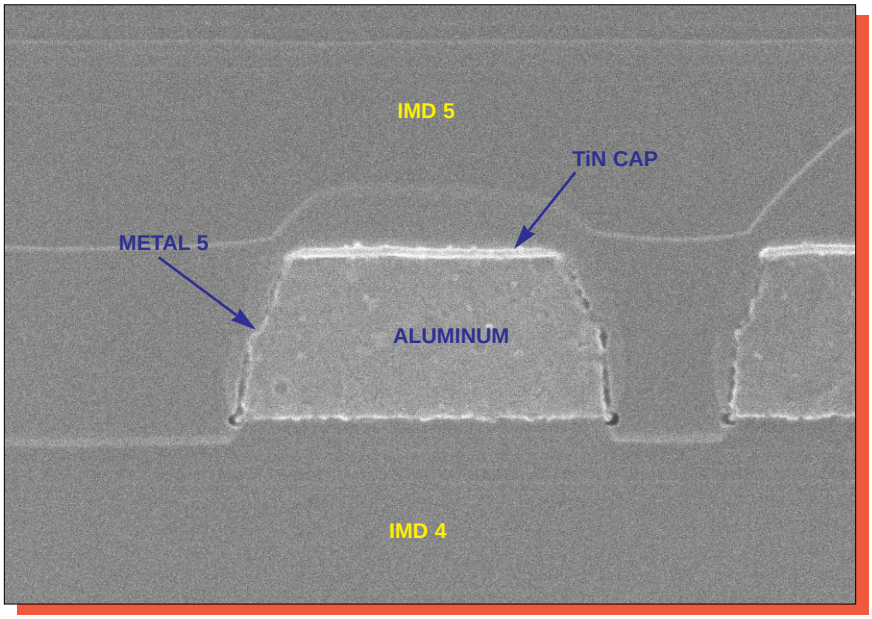


Mag. 25,000x, 60°

Figure 13. SEM views of metal 6-to-metal 5 via plugs.

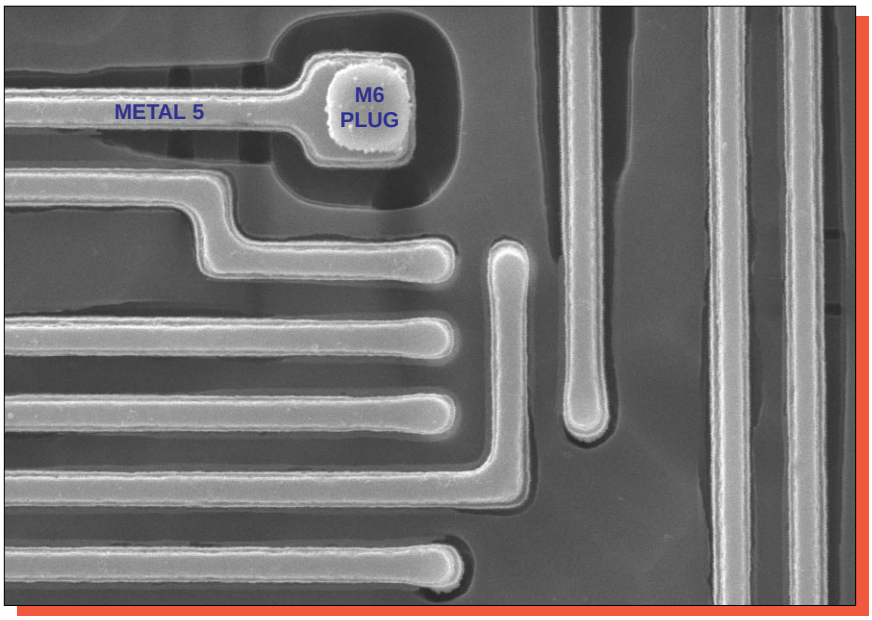


Mag.17,600x

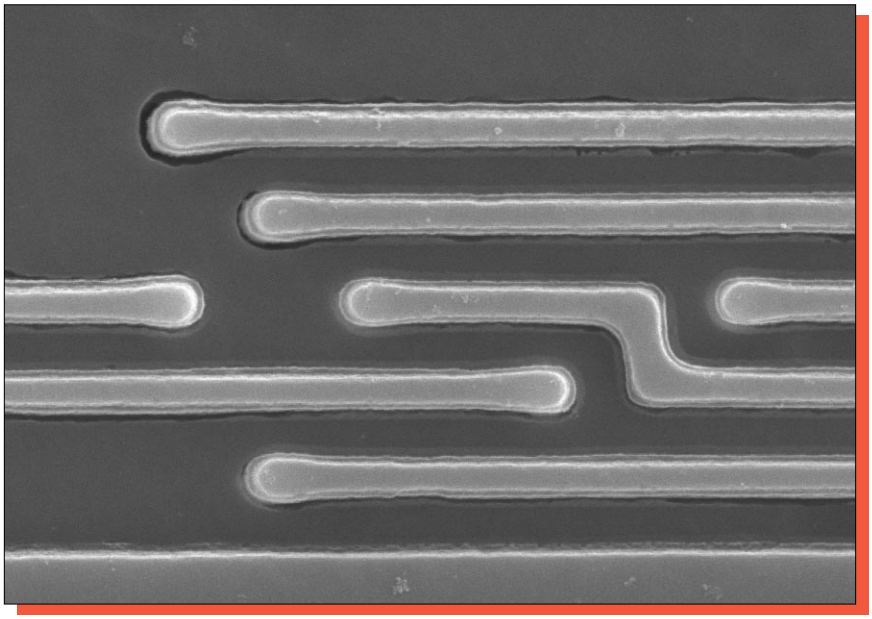


Mag. 26,000x

Figure 14. SEM section views of metal 5 line profiles.

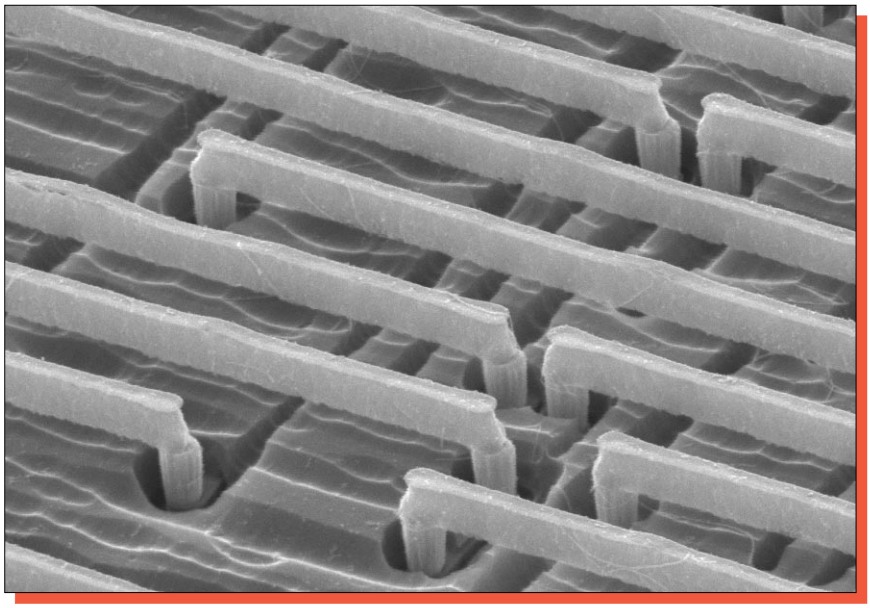


Mag. 8000x

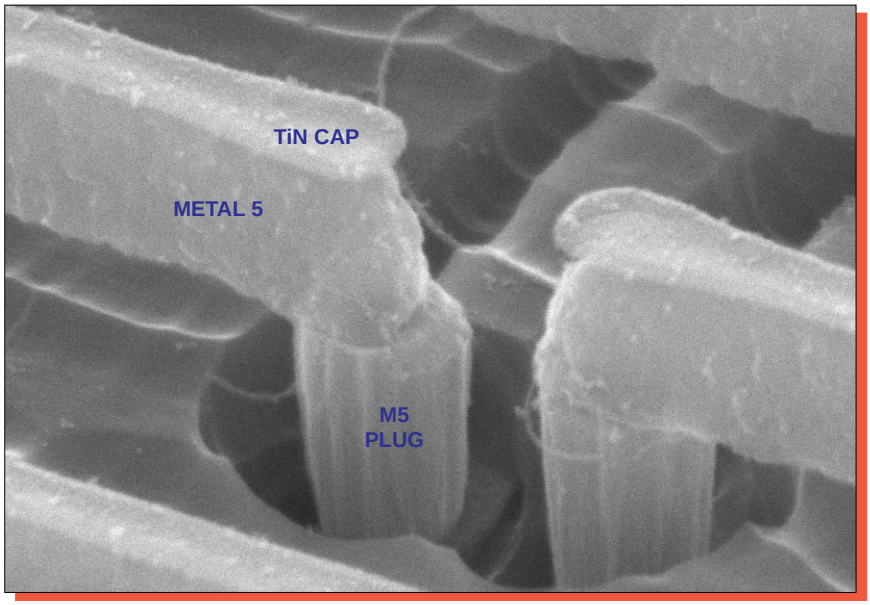


Mag. 10,000x

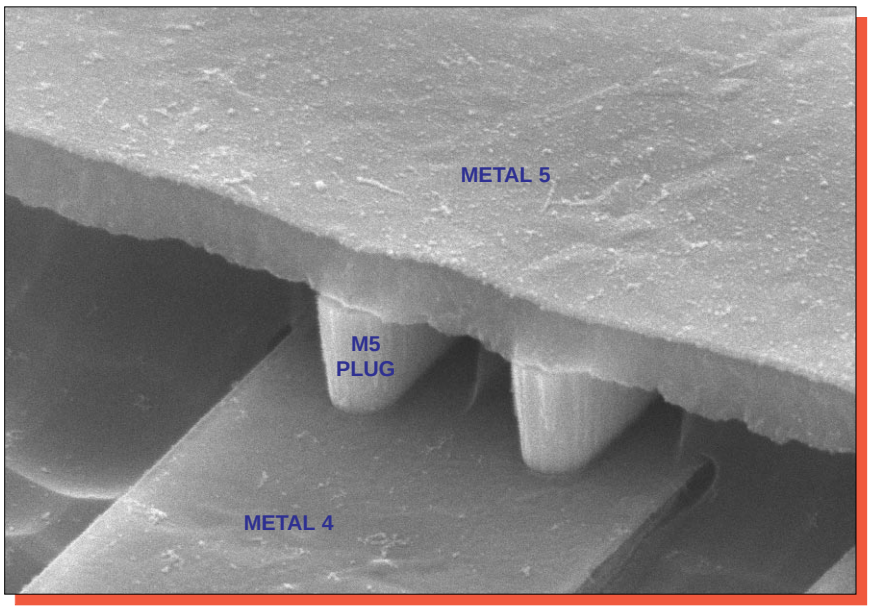
Figure 15. Topological SEM views of metal 5 patterning. 0°.



Mag. 7400x

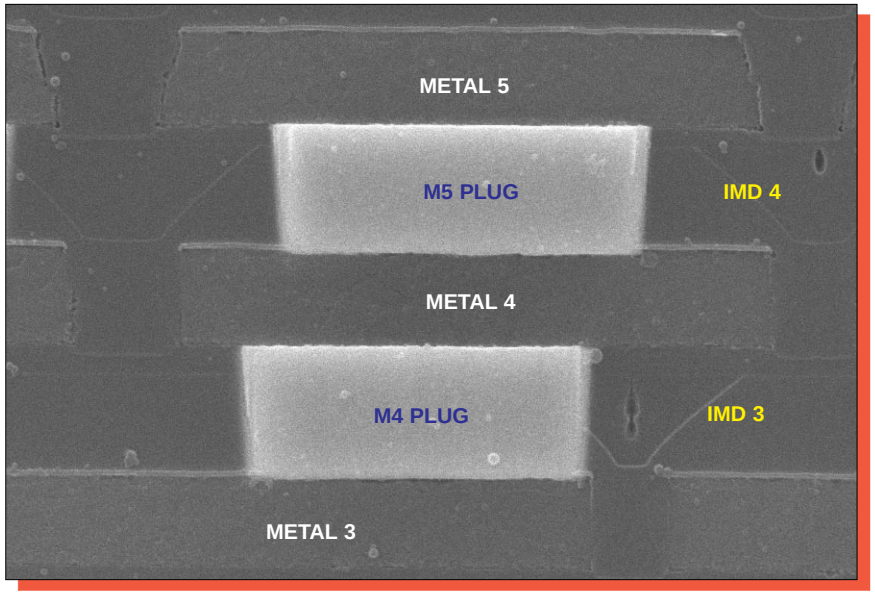


Mag. 30,000x

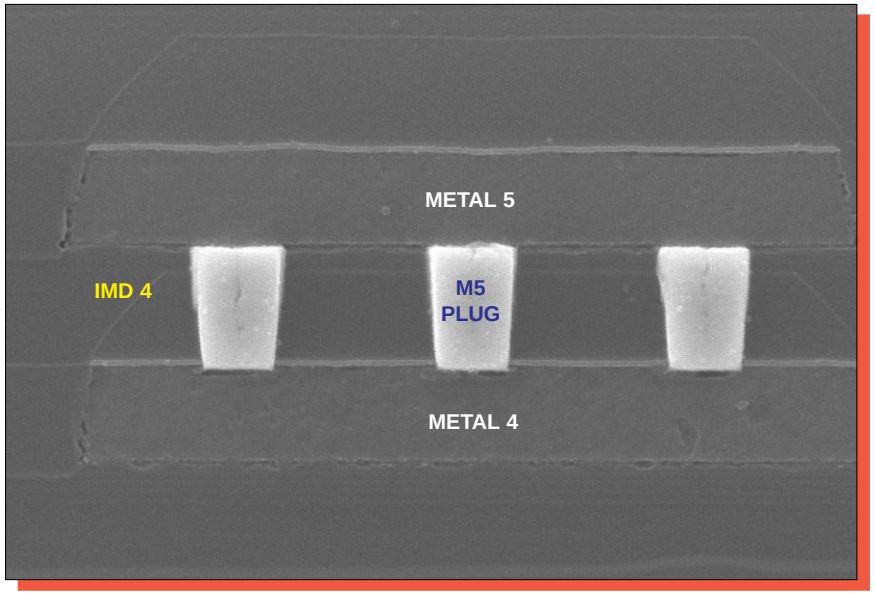


Mag. 15,000x

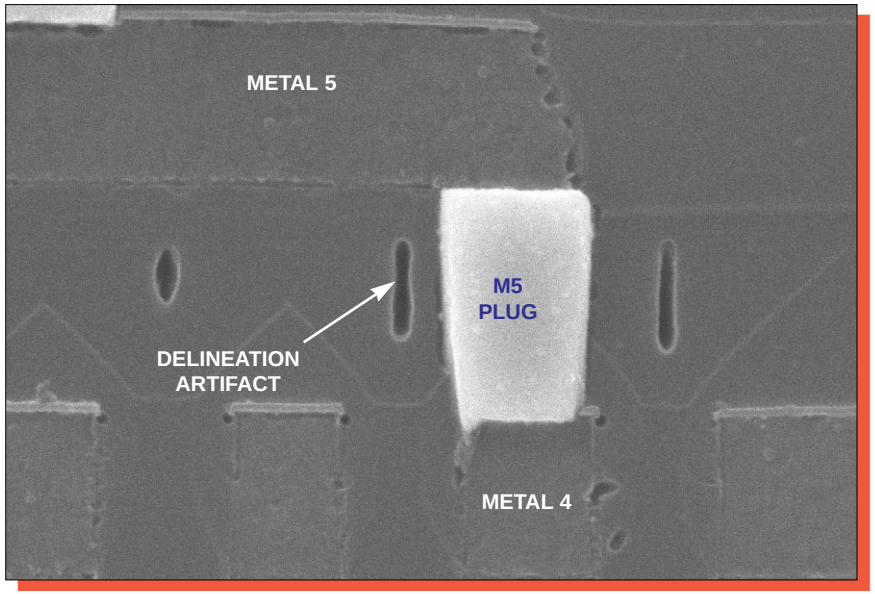
Figure 16. SEM views of general metal 5 integrity. 55°.



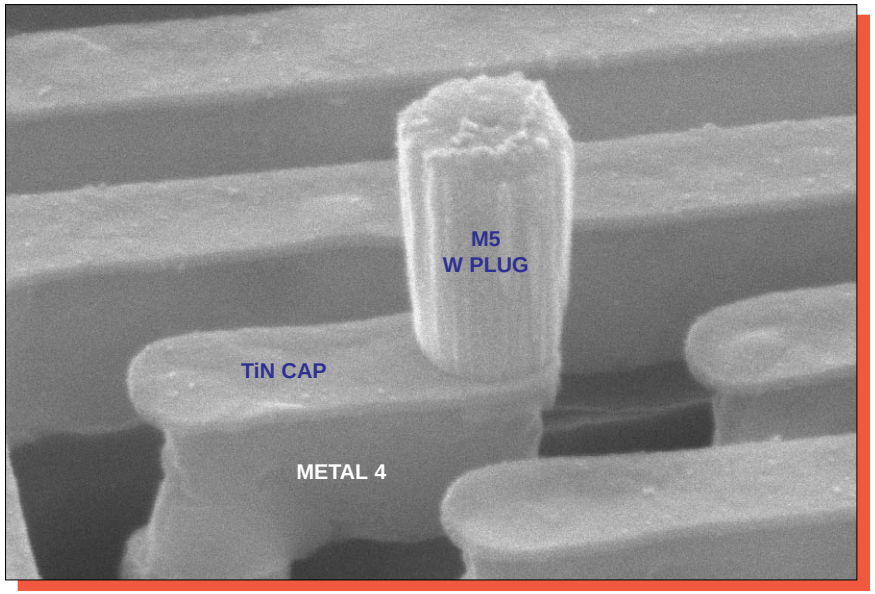
Mag. 15,000x



Mag. 15,000x

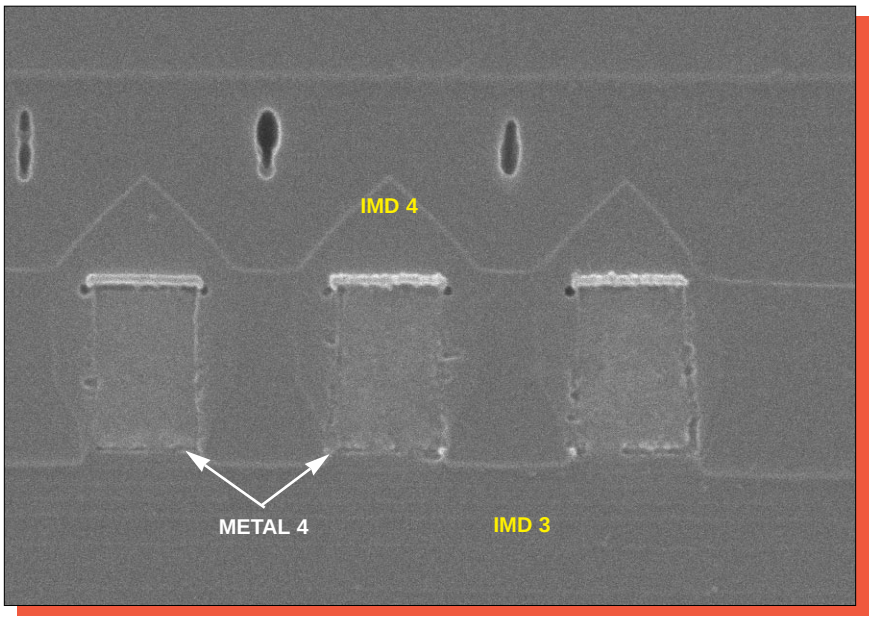


Mag. 26,000x

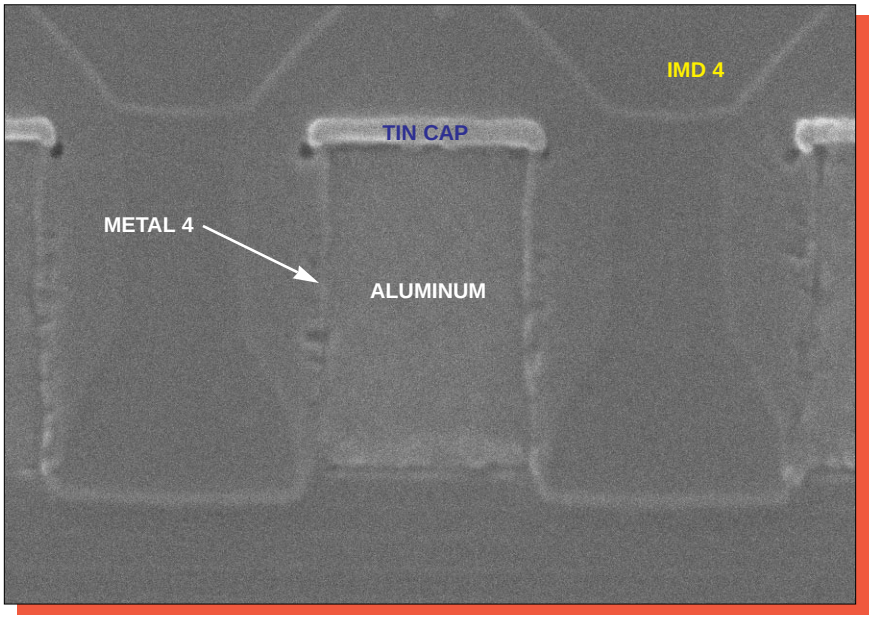


Mag. 30,000x, 55°

Figure 17. SEM views of metal 5-to-metal 4 vias and metal 5 plugs.

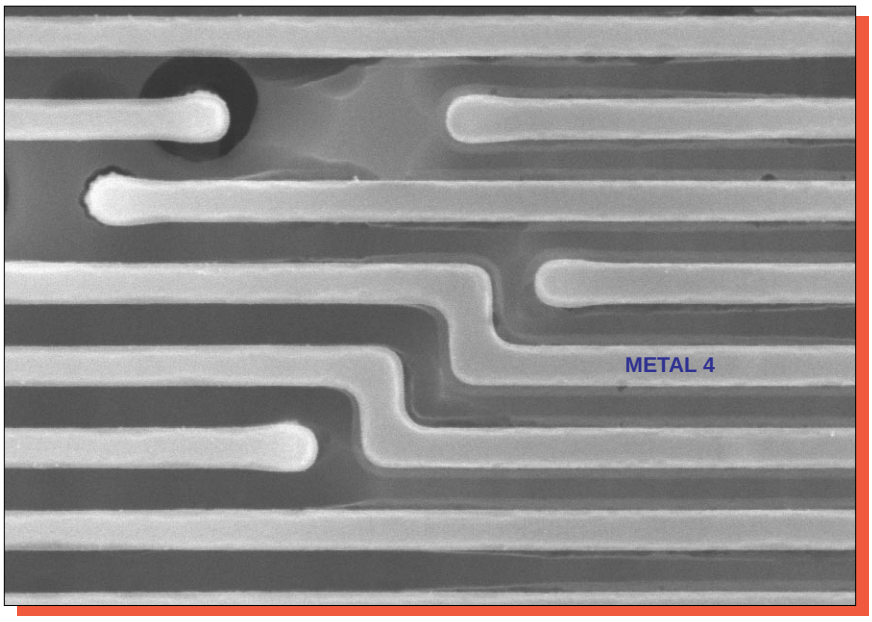


Mag. 26,000x



Mag. 52,000x

Figure 18. SEM section views of metal 4 line profiles.



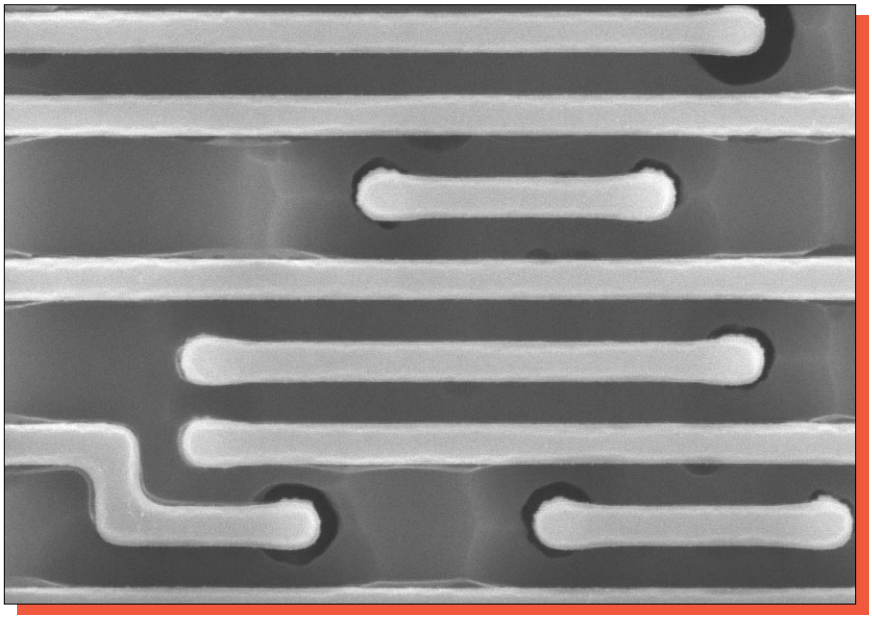
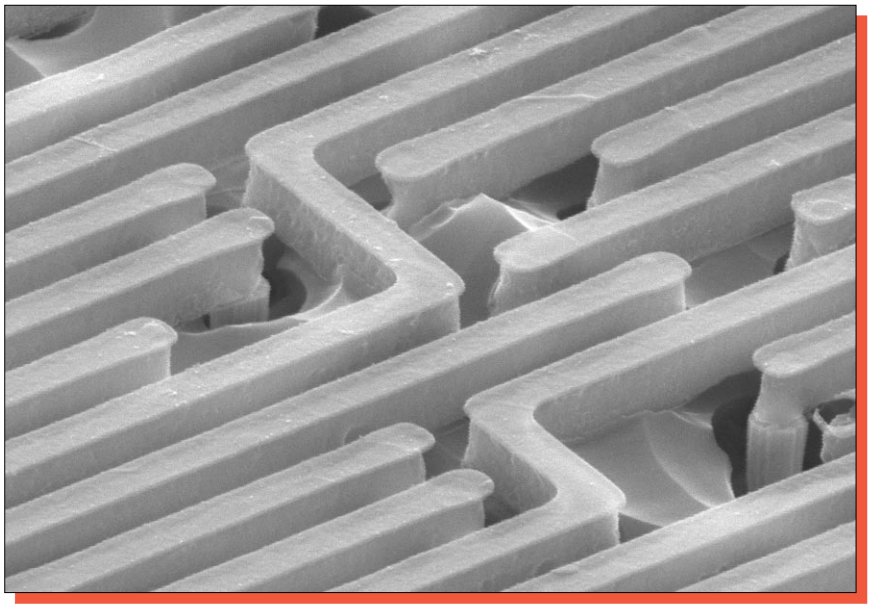
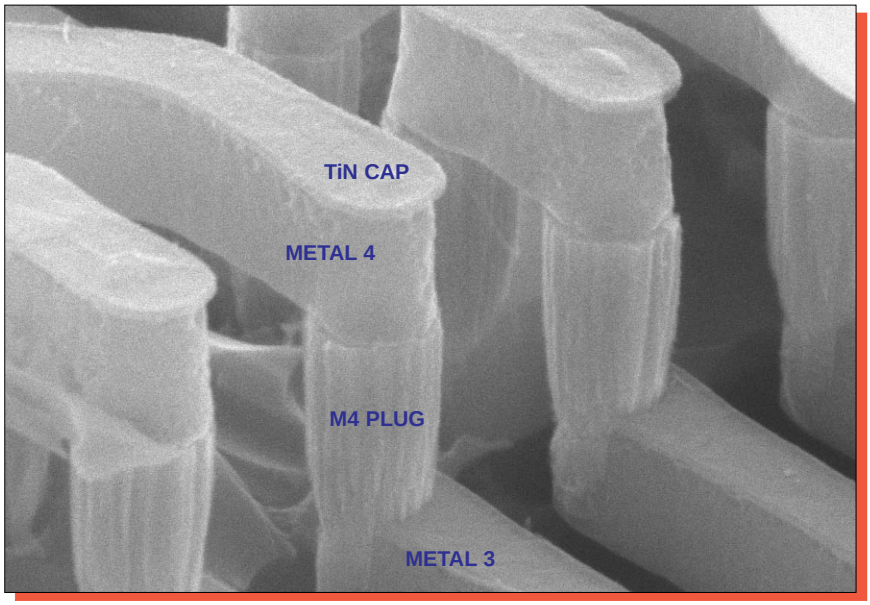


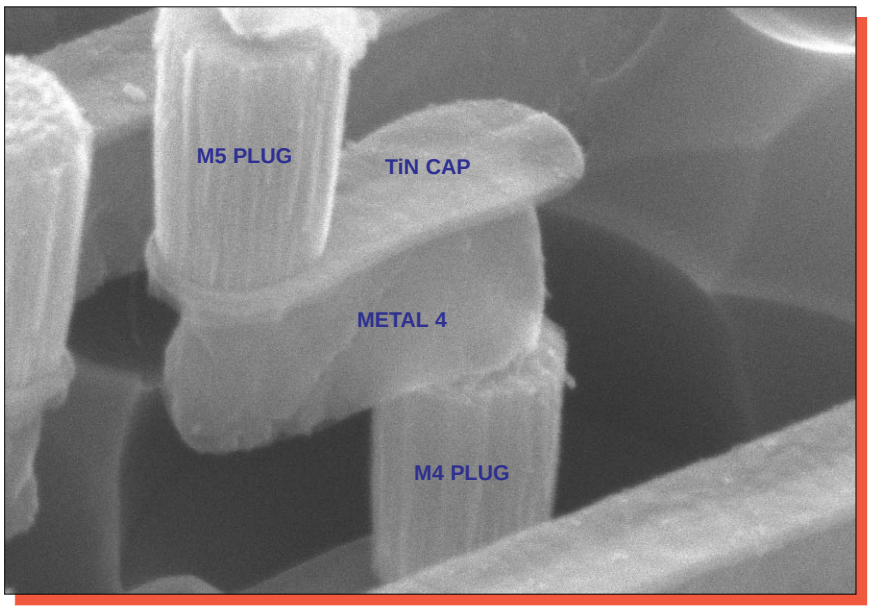
Figure 19. Topological SEM views of metal 4 patterning. Mag. 9000x, 0°.



Mag. 11,000x

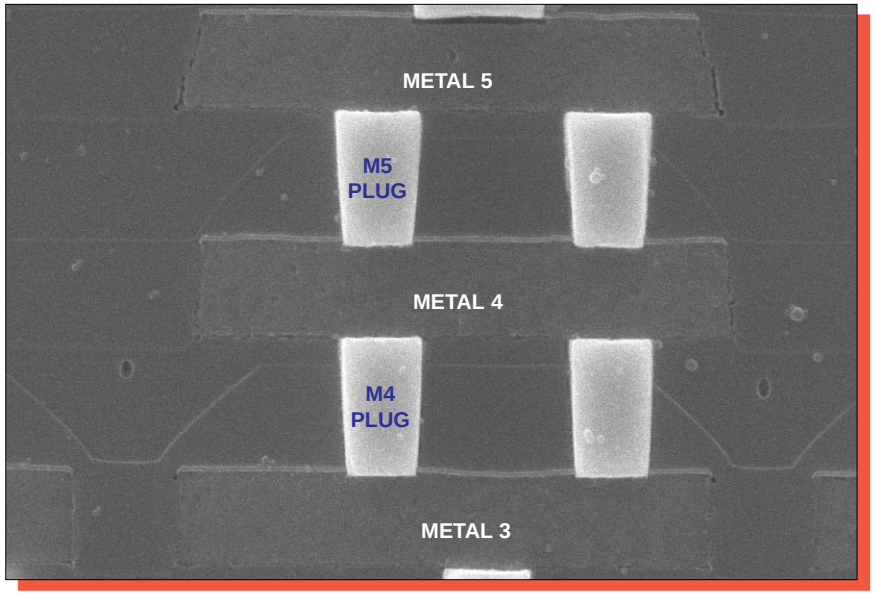


Mag. 25,000x

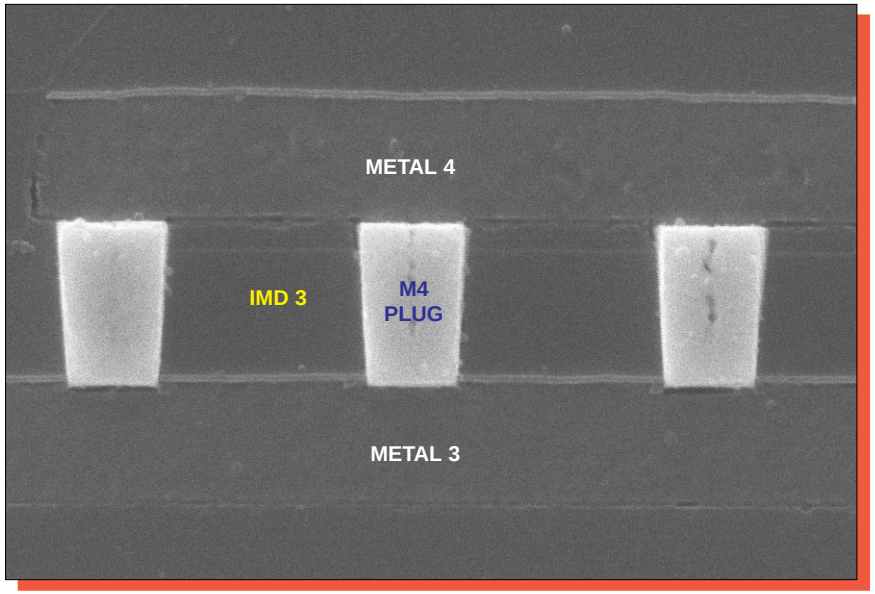


Mag. 35,000x

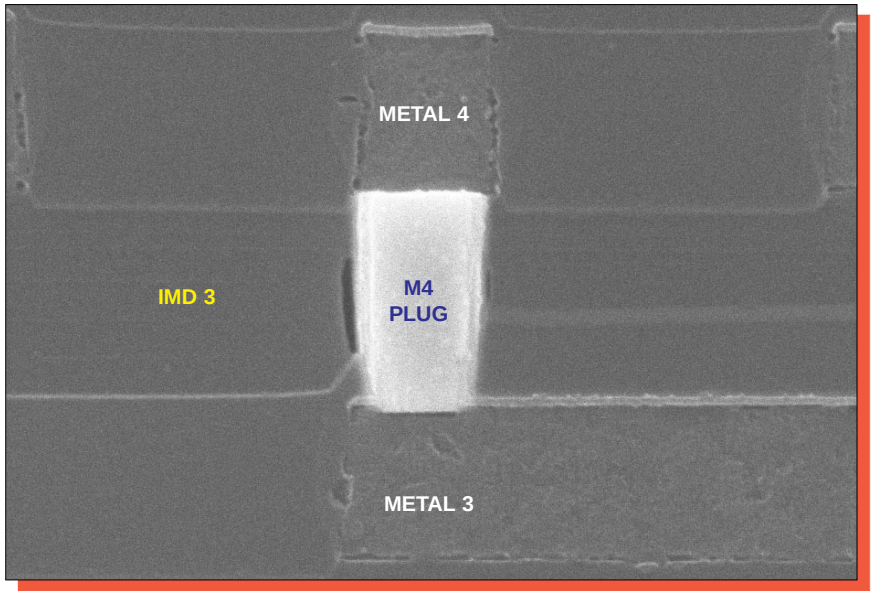
Figure 20. SEM views illustrating general metal 4 integrity. 55°.



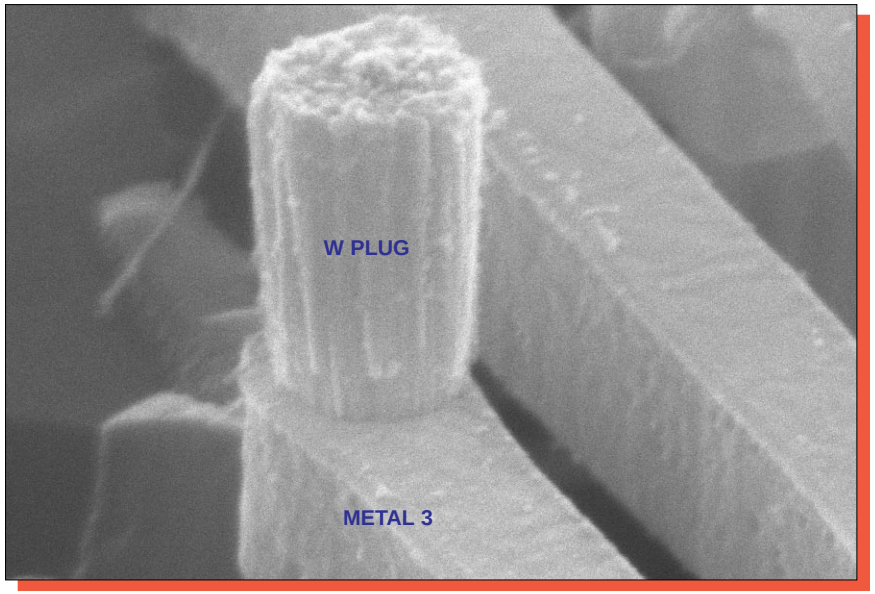
Mag. 15,000x



Mag. 20,000x

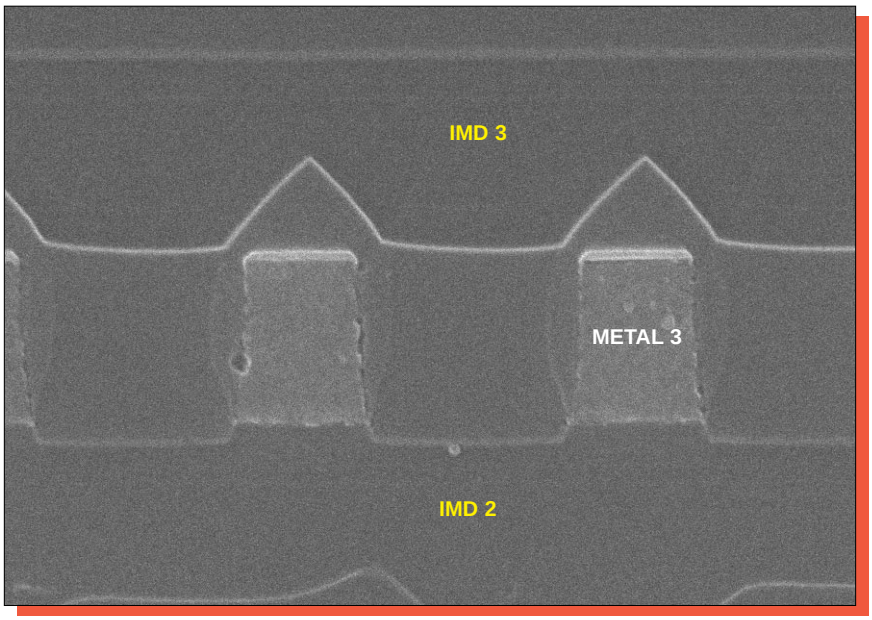


Mag. 26,000x

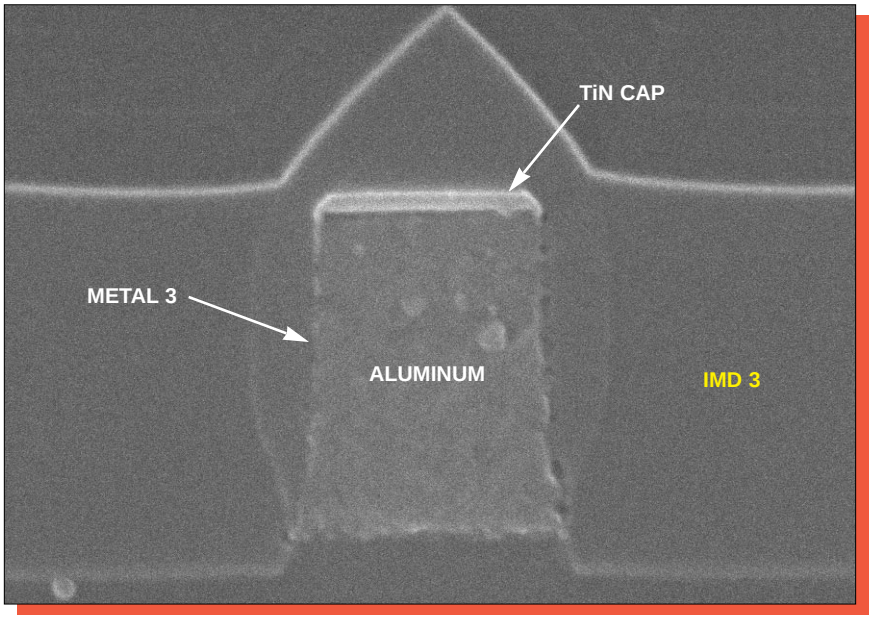


Mag. 45,000x, 60°

Figure 21. SEM views of metal 4-to-metal 3 via plugs.

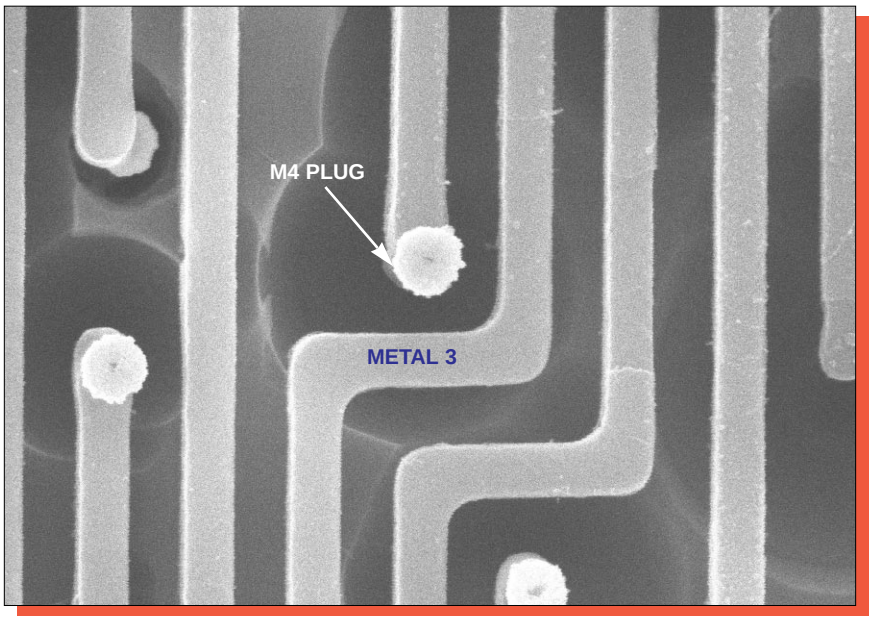


Mag. 26,000x

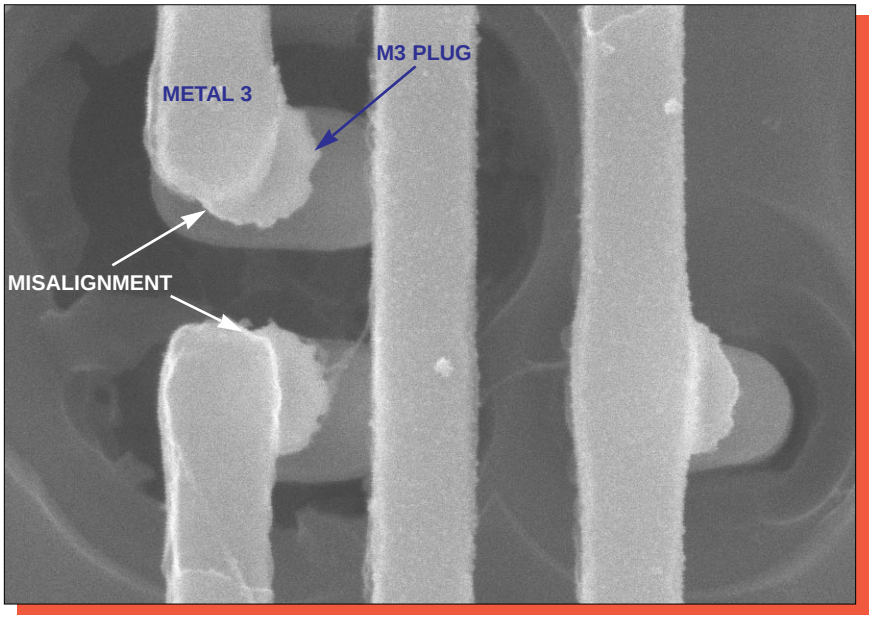


Mag. 52,000x

Figure 22. SEM section views of metal 3 line profiles.

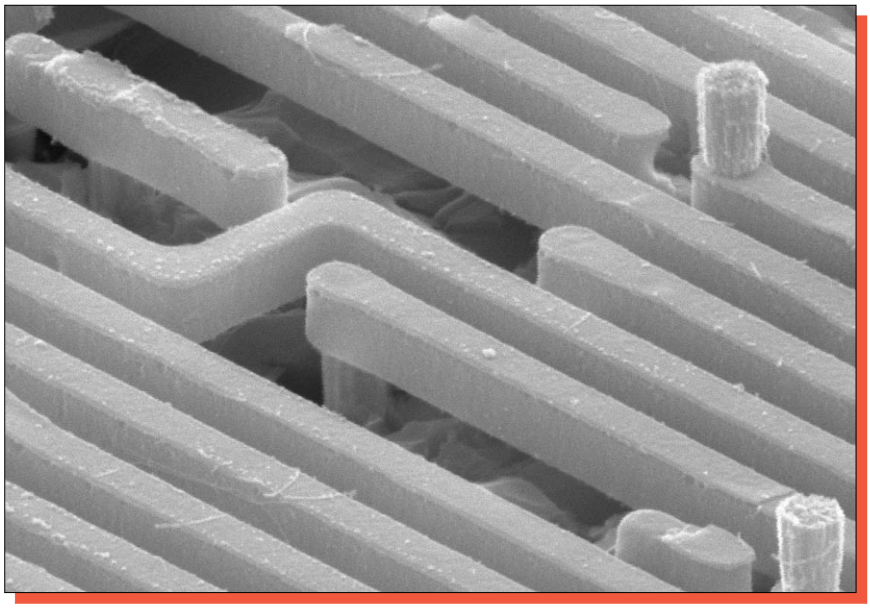


Mag. 13,000x

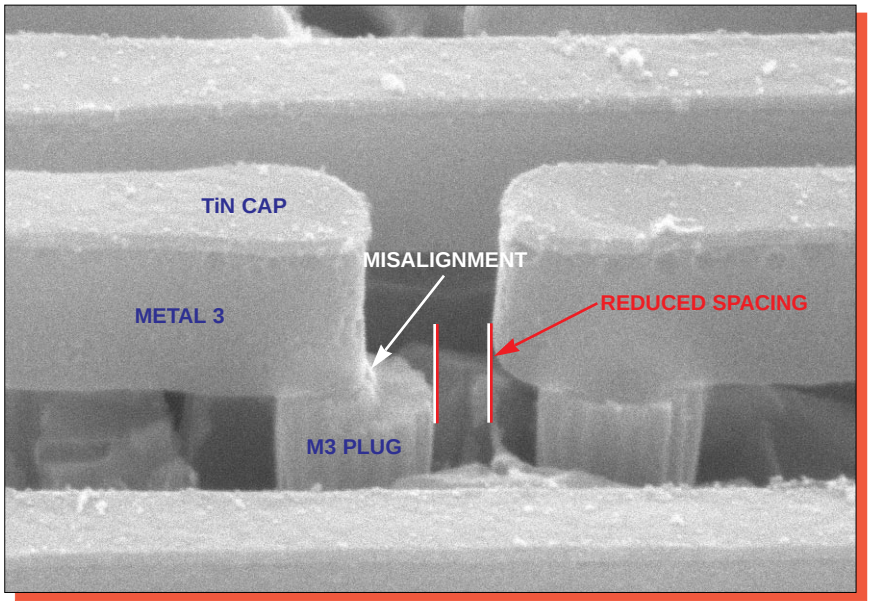


Mag. 26,000x

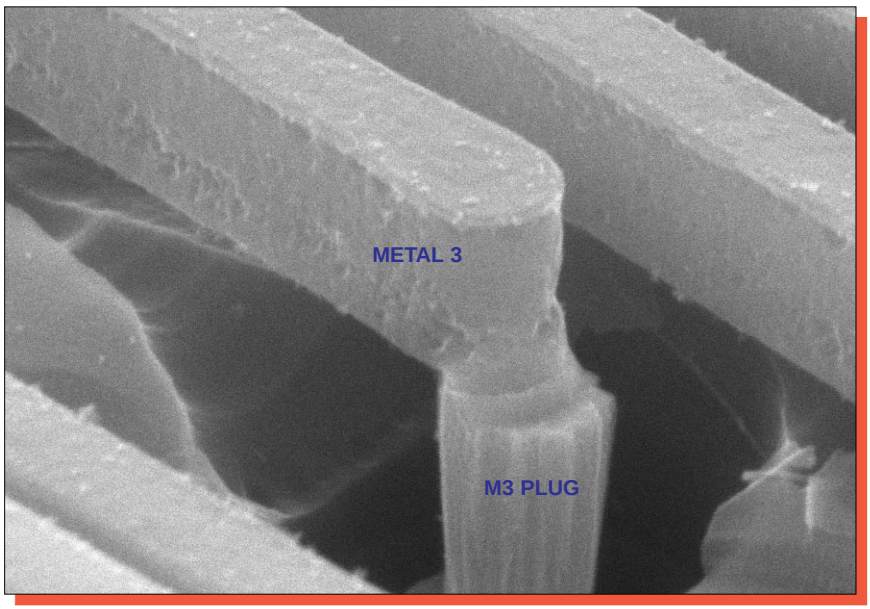
Figure 23. Topological SEM views illustrating metal 3 patterning. 0°.



Mag. 13,000x

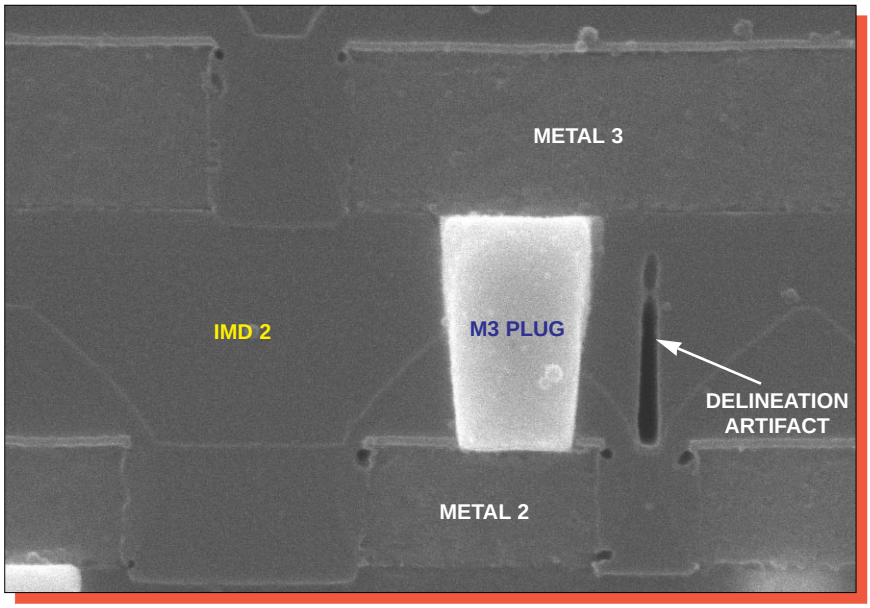


Mag. 30,000x

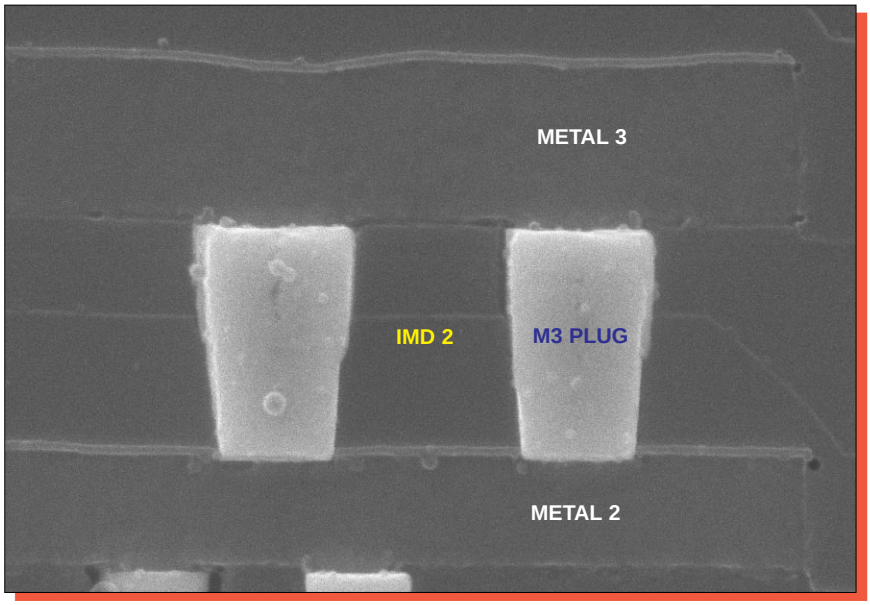


Mag. 30,000x

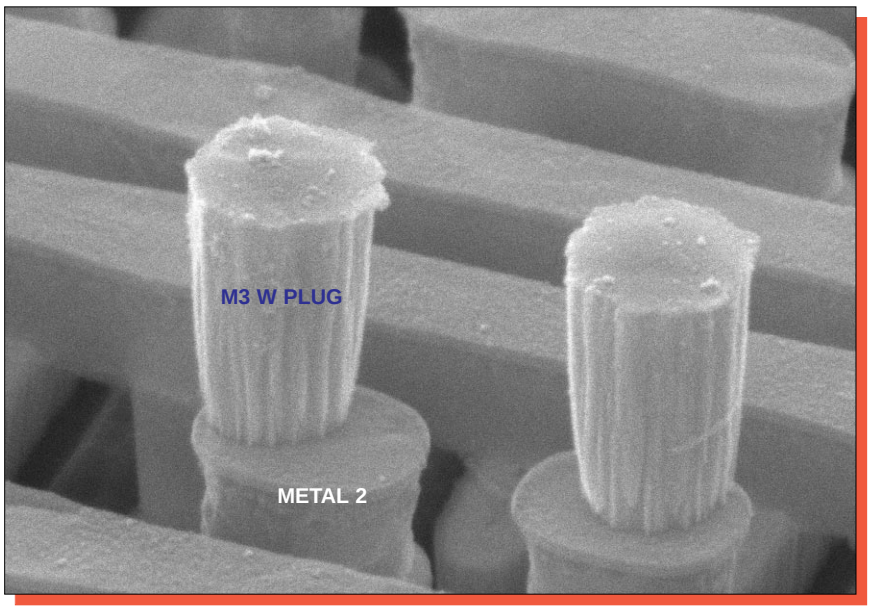
Figure 24. SEM views illustrating general metal 3 integrity. 60°.



Mag. 26,000x

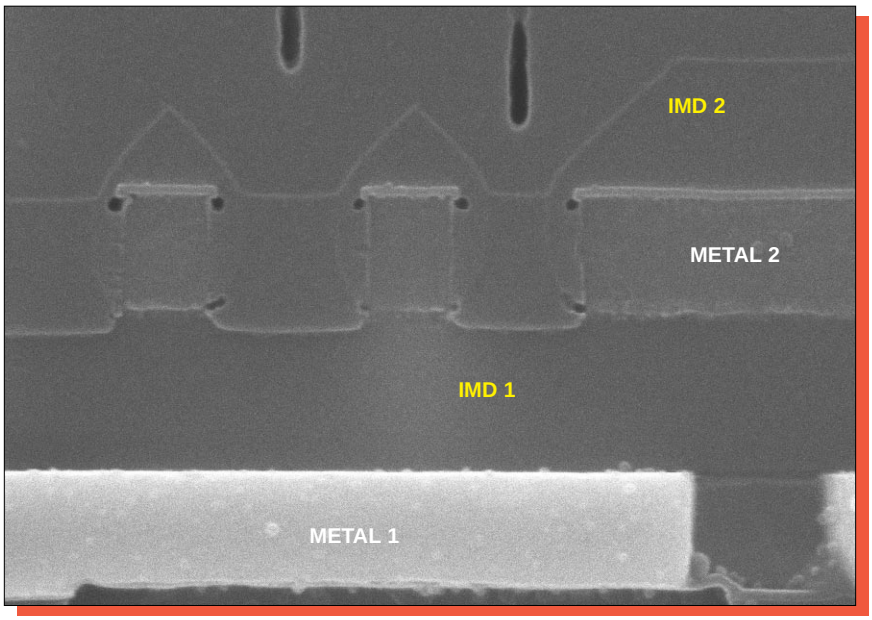


Mag. 26,000x

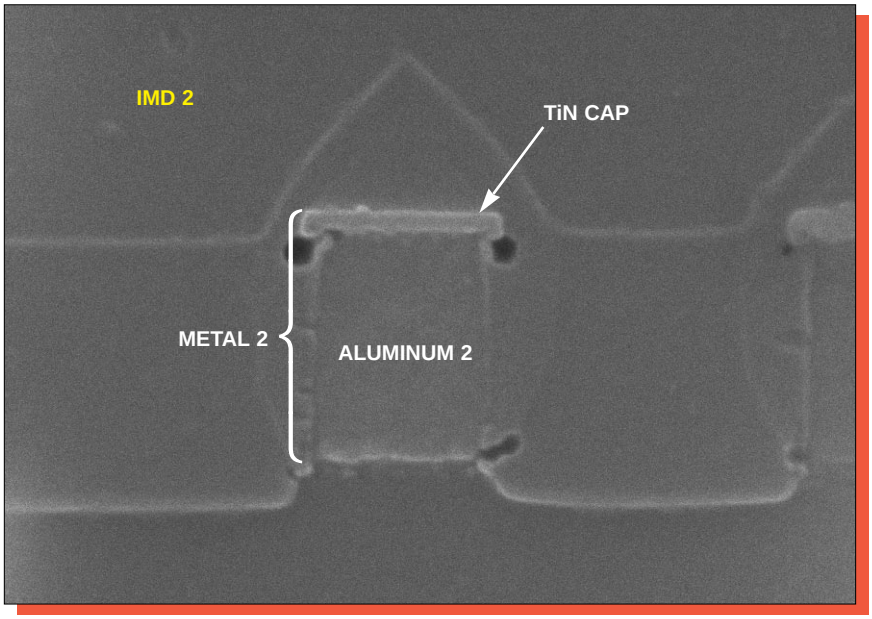


Mag. 32,000x, 55°

Figure 25. SEM views of metal 3-to-metal 2 via plugs.

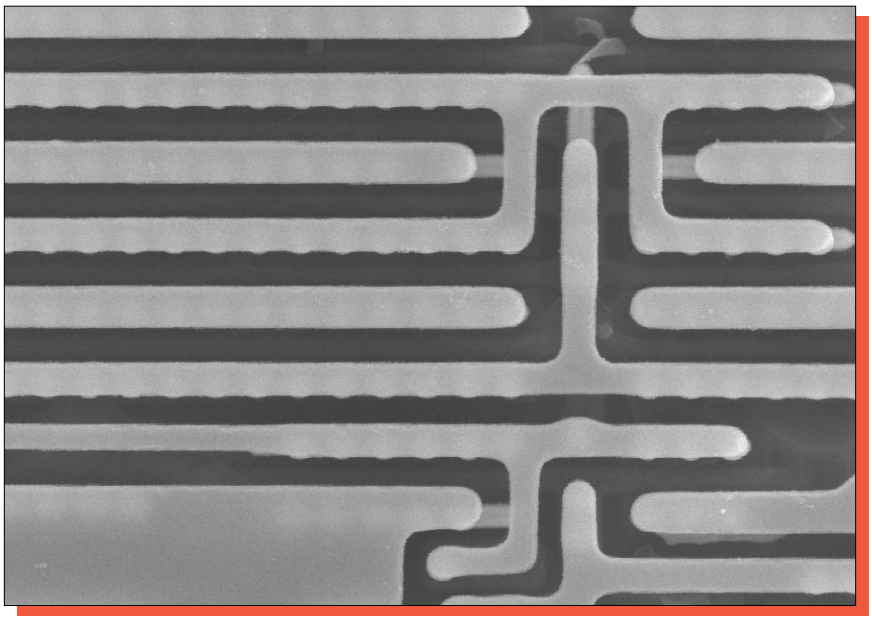


Mag. 26,000x



Mag. 52,000x

Figure 26. SEM section views of metal 2 line profiles.



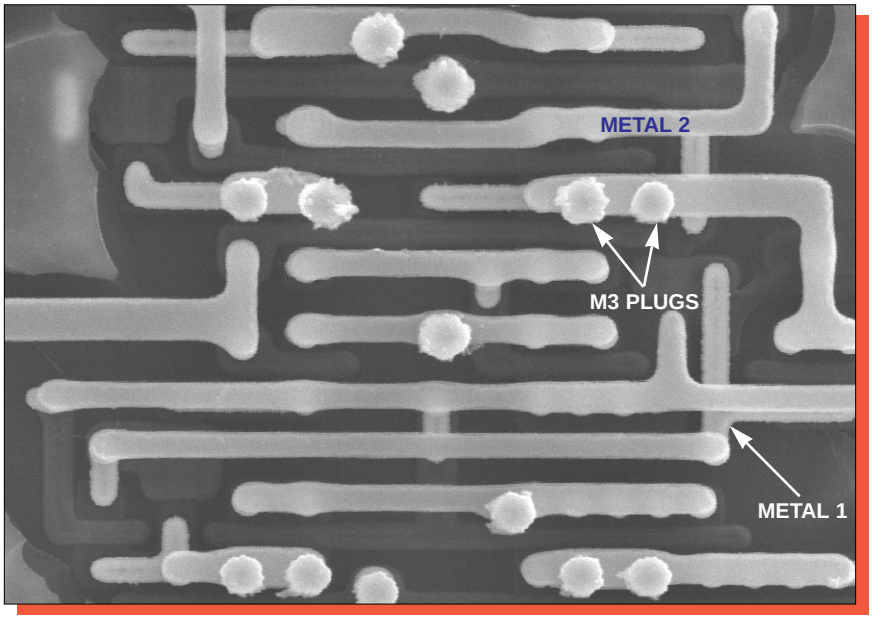
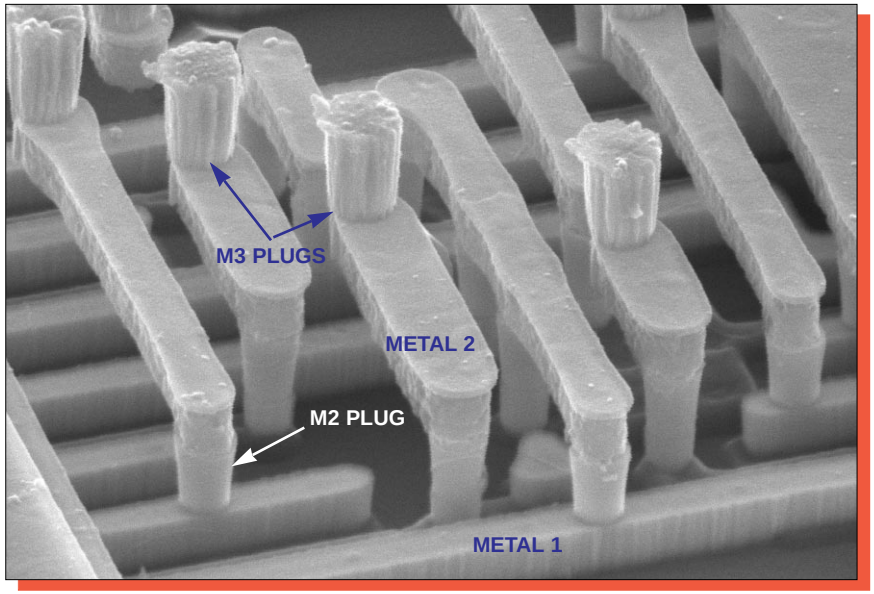
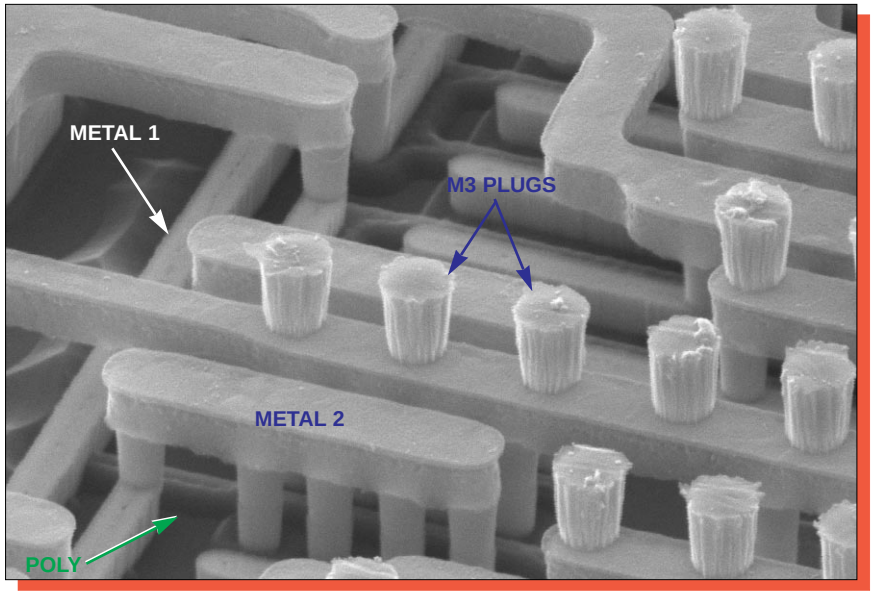


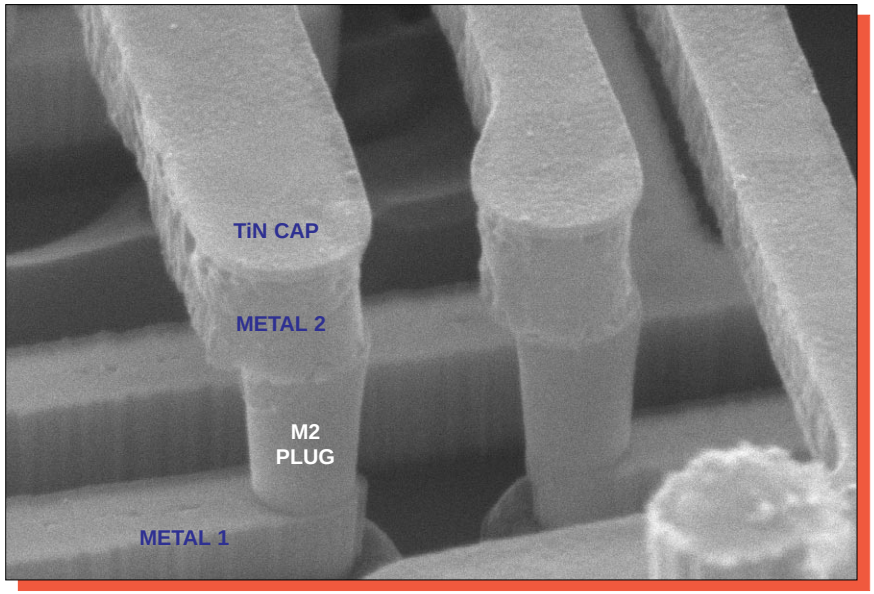
Figure 27. Topological SEM views of metal 2 patterning. Mag. 8000x, 0°.



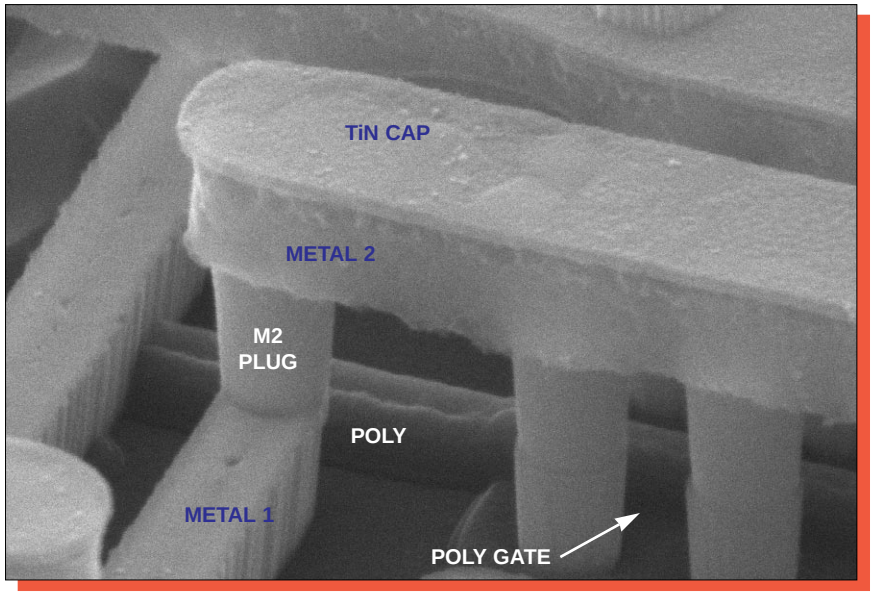
Mag. 13,500x



Mag. 13,000x

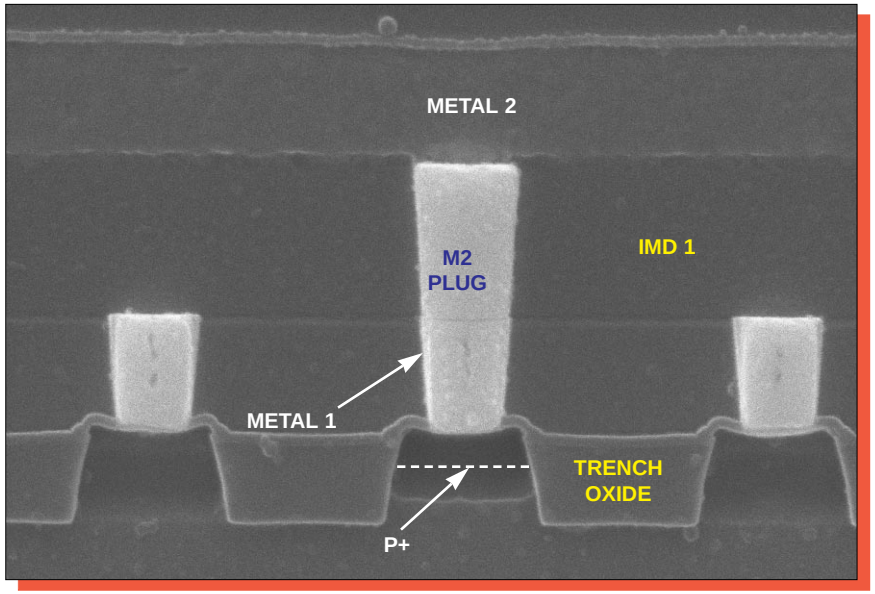


Mag. 30,000x

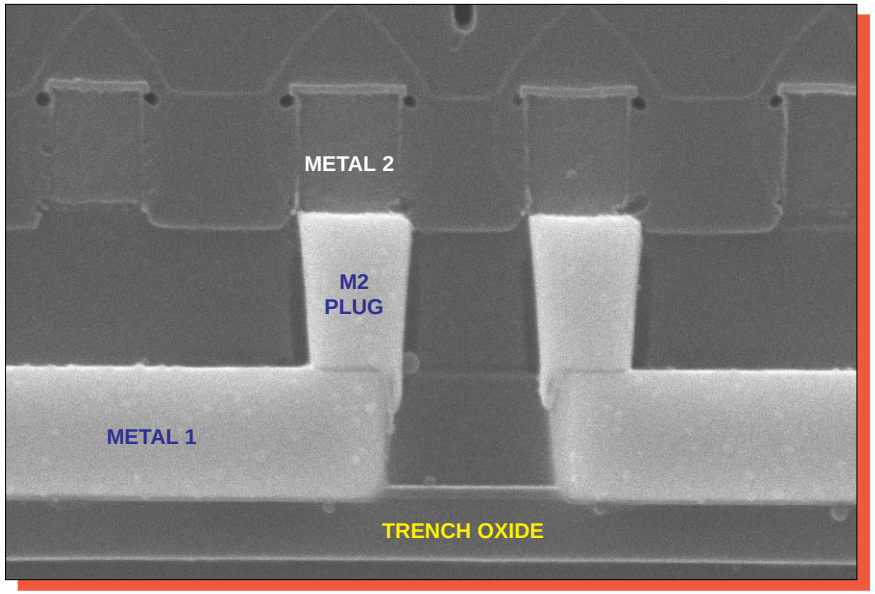


Mag. 32,000x

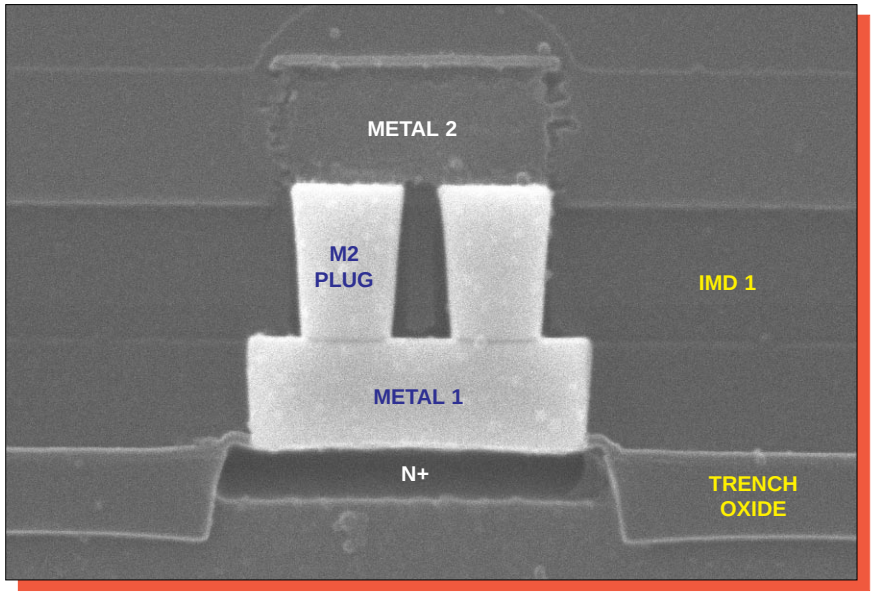
Figure 28. SEM views illustrating general metal 2 integrity. 55°.



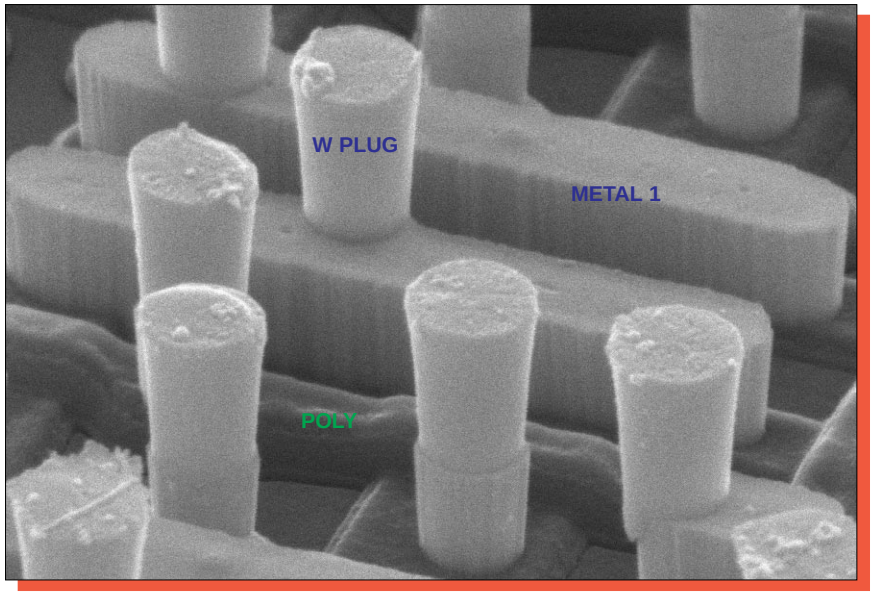
Mag. 26,000x



Mag. 26,000x

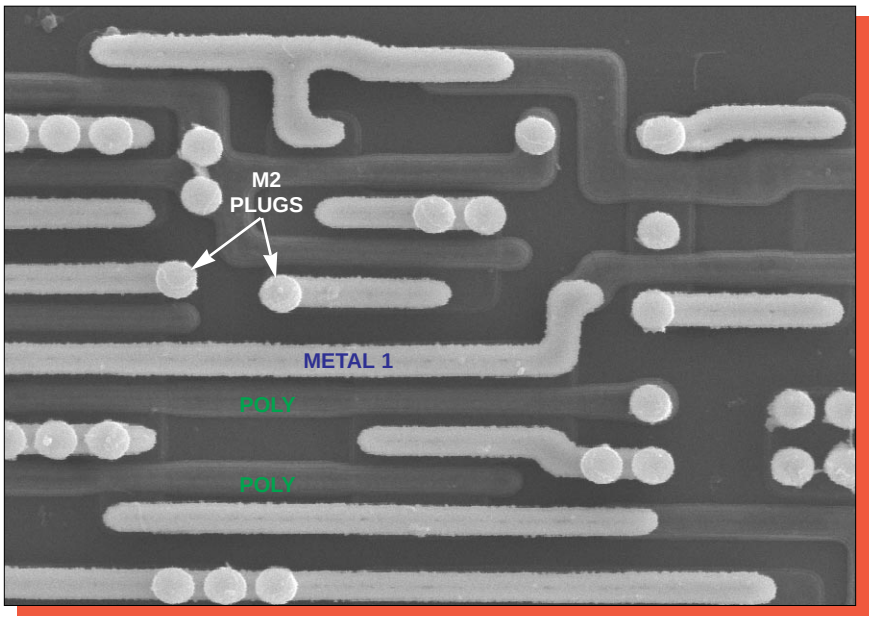


Mag. 26,000x



Mag. 30,000x, 55°

Figure 29. SEM views of metal 2-to-metal 1 via plugs.



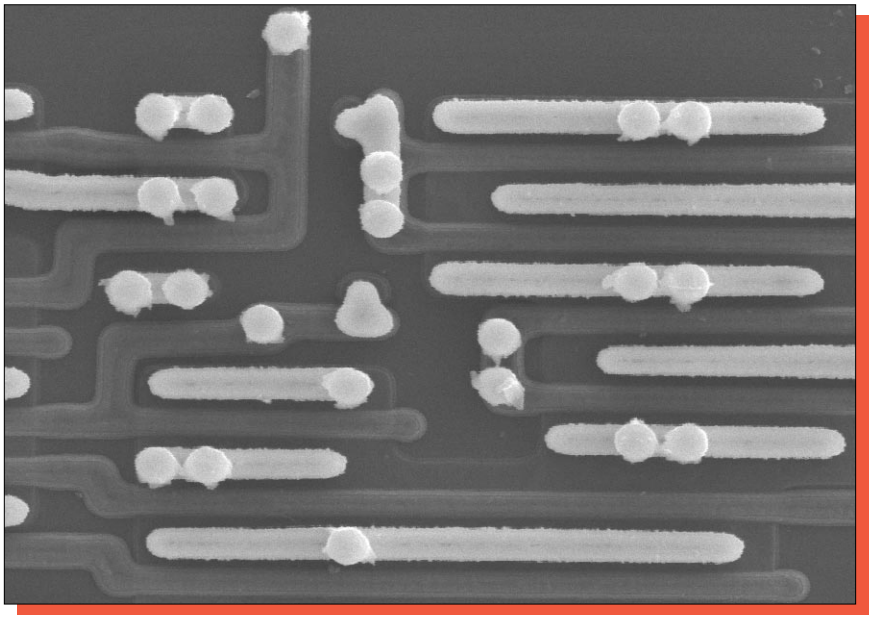
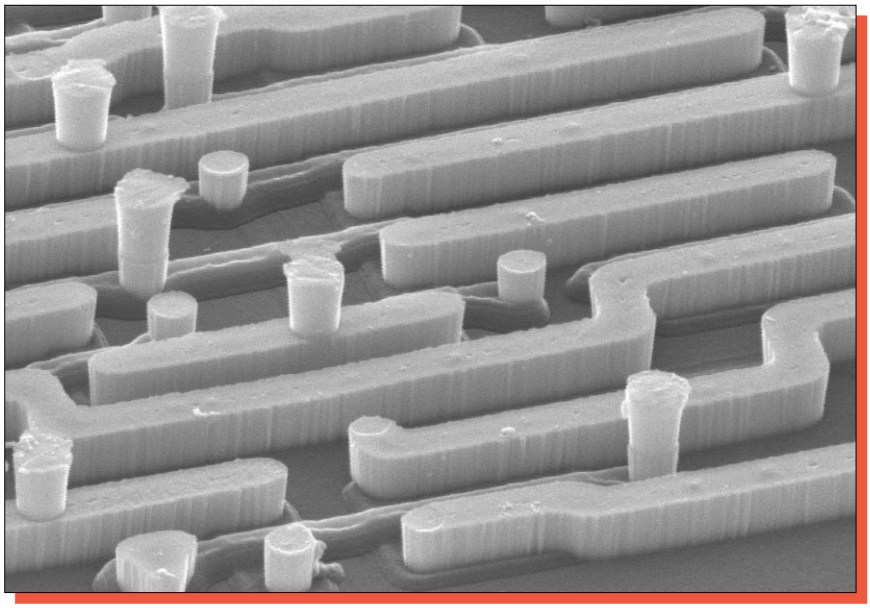
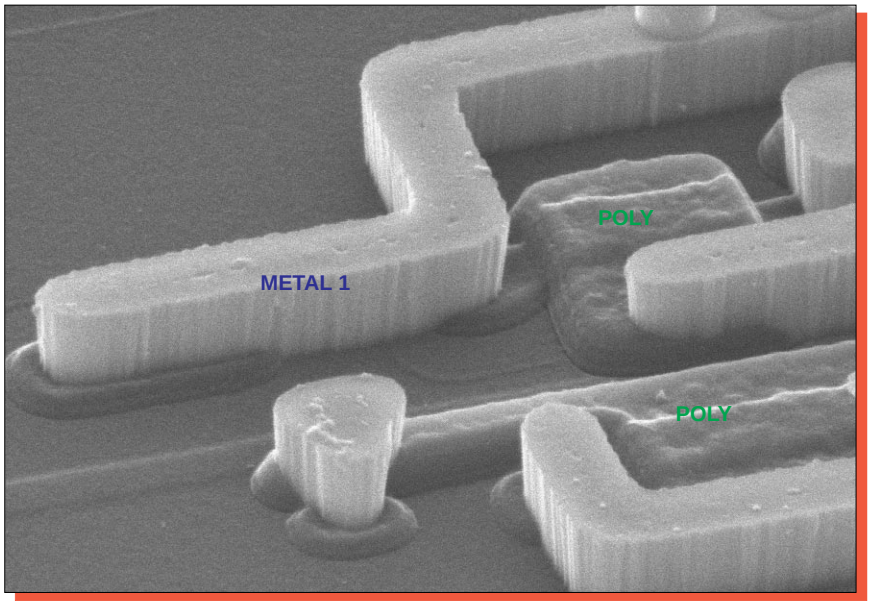


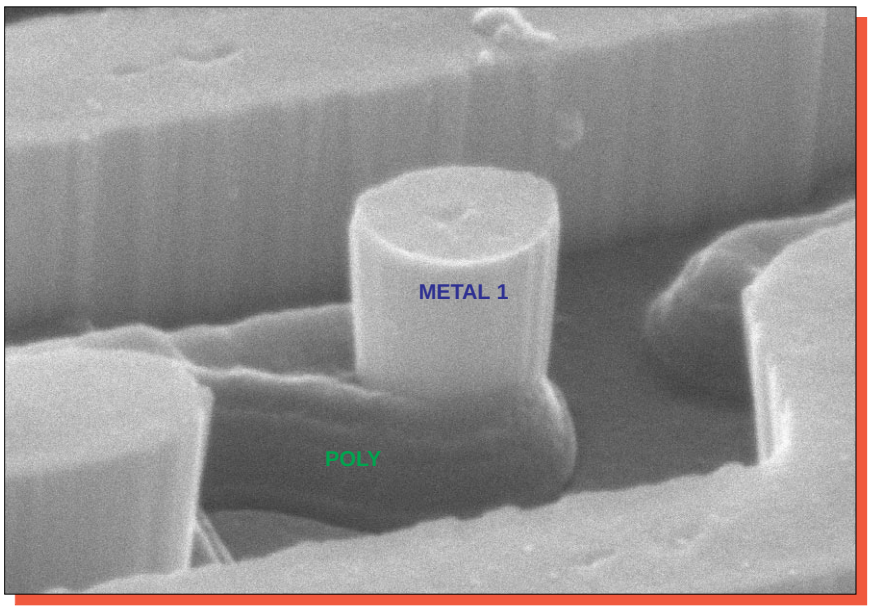
Figure 30. Topological SEM views of metal 1 patterning. Mag. 10,000x, 0°.



Mag. 13,500x

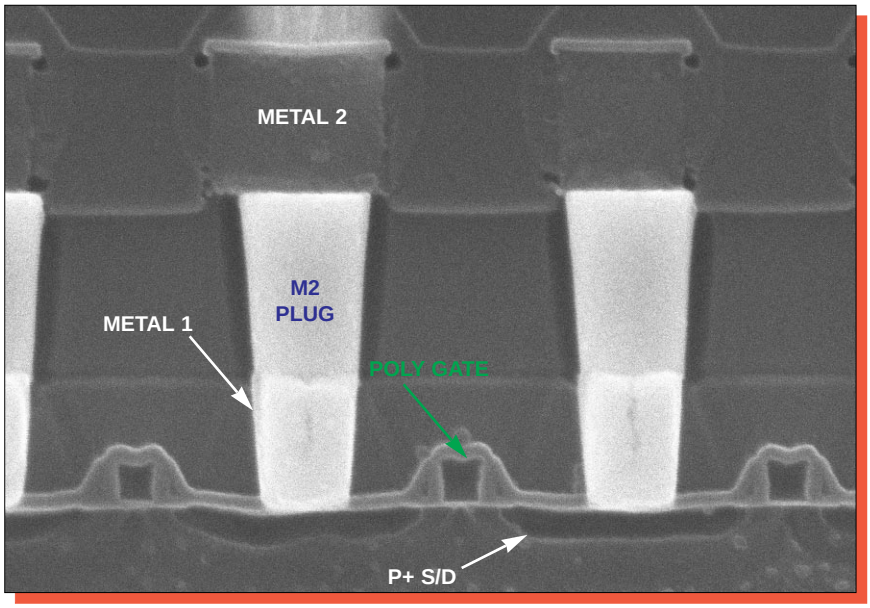


Mag. 22,000x

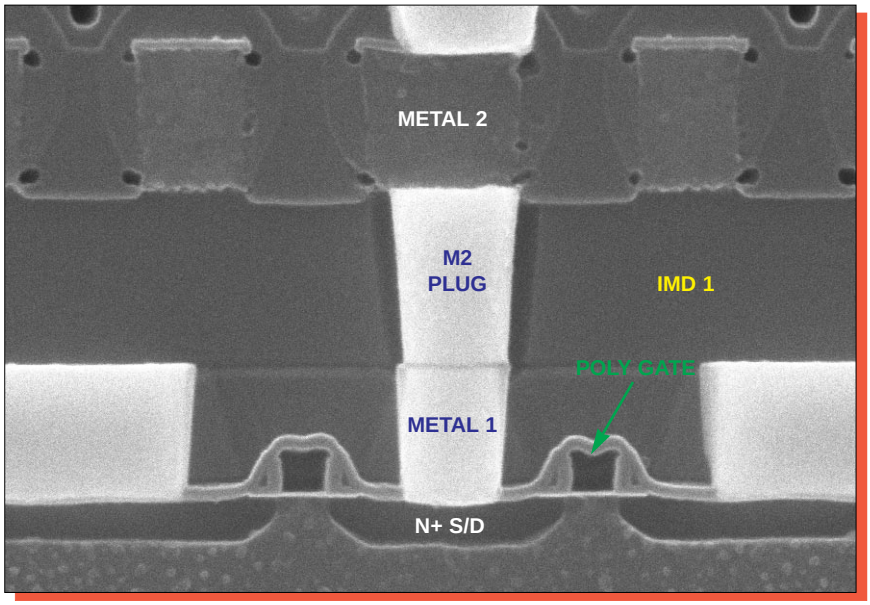


Mag. 60,000x

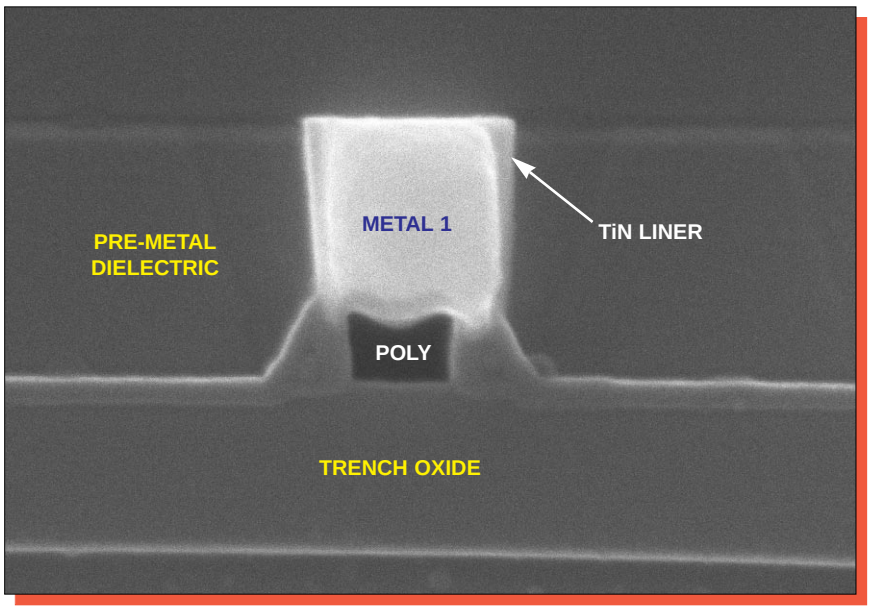
Figure 31. SEM views of general metal 1 coverage. 55°.



Mag. 30,000x

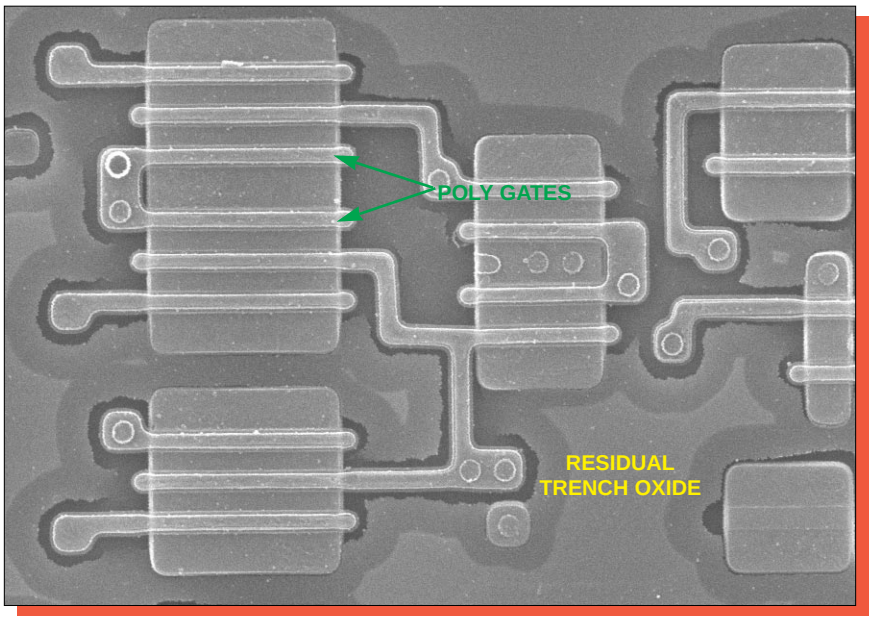


Mag. 30,000x

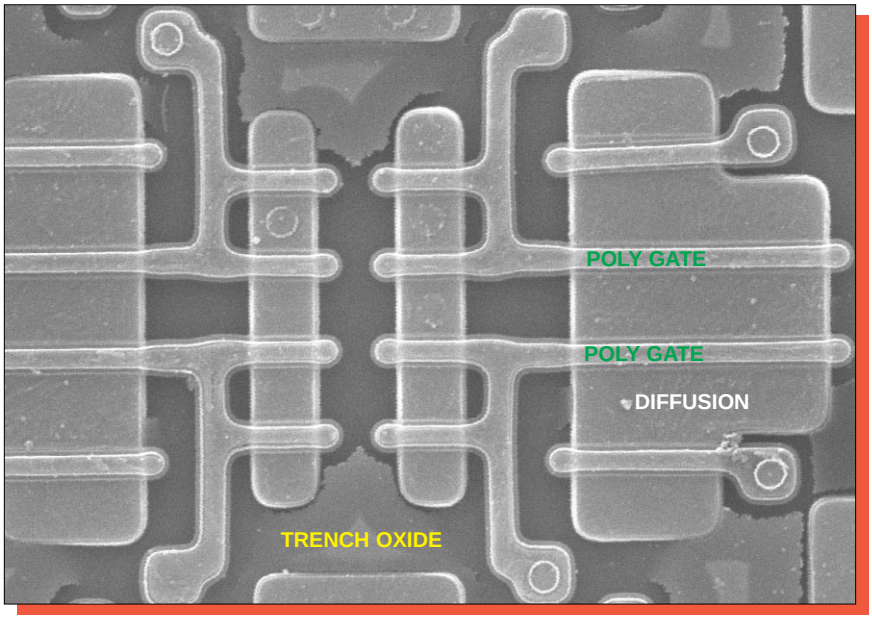


Mag. 60,000x

Figure 32. SEM section views of metal 1 contacts.

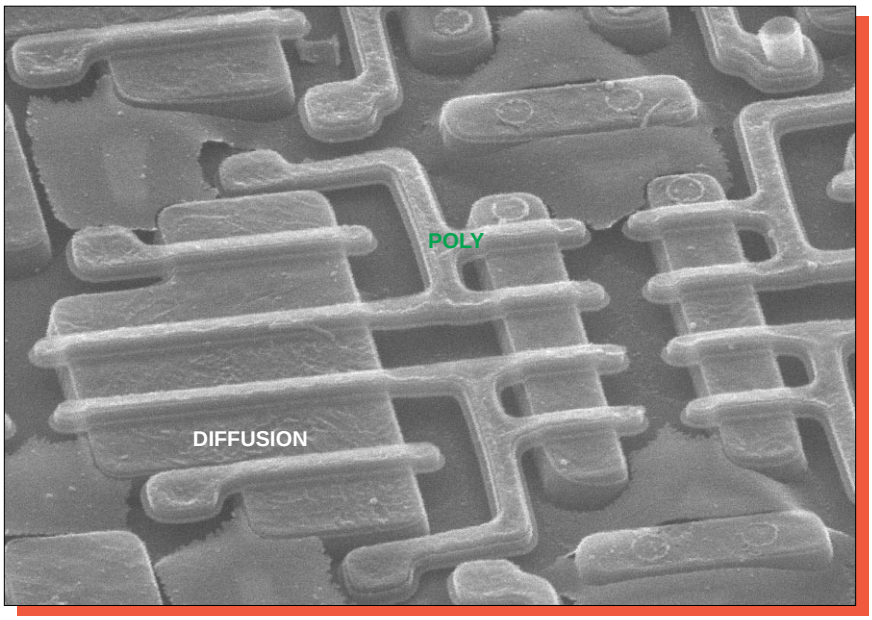


Mag. 6500x

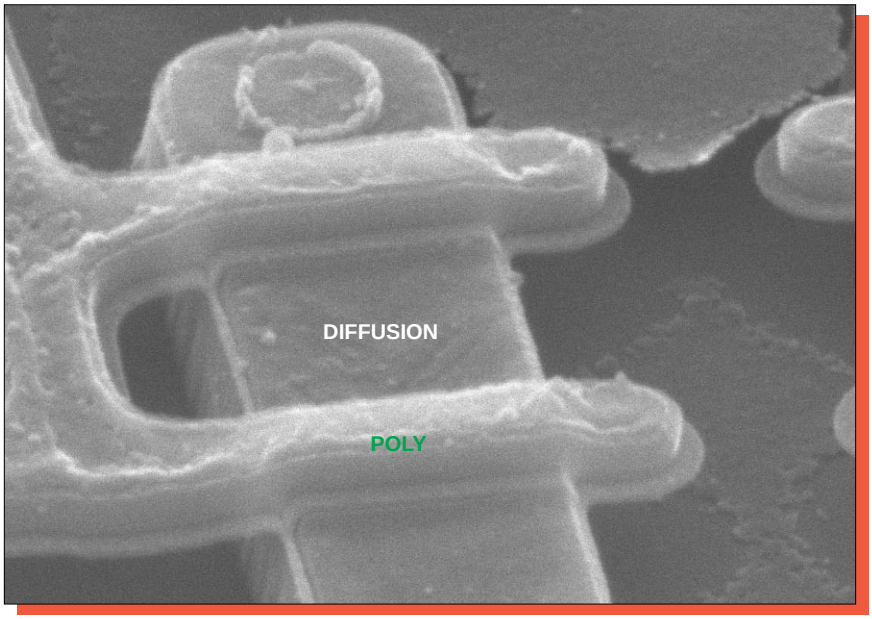


Mag. 10,000x

Figure 33. Topological SEM views of poly patterning. 0°.

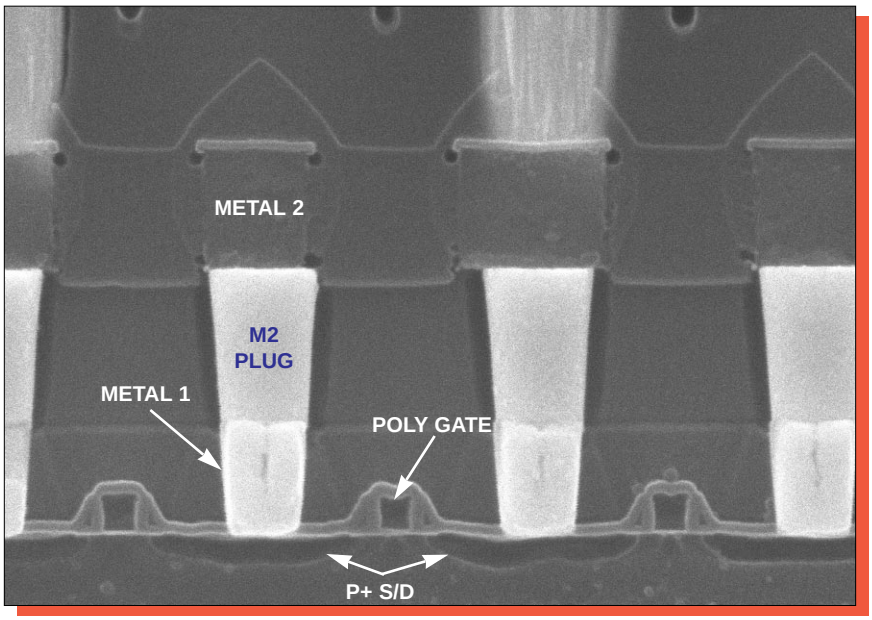


Mag. 13,000x

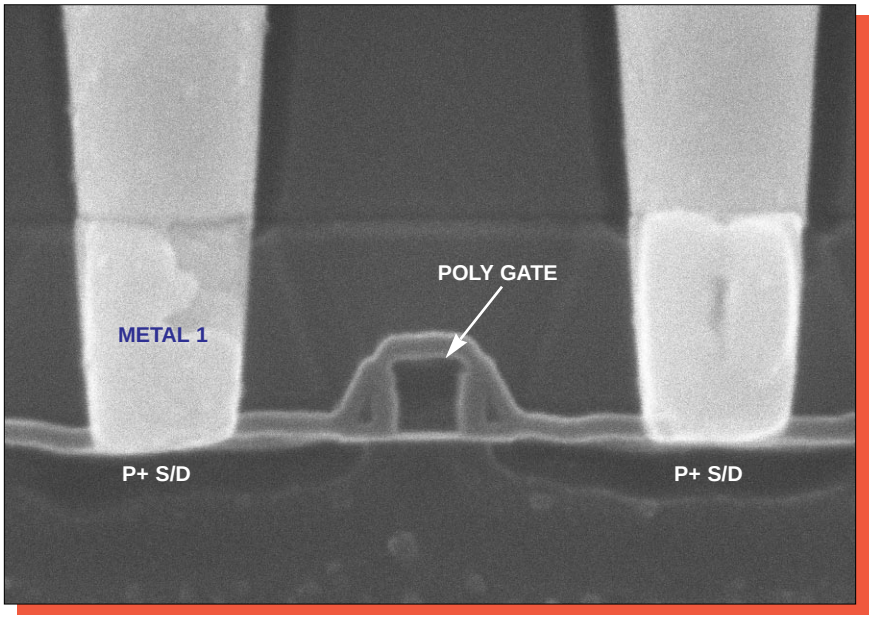


Mag. 47,000x

Figure 34. Perspective SEM views of poly coverage. 55°.

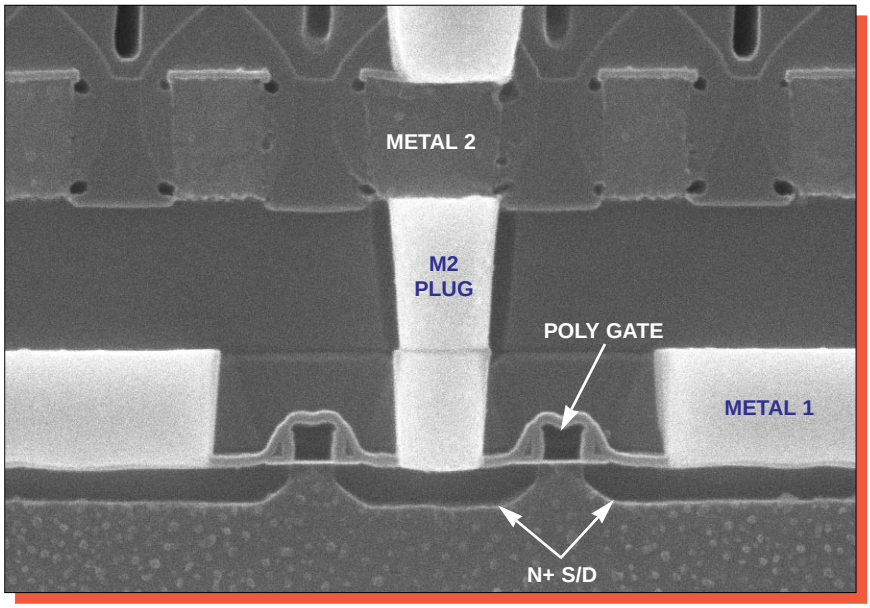


Mag. 26,000x

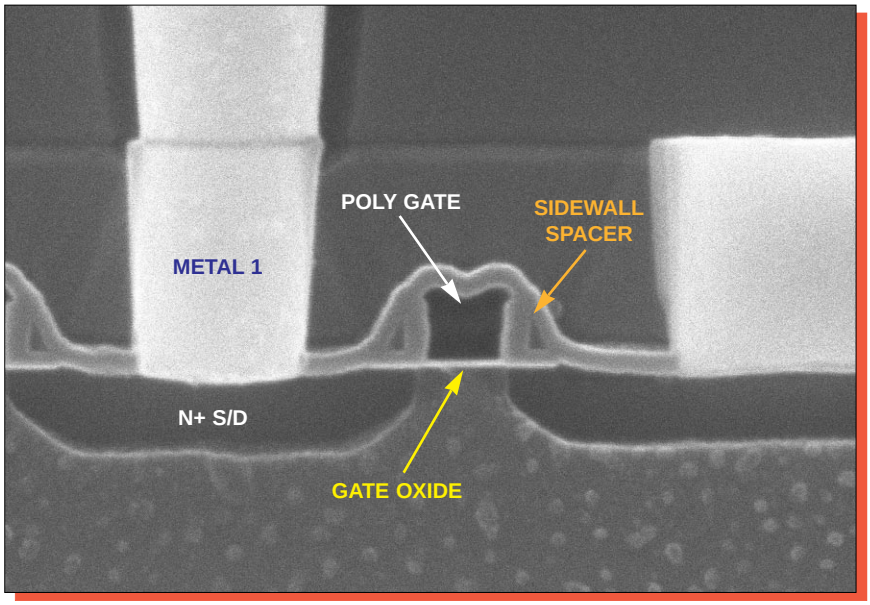


Mag. 52,000x

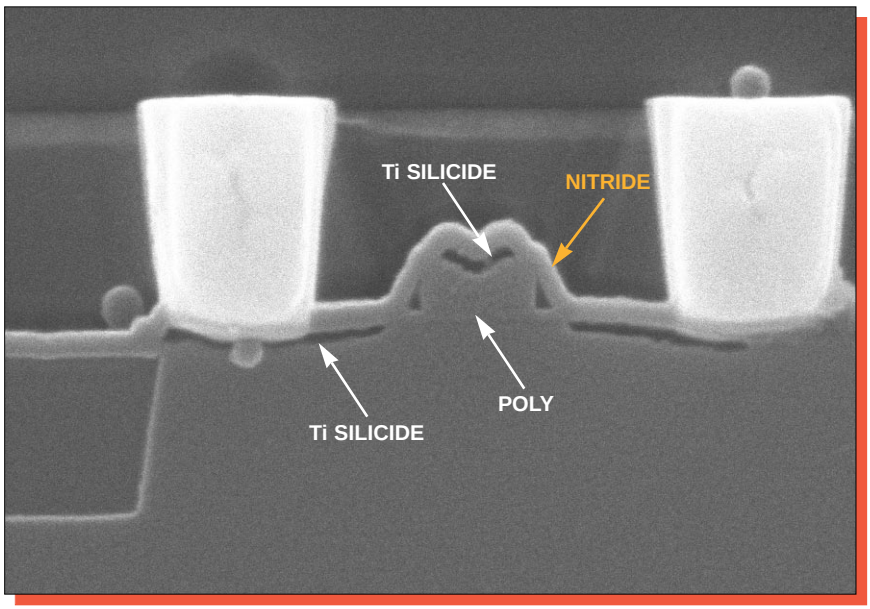
Figure 35. SEM section views of P-channel transistors.



Mag. 26,000x

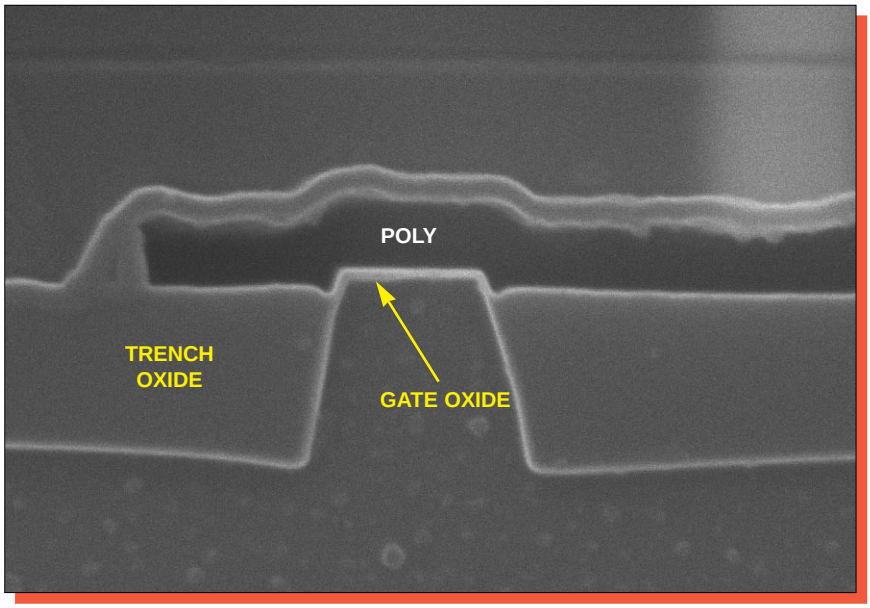


Mag. 52,000x

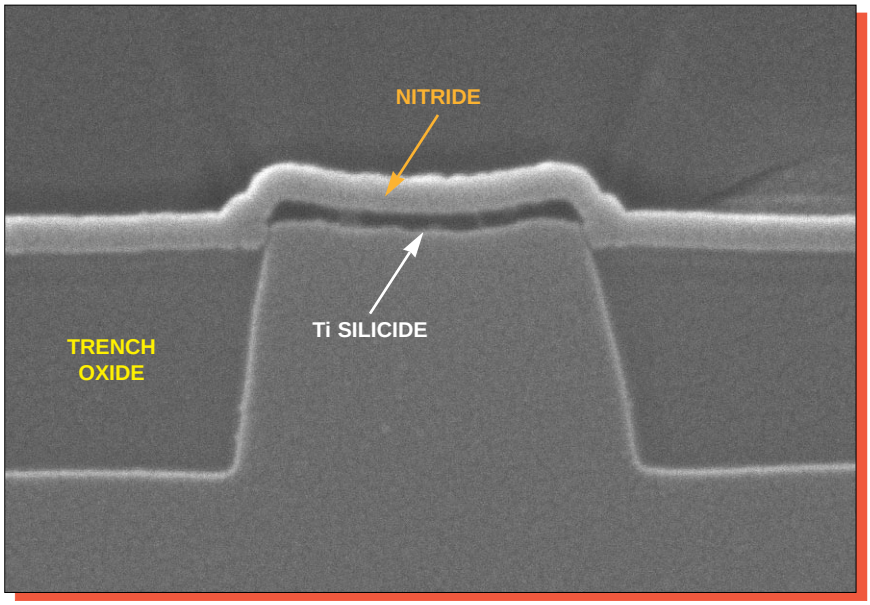


glass-etch,
Mag. 52,000x

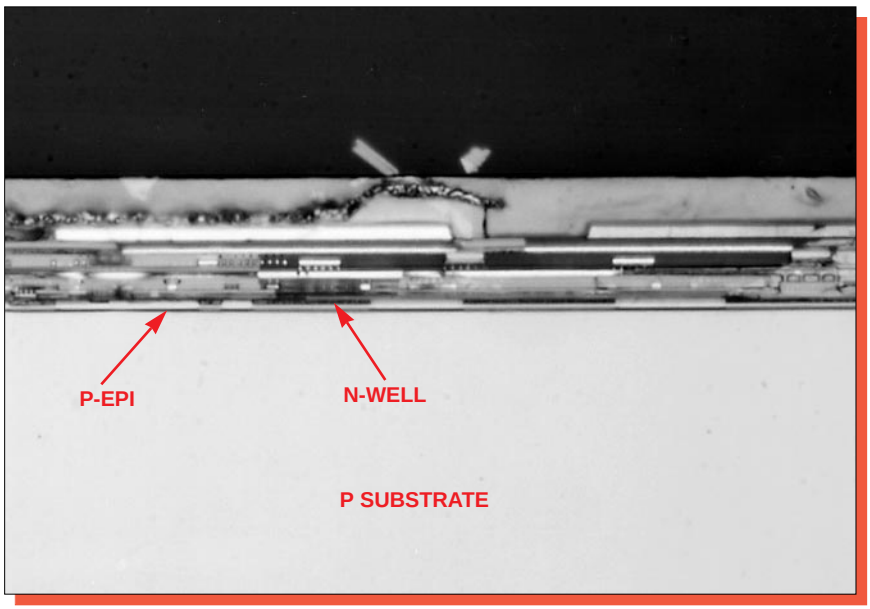
Figure 36. SEM section views of N-channel transistors.



Mag. 52,000x

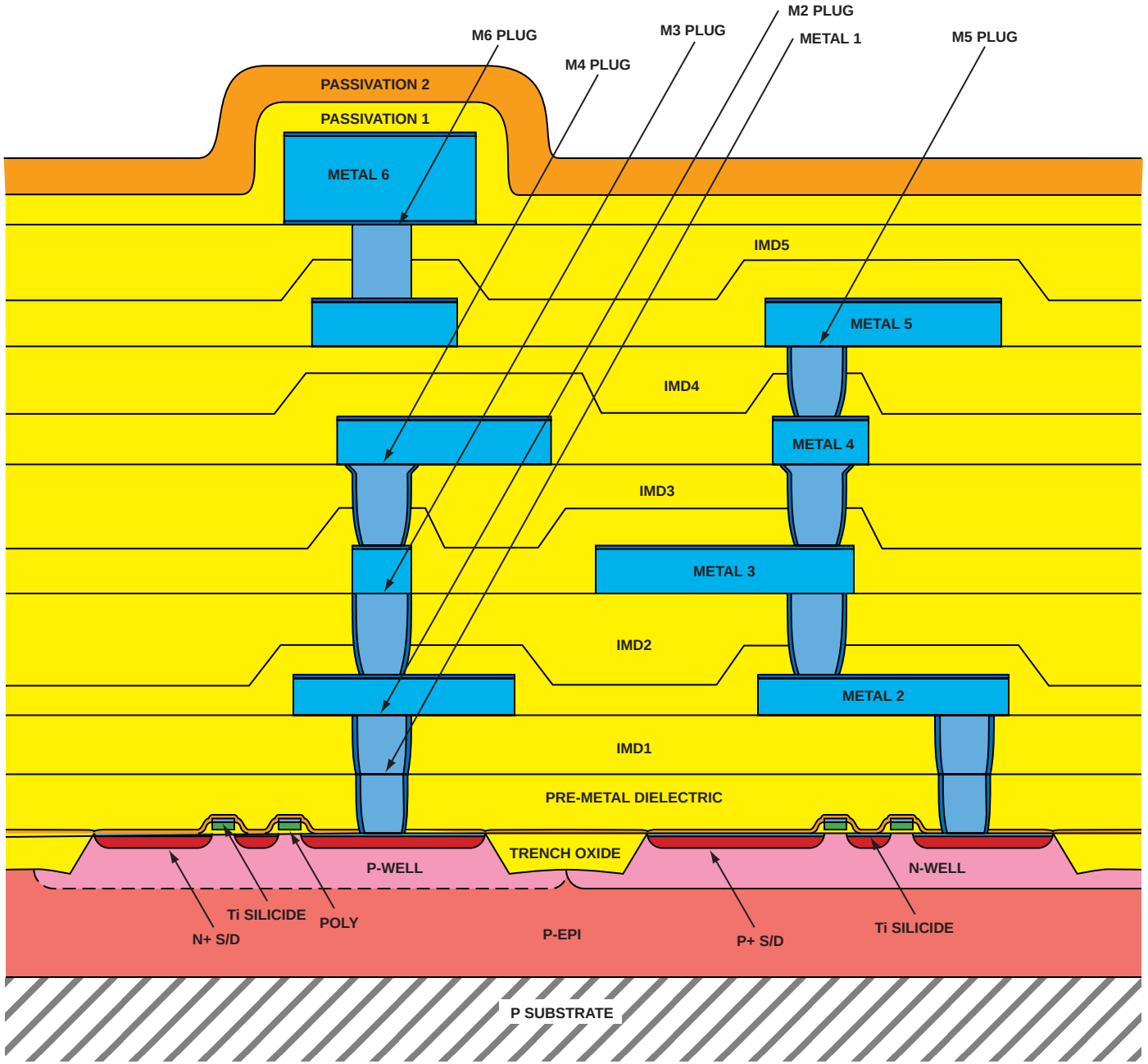


glass-etch,
Mag. 76,500x



Mag. 800x

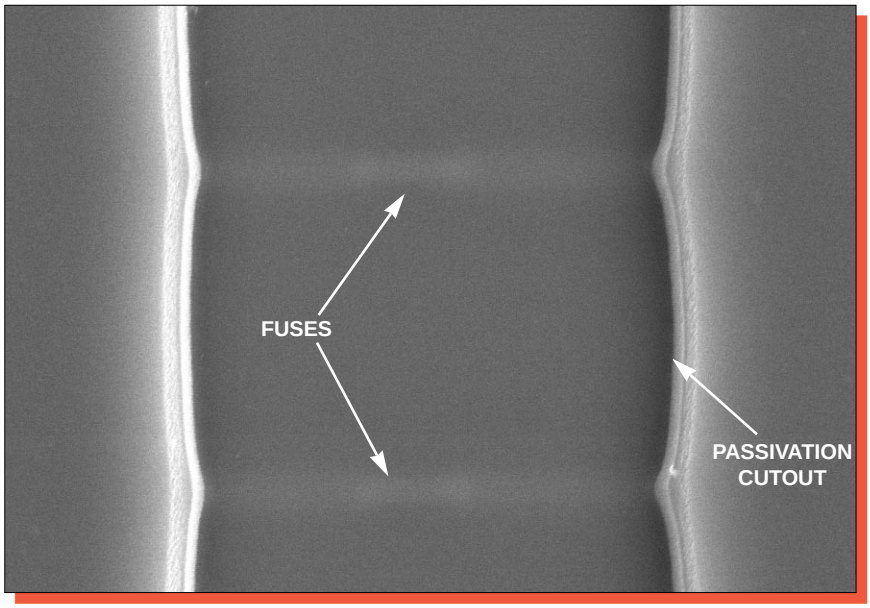
Figure 37. SEM section views of trench oxide and well structures.



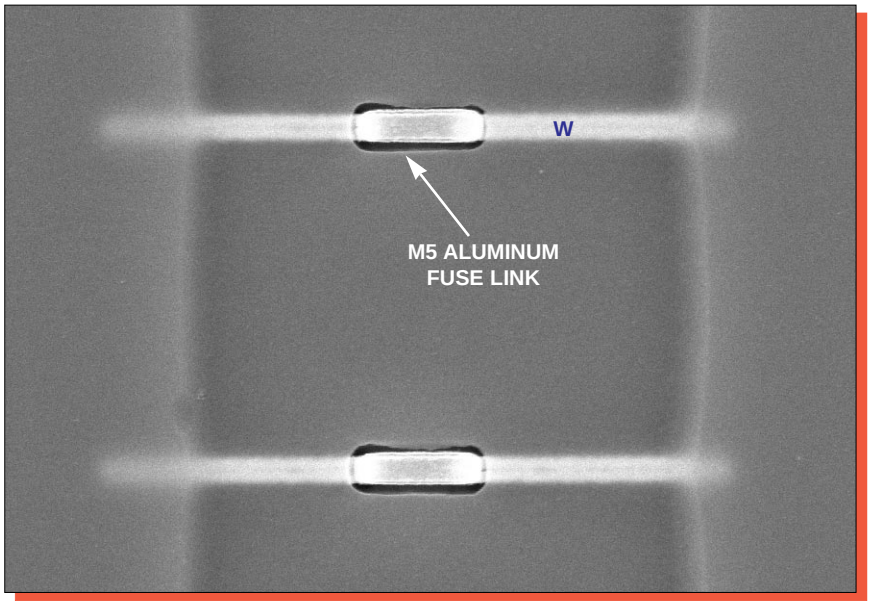
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

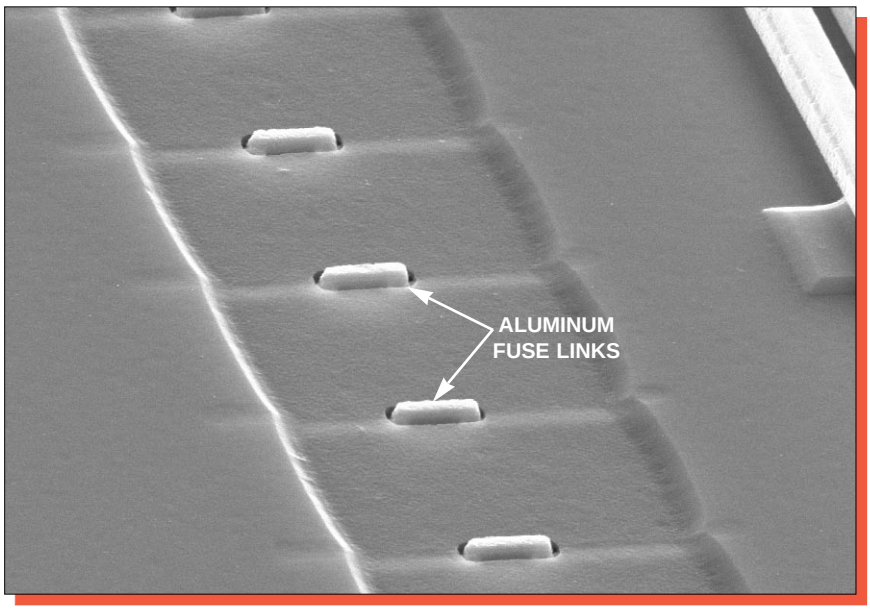
Figure 38. Color cross section drawing illustrating device structure.



intact,
Mag. 4400x, 0°

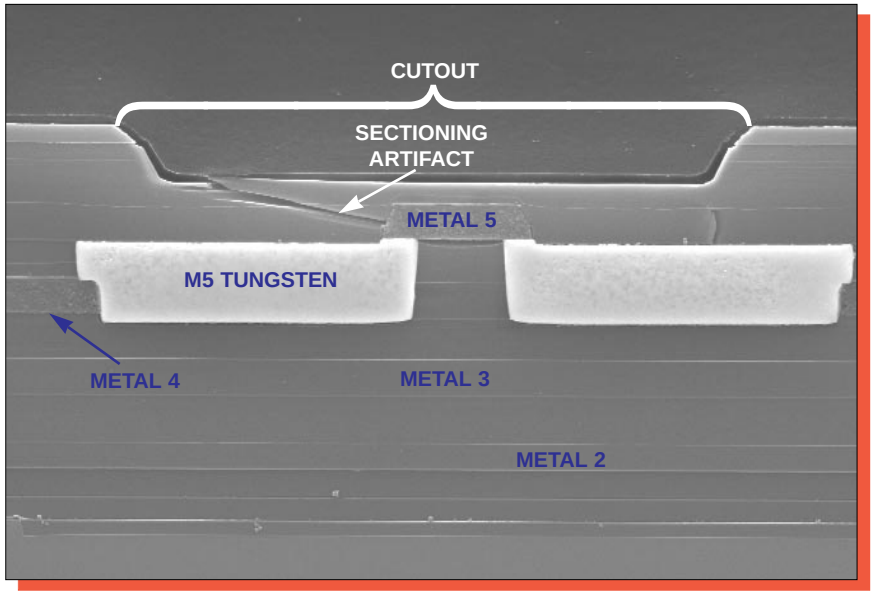


passivation removed,
Mag. 4400x, 0°

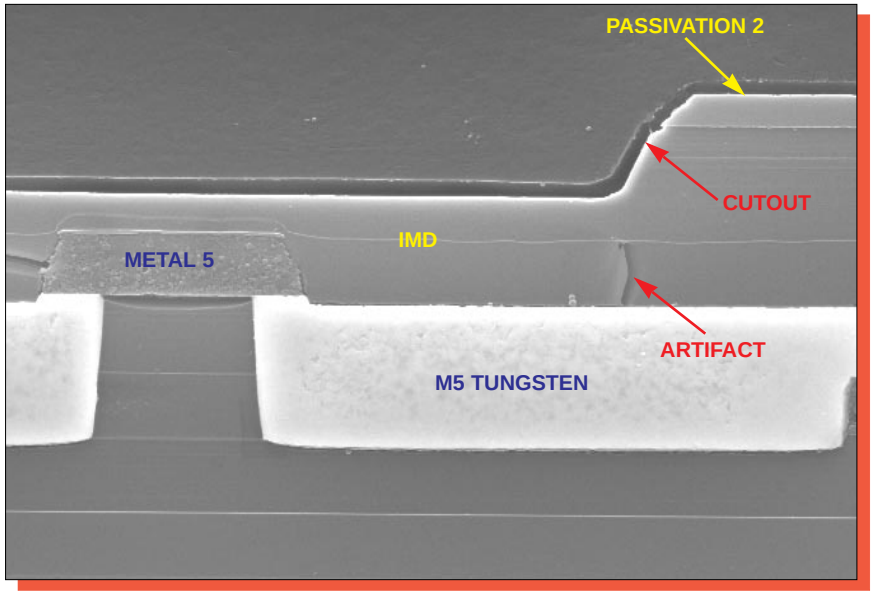


passivation removed,
Mag. 3400x, 60°

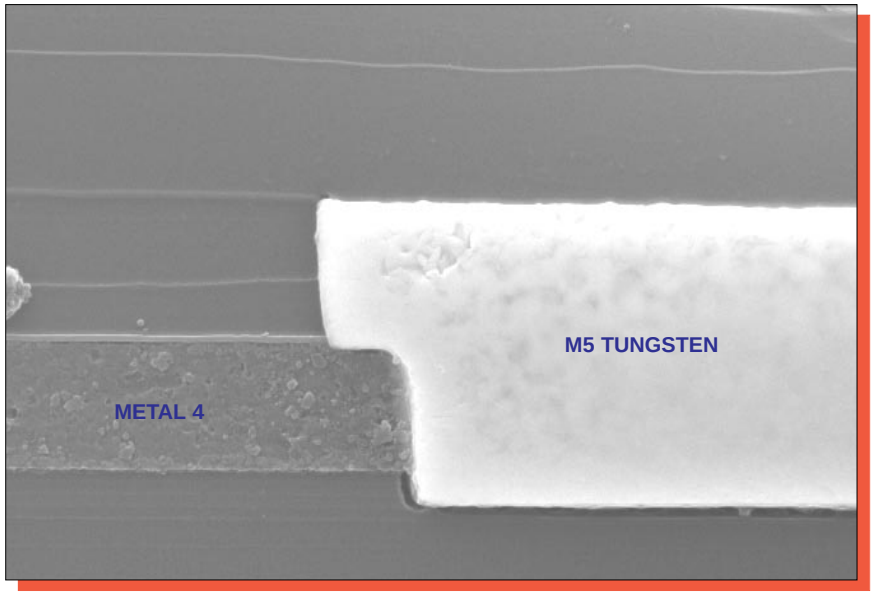
Figure 39. SEM views of typical fuses.



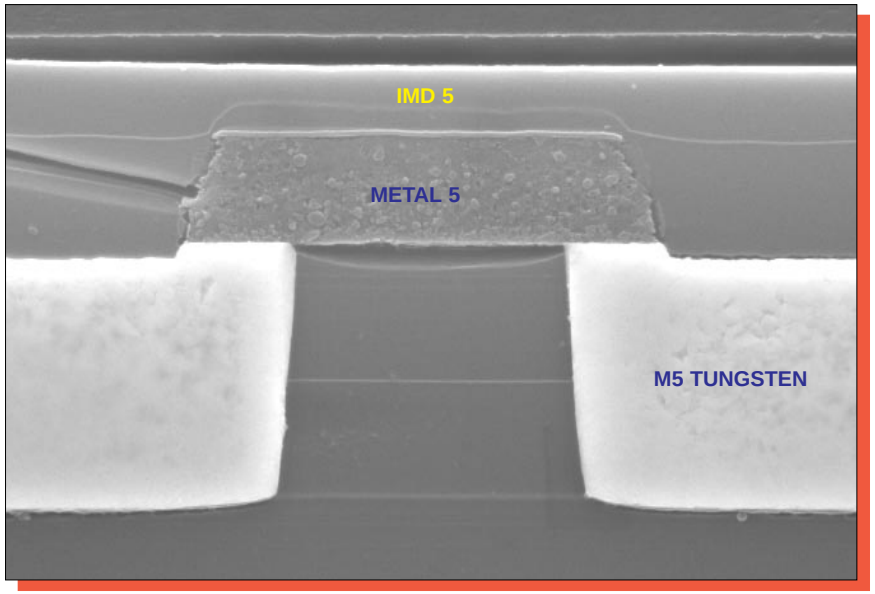
Mag. 5000x



Mag. 9000x



Mag. 19,000x



Mag. 16,000x

Figure 39a. SEM section views of a metal 5 fuse.

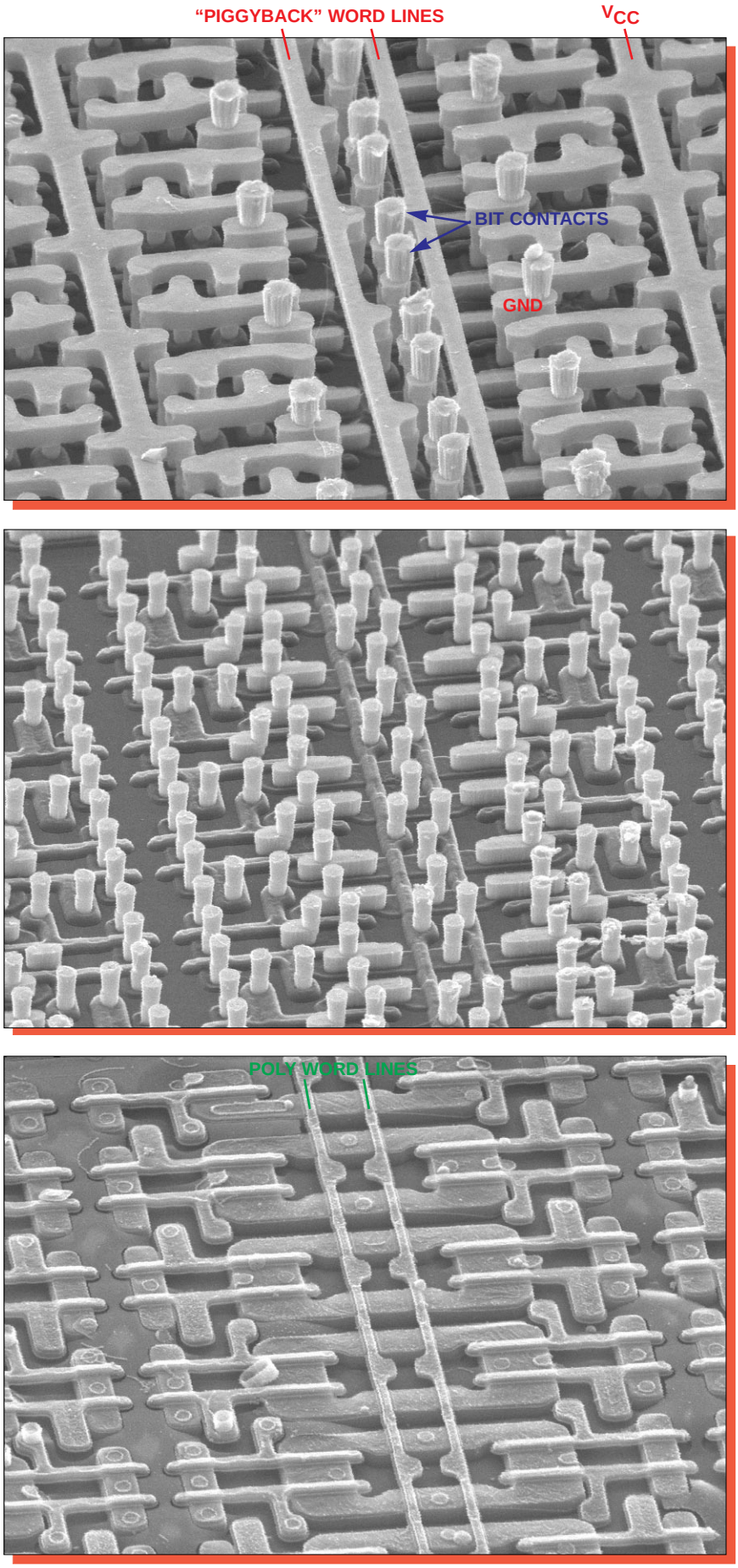
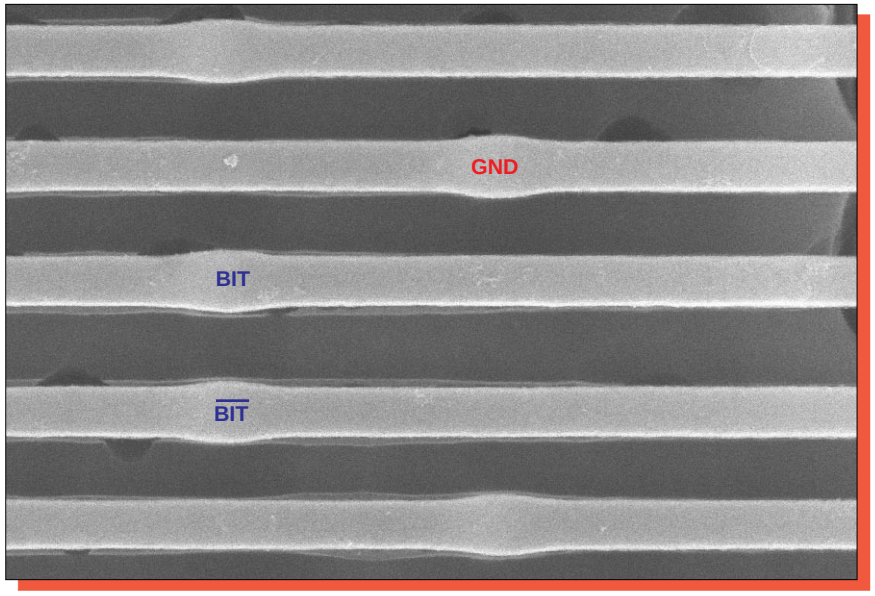
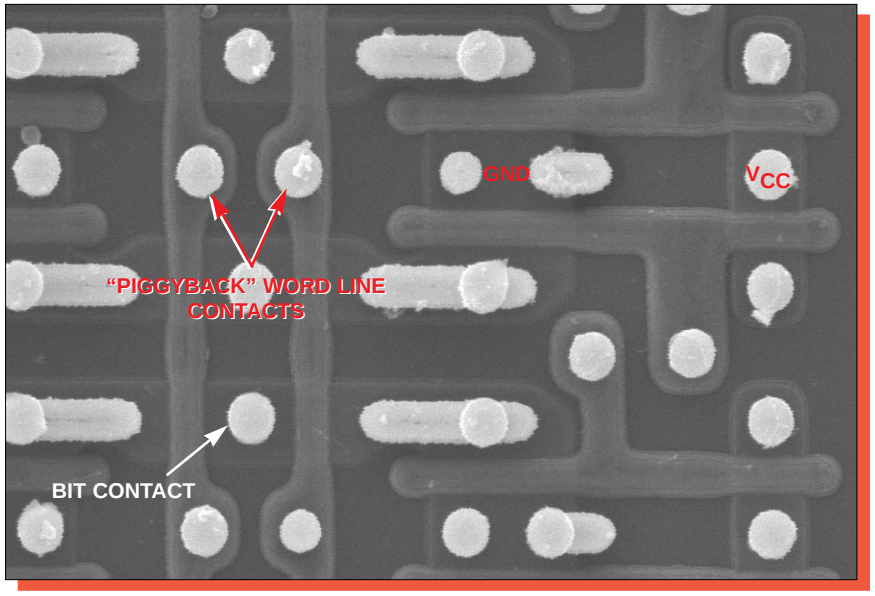


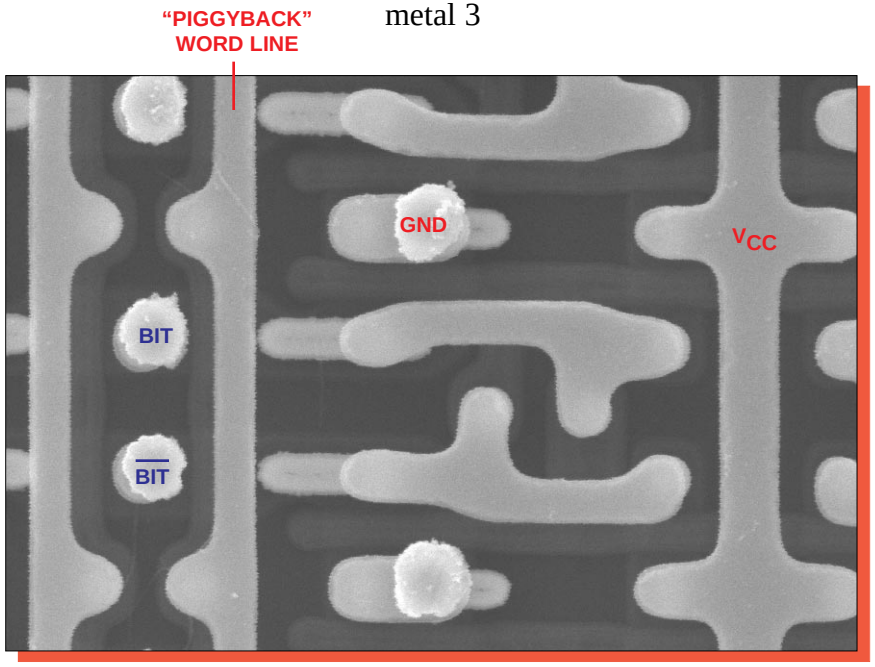
Figure 40. Perspective SEM views of SRAM cell array (Array A). Mag. 6500x, 55°.



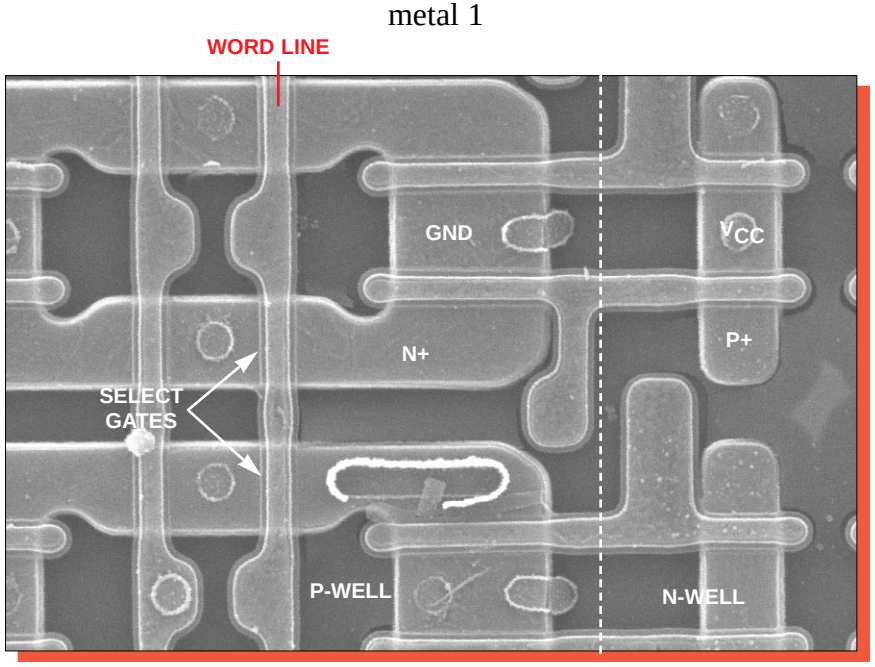
metal 3



metal 1

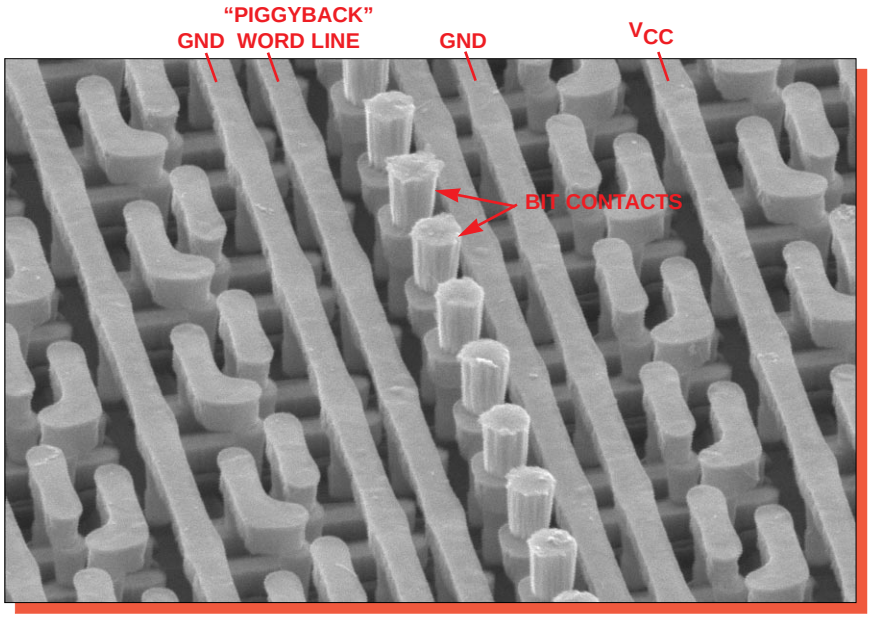


metal 2

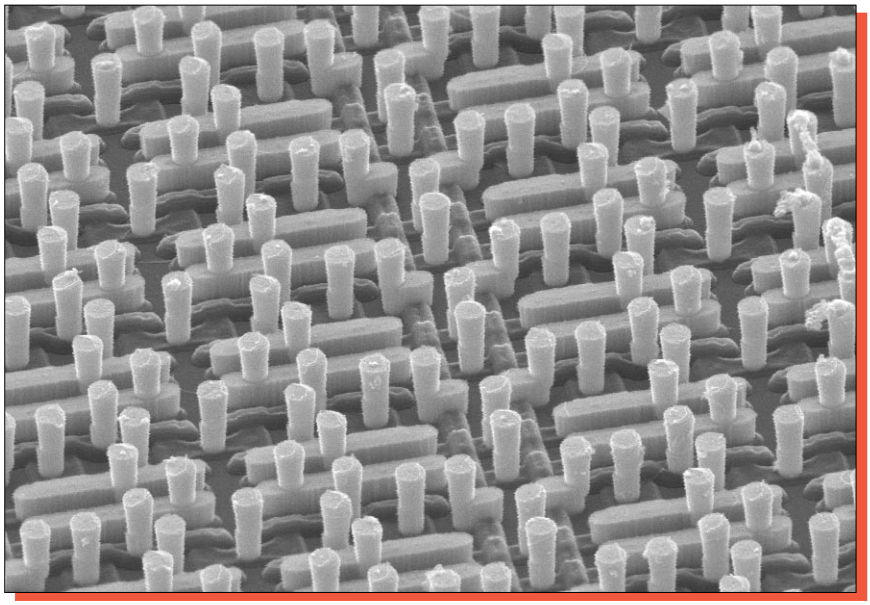


poly

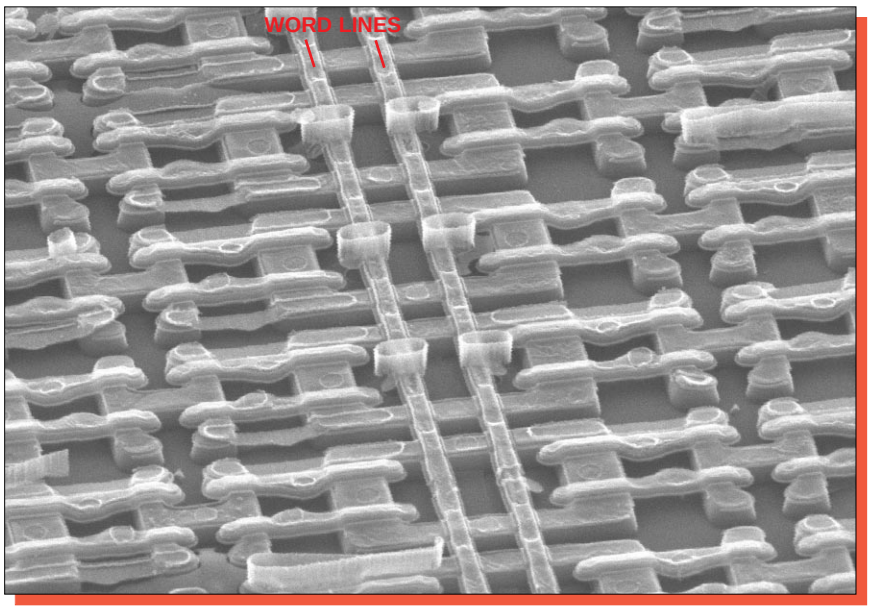
Figure 41. Topological detail SEM views of the SRAM cell (Array A). Mag. 12,000x, 0°.



metal 2

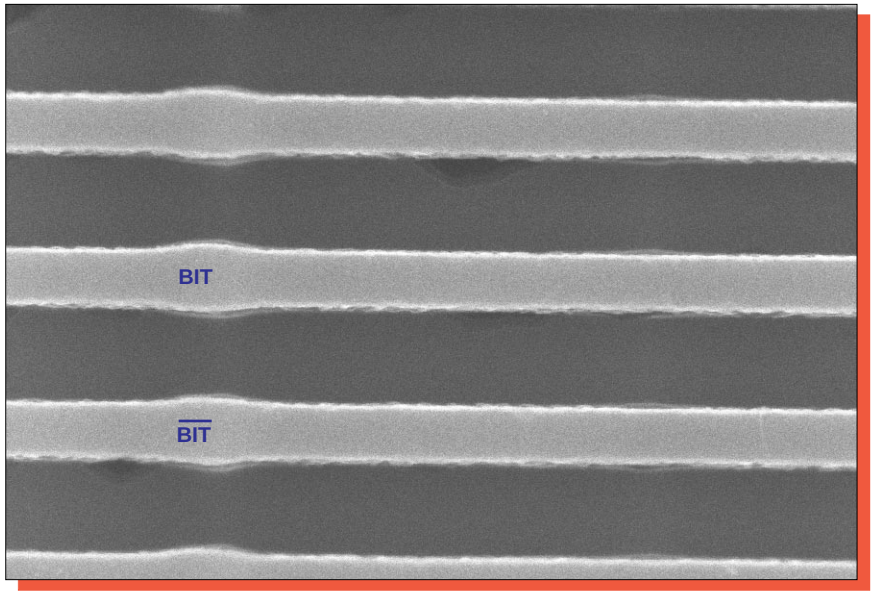


metal 1

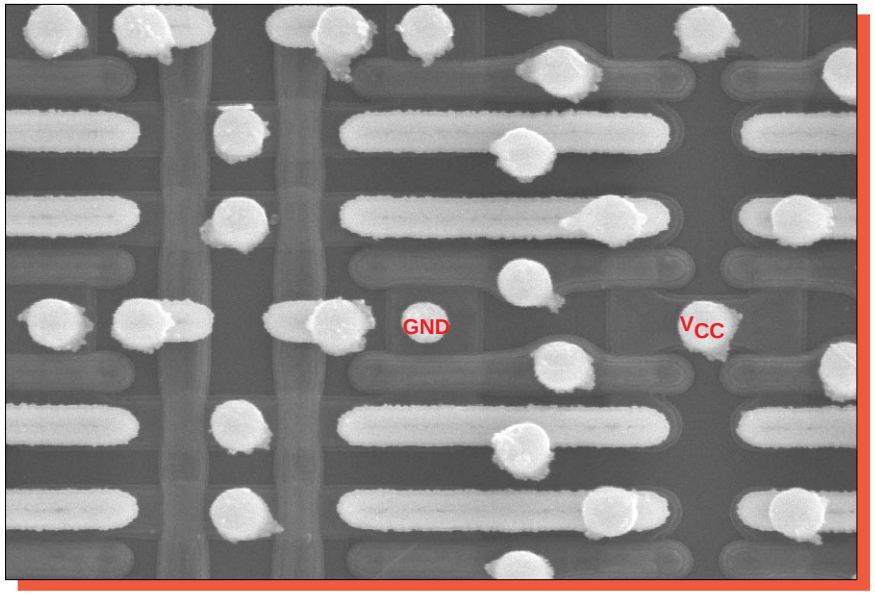


poly

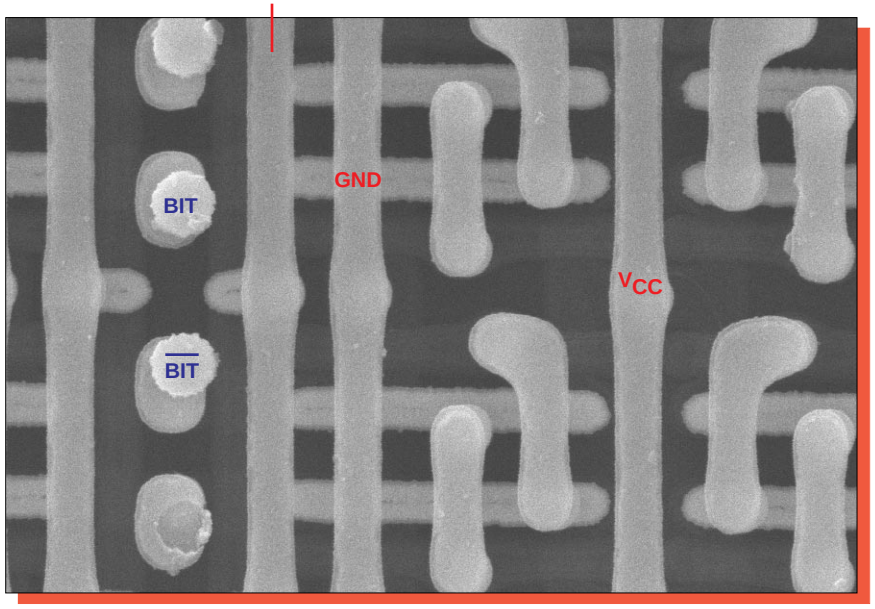
Figure 42. Perspective SEM views of SRAM cell (Array B). Mag. 8000x, 55°.



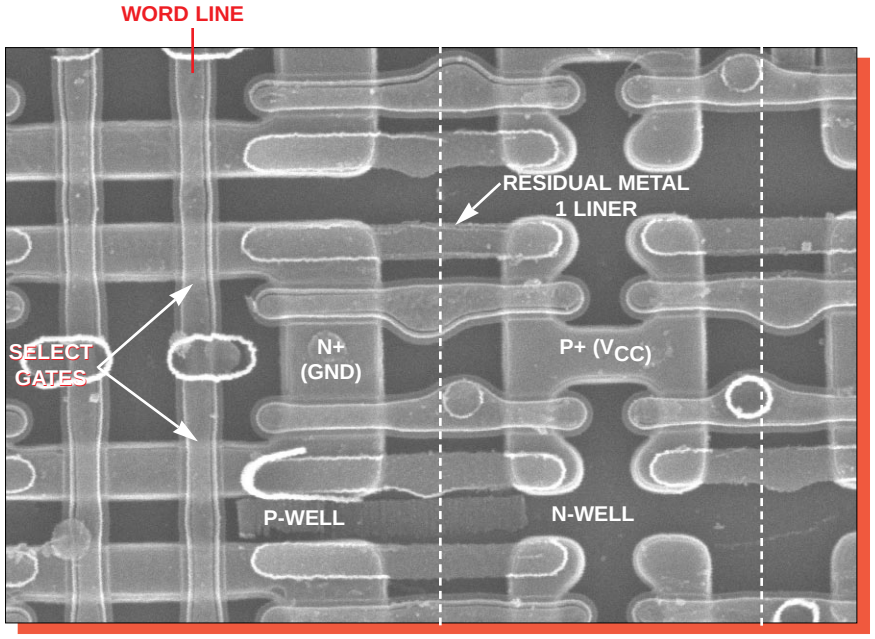
metal 3



metal 1



metal 2



poly

Figure 43. Topological detail views of the SRAM cell (Array B). Mag. 13,000x, 0°.