Construction Analysis

PLX Technology
PCI 9080 I/O Accelerator

Report Number: SCA 9710-558

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the PLX Technology PCI 9080 I/O Accelerator. Five devices were supplied for the analysis which were packaged in 208-pin Plastic Quad Flat Packs (PQFPs).

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Three metal, CMOS process employing twin-wells on a P-substrate.
- Sub-micron gate lengths (0.45 micron).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 208-pin Plastic Quad Flat Packs (PQFPs).
- Copper (Cu) gull-wing leadframe tinned with tin-lead (SnPb) solder.
- Dimpled paddle for added package strength were used on Samples 2 and 3 only.
- Header was constructed of copper (Cu) and internally plated with silver (Ag).
- Lead-locking provisions (anchors) at all pins.
- Thermosonic ball bond method employing 1.2 mil O.D. gold wire.
- Sawn dicing (full depth).
- Silver-epoxy die attach.

Die Process

- Fabrication process: Selective oxidation CMOS process employing twin-wells, on a P-substrate.
- Overlay passivation: A layer of nitride over a thin layer of silicon dioxide.
- Metallization: Three levels of metal defined by standard dry-etch techniques. All levels consisted of aluminum with titanium-nitride caps and barriers. All metal levels utilized tungsten plugs for vias and contacts. Metal 1 used an adhesion layer under the metal layer.

TECHNOLOGY DESCRIPTION (continued)

- Intermetal dielectrics (IMD2 and IMD1): Both interlevel dielectrics consisted of multiple layers of deposited glass with a spin-on-glass (SOG) in between to aid in planarization. The SOG layers had been subjected to an etchback.

- Pre-metal glass: A single layer of reflow glass over a layer of densified oxide.

- Polysilicon: A single layer of dry-etched polycide (poly and tungsten-silicide). This layer was used to form all gates on the die.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing.

- Isolation: LOCOS (local oxide).

- Wells: Twin-wells were employed on a P substrate. A step was noted in the oxide at the well boundaries.

- Buried contacts: No buried (poly-to-diffusion) contacts were employed.

- No fuses were noted.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 8a**

Questionable Items:[1] None.

Special Features:

- Dimpled paddles for added package strength were used on Samples 2 and 3 only.

General Items:

- Devices were packaged in 208-pin Plastic Quad Flat Packs (PQFPs).

- Overall package quality: Normal. No defects were found on the external or internal portions of the packages. The leadframe was constructed of copper (Cu). Pins were plated externally with tin-lead (SnPb). External pins were well formed and tinning of the leads was complete. No gaps were noted at lead exits. The paddle was plated with silver (Ag). Dimpled paddles were used with Samples 2 and 3 for added package strength.

- Wirebonding: Thermosonic ball bond method using 1.2 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 10). Wire spacing and placement was also good; intermetallic formation was complete. All three metal levels formed the bond pad structure.

- Die attach: Silver-epoxy of normal quantity and quality.

- Die dicing: Die separation was by sawing (100 percent) and showed normal quality workmanship. No large chips or cracks were present at the die surface.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process and Design: **Figures 9 - 31**

Questionable Items:[1] None.

Special Features:

- Sub-micron gate lengths (0.45 micron N-channel).

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P substrate.

- Design and layout: Die layout was clean and efficient. Alignment was good at all levels.

- Die surface defects: None. No contamination, toolmarks or processing defects were noted.

- Overlay passivation: A layer of nitride over a layer of silicon-dioxide. Overlay integrity tests indicated defect-free passivation. Edge seal was good.

- Metallization: All levels consisted of aluminum with titanium-nitride caps and barriers. All metal levels utilized tungsten plugs for vias and contacts. Metal 1 used an adhesion layer under the metal layer.

- Metal patterning: All metal layers were defined by a dry etch of good quality.

- Metal defects: None. No voiding, notching, or neckdown of the metal layers was found. No silicon nodules were observed following removal of the metal layers.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Intermetal dielectrics (IMD2 and IMD1): Both interlevel dielectrics consisted of multiple layers of deposited glass with a spin-on-glass (SOG) in between to aid in planarization. The SOG layers had been subjected to an etchback. No problems were found with the dielectric layers.

- Contacts: Via and contact cuts appeared to be defined by a dry-etch process. No significant over-etching was found. Contact cuts were sloped significantly at all levels to aid in metal coverage.

- Pre-metal glass: A single layer of reflow glass over a layer of densified oxide. No problems were found.

- Polysilicon: A single layer of dry-etched polycide (poly and tungsten-silicide). This layer was used to form all gates on the die. Definition and coverage was good.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. An LDD process was used employing oxide sidewall spacers. The spacers were left in place. Diffusions were not silicided. No problems were found in these areas.

- Wells: Twin-wells on a P substrate. Definition was normal.

- Buried contacts: Direct poly-to-diffusion (buried) contacts were not used.

Special Items:

- ESD sensitivity: ESD results will be supplied as soon as possible.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Package section and material analysis

Decapsulation

Internal optical inspection

SEM inspection of assembly features and passivation

Passivation integrity test

Wirepull test

Passivation removal and inspect metal 3

Delayer to metal 2 and inspect

Delayer to metal 1 and inspect

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	G
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	N
Contact coverage	G
Contact registration	G
Contact defects	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

	Top	Bottom
Samples 1, 4, 5	(PLX LOGO) TECHNOLOGY PCI9080 REV.2 29-1997 T2B B62223.5	Taiwan B62223.5
Samples 2, 3	(PLX LOGO) TECHNOLOGY PCI9080 REV.2 25-1997 T2B B62223.1	22 Taiwan

WIREBOND STRENGTH

Wire material: 1.2 mil diameter gold

Die pad material: aluminum

Material at package post: silver

Sample # **1**

# of wires tested:	62	
Bond lifts:	0	
Force to break - high:	10 g	
- low:	5 g	
- avg.:		5.7 g
- std. dev.:	1.1	

DIE MATERIAL ANALYSIS

Passivation: *	A layer of nitride over a layer of silicon-dioxide.
Metal 3:	Aluminum.
Intermetal dielectrics (IMD2 and IMD1):	Multiple layers of silicon-dioxide with a filler glass (SOG) in between.
Metal 2:	Aluminum with a titanium-nitride barrier.
Metal 1:	Aluminum with a titanium-nitride barrier.
Pre-metal glass: *	A single layer of glass over a layer of densified oxide.
Polycide:	Tungsten-silicide on polysilicon.
Plugs:	Tungsten.

** WDX analysis results will be supplied as soon as possible.*

PACKAGE MATERIAL ANALYSIS

Leadframe:	Copper (Cu)
Internal plating:	Silver (Ag)
External plating:	Tin-solder (SnPb)
Die attach:	Silver-epoxy (Ag)

HORIZONTAL DIMENSIONS

Die size:	5.9 x 5.9 mm (234 x 234 mils)
Die area:	34.8 mm^2 (54,756 $mils^2$)
Min pad size:	0.08 x 0.08 mm (3.3 x 3.3 mils)
Min pad window:	0.07 x 0.07 mm (3 x 3 mils)
Min pad space:	7.6 microns
Min metal 3 width:	0.8 micron
Min metal 3 space:	0.8 micron
Min metal 3 pitch:	1.6 micron
Min via (M3 - M2):	0.7 micron (round)
Min metal 2 width:	0.6 micron
Min metal 2 space:	0.8 micron
Min metal 2 pitch:	1.4 micron
Min via (M2 - M1):	0.8 micron (round)
Min metal 1 width:	0.6 micron
Min metal 1 space:	0.75 micron
Min metal 1 pitch:	1.35 micron
Min contact:	0.55 micron (round)
Min polycide 1 width:	0.45 micron
Min polycide 1 space:	0.5 micron
Min gate length - (N-channel):	0.45 micron
- (P-channel):	0.65 micron

VERTICAL DIMENSIONS

Die thickness:		0.5 mm (19.5 mils)

Layers

Passivation 2:		0.6 micron
Passivation 1:		0.2 micron
Metallization 3	- cap:	0.05 micron (approximate)
	- aluminum:	0.85 micron
	- barrier:	0.1 micron
Intermetal dielectric 2 (IMD2)	- glass 4:	0.2 micron
	- glass 3 (SOG):	0 - 0.4 micron
	- glass 2:	0.4 micron
	- glass 1:	0.2 micron
Metallization 2	- cap:	0.15 micron
	- aluminum:	0.5 micron
	- barrier:	0.06 micron
Intermetal dielectric 1 (IMD 1)	- glass 4:	0.25 micron
	- glass 3 (SOG):	0 - 0.66 micron
	- glass 2:	0.5 micron
	- glass 1:	0.2 micron
Metallization 1	- cap:	0.15 micron
	- aluminum:	0.5 micron
	- barrier:	0.10 micron
Pre-metal glass:		0.6 micron
Polycide	- silicide:	0.1 micron
	- poly:	0.15 micron
Local oxide:		0.4 micron
N+ diffusion:		0.25 micron
P+ diffusion:		0.2 micron
N-well:		2.8 microns (approximate)

INDEX TO FIGURES

top view

bottom view

Figure 1. The PLX Technology PCI9080 package (Samples 1, 4, and 5). Mag. 2x.

top view

bottom view

Figure 2. The PLX Technology PCI9080 package (Samples 2 and 3). Mag. 2x.

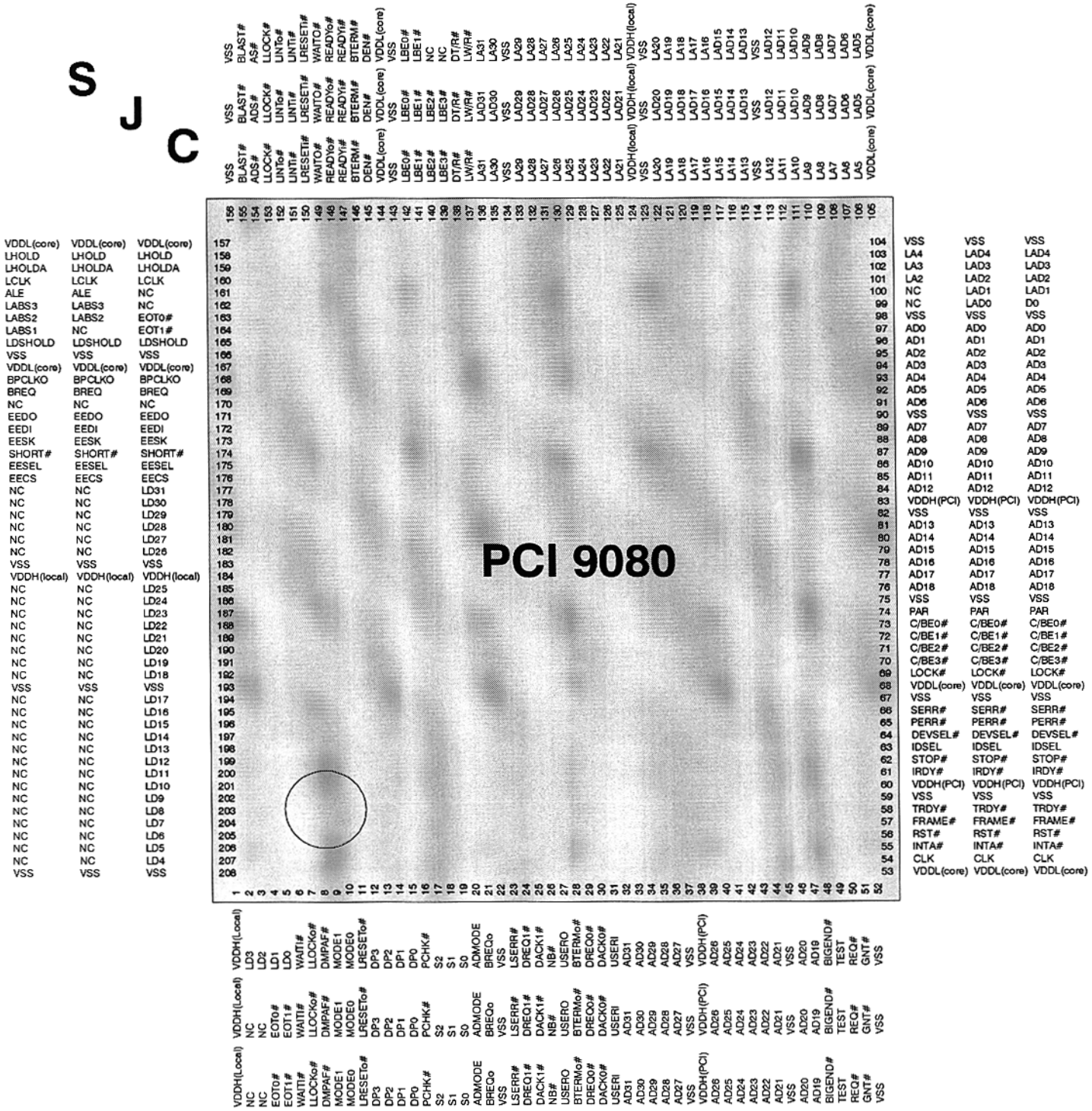
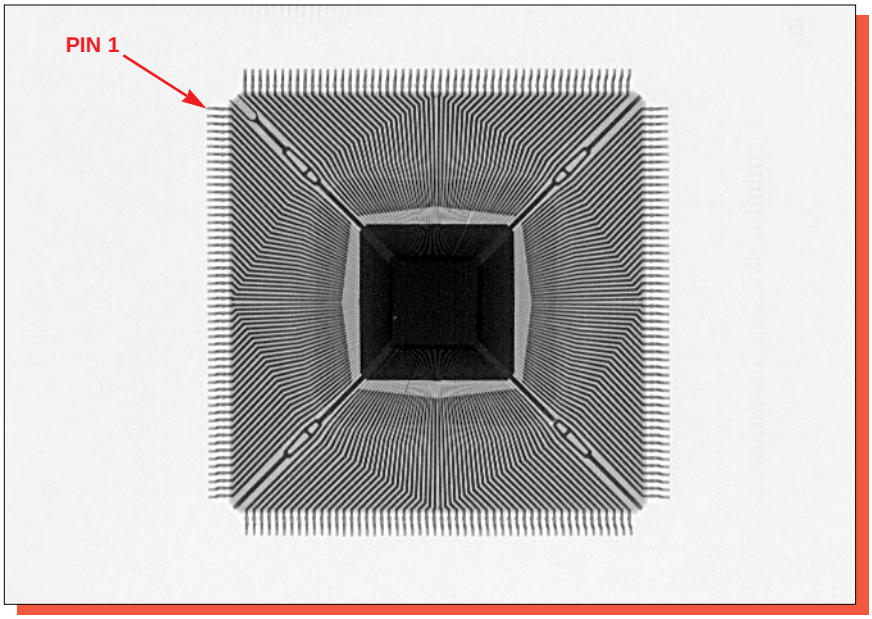
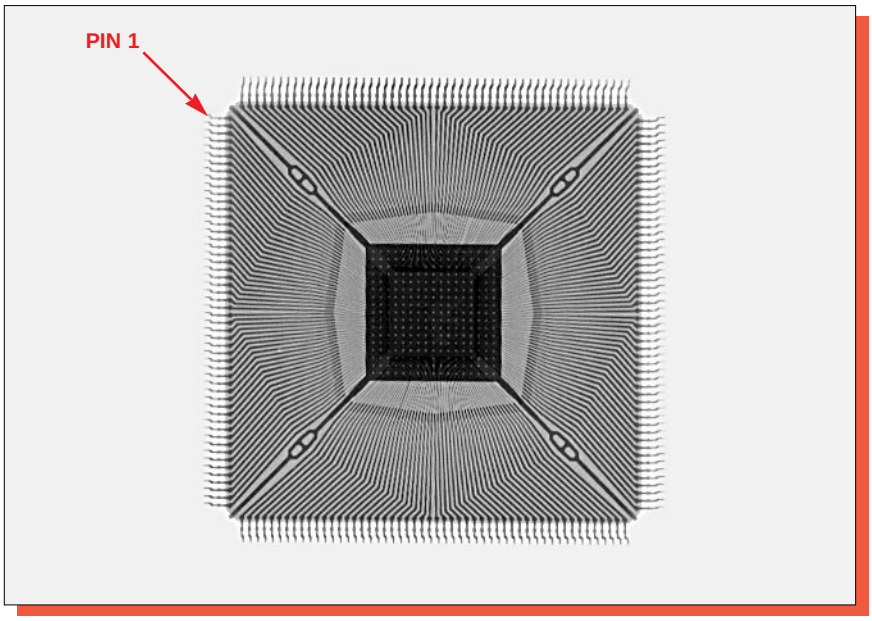


Figure 3. The PLX technology PCI 9080 pinout.

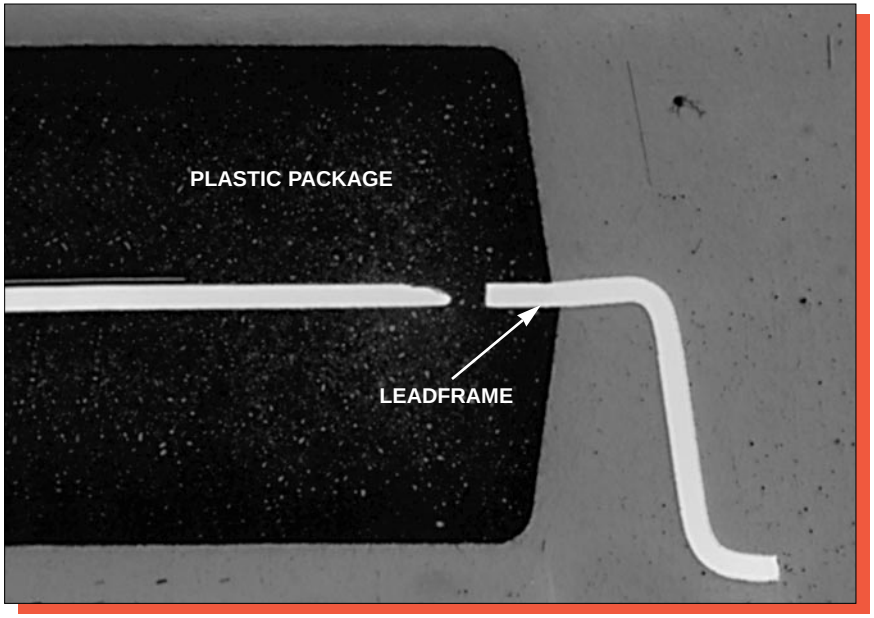


Samples 1, 4, and 5



Samples 2 and 3

Figure 4. X-ray views of the packages. Mag. 2x.



Sample 1

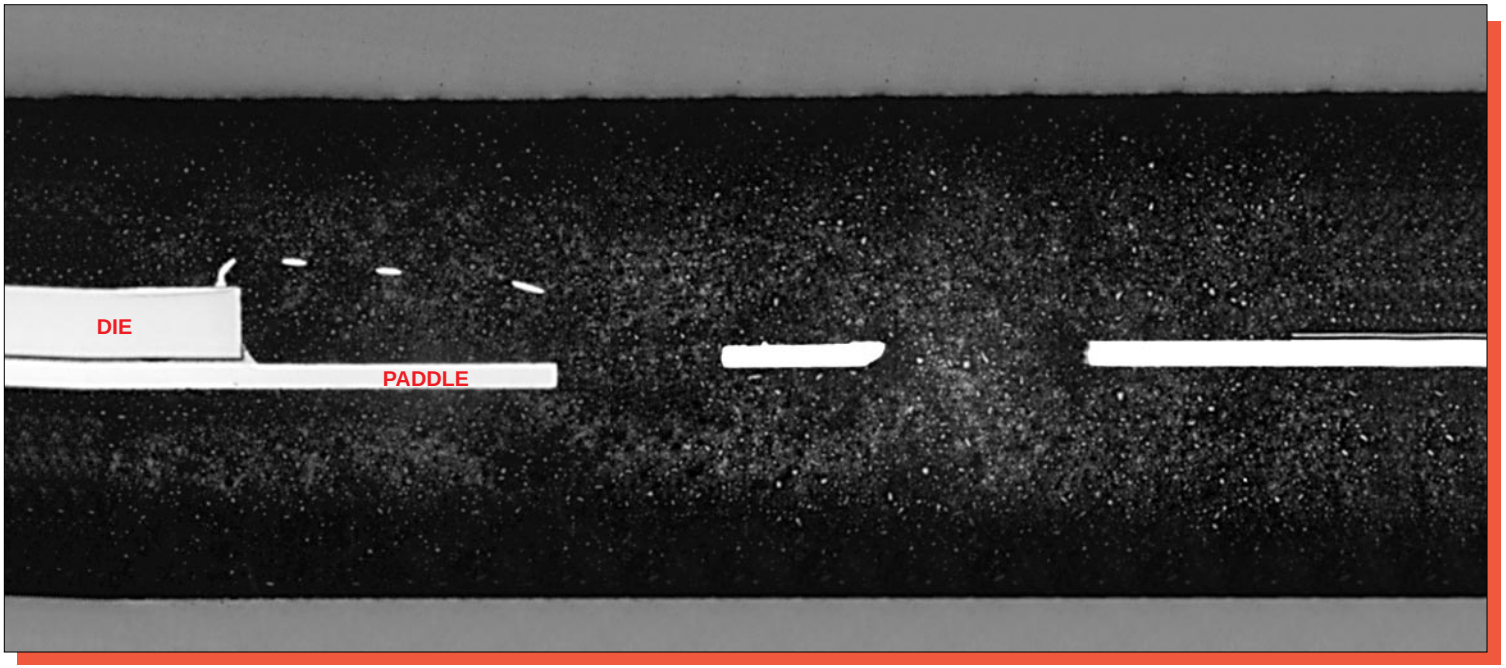
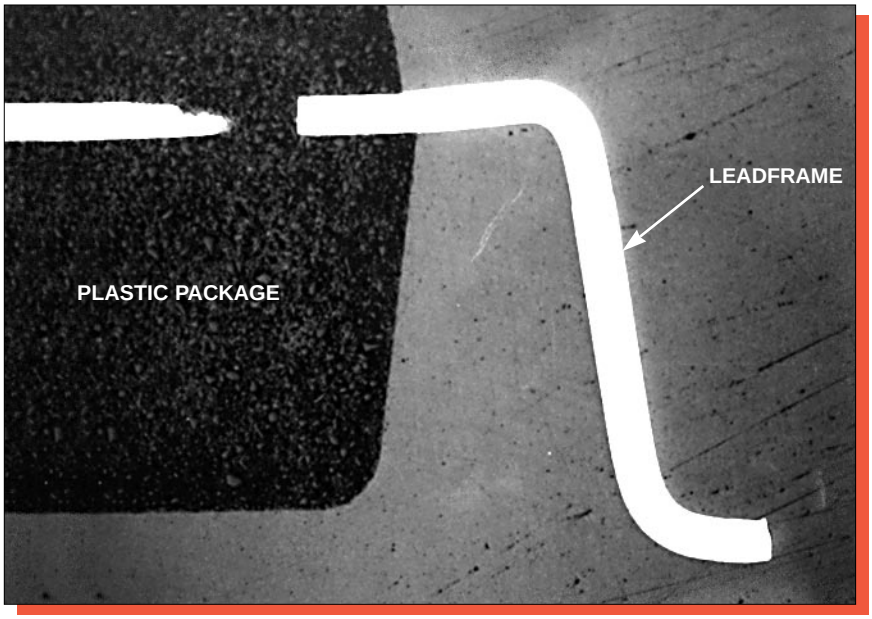
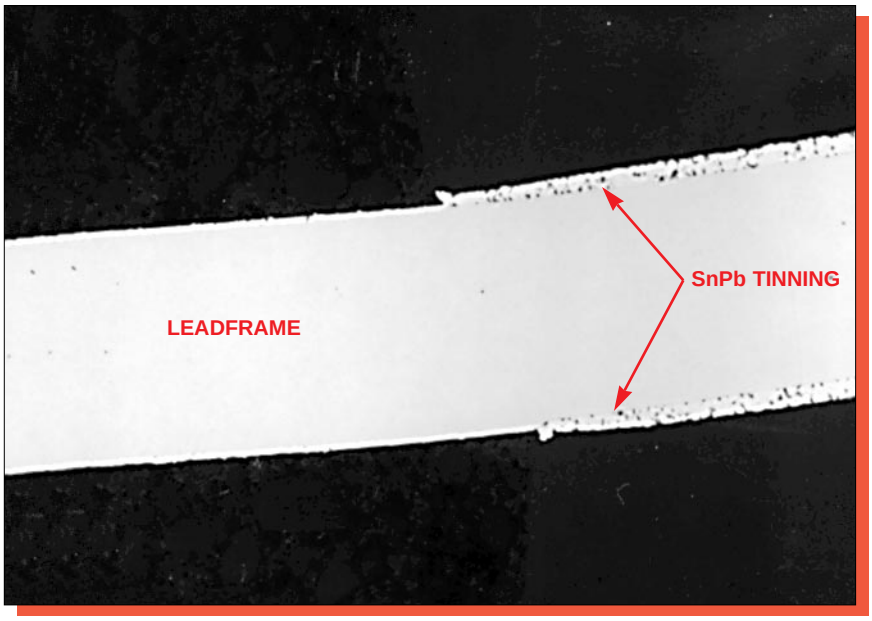


Figure 4a. Optical views of the PLX Technology package illustrating general construction. Mag. 20x.

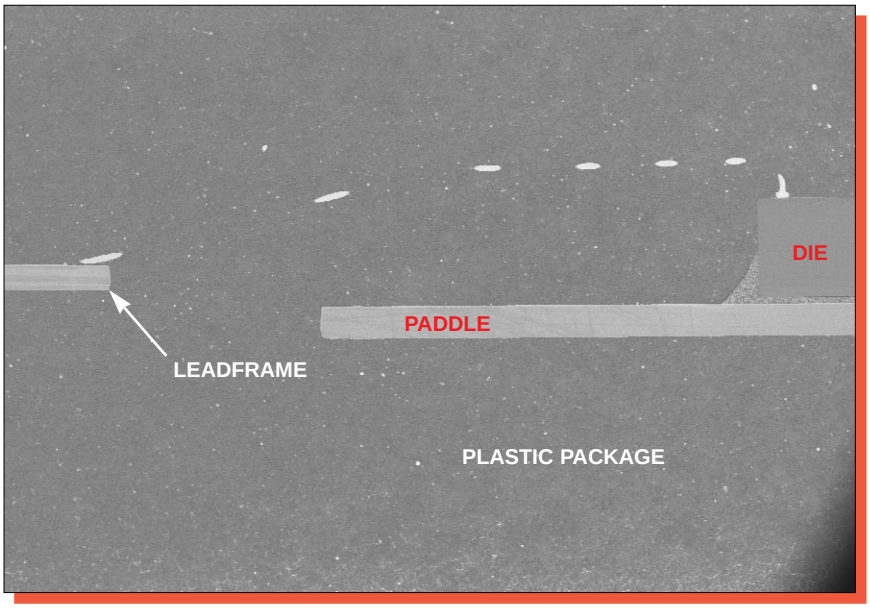


Mag. 32x

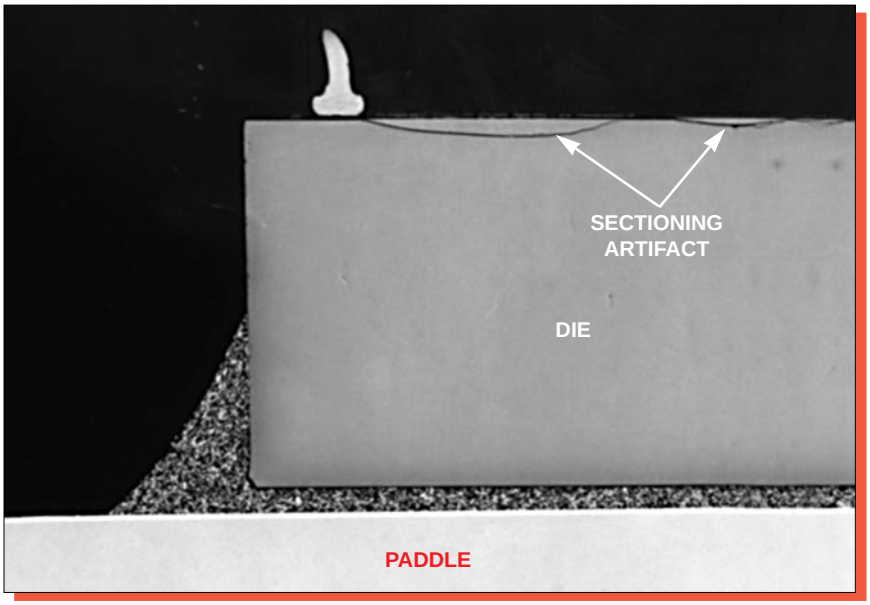


Mag. 200x

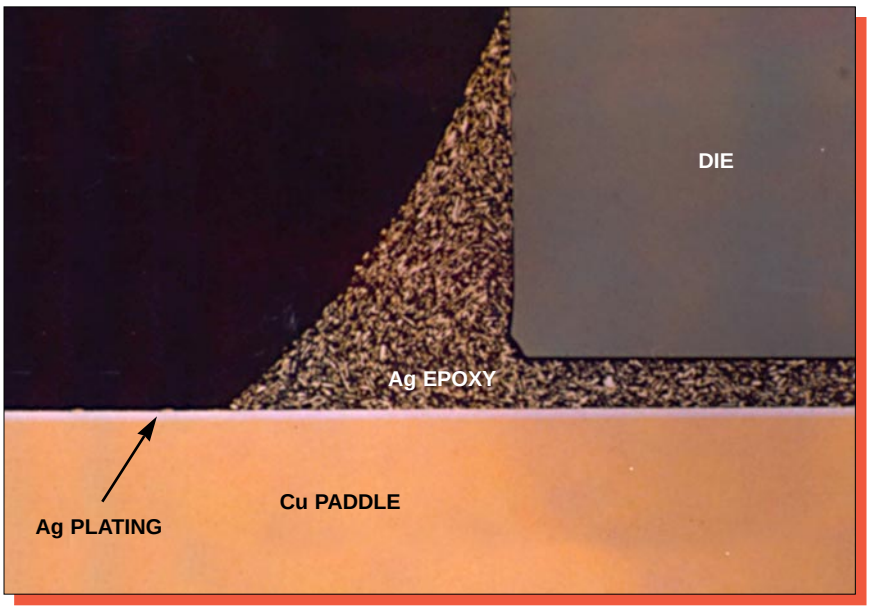
Figure 5. Optical views of lead forming and lead exit.



Mag. 25x

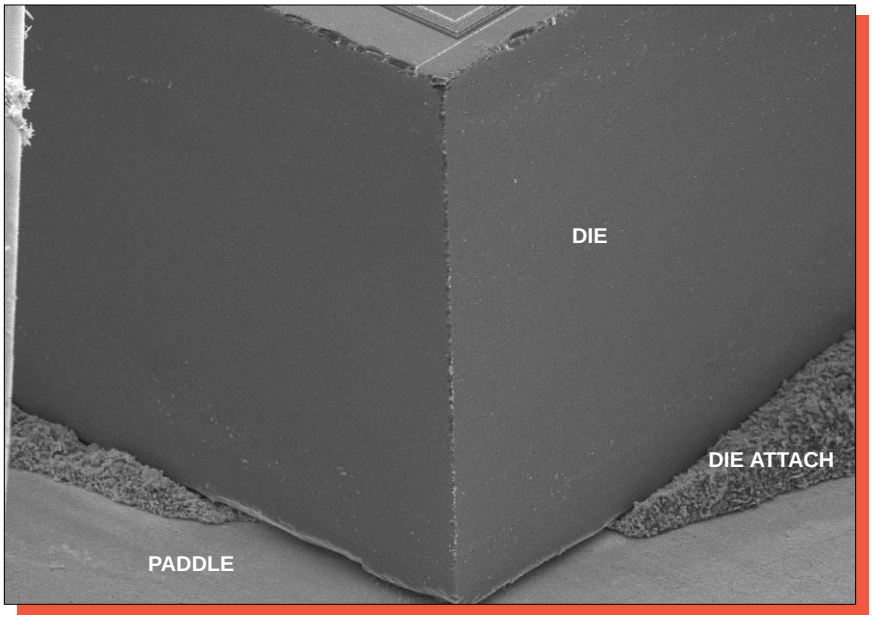


Mag. 100x

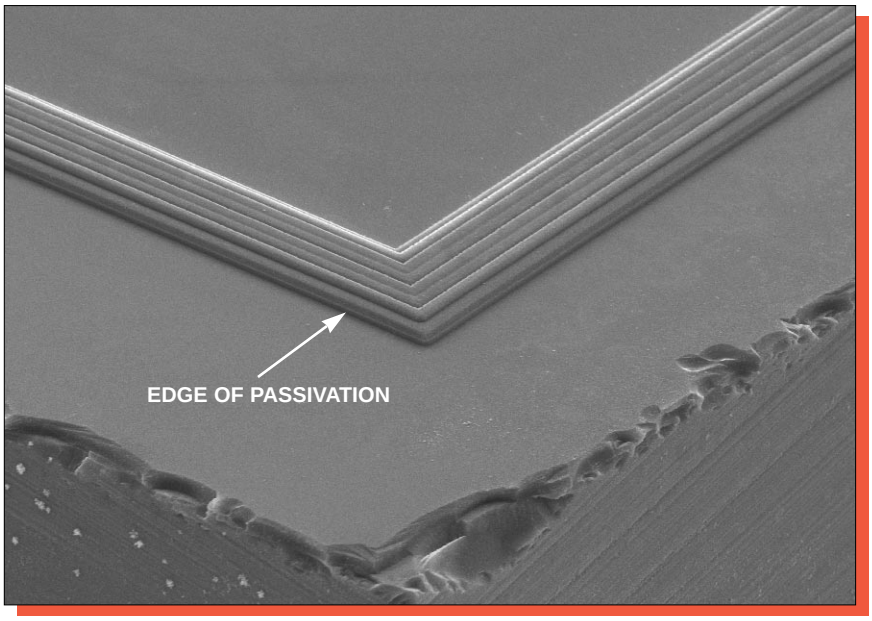


Mag. 200x

Figure 6. Optical views of dicing and die attach.

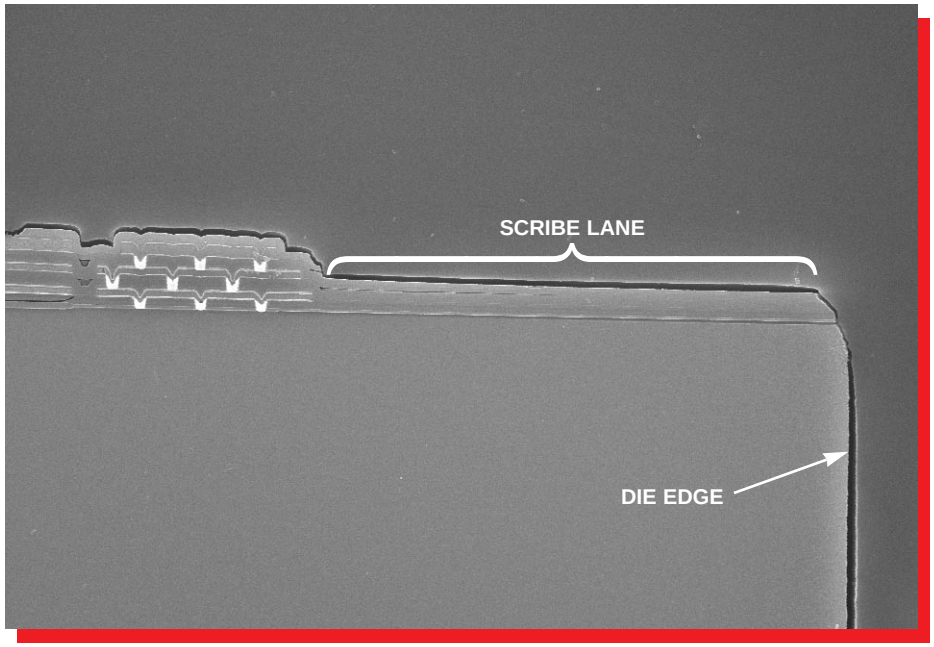


Mag. 170x

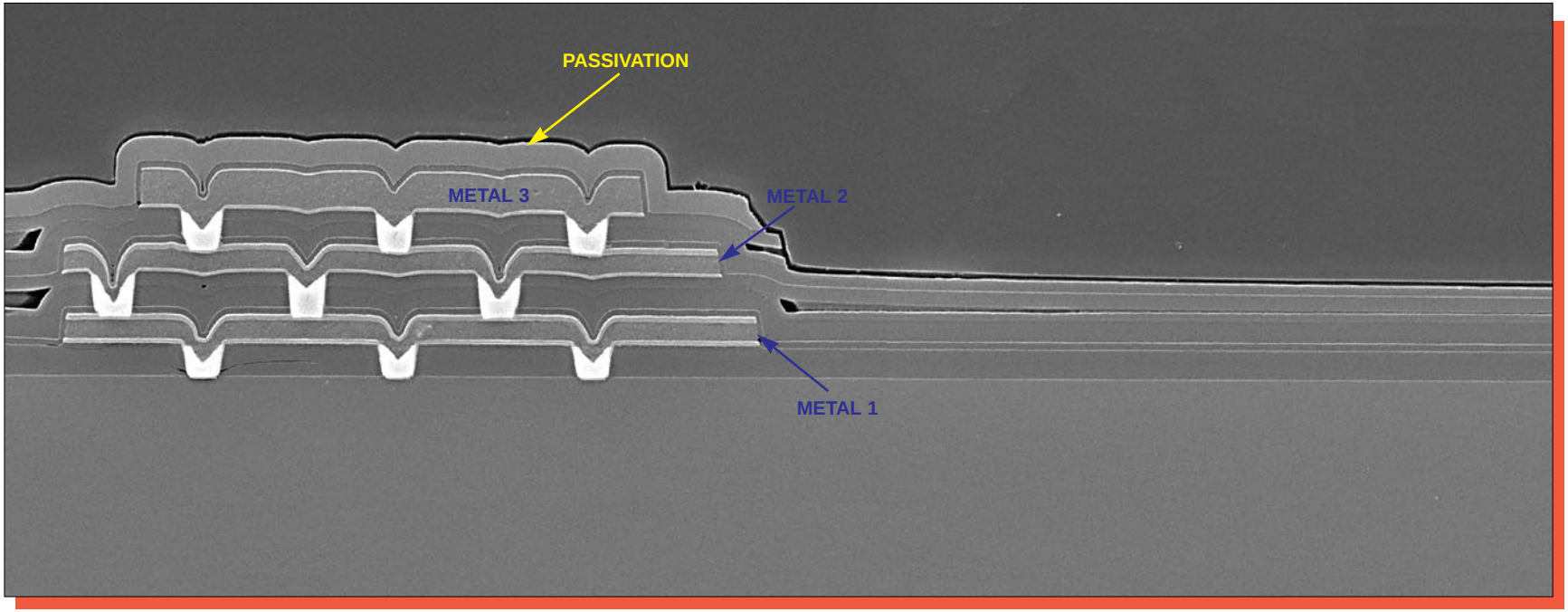


Mag. 900x

Figure 7. SEM views of die corner and edge seal. 60°.

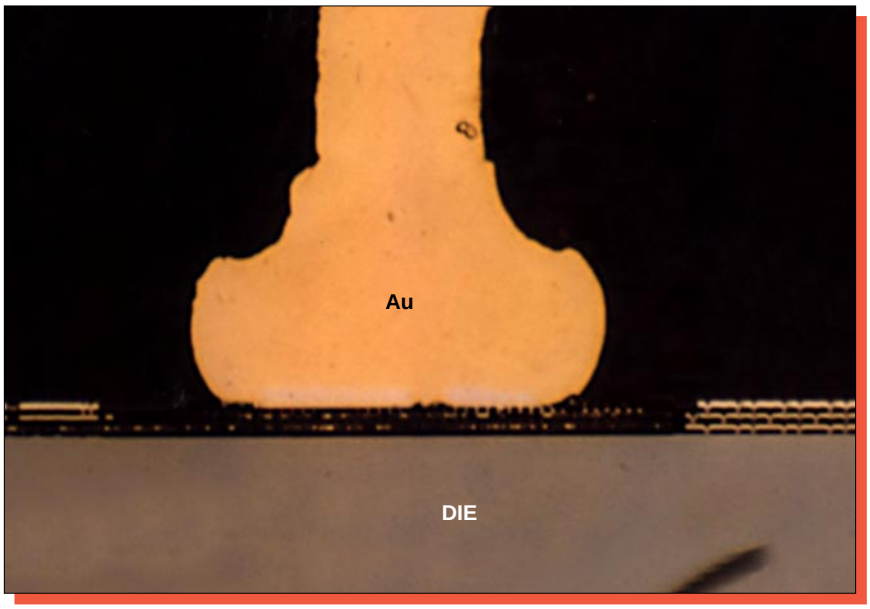


Mag. 1600x

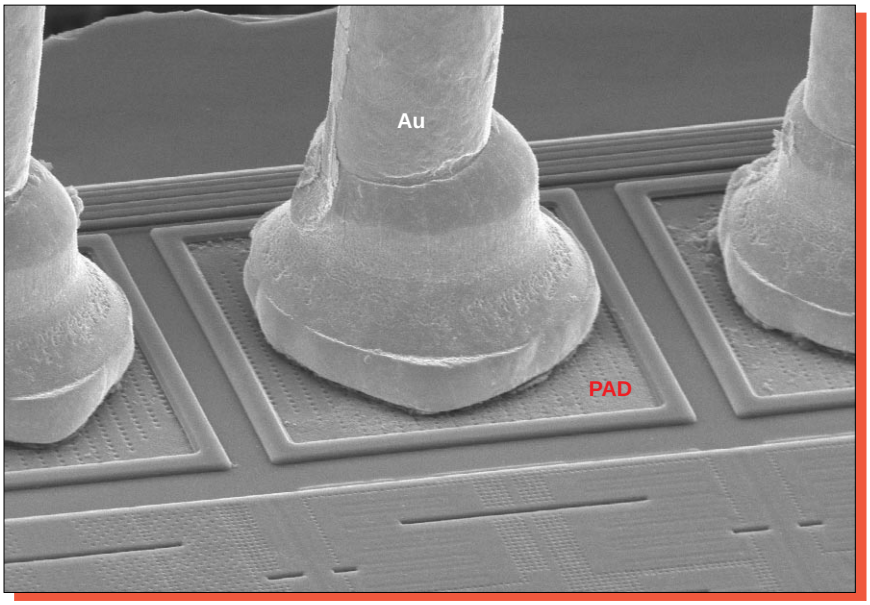


Mag. 6000x

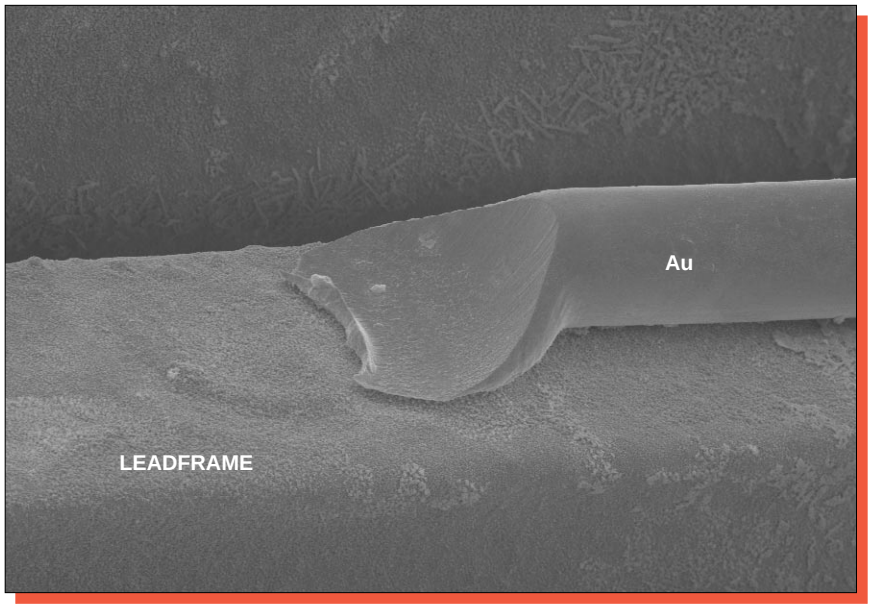
Figure 7a. SEM section views of the edge seal.



Mag. 600x, 60°

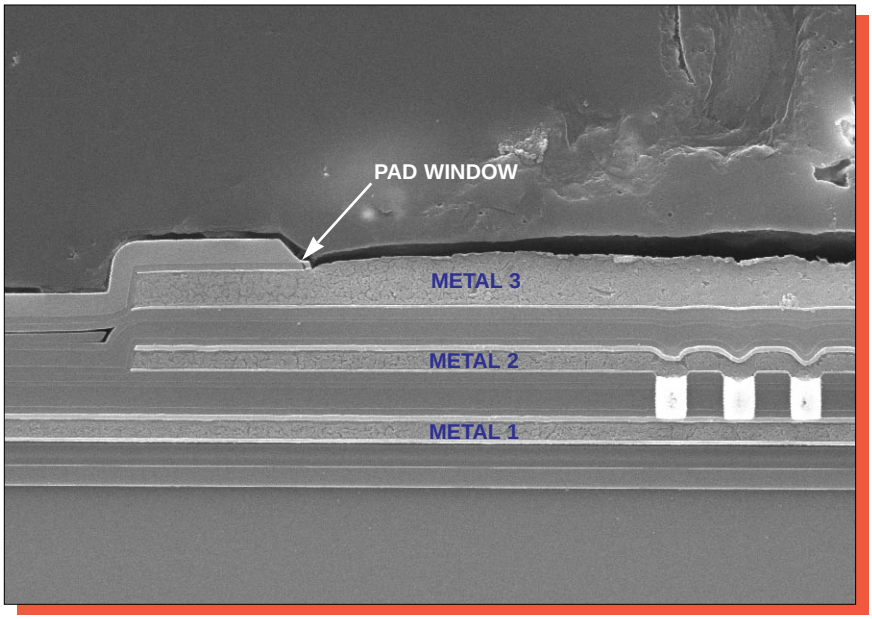


Mag. 700x, 60°

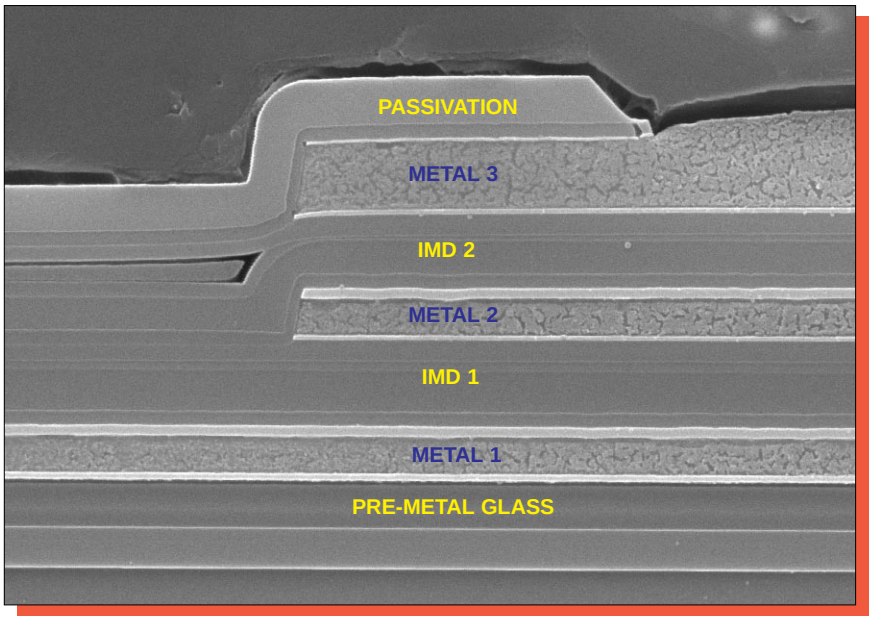


Mag. 800x

Figure 8. Optical and SEM views of typical wirebonds.



Mag. 5000x



Mag. 10,000x

Figure 8a. SEM section views of the pad structure.

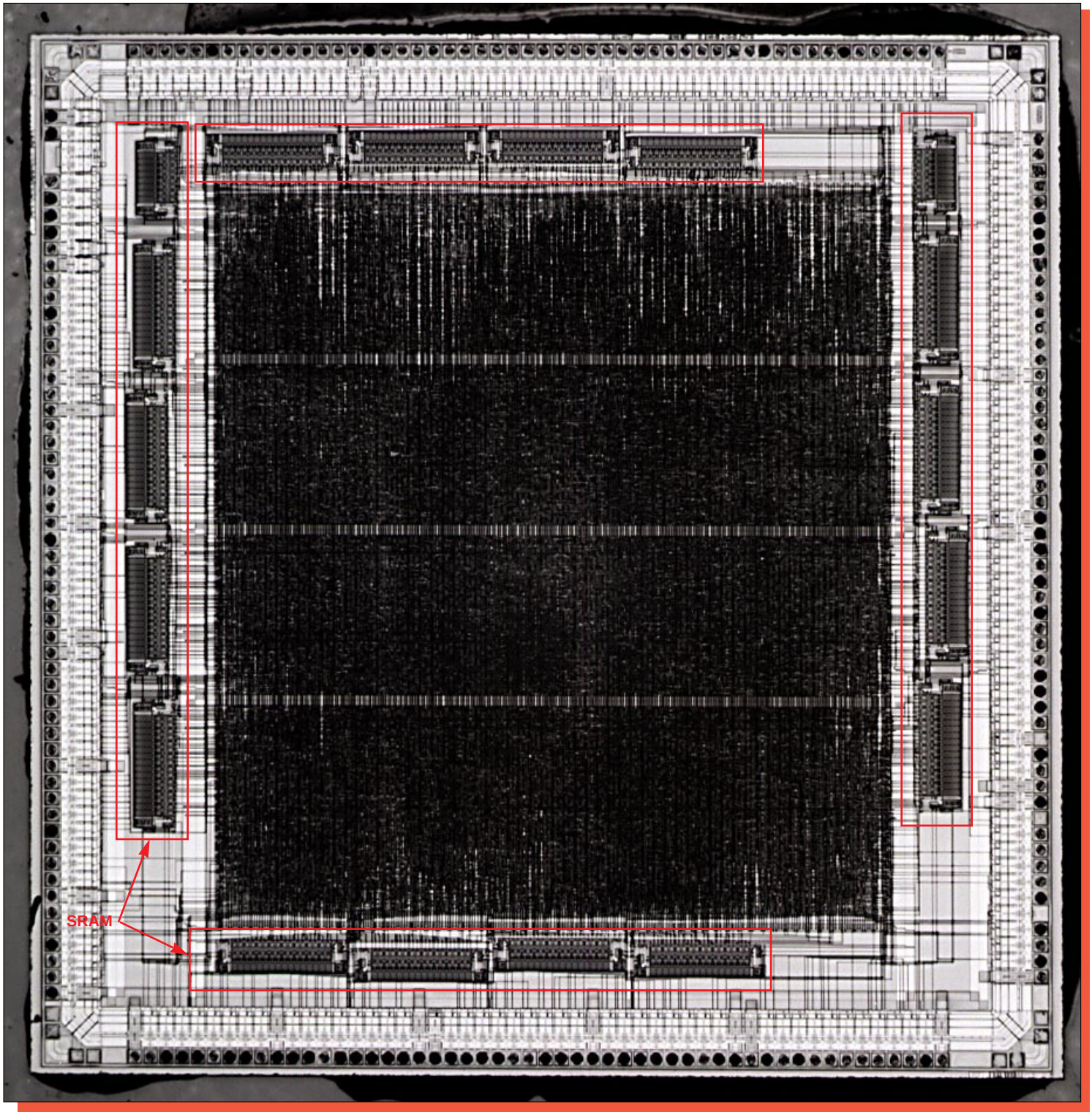


Figure 9. The PLX Technology PCI9080 intact circuit die. Mag. 29x.

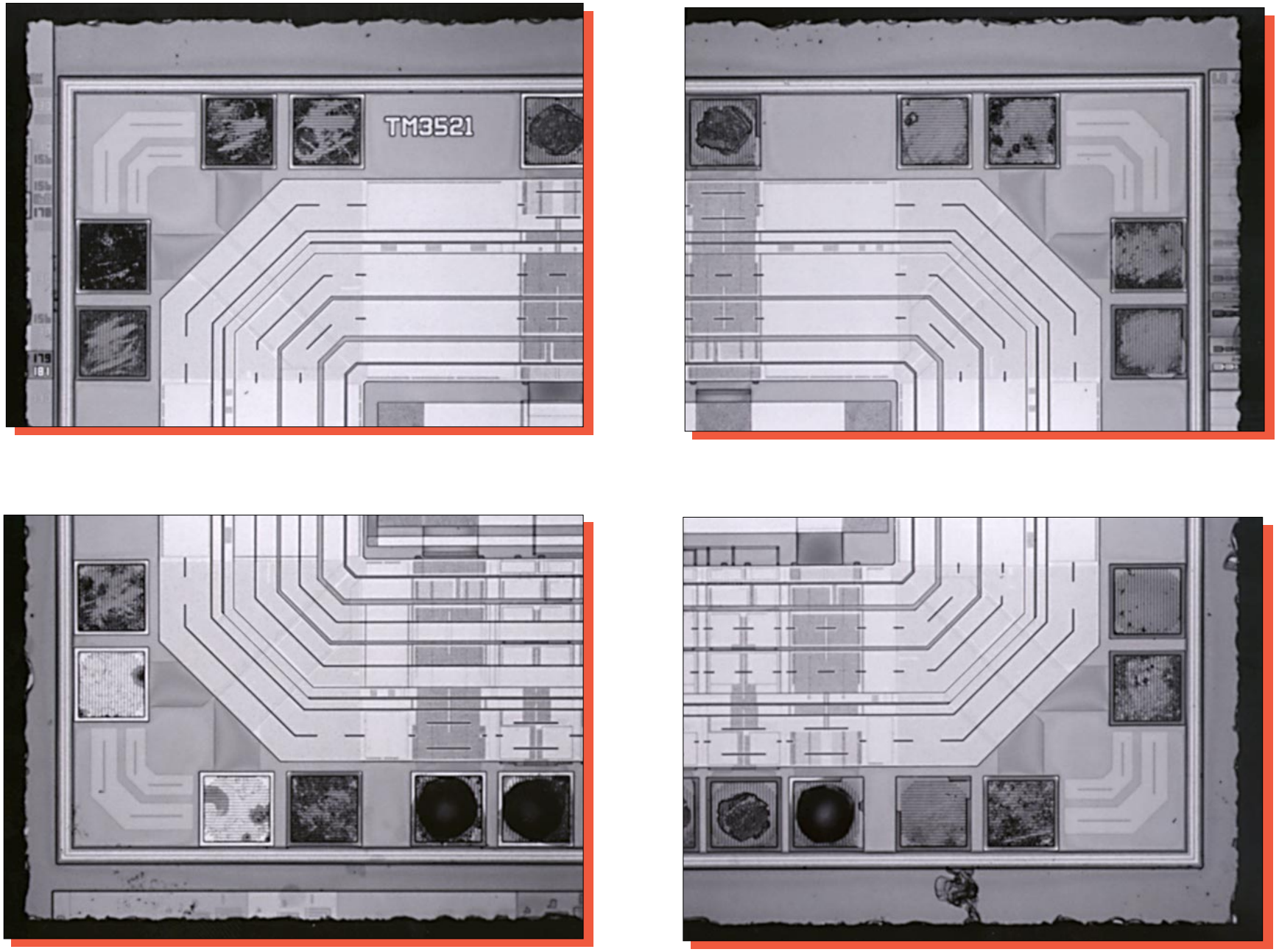
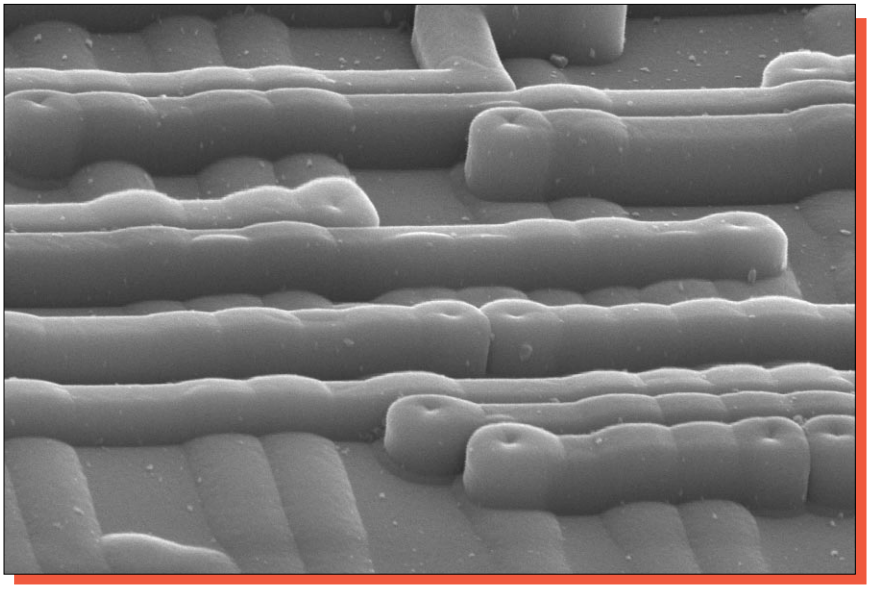
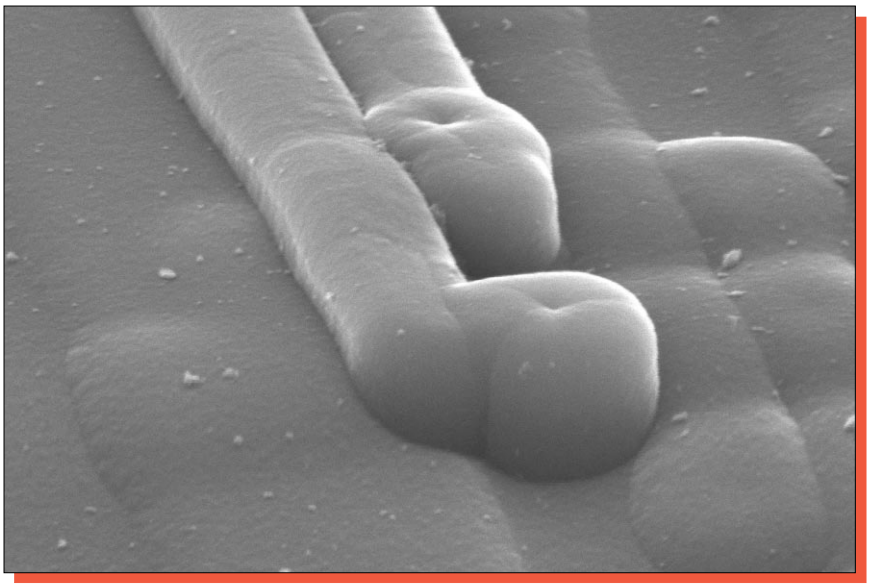


Figure 9a. Optical views of the die corners on the PLX Technology PCI9080 device. Mag. 160x.

Figure 10. Optical view of the die markings from the surface. Mag. 500x.

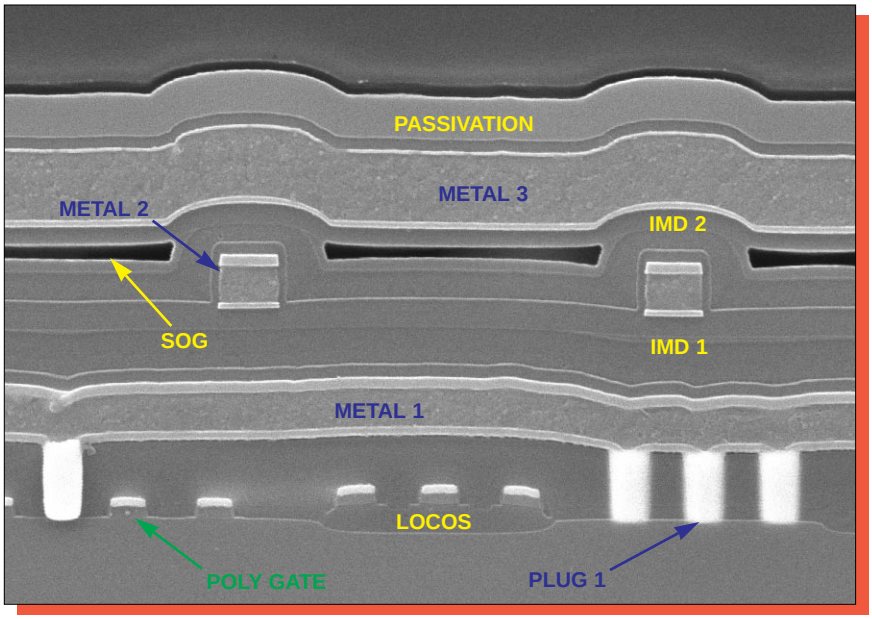


Mag. 4800x

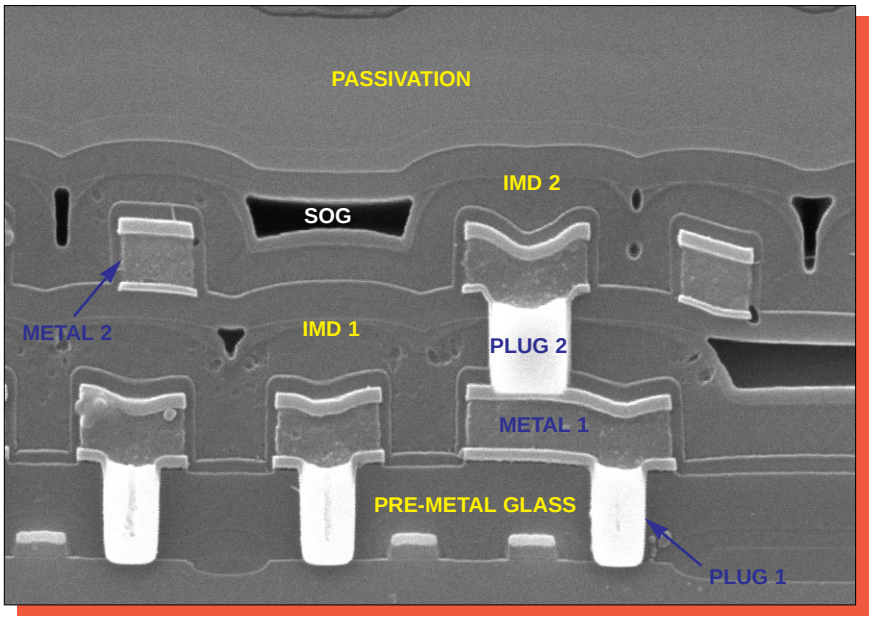


Mag. 10,000x

Figure 11. SEM views of passivation coverage. 60°.

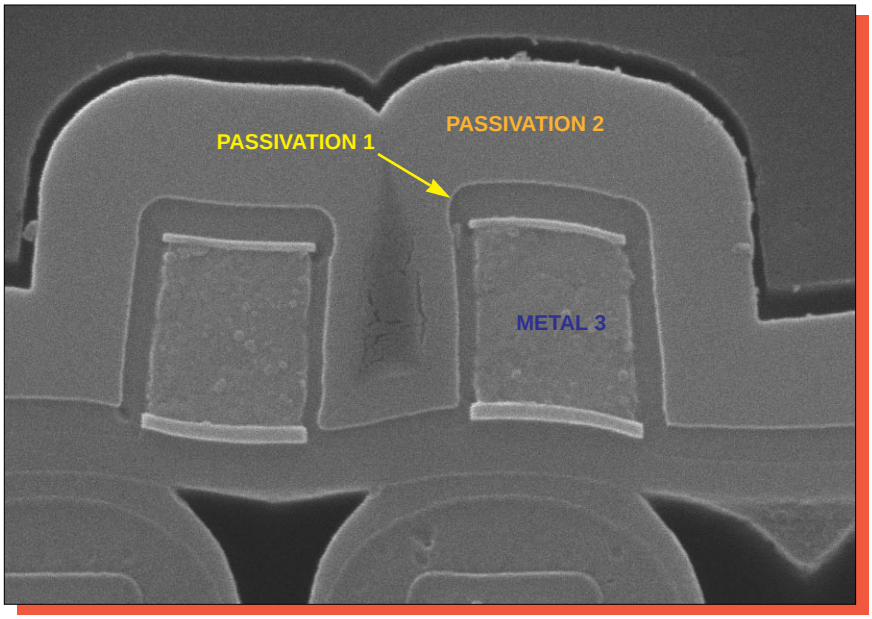


Mag. 10,000x

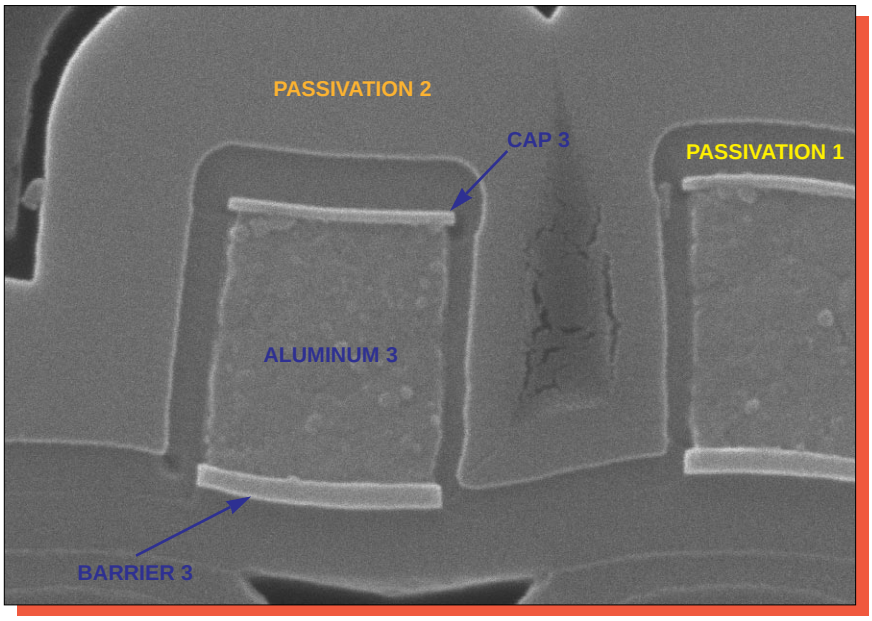


Mag. 13,000x

Figure 12. SEM section views illustrating general construction (glass-etch).

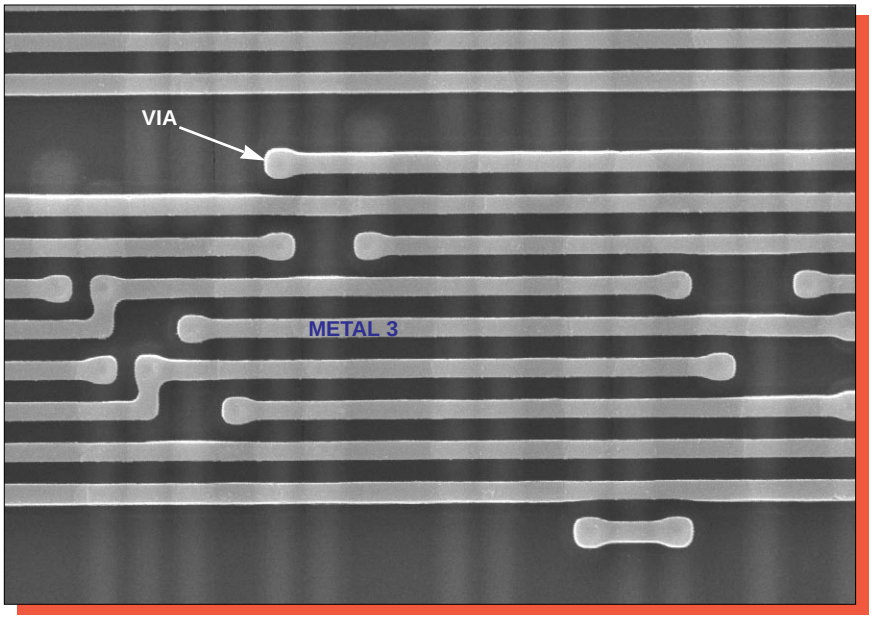


Mag. 26,000x

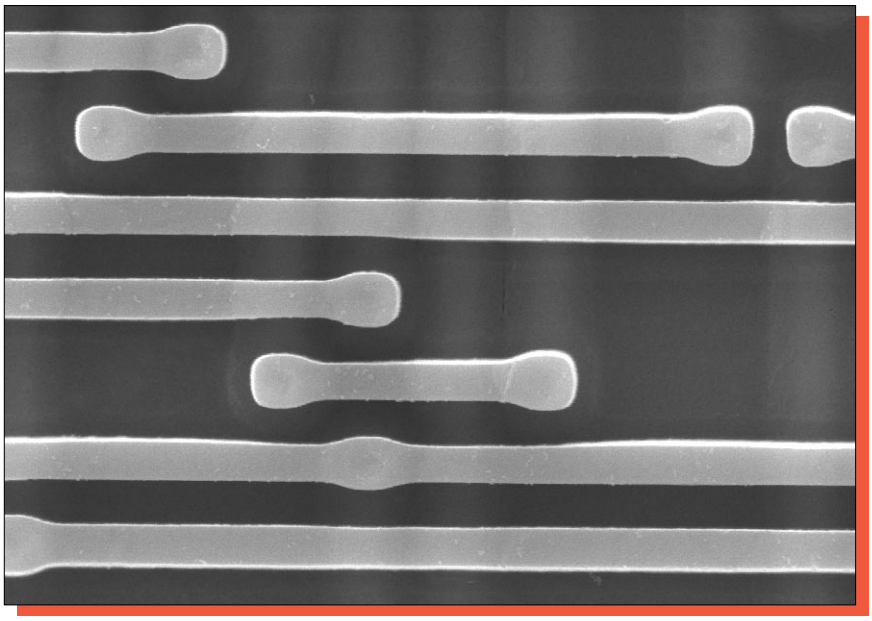


Mag. 40,000x

Figure 13. SEM section views of metal 3 line profiles.

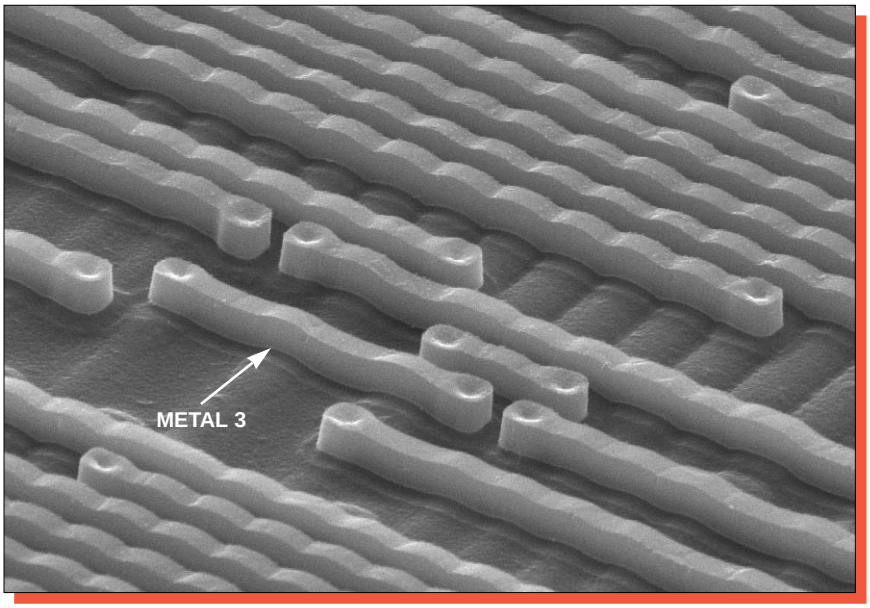


Mag. 3300x

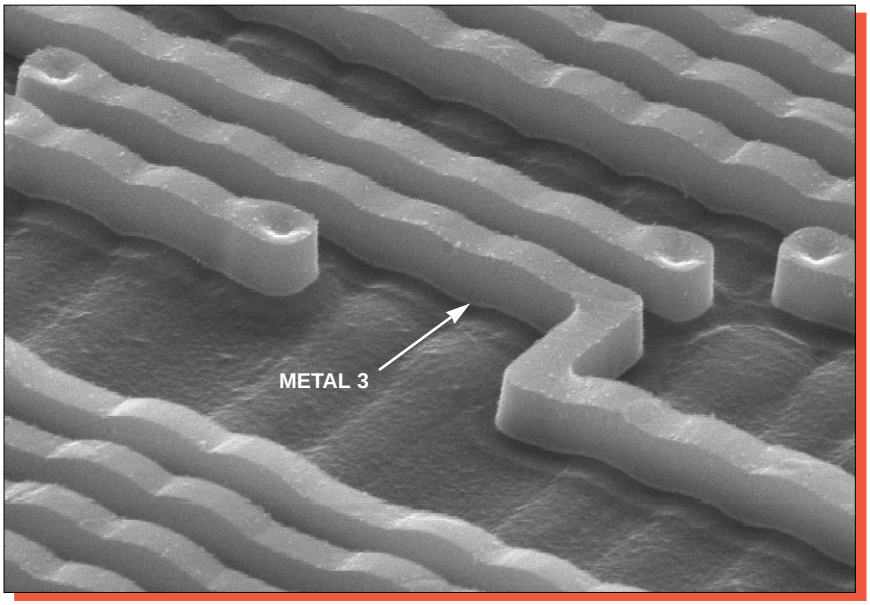


Mag. 6500x

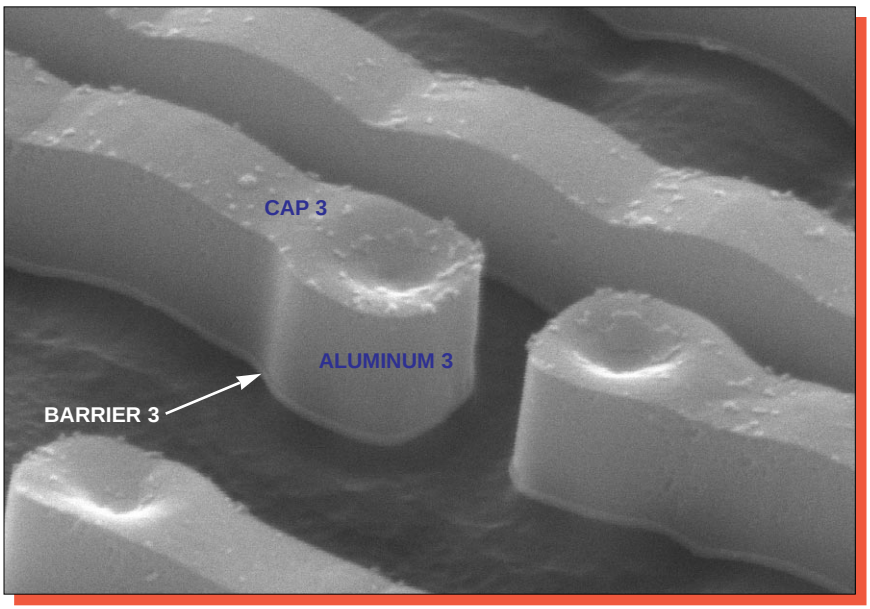
Figure 14. Topological SEM views of metal 3 patterning. 0°.



Mag. 5000x

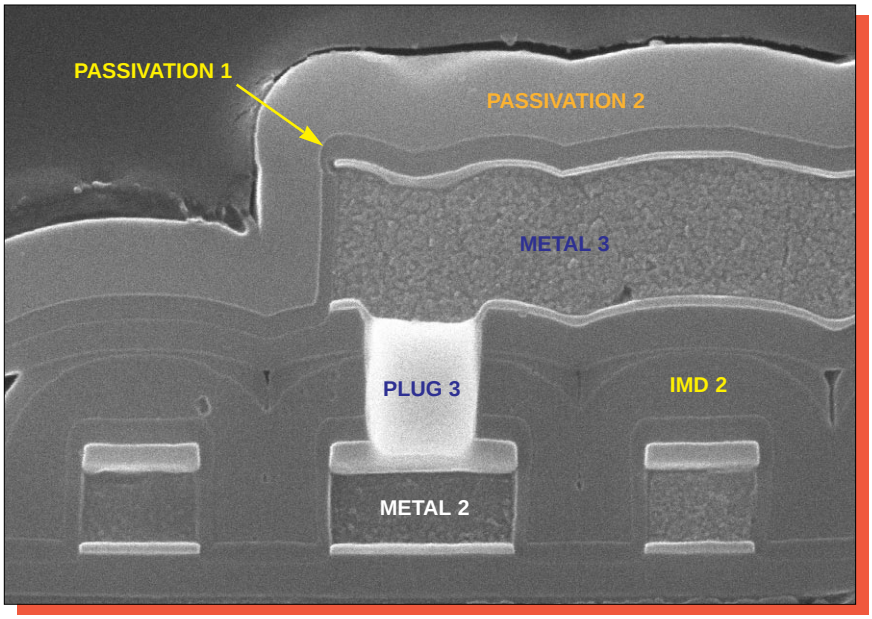


Mag. 8000x

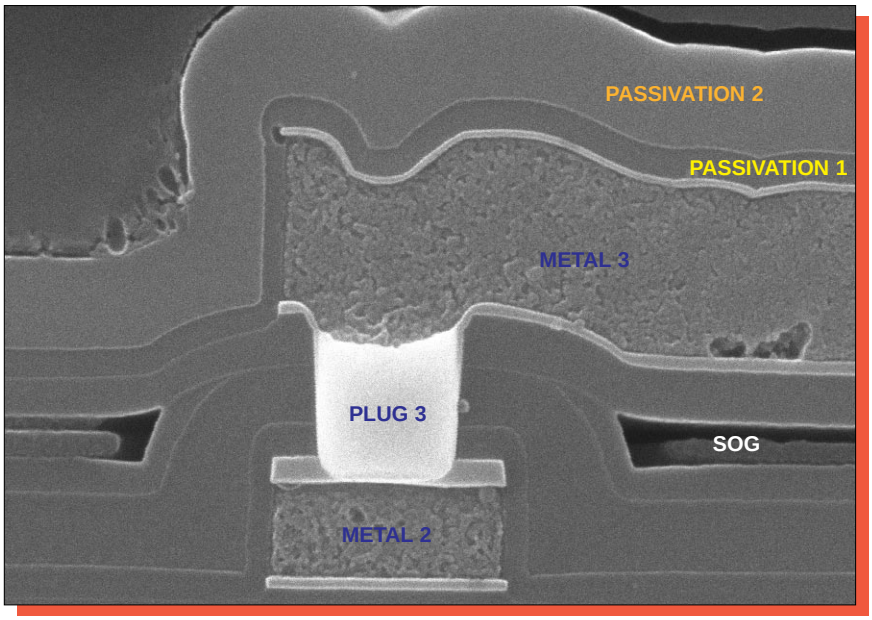


Mag. 20,000x

Figure 15. Perspective SEM views of metal 3 integrity. 60°.

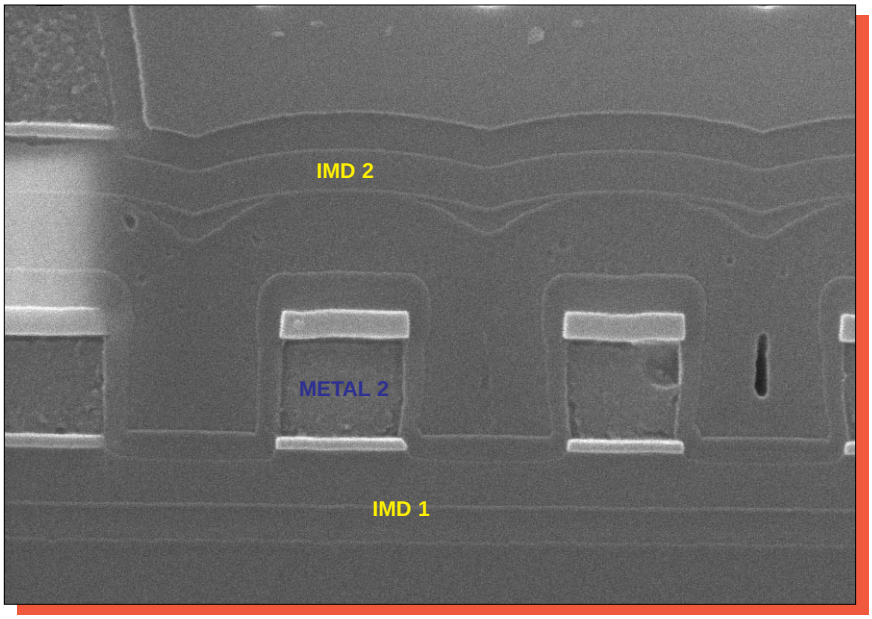


Mag. 20,000x

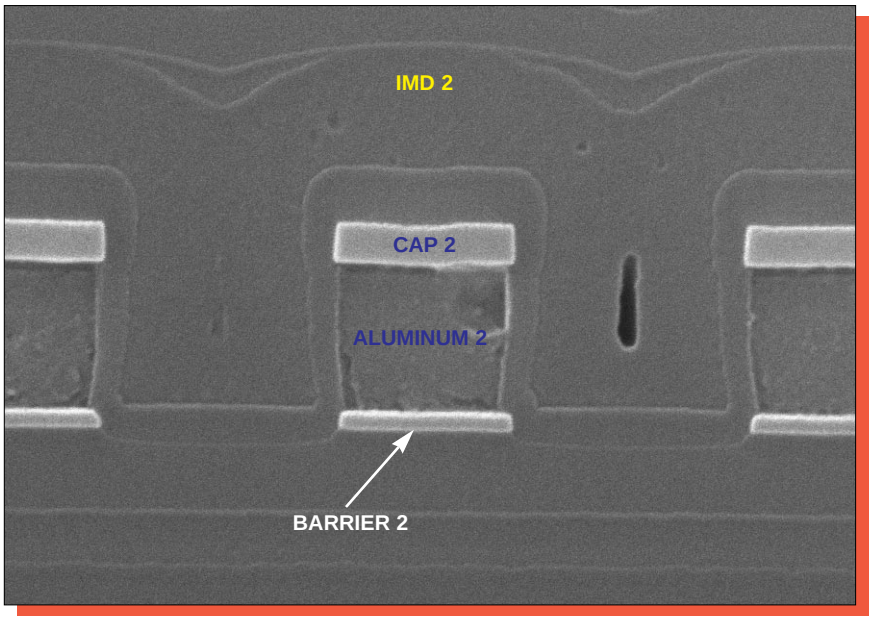


Mag. 26,000x

Figure 16. SEM section views of metal 3-to-metal 2 vias.

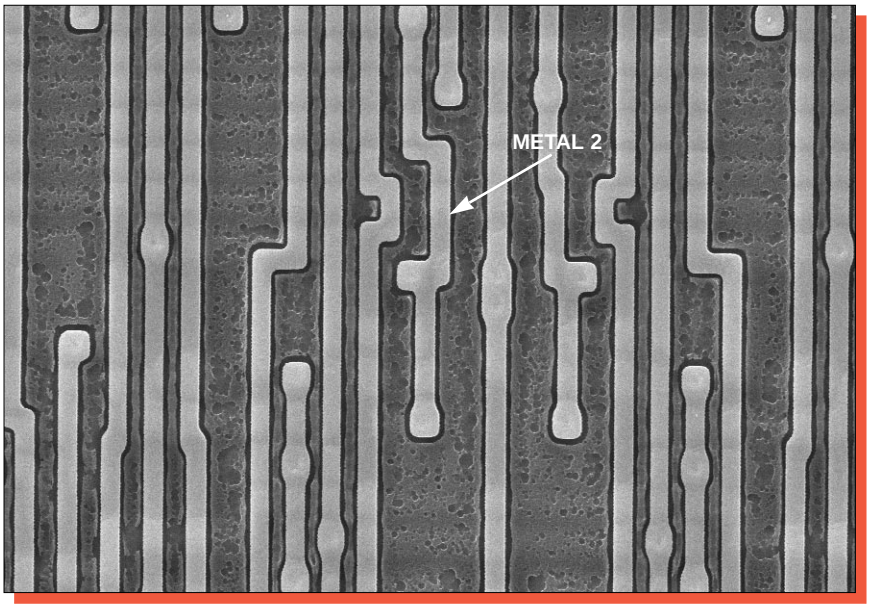


Mag. 26,000x

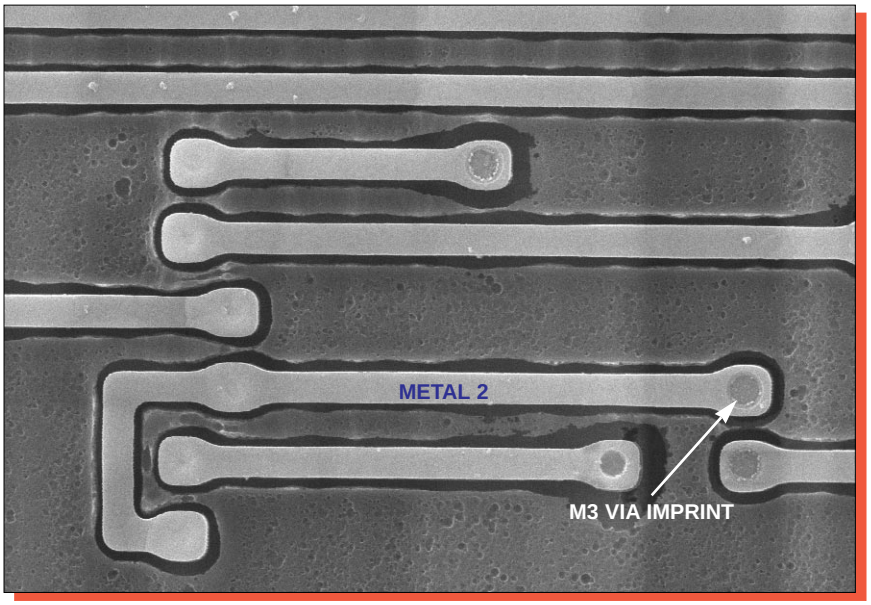


Mag. 40,000x

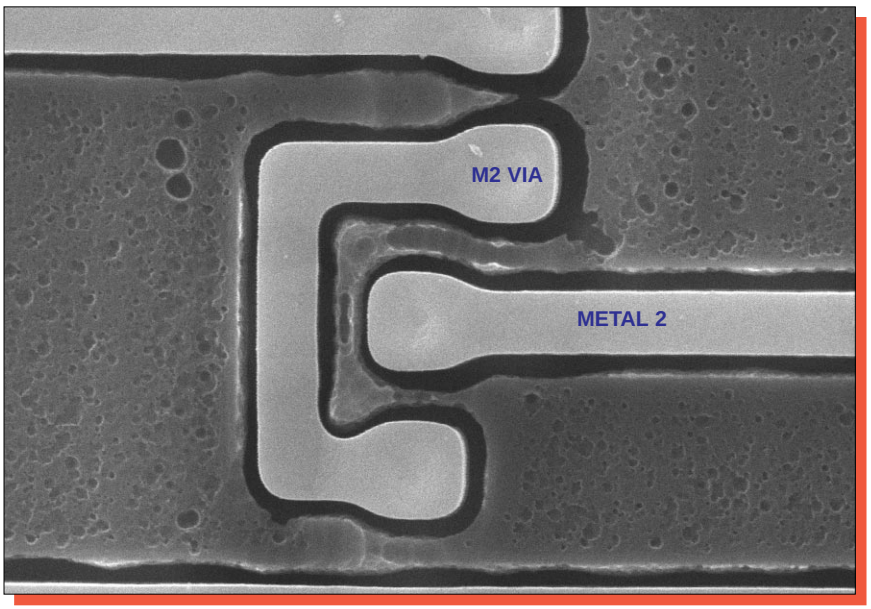
Figure 17. SEM section views of metal 2 line profiles.



Mag. 2500x

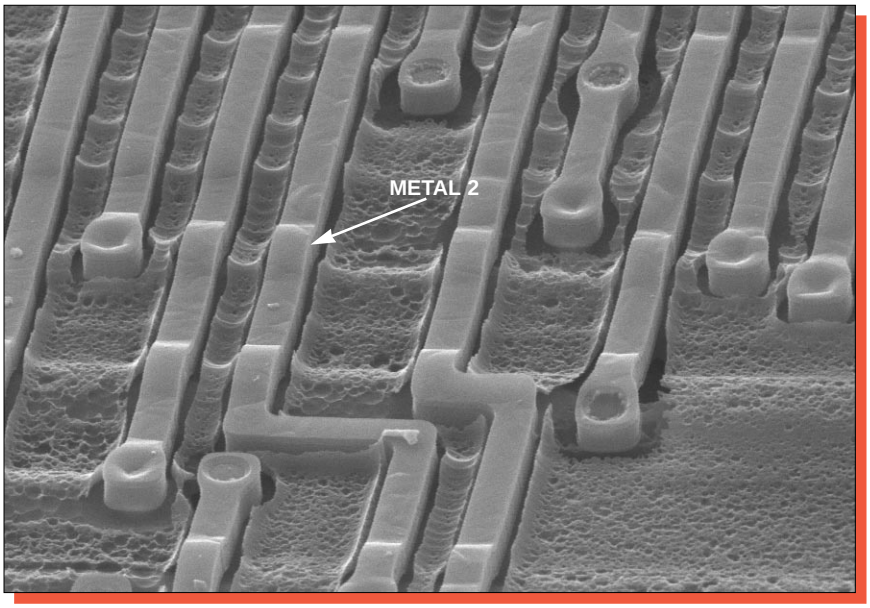


Mag. 5000x

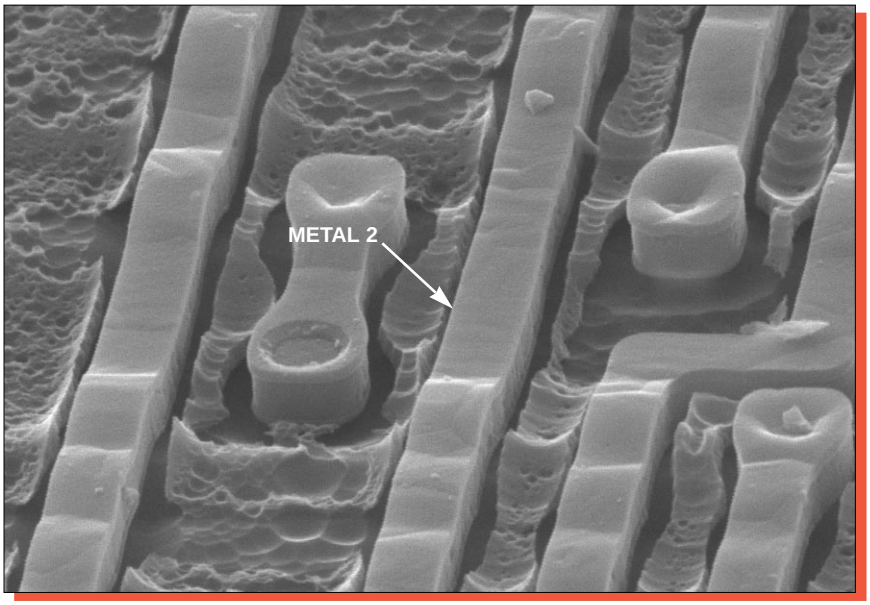


Mag. 10,000x

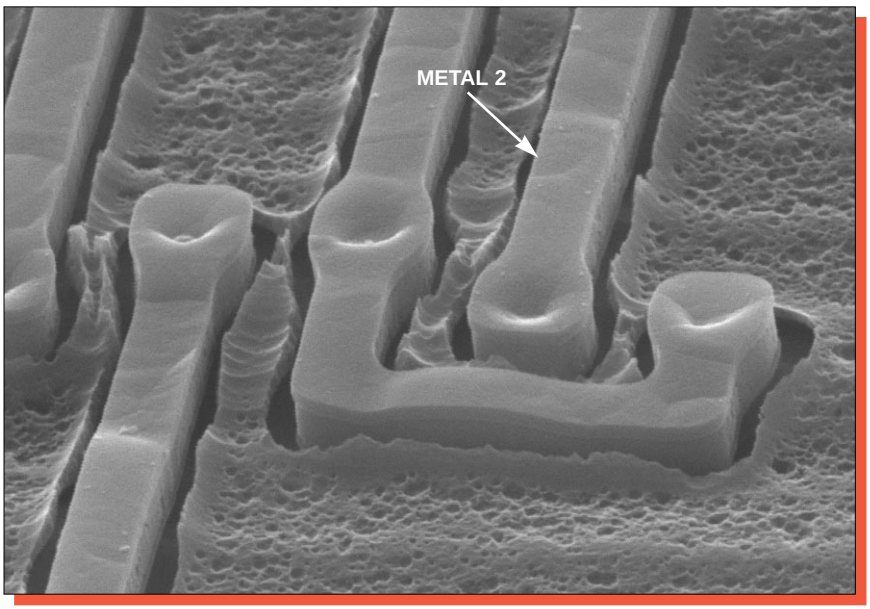
Figure 18. Topological SEM views of metal 2 patterning. 0°.



Mag. 6000x

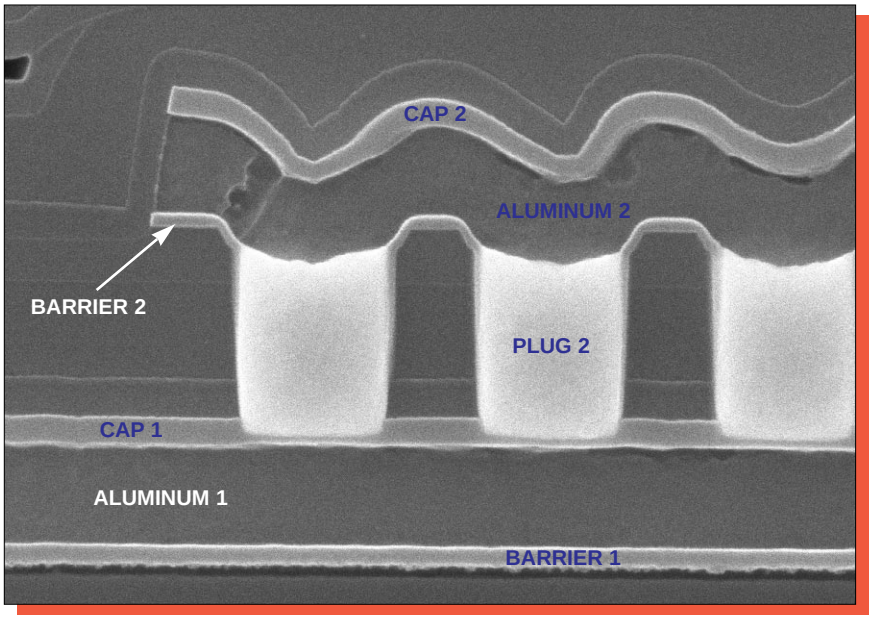


Mag. 11,000x

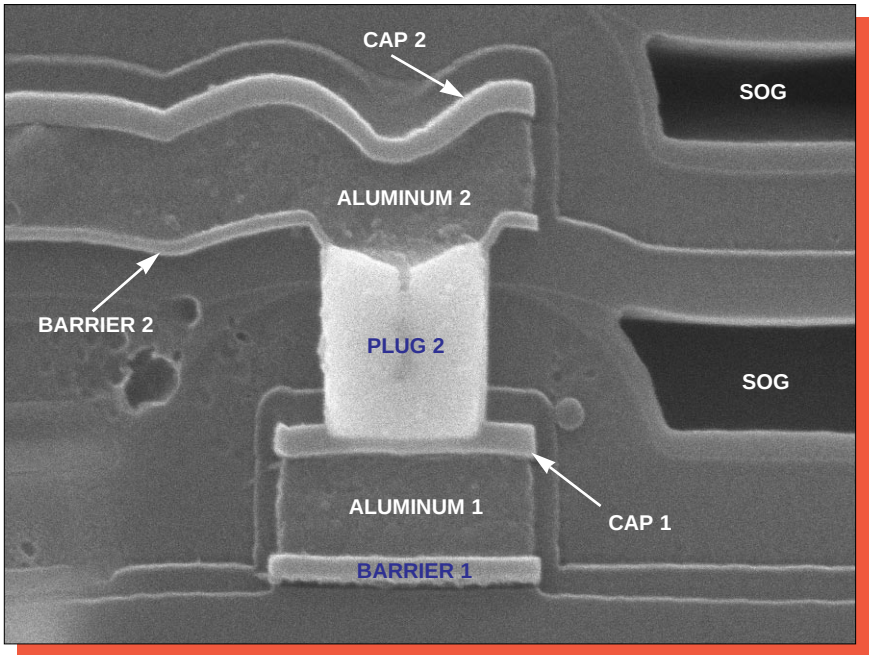


Mag. 12,000x

Figure 19. Perspective SEM views of metal 2 integrity. 60°.



Mag. 26,000x



Mag. 27,000x

Figure 20. SEM section views of metal 2-to-metal 1 vias.

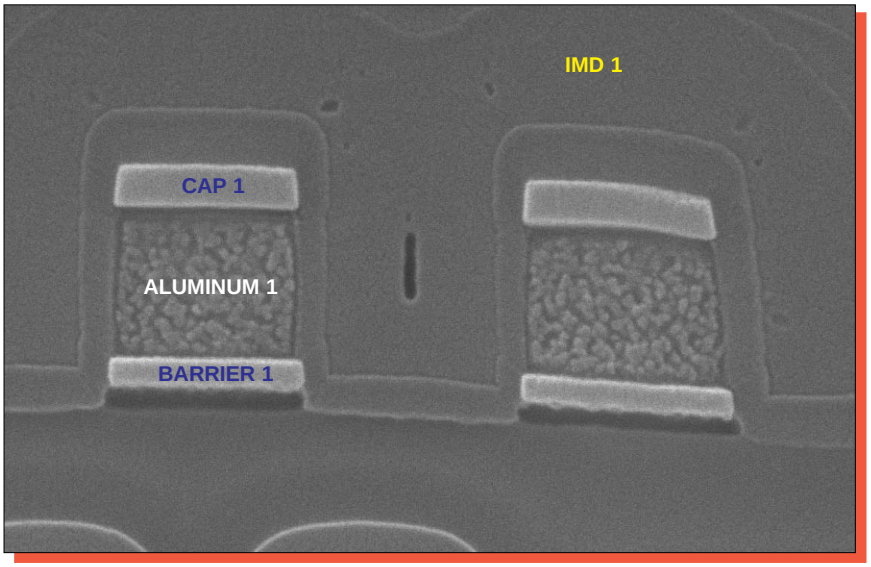
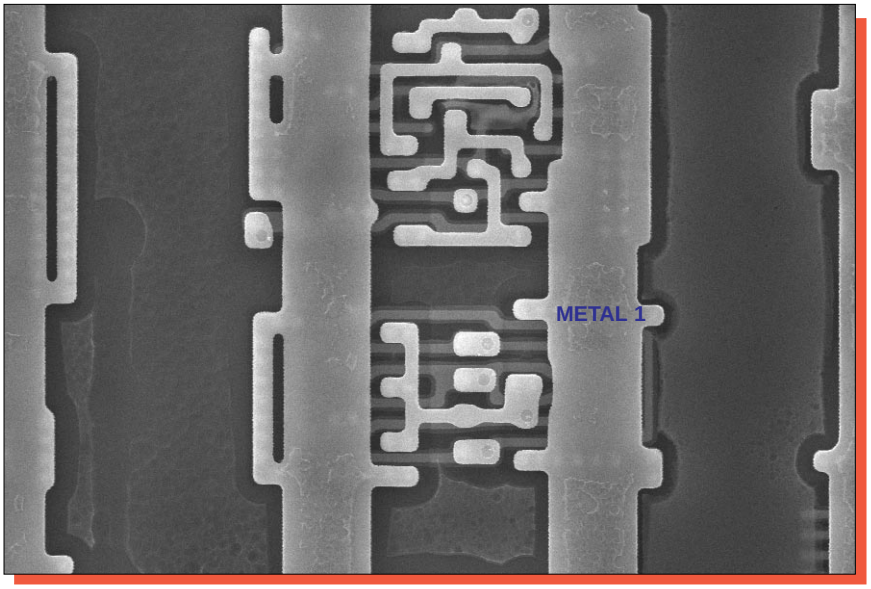
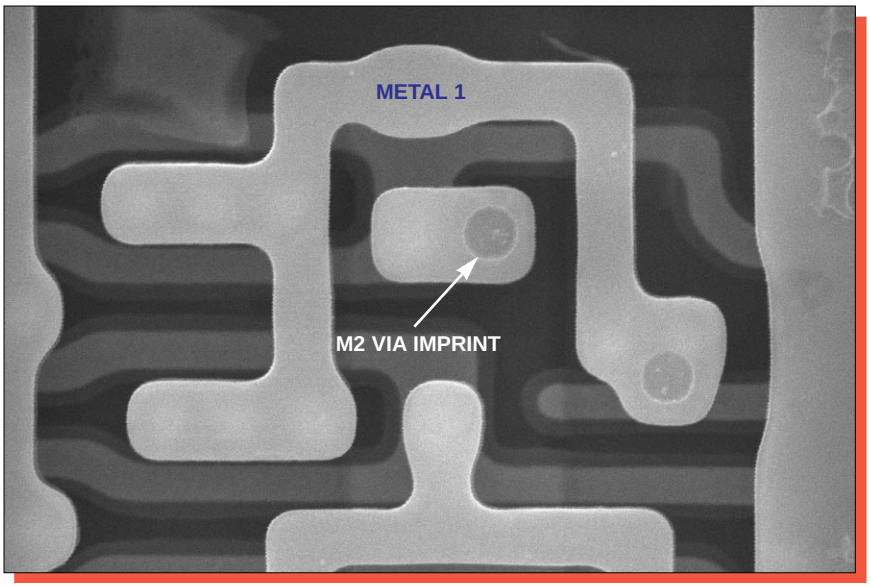


Figure 21. SEM section view of metal 1 line profiles. Mag. 40,000x.

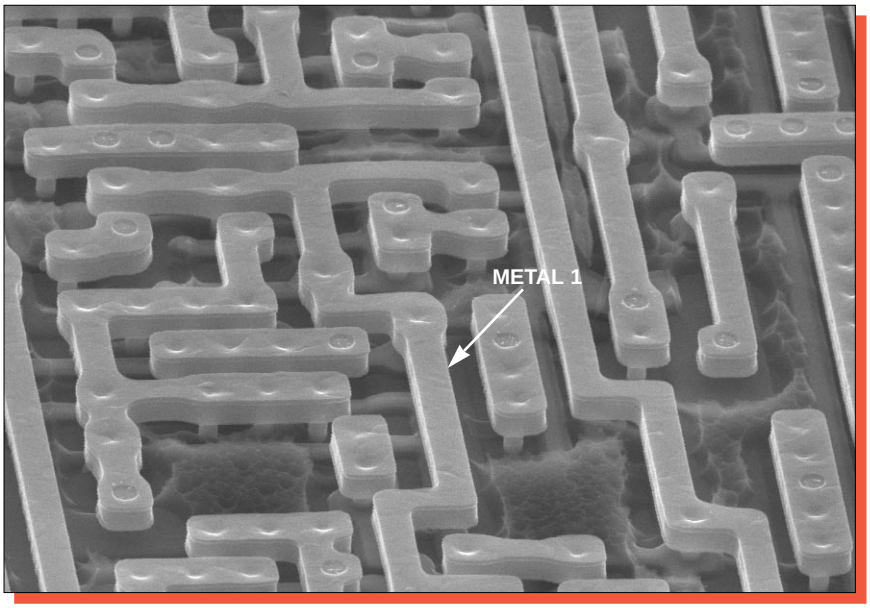


Mag. 2500x

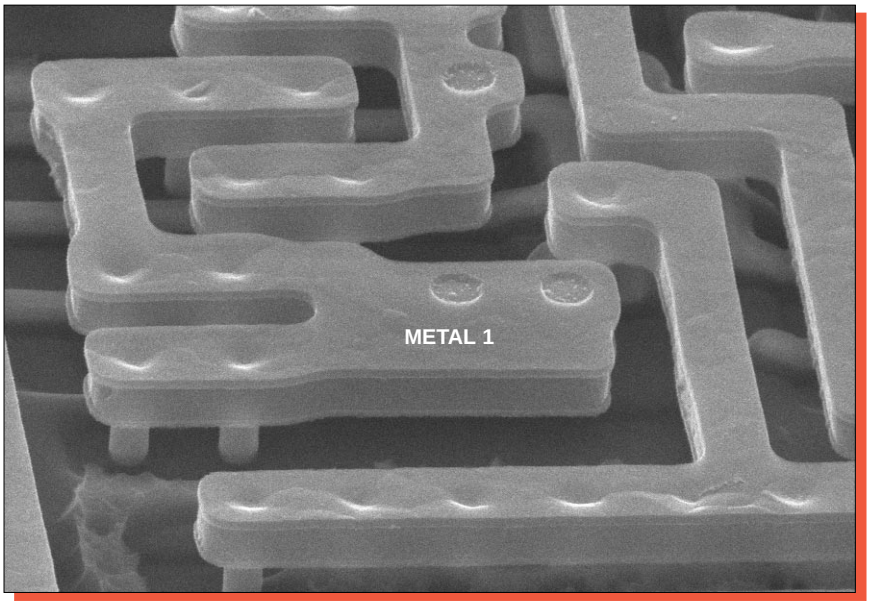


Mag. 10,000x

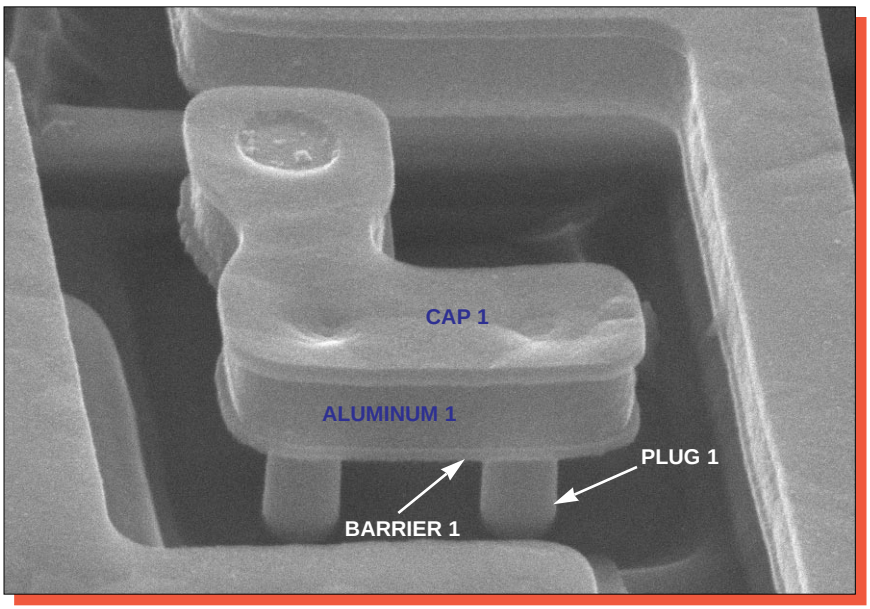
Figure 21a. Topological SEM views of metal 1 patterning. 0°.



Mag. 5000x

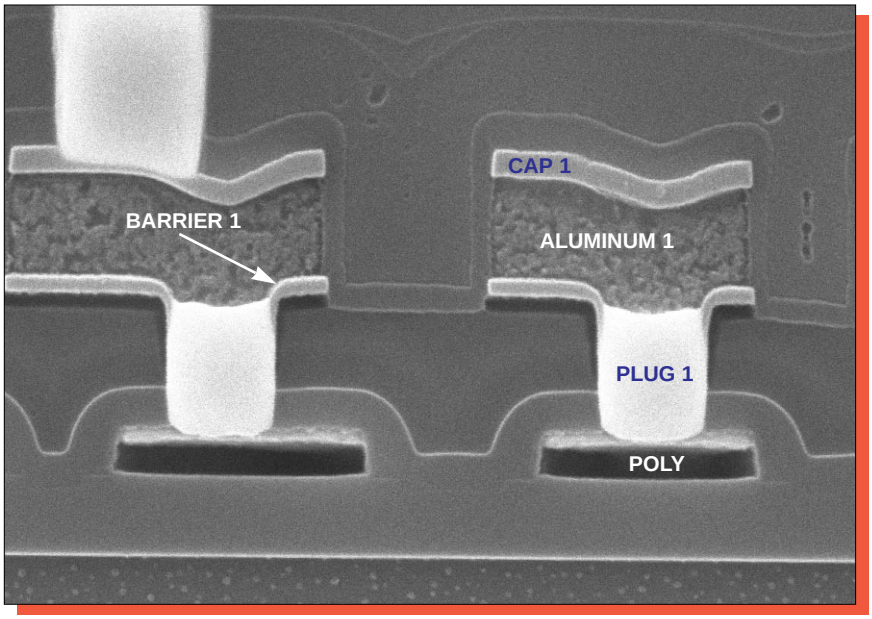


Mag. 10,000x

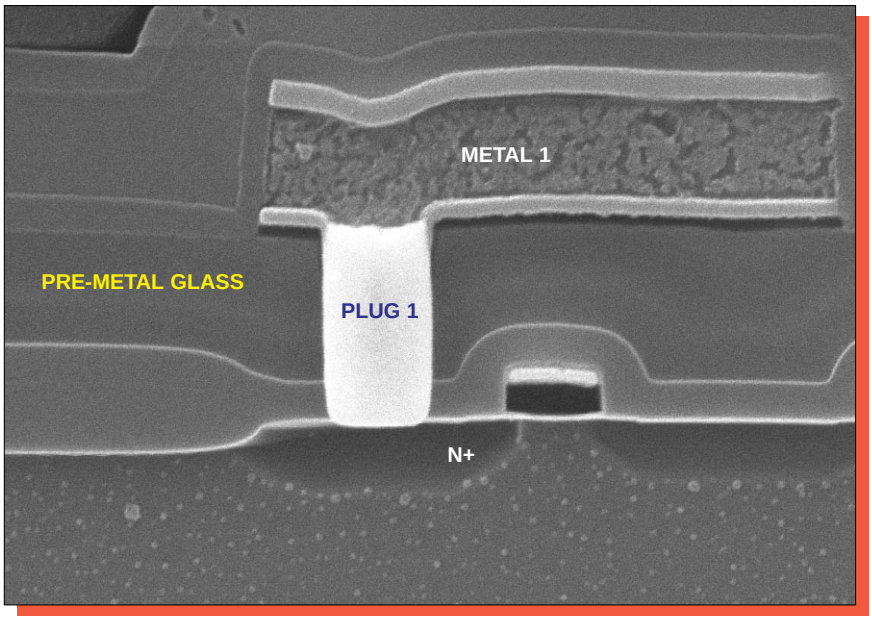


Mag. 20,000x

Figure 22. Perspective SEM views of metal 1 integrity. 60°.

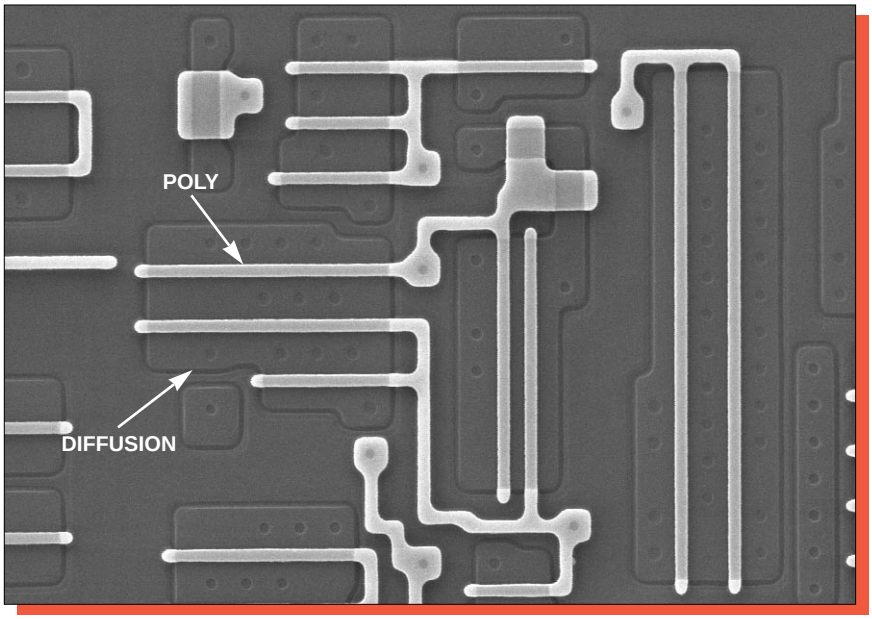


metal-to-poly

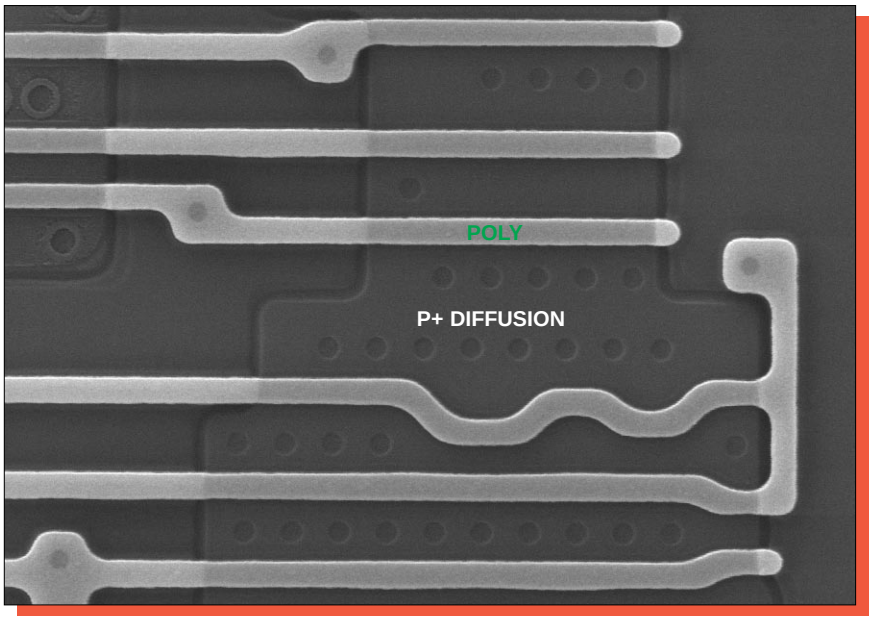


metal 1-to-N+

Figure 23. SEM section views of typical contacts. Mag. 26,000x.

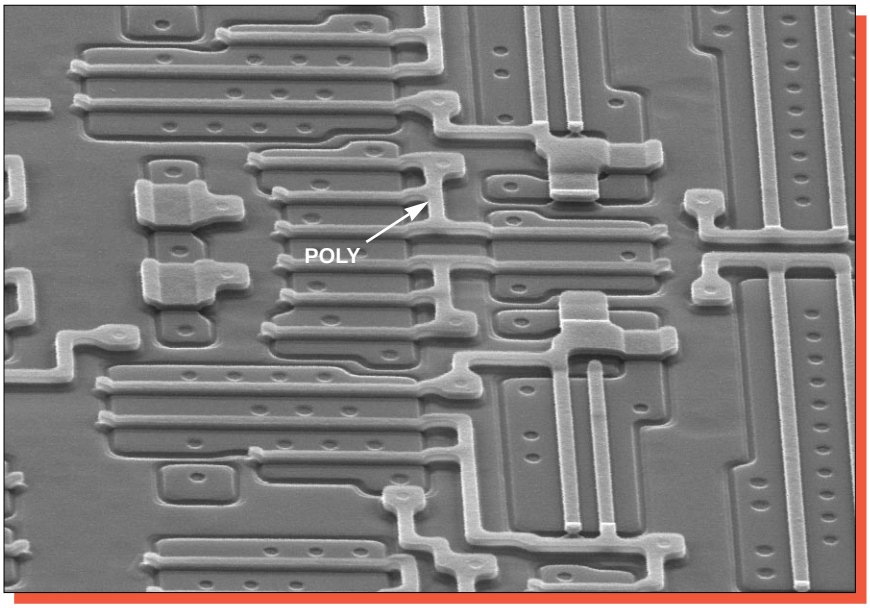


Mag. 3300x

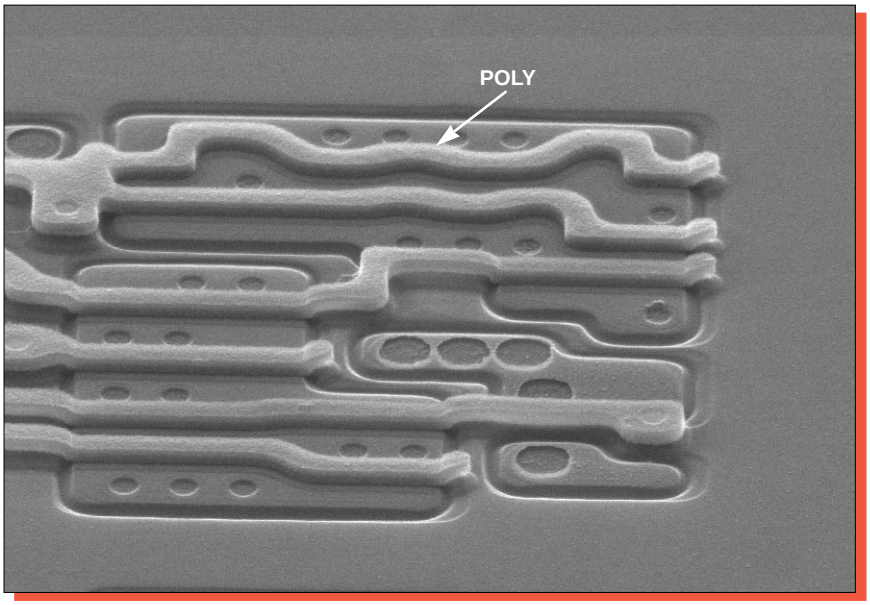


Mag. 6500x

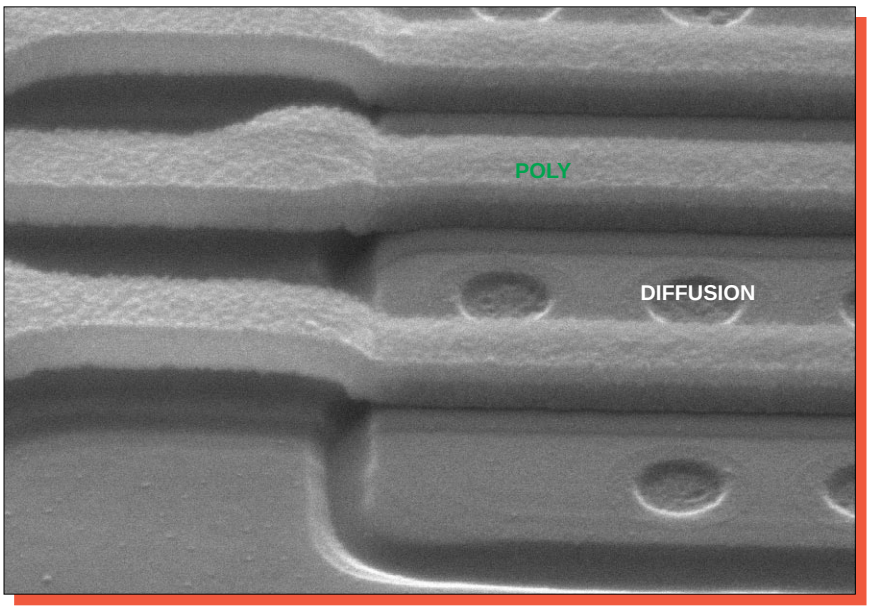
Figure 24. Topological SEM views of polycide patterning. 0°.



Mag. 4000x

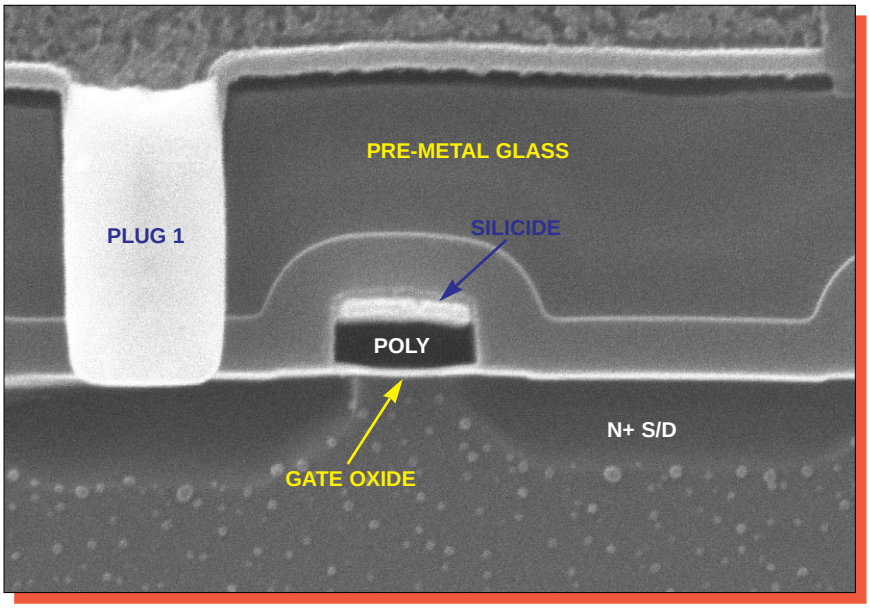


Mag. 8000x

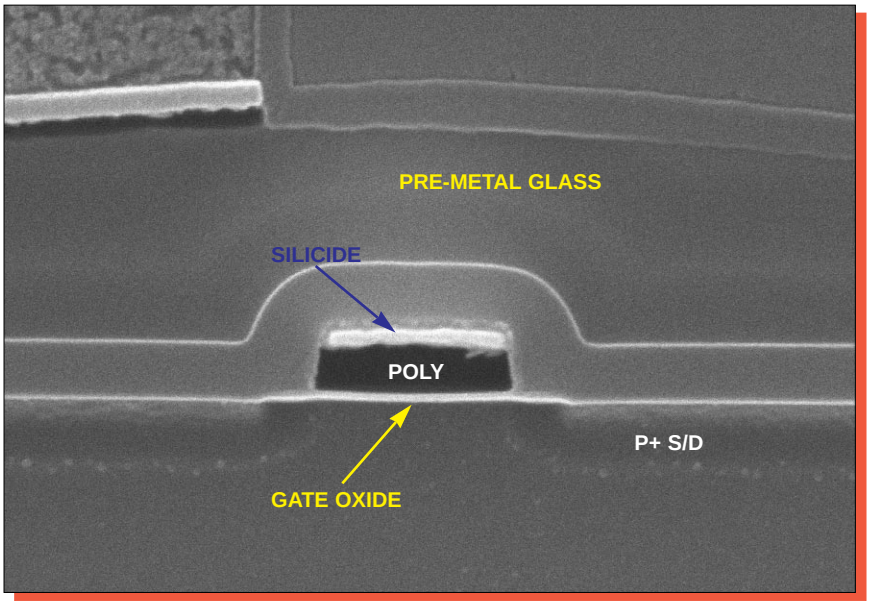


Mag. 26,000x

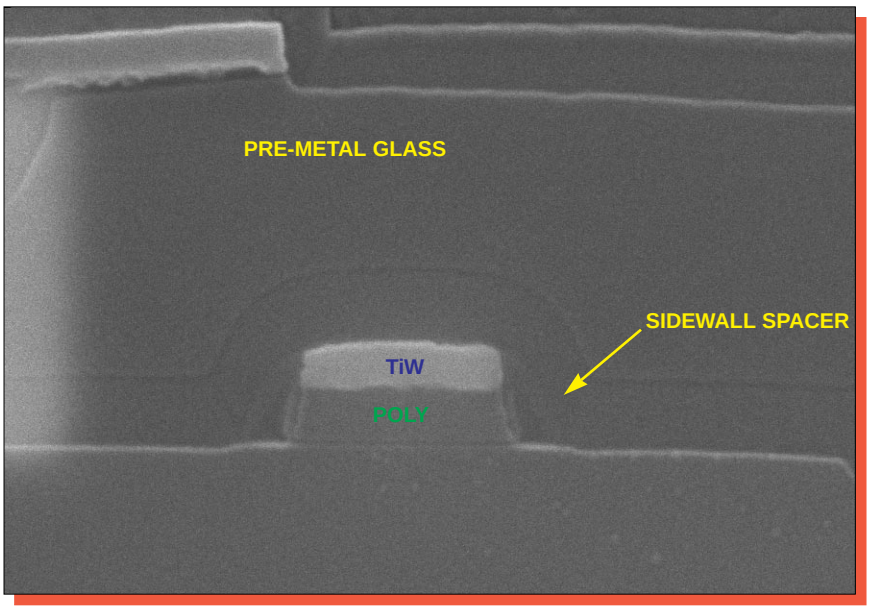
Figure 25. SEM views of polycide coverage. 60°.



N-channel,
Mag. 40,000x



P-channel,
Mag. 40,000x



glass etch,
Mag. 52,000x

Figure 26. SEM section views of typical transistors.

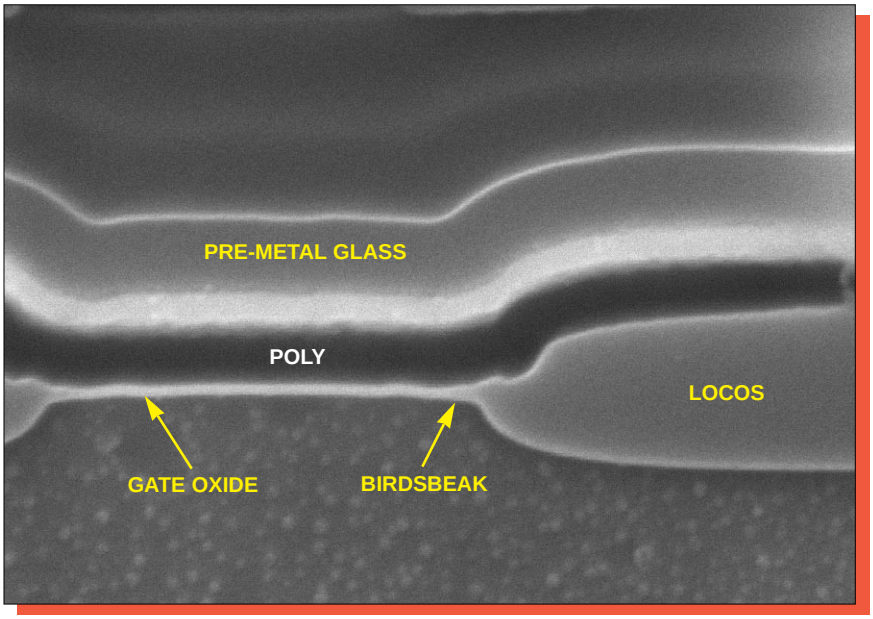


Figure 27. SEM section view of a local oxide birdsbeak. Mag. 52,000x.

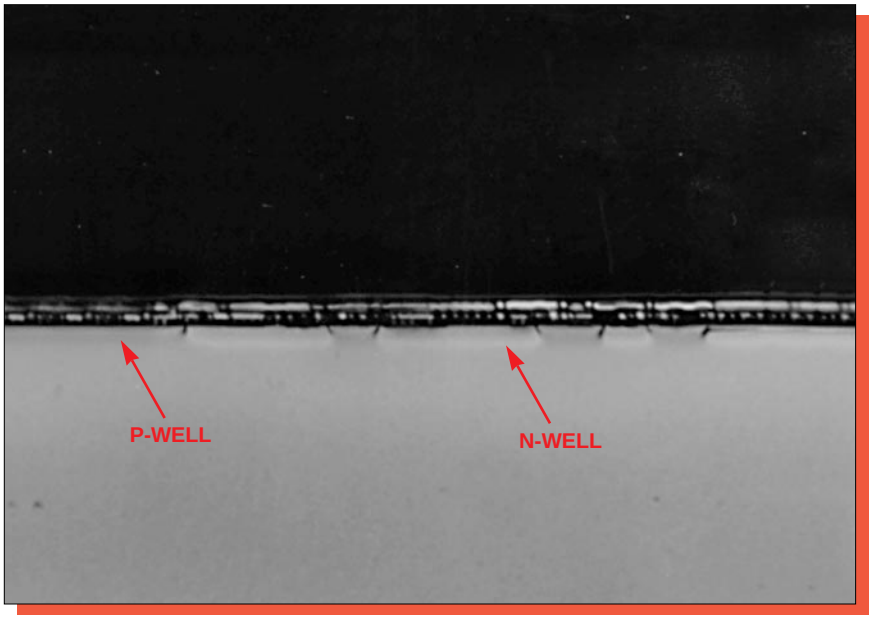
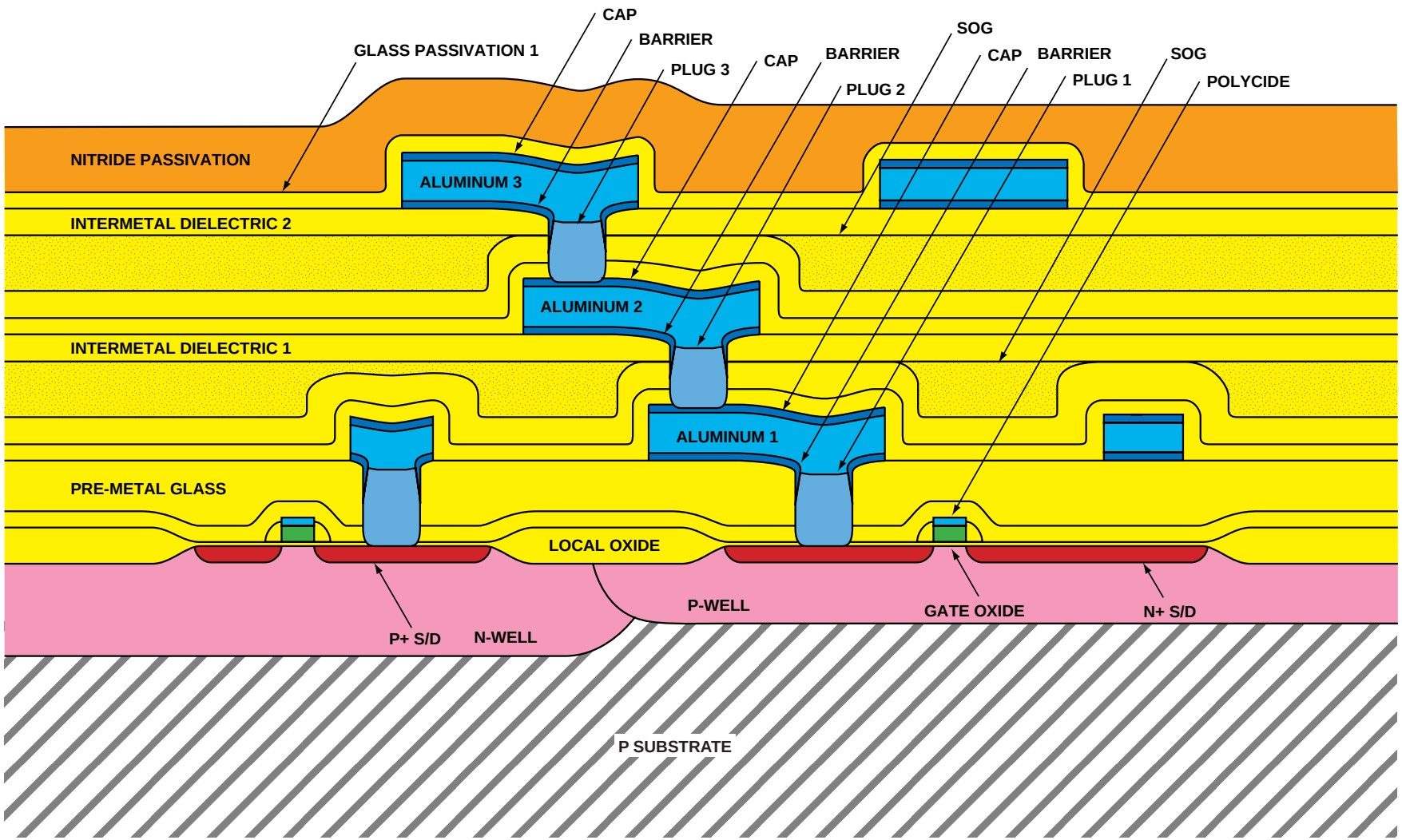


Figure 28. Optical section view of the well structure. Mag. 800x.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 28a. Color cross section drawing illustrating device structure.

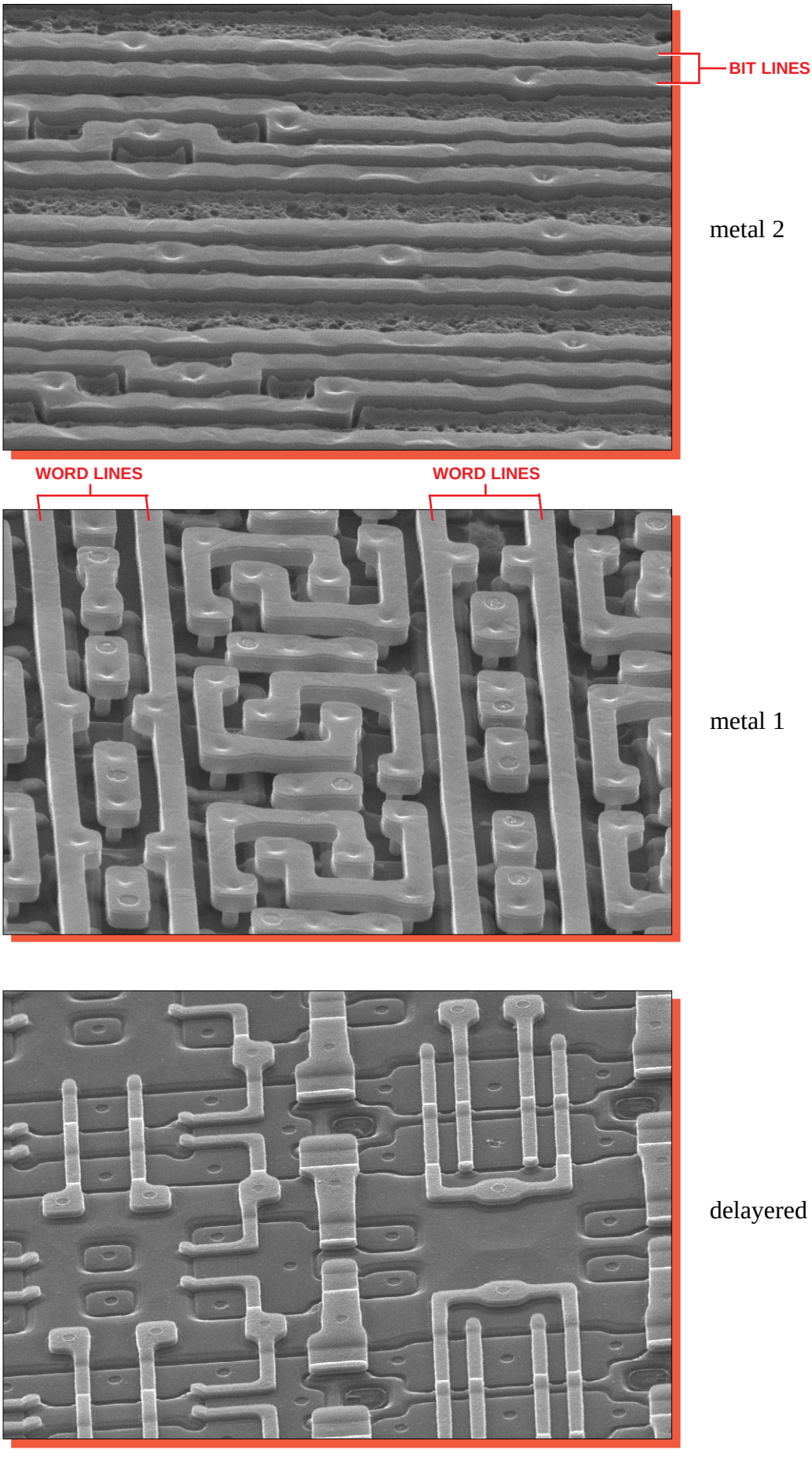
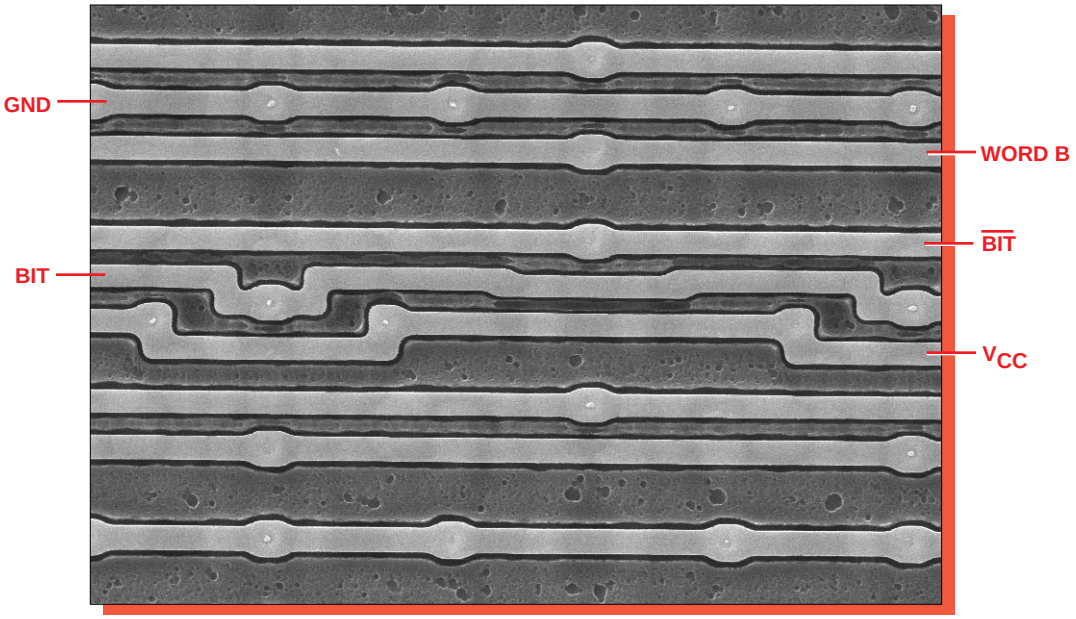
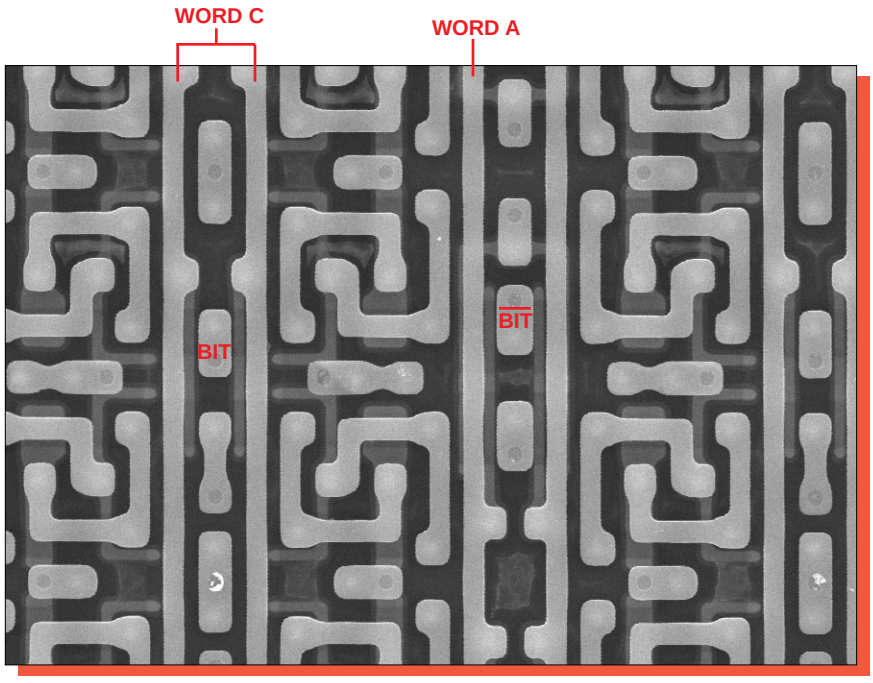


Figure 29. Perspective SEM views of the SRAM cell array. Mag. 5000x, 60°.

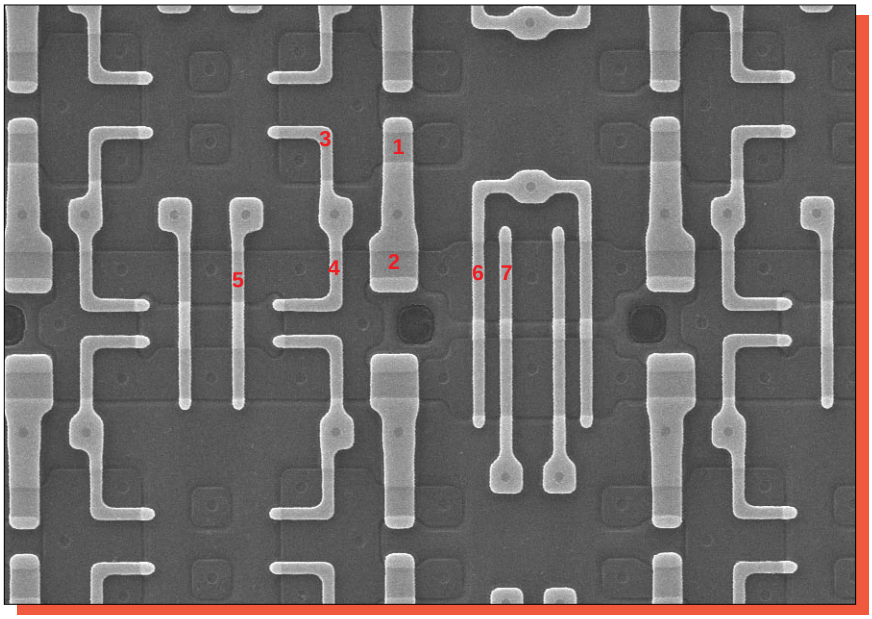


metal 2



metal 1

Figure 30. Topological SEM view of the SRAM cell. Mag. 3000x, 0°.



delayered

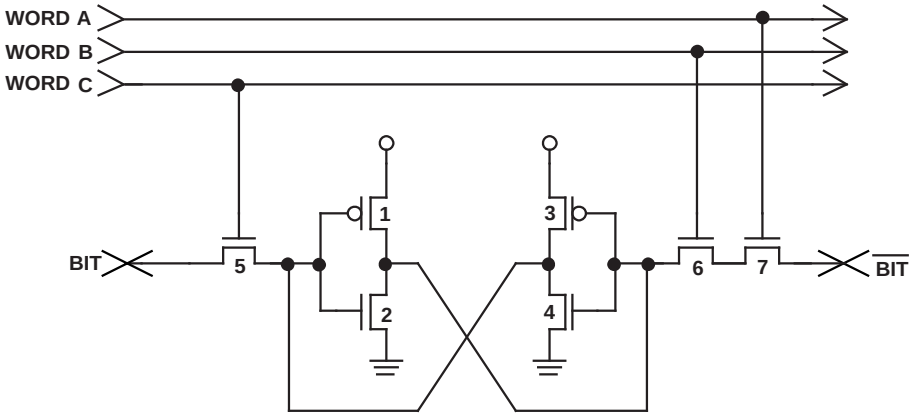


Figure 31. Topological SEM view and schematic of the SRAM cell. Mag. 3000x, 0°.