Construction Analysis

Rockwell R6732-13
RF to IF Down Converter

Report Number: SCA 9709-552

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a competitive analysis of the Rockwell R6732-13 RF-to-IF down converter. One device packaged in an 80-pin Square Quad Flat Package (SQFP) was received for the analysis. The device was taken from a GPS receiver chipset manufactured by IST. The IC was date coded 9642. Two dice, one GaAs and one Si, were encapsulated in the package. This report describes the analysis performed on the Si IC.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 2 aluminum thinned up to 100 percent[2] at some locations of some vias. Barrier metal remained intact to provide continuity.

- Metal 1 aluminum thinned up to 100 percent[2] at some locations of some contacts. Barrier metal remained intact to provide continuity.

Special Features:

- Titanium silicided diffusion structures.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- The device was encapsulated in an 80-pin plastic Square Quad Flat Package (SQFP).
- Copper (Cu) leadframe was internally plated with silver (Ag). The leadframe was split to accommodate both dice.
- External pins were tinned with tin-lead (SnPb) solder.
- Lead-locking provisions (anchors) at all pins. Holes were also present in the GaAs leadframe.
- Thermosonic ball bonding using 1.2 mil O.D. gold wire.
- Pins 1 - 40 were used with the GaAs IC. Pins 41 - 80 were used with the Si IC. Pins 50, 51, 60, 61, 70 were connected to the Si IC's leadframe biasing the P-substrate to GND.
- Sawn dicing (full-depth).
- Silver-filled epoxy die attach.

Die Process:

- Fabrication process: Selective oxidation CMOS process employing multiple wells in a P-epi on a P-substrate.
- Final passivation: A layer of nitride over a layer of glass.
- Metallization: Two levels of metal defined by standard dry-etch techniques. Both consisted of aluminum with a titanium-nitride cap and barrier. Standard vias and contacts were used (no plugs).

TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them. The SOG had been etched back.

- Polysilicon: A single layer of polycide (titanium silicide on poly) was used to form all gates on the die and the bottom plates of capacitors. Poly resistors were formed without the titanium silicide by the use of a patterned oxide mask (Figure 29). Definition was by a dry etch of normal quality. Direct poly-to-diffusion (buried) contacts were not used.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. Diffusions were silicided (salicide process) with titanium. An LDD process was used with oxide sidewall spacers left in place.

- Wells: A complex well structure employing multiple wells in a P-epi on a P-substrate. A step was present at well boundaries.

- Redundancy: Fuses were not used.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 6**

Questionable Items: None.

General items:

- The device was encapsulated in an 80-pin plastic Square Quad Flat Package (SQFP).

- Overall package quality: Good. Internal plating of the copper leadframe was silver. External pins were tinned with tin-lead (SnPb). No cracks or voids present. No gaps were noted at lead exits.

- Lead-locking provisions (anchors) were present at all pins.

- Wirebonding: Thermosonic ball method using 1.2 mil O.D. gold wire. Nine bond lifts occurred during wire pull tests; however, metal 2 at the bond pads had been etched during decapsulation. The remaining pad metal (metal 1) was "ripped out" during bond lifts indicating that an intermetallic bond had been formed. It was noted that all bond pull strengths were within MIL-STD requirements.

- Pins 50, 51, 60, 61, 70 were connected to the Si IC's leadframe biasing the P-substrate to GND.

- Die attach: Silver-filled epoxy of good quality. No voids were noted in the die attach and no problems are foreseen.

- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

ANALYSIS RESULTS II

Die Process and Design: **Figures 7 - 33**

Questionable Items:[1]

- Metal 2 aluminum thinned up to 100 percent[2] at some via locations. Barrier metal remained intact to provide continuity.

- Metal 1 aluminum thinned up to 100 percent[2] at some contact locations. Barrier metal remained intact to provide continuity.

Special Features:

- Titanium silicided diffusion structures.

General items:

- Fabrication process: Devices were fabricated using selective oxidation CMOS process employing multiple wells in a P-epi on a P-substrate.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.

- Die coat: No die coat was present.

- Final passivation: A layer of nitride over a layer of glass. Overlay integrity test indicated defect-free passivation. Edge seal was good as the passivation extended

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

beyond the metal at the edge of the die. The voids above metal 2 vias are not considered areas of concern.

- Metallization: Two levels of metal were used. Both consisted of aluminum with titanium-nitride caps and barriers. Standard vias and contacts were used (no plugs).

- Metal patterning: Both metal levels were patterned by a dry etch of normal quality.

- Metal defects: No voiding, notching, or neckdown was noted in either of the metal layers. No silicon nodules were noted following removal of either metal.

- Metal step coverage: Metal 2 aluminum thinned up to 100 percent at several via locations. Barrier metal maintained continuity. Metal 1 aluminum also thinned up to 100 percent at some contact locations. Typical metal 1 thinning was 90 percent.

- Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them. The SOG had been etched back.

- Pre-metal glass: A layer of reflow glass (BPSG) over densified oxide was used under metal 1. Reflow was performed prior to contact cuts only.

- Contact defects: Contact and via cuts were defined by a two-step process. No over-etching of the contacts or vias was noted. No problems were found, except for the one instance shown in Figure 16.

- Polysilicon: A single layer of polycide (titanium silicide on poly) was used to form all gates on the die and bottom plates of capacitors. Poly resistors were formed without the titanium silicide by use of a patterned oxide mask. Definition was by a dry-etch of normal quality. Direct poly-to-diffusion (buried) contacts were not used.

ANALYSIS RESULTS II (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. Diffusions were silicided (salicide process) with titanium. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

- Isolation: LOCOS (local oxide isolation). A step was present at the well boundaries.

- Redundancy: Fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal to Poor

DETAIL OF EVALUATION

Package integrity	G
Package markings	N
Die placement	N
Die attach quality	G
Wire spacing	G
Wirebond placement	G
Wirebond quality	N
Dicing quality	G
Wirebond method	Thermosonic ball bond method using 1.2 mil O.D. gold wire.
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects	NP
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	N
Metal registration	N
Contact coverage	N
Contact registration	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

R6732-13
©ROCKWELL 93
9642 B21401-12
MEXICO (LOGO)

WIREBOND STRENGTH

Wire material:	1.2 mil O.D. gold
Die pad material:	aluminum
Material at package lands:	silver

Sample #	**1**
# of wires tested:	20
Bond lifts:	9
Force to break - high:	15.0g
- low:	3.0g
- avg.:	9.0g
- std. dev.:	3.5

DIE MATERIAL ANALYSIS

Overlay passivation:	A layer of silicon-nitride over a layer of glass.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Polycide:	Titanium (Ti) silicide on poly.
Diffusions:	Titanium (Ti) silicide.

HORIZONTAL DIMENSIONS

Die size:	3.3 x 4.2 mm (131 x 164 mils)
Die area:	14 mm^2 (21,484 $mils^2$)
Min pad size:	0.12 x 0.12 mm (4.9 x 4.9 mils)
Min pad window:	0.11 x 0.11 mm (4.3 x 4.3 mils)
Min pad space:	0.07 mm (2.9 mils)
Min metal 2 width:	2.1 microns
Min metal 2 space:	1.0 micron
Min metal 2 pitch:	3.1 microns
Min metal 1 width:	2.1 microns
Min metal 1 space:	1.0 micron
Min metal 1 pitch:	3.1 microns
Min via:	0.85 micron (round)
Min contact:	1.0 micron (round)
Min poly 1 width:	0.8 micron
Min poly 1 space:	1.5 micron
Min diffusion space:	1.4 micron
Min gate length* - (N-channel):	0.8 micron
- (P-channel):	1.0 micron

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:		0.5 mm (19.7 mils)

Layers

Passivation 2:		0.55 micron
Passivation 1:		0.35 micron
Metal 2 - cap:		0.07 micron (approx.)
	- aluminum:	0.75 micron
	- barrier:	0.1 micron
Intermetal dielectric	- glass 2:	0.65 micron
	- SOG:	0 - 1.3 micron
	- glass 1:	0.4 micron
Metal 1 - cap:		0.07 micron (approx.)
	- aluminum:	0.45 micron
	- barrier:	0.1 micron
Pre-metal glass:		0.7 micron (average)
Poly	- silicide:	0.07 micron
	- poly:	0.13 micron
Poly	- resistor:	0.25 micron
Local oxide:		0.45 micron
N+ S/D diffusion:		0.2 micron
P+ S/D diffusion:		0.2 micron
P-well:		3.0 microns (approx.)
N-well:		4.5 microns (approx.)
P-epi:		6.5 microns (approx.)

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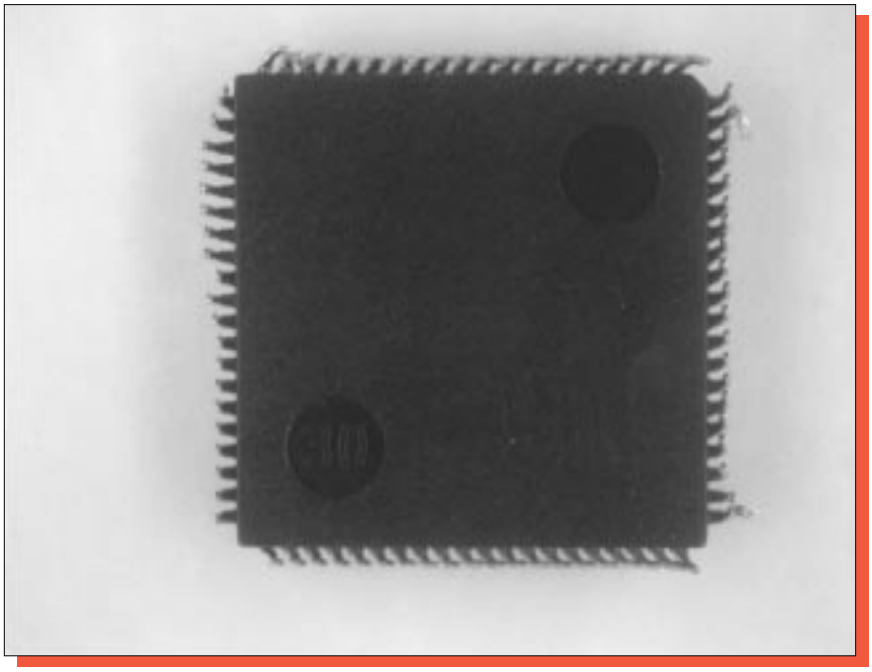


Figure 1. Package photographs of the Rockwell R6732-13. Mag. 4.5x.

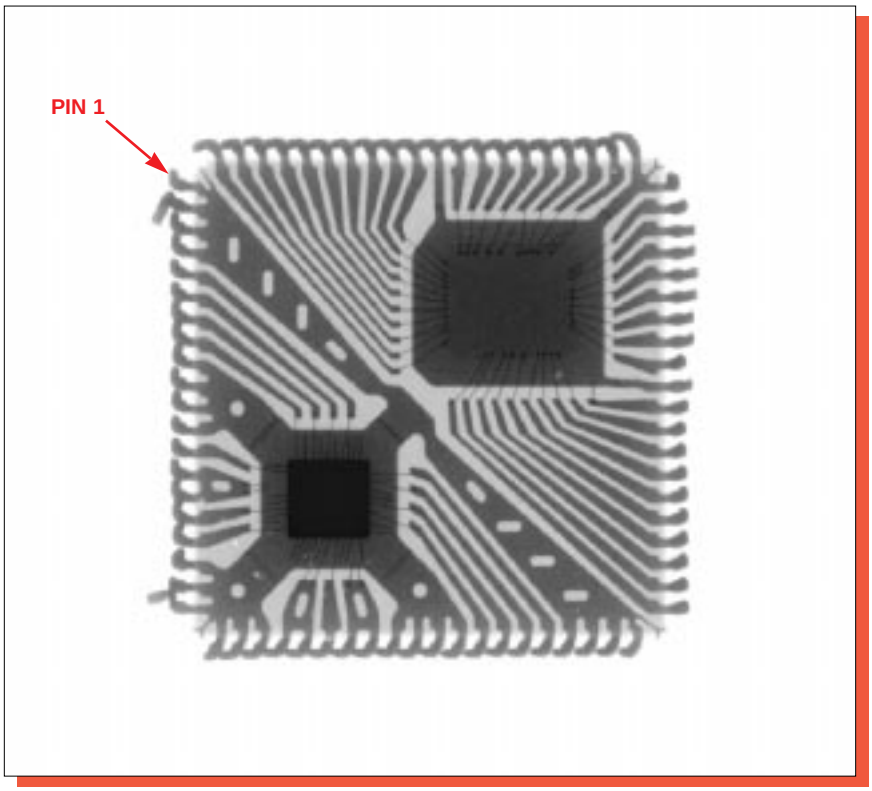


Figure 2. X-ray view of the package. Mag. 4.5x.

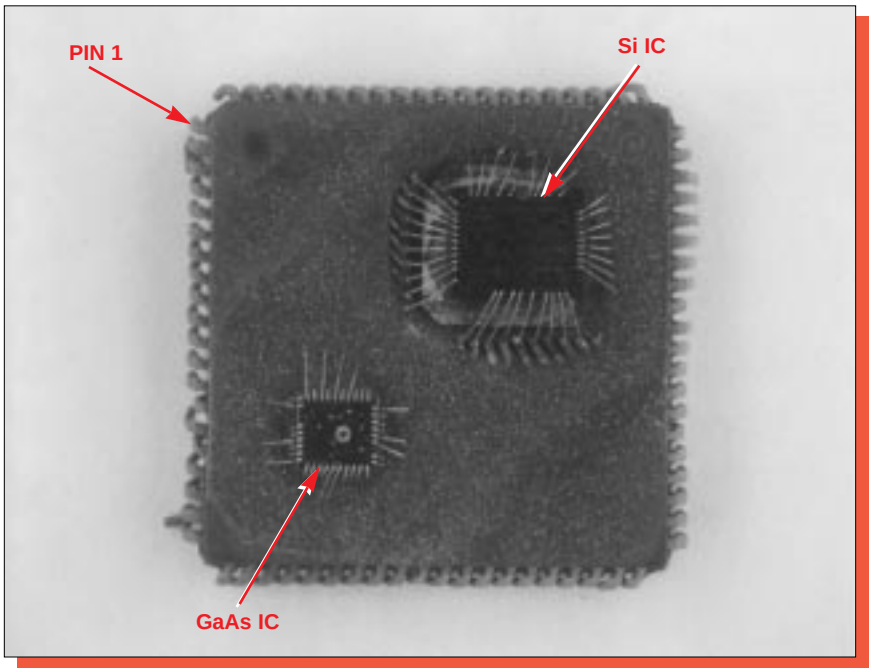
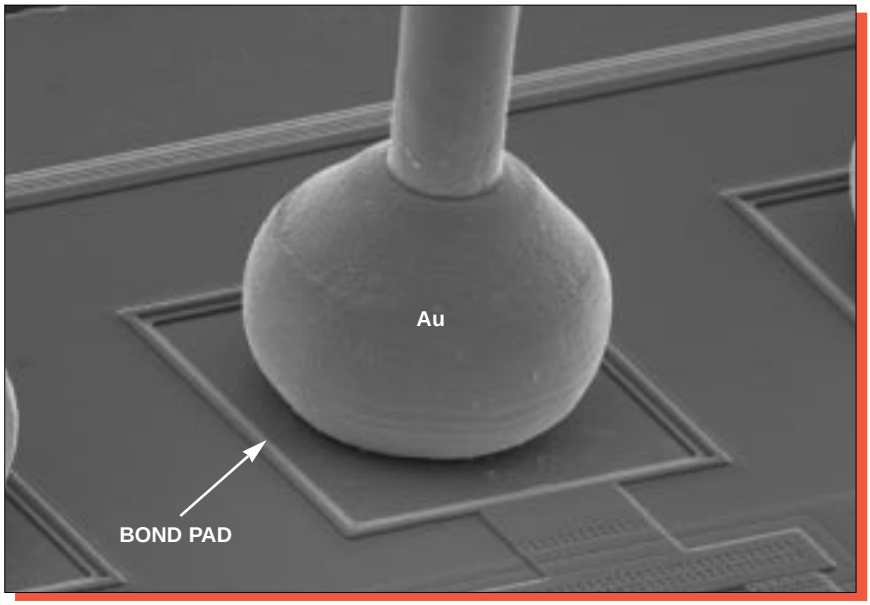
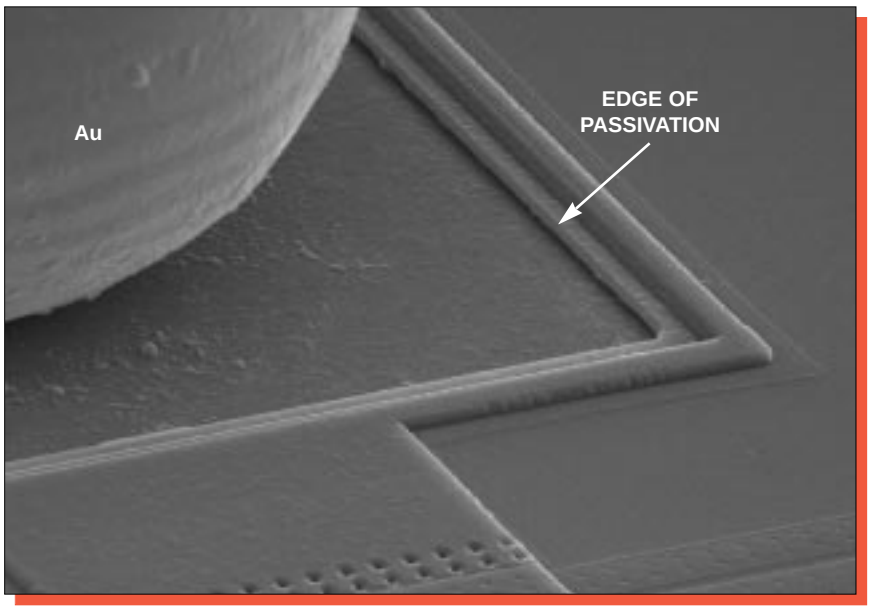


Figure 3. Optical view illustrating decapsulated package. Mag. 4.5x.

Mag. 620x



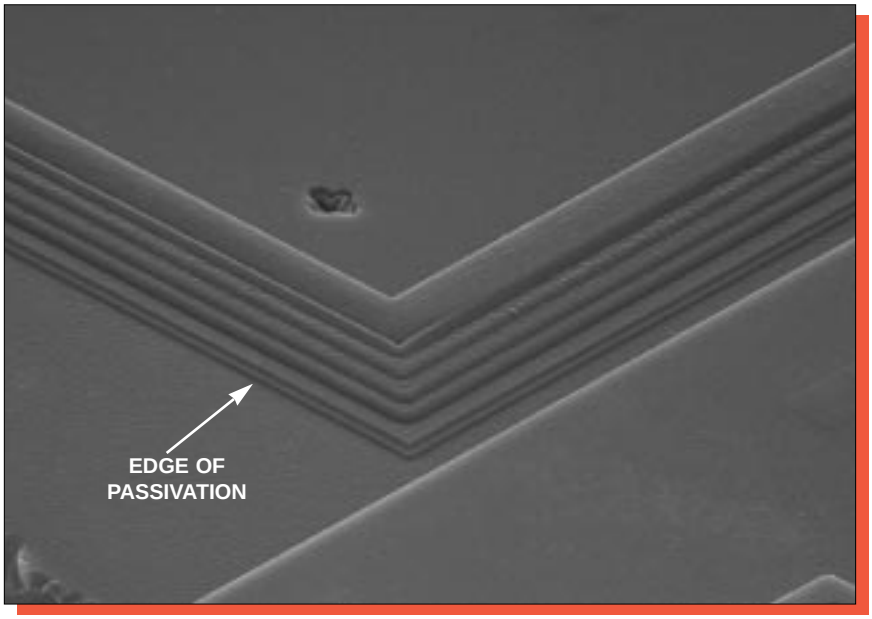
Mag. 480x



Mag. 1600x

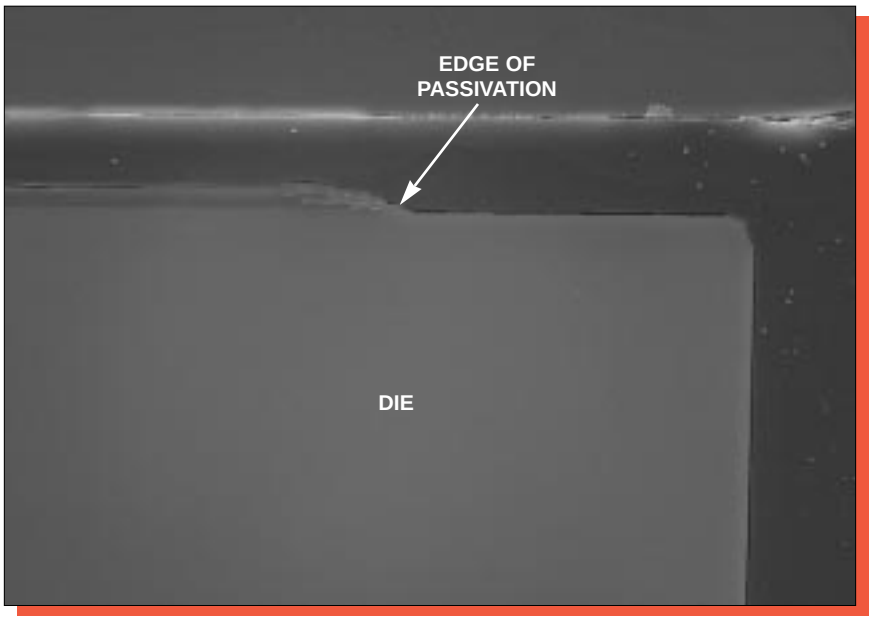
Figure 4. SEM views of typical wirebonding. 60°.

Mag. 120x

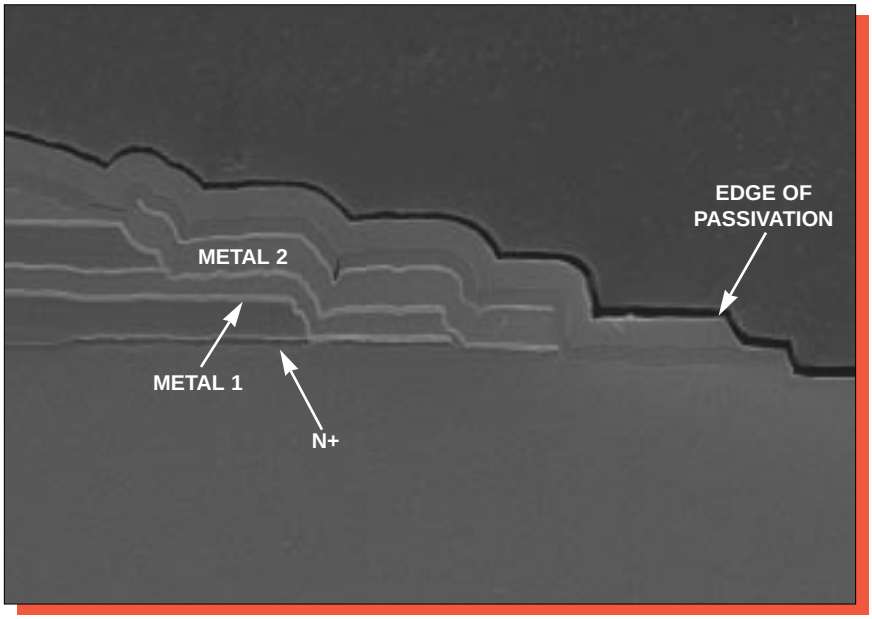


Mag. 1100x

Figure 5. SEM views illustrating dicing and edge seal. 60°



Mag. 800x



Mag. 6500x

Figure 6. SEM section views of the edge seal.

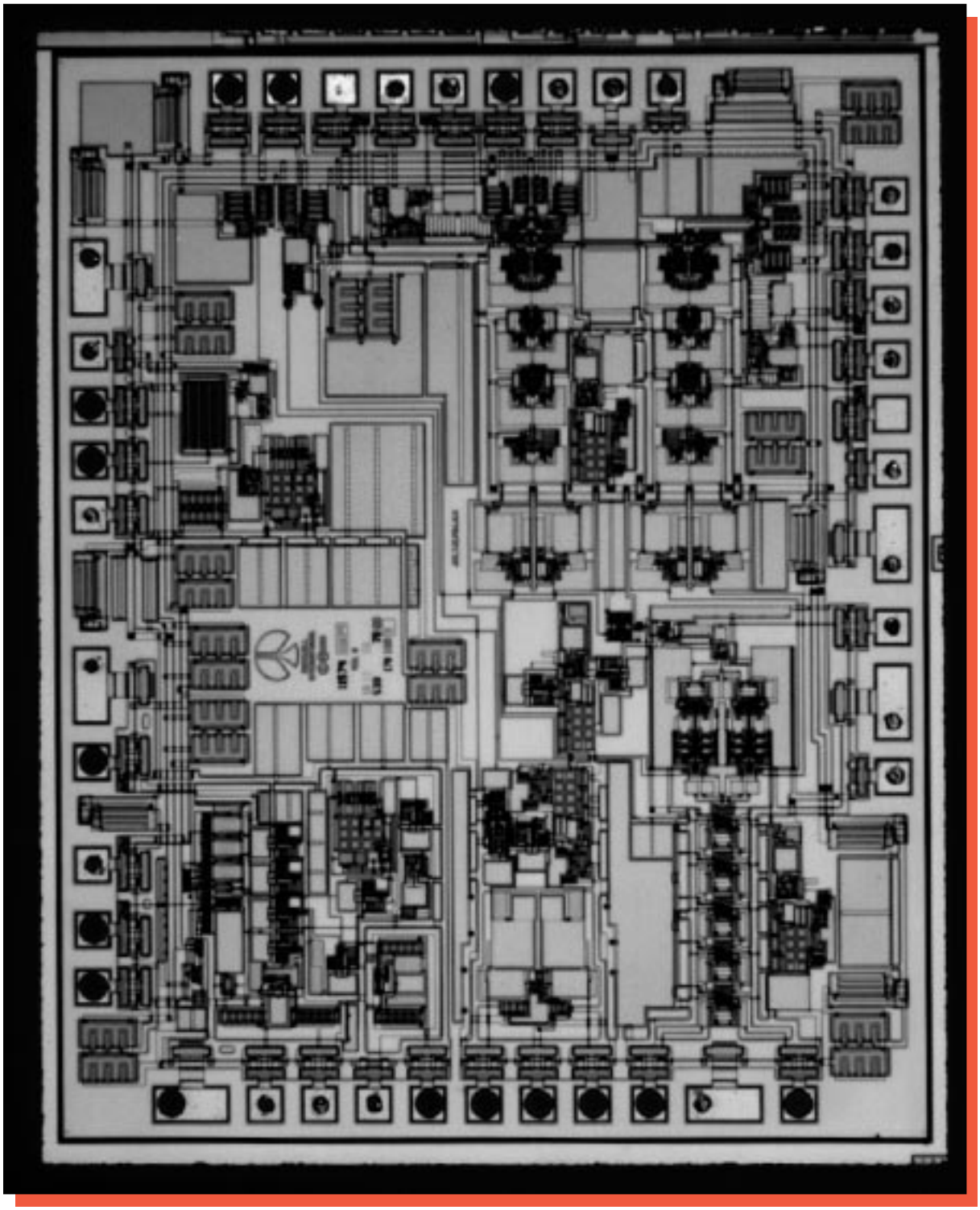
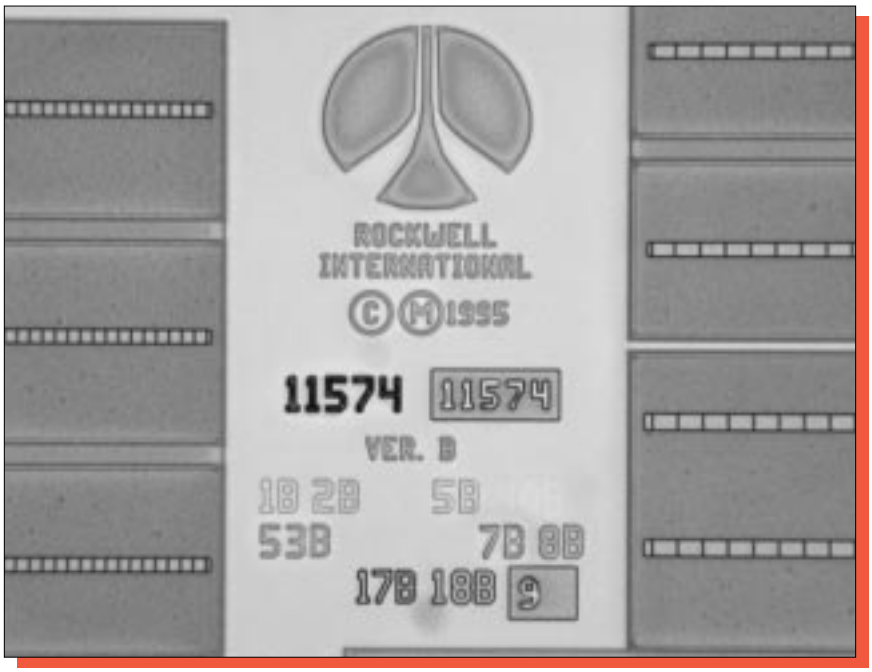
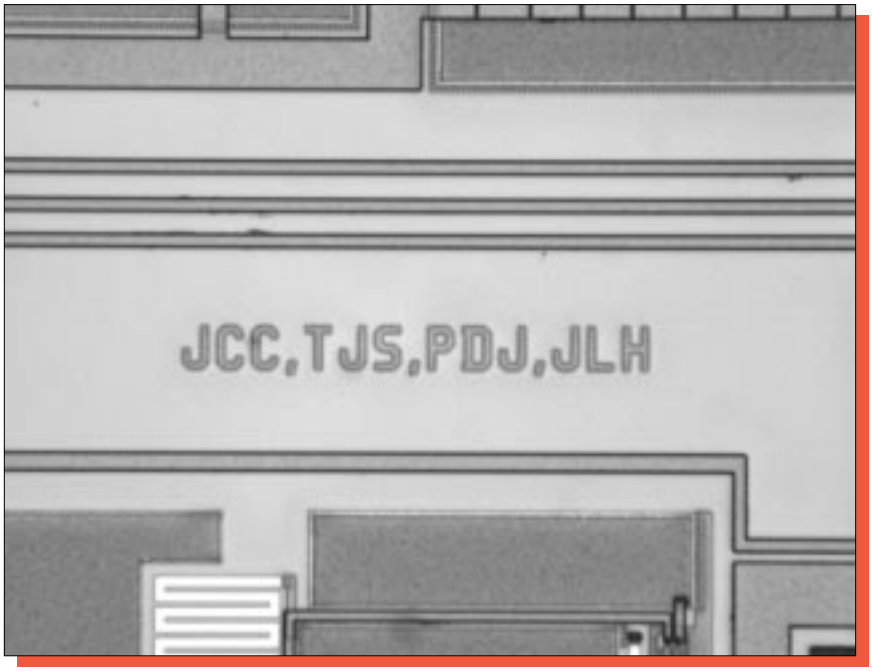


Figure 7. Whole die photograph of the Silicon IC. Mag. 45x.



Mag. 150x



Mag. 300x

Figure 8. Optical views of die markings.

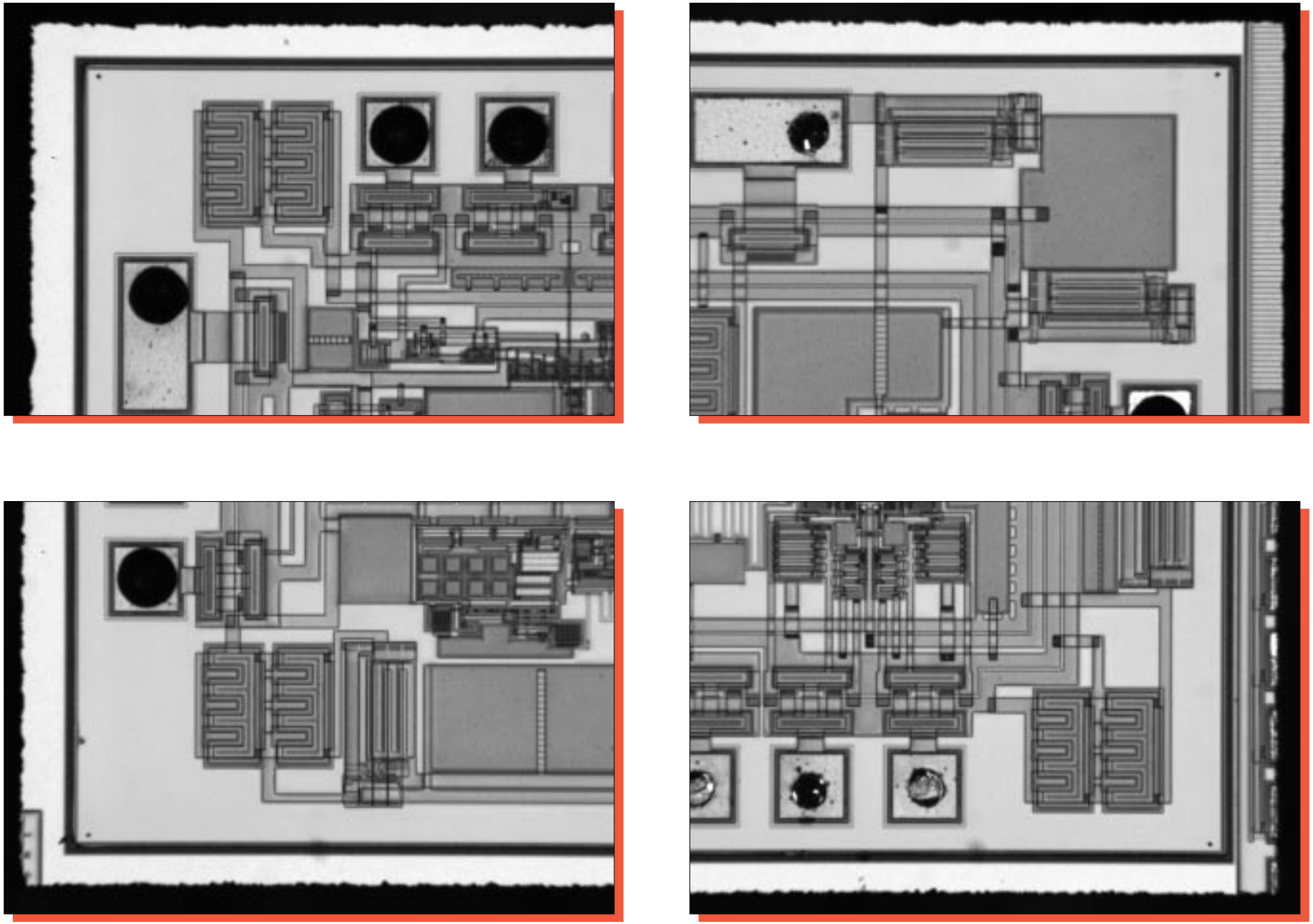
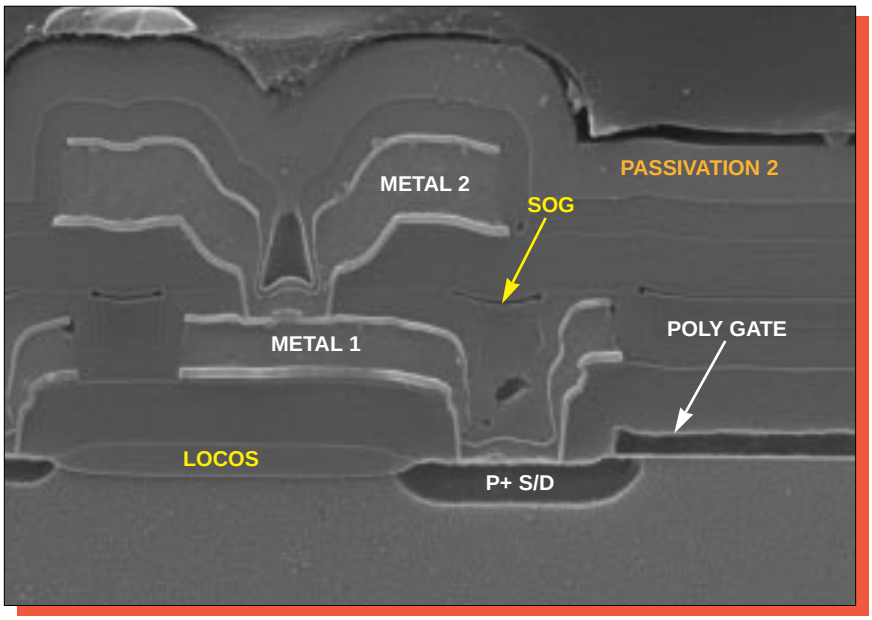
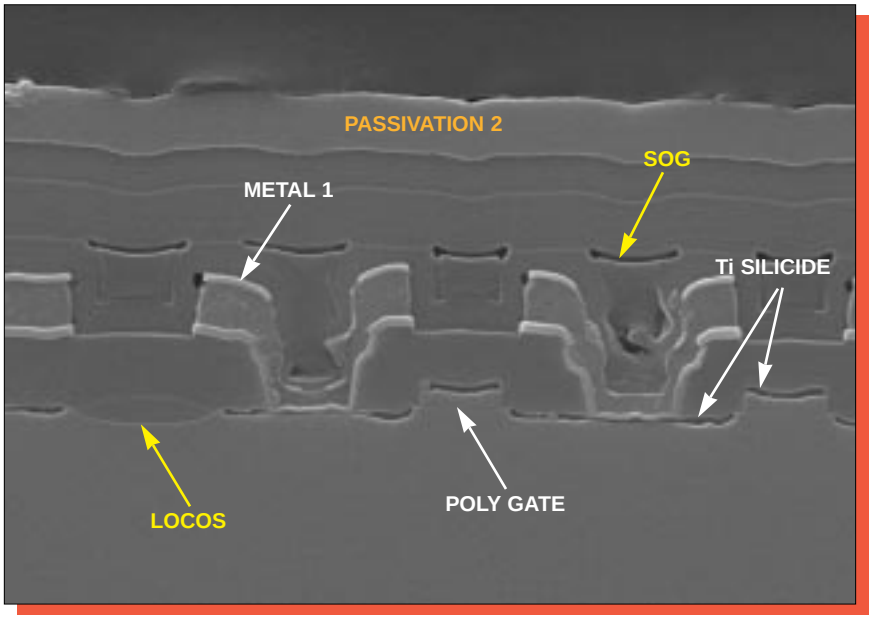


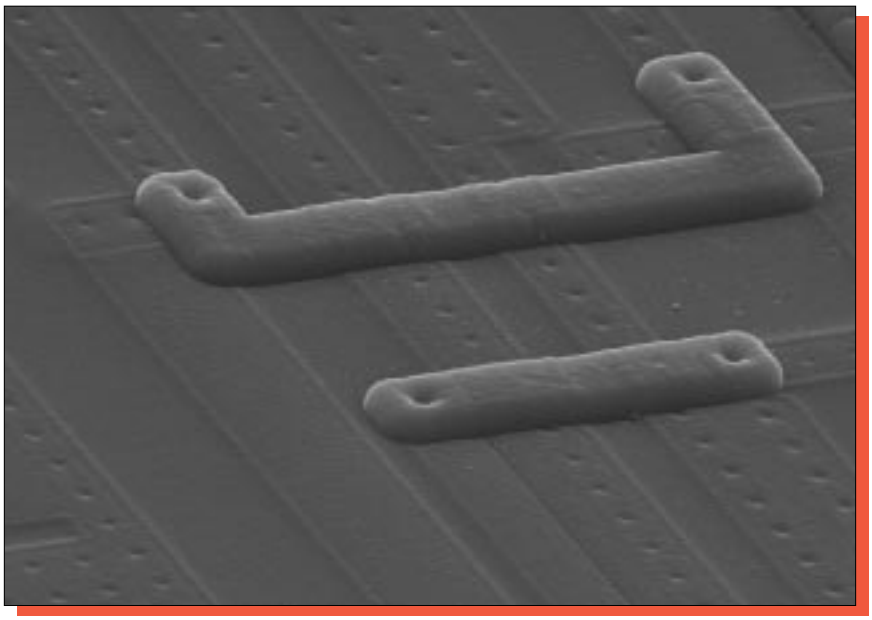
Figure 9. Optical views of die corners. Mag. 100x.



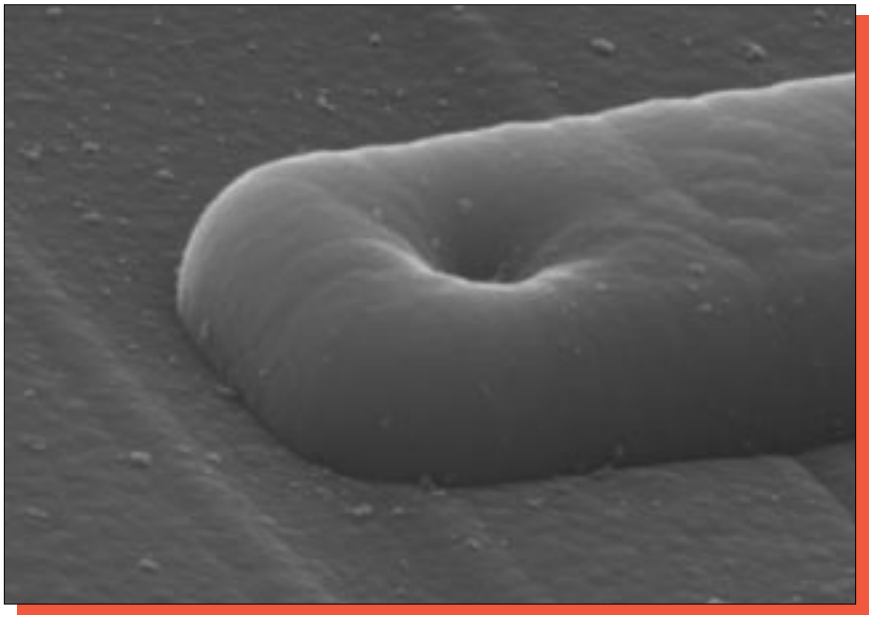


glass etch

Figure 10. SEM section views illustrating general structure. Mag. 13,000x.

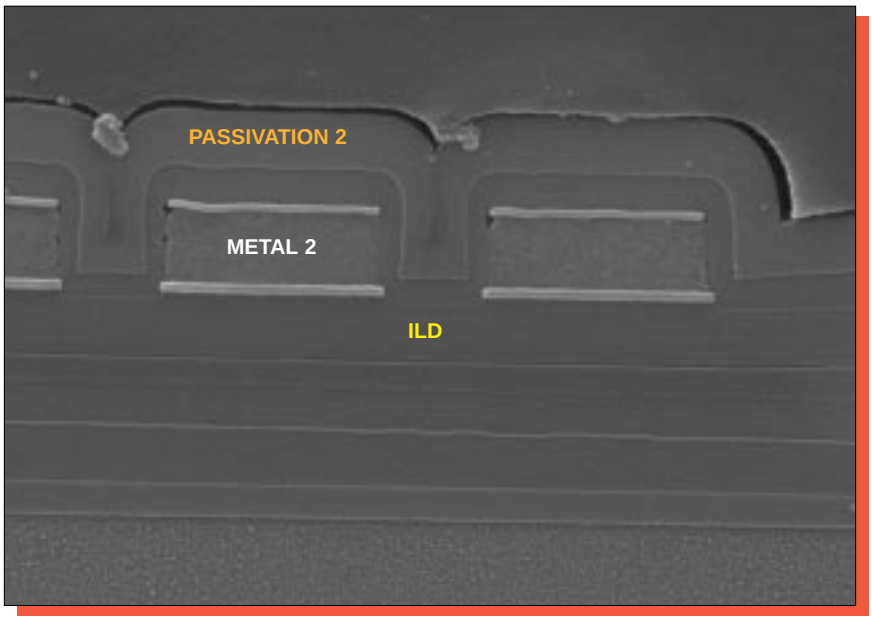


Mag. 3700x

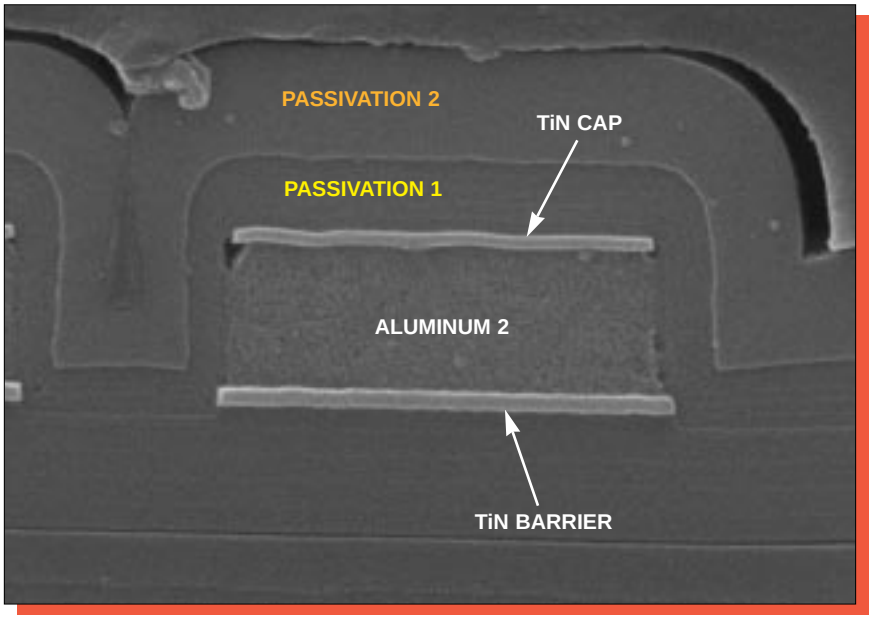


Mag. 20,000x

Figure 11. SEM views illustrating final passivation. 60°.



Mag. 13,000x



Mag. 26,000x

Figure 12. SEM section views of metal 2 line profiles.

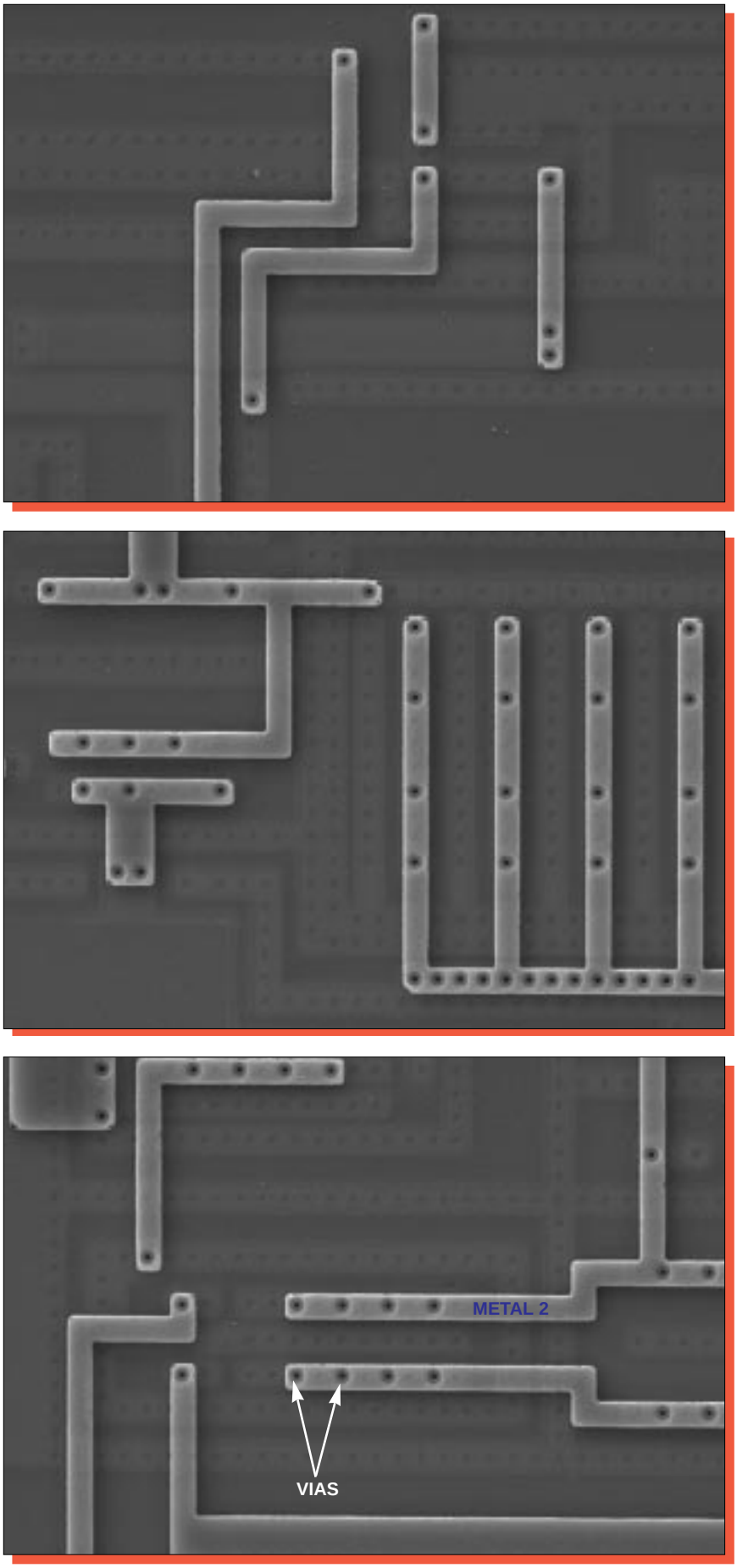
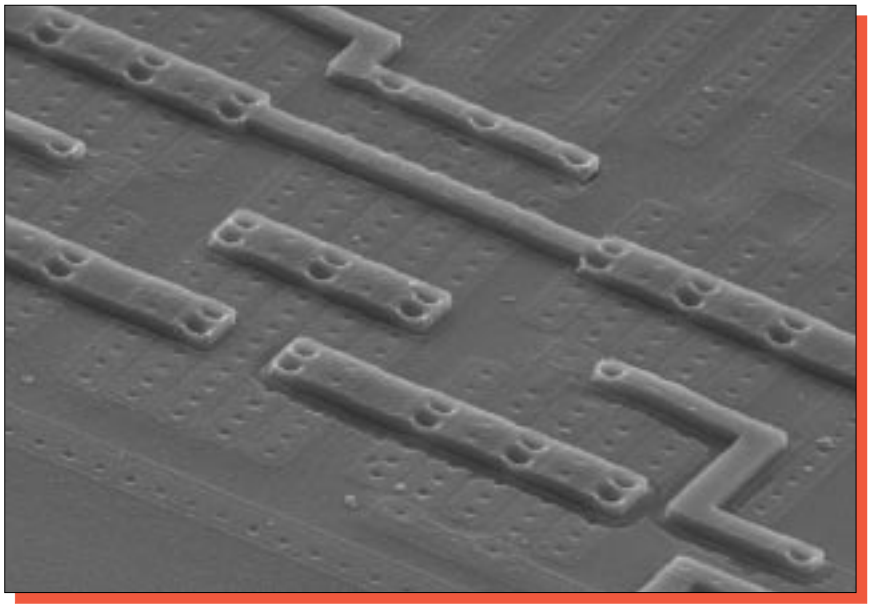
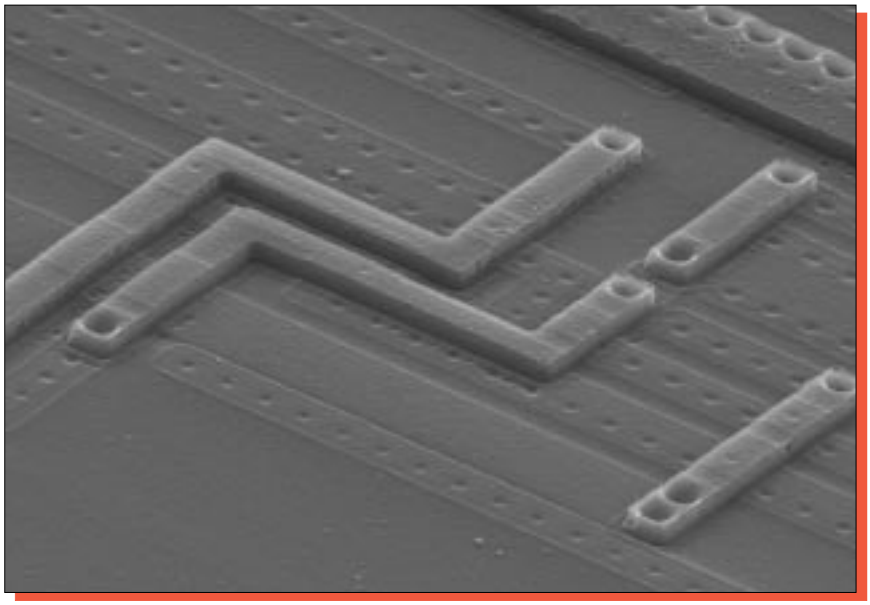


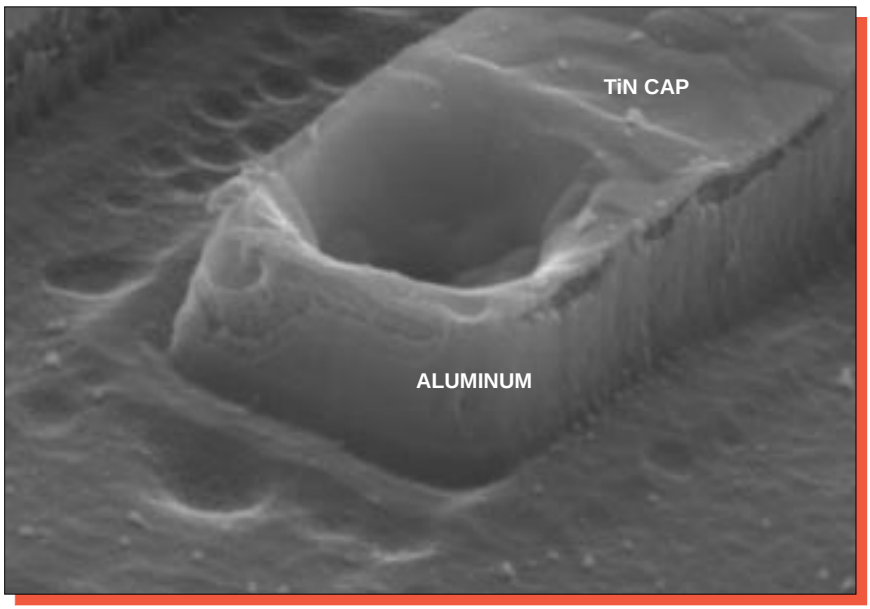
Figure 13. Topological SEM views of metal 2 patterning. Mag. 1600x, 0°.



Mag. 2000x

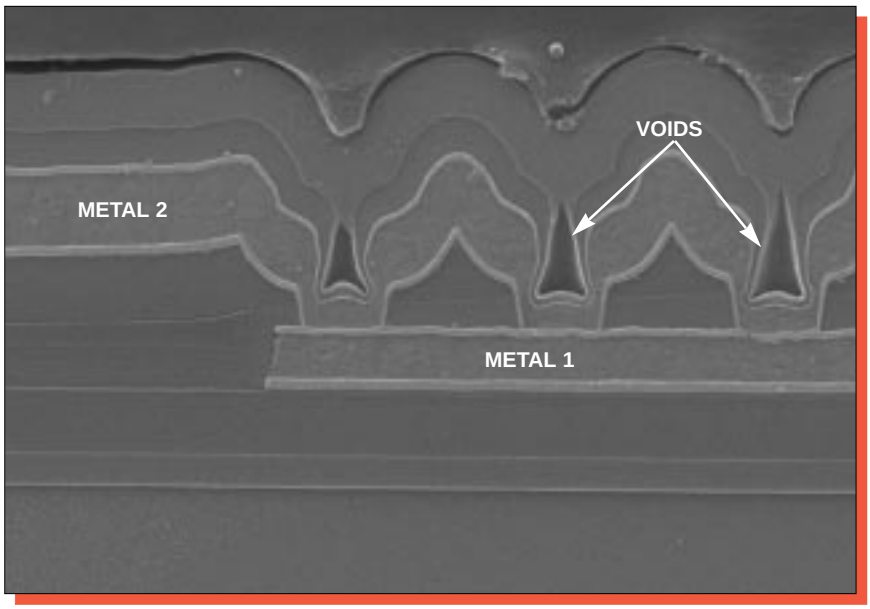


Mag. 2700x

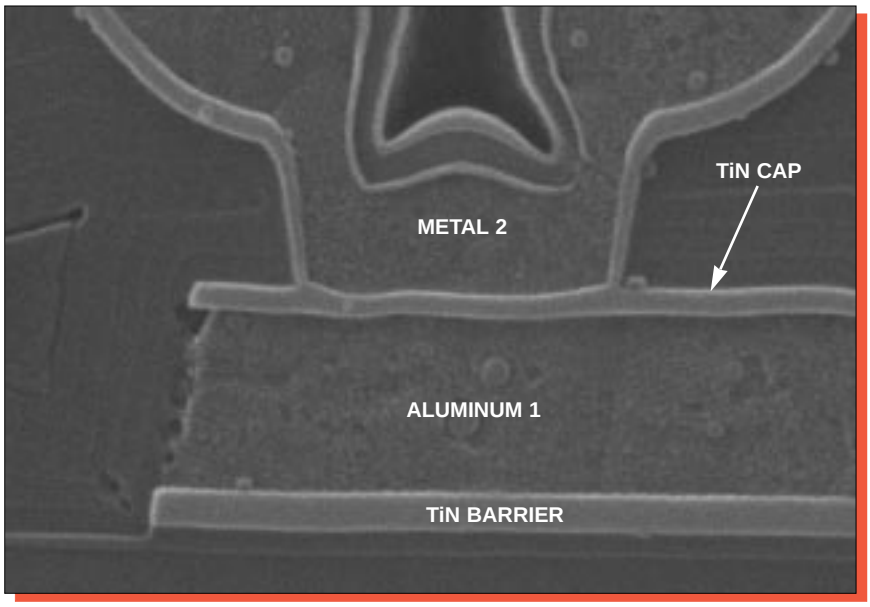


Mag. 22,000x

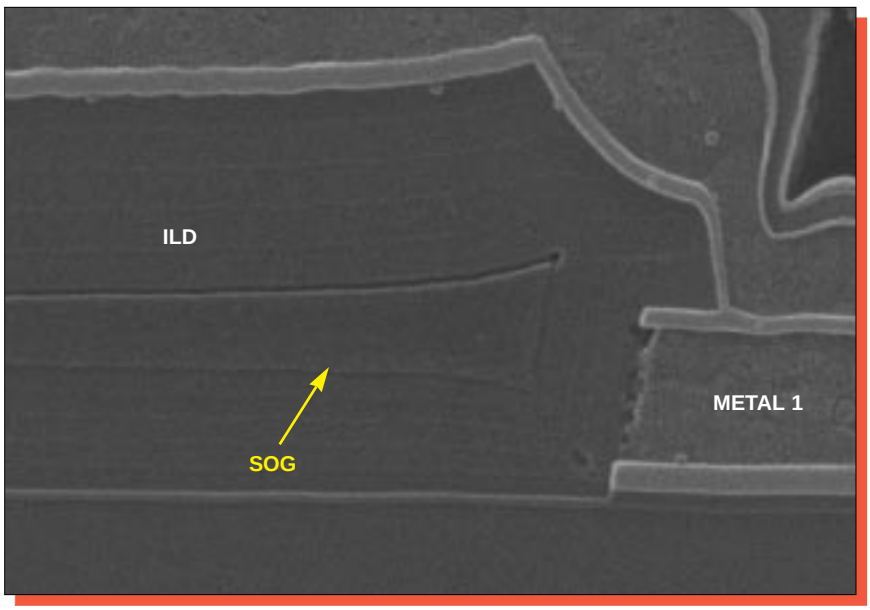
Figure 14. Perspective SEM views of metal 2 step coverage. 60°.



Mag. 13,000x

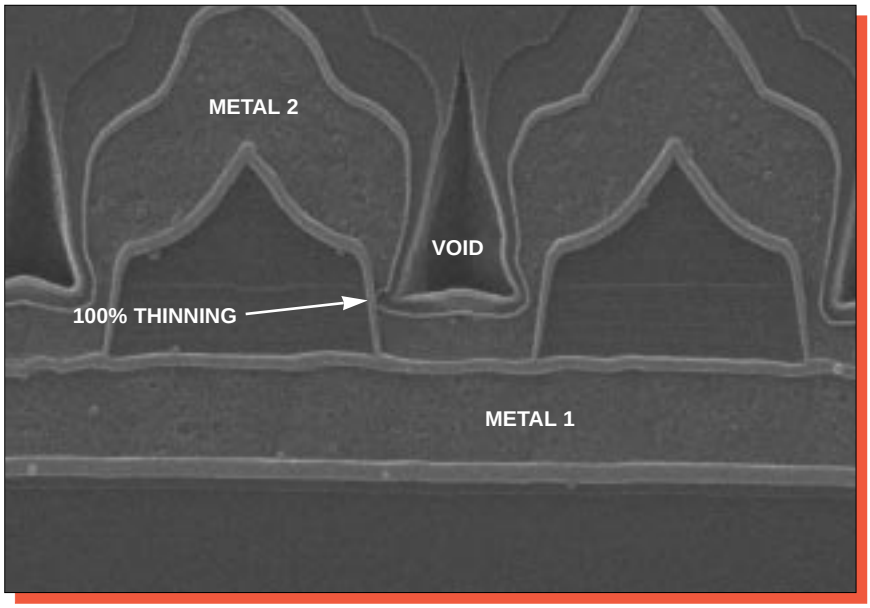


Mag. 52,000x

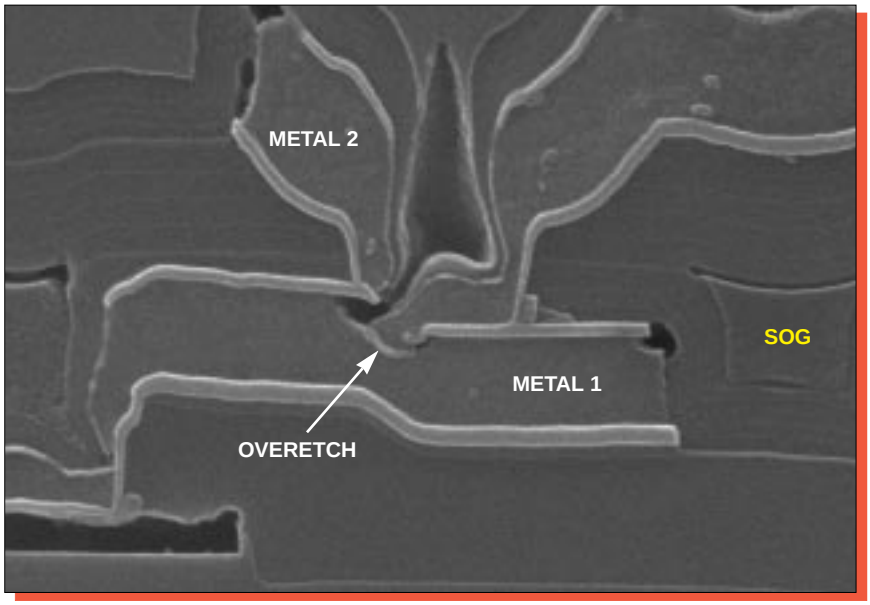


Mag. 40,000x

Figure 15. SEM section views illustrating typical vias and interlevel dielectric composition.



Mag. 26,000x



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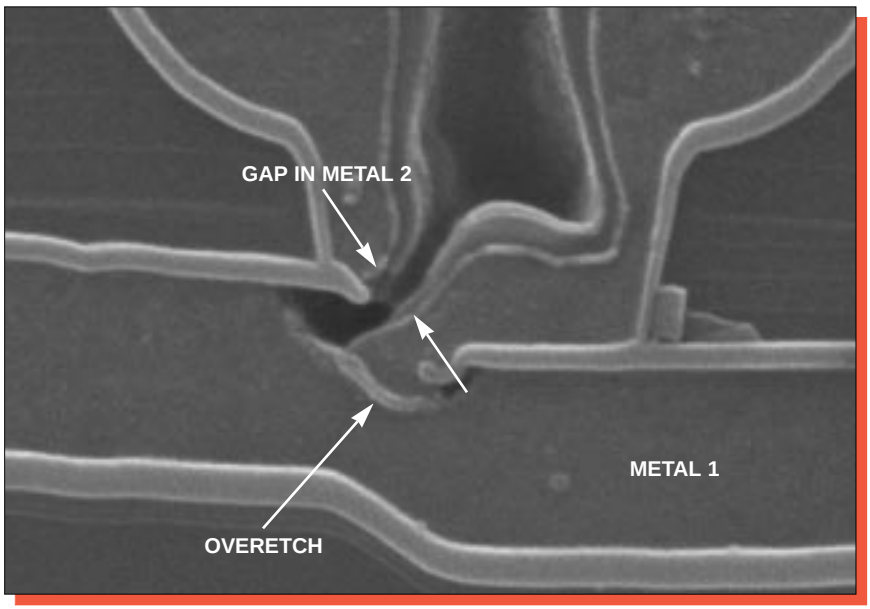
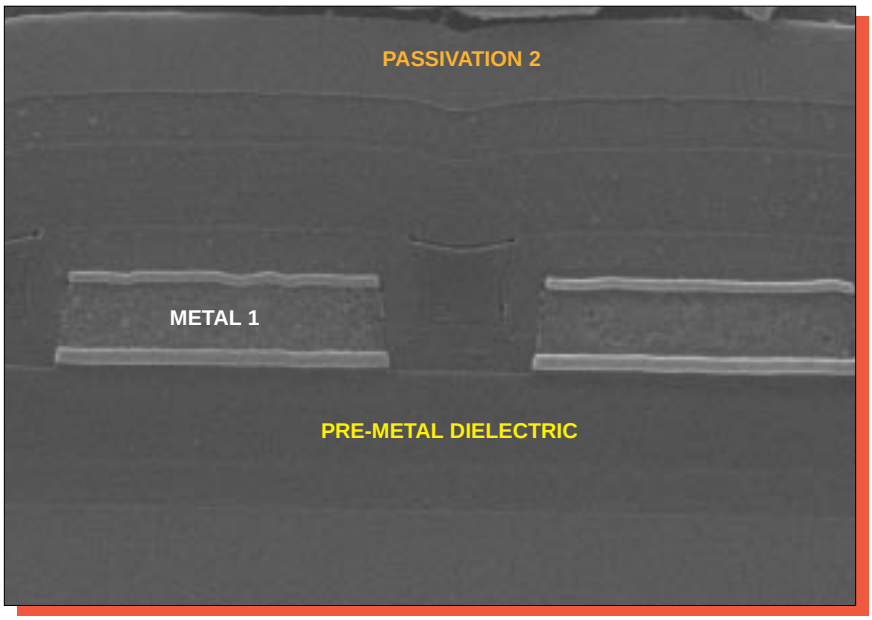
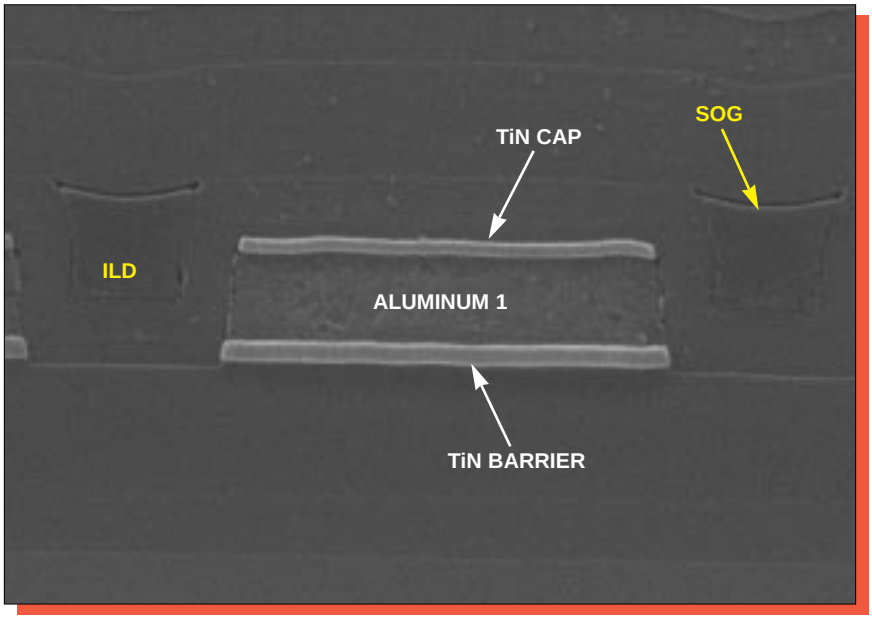


Mag. 52,000x

Figure 16. SEM section views of via defects.

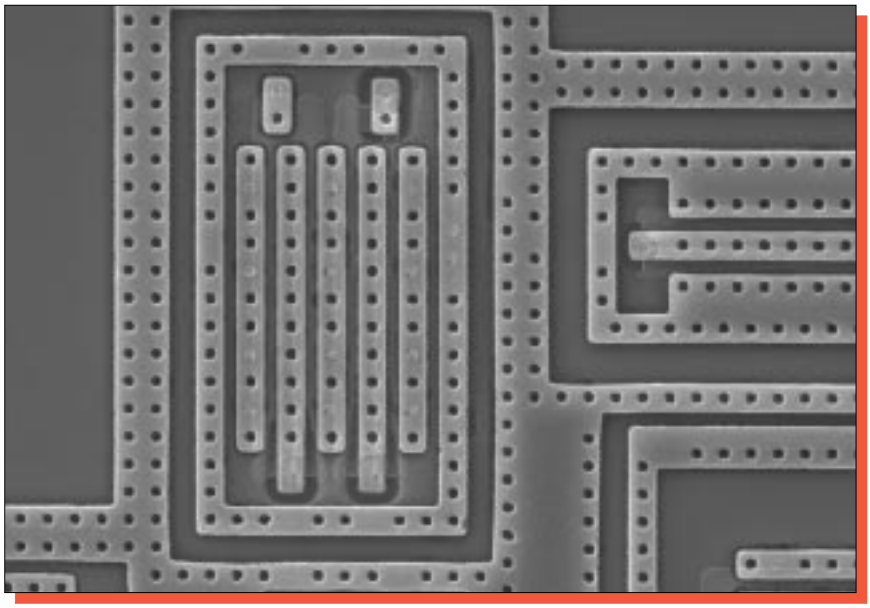


Mag. 20,000x

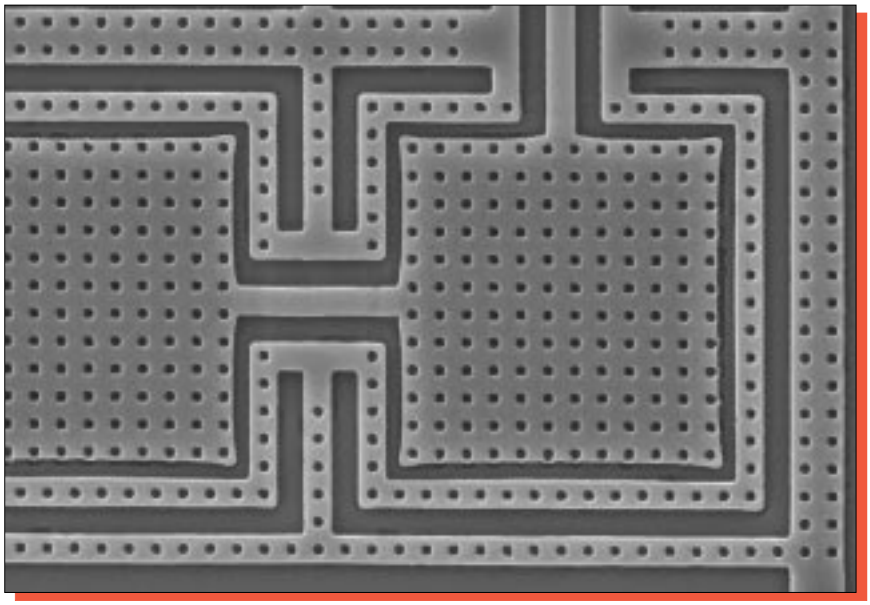


Mag. 26,000x

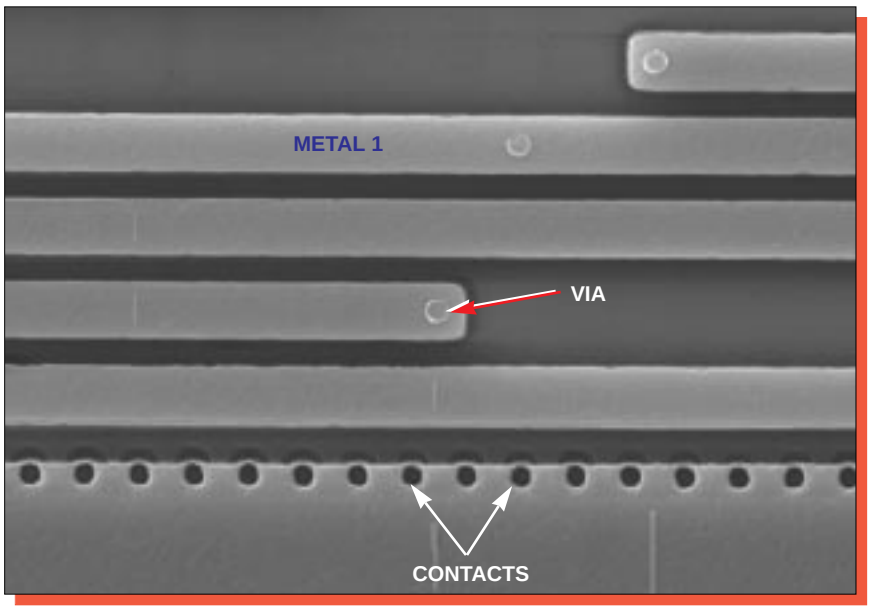
Figure 17. SEM section views of metal 1 line profiles.



Mag. 1600x

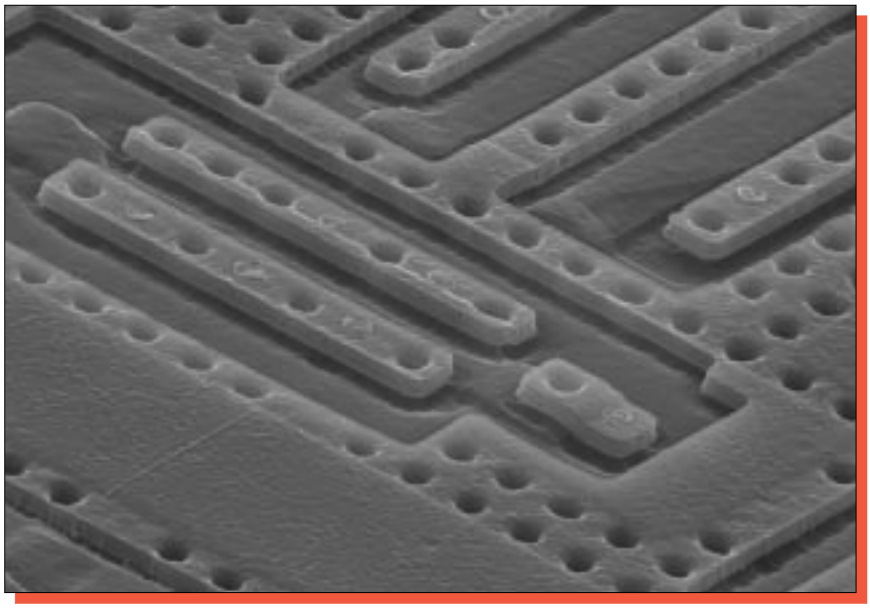


Mag. 1600x

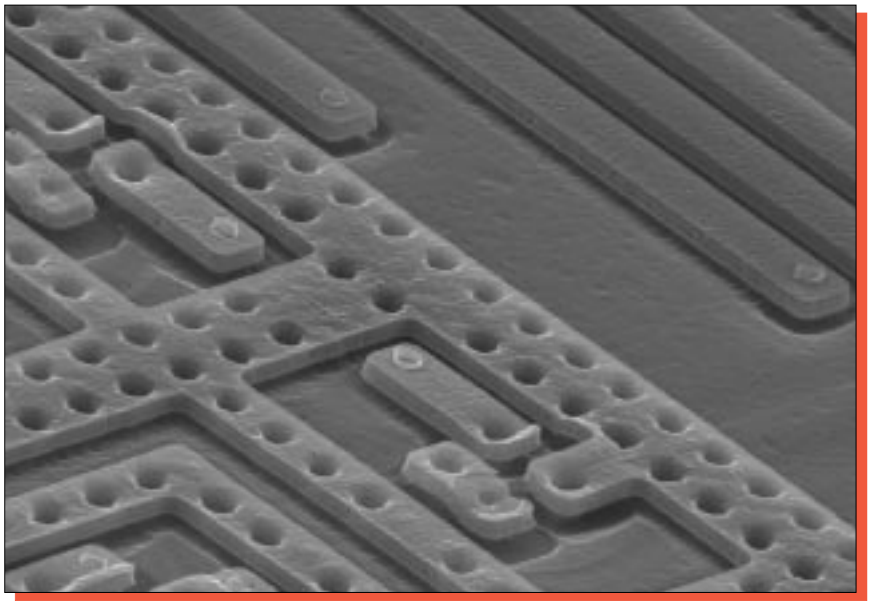


Mag. 3200x

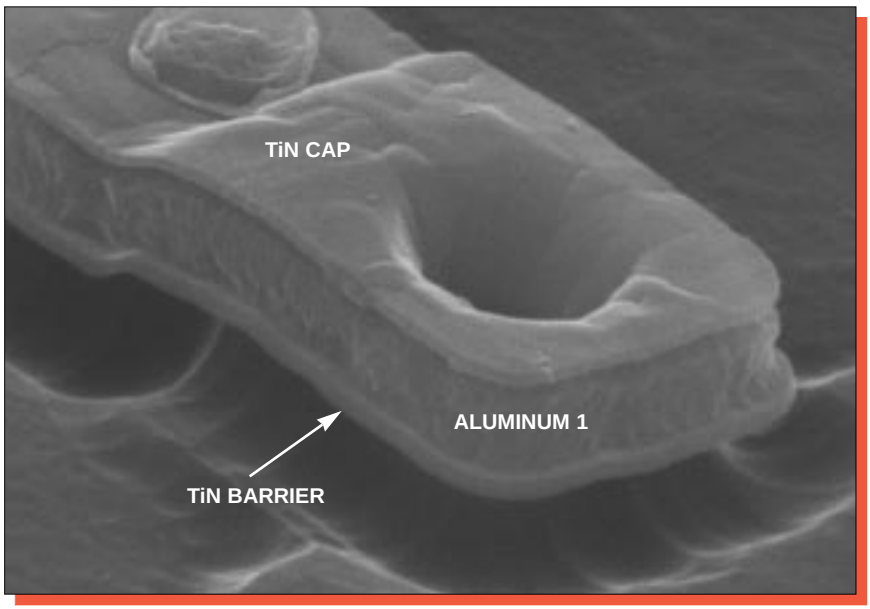
Figure 18. Topological SEM views of metal 1 patterning. 0°.



Mag. 4000x



Mag. 4000x



Mag. 27,000x

Figure 19. Perspective SEM views of metal 1 step coverage. 60°.

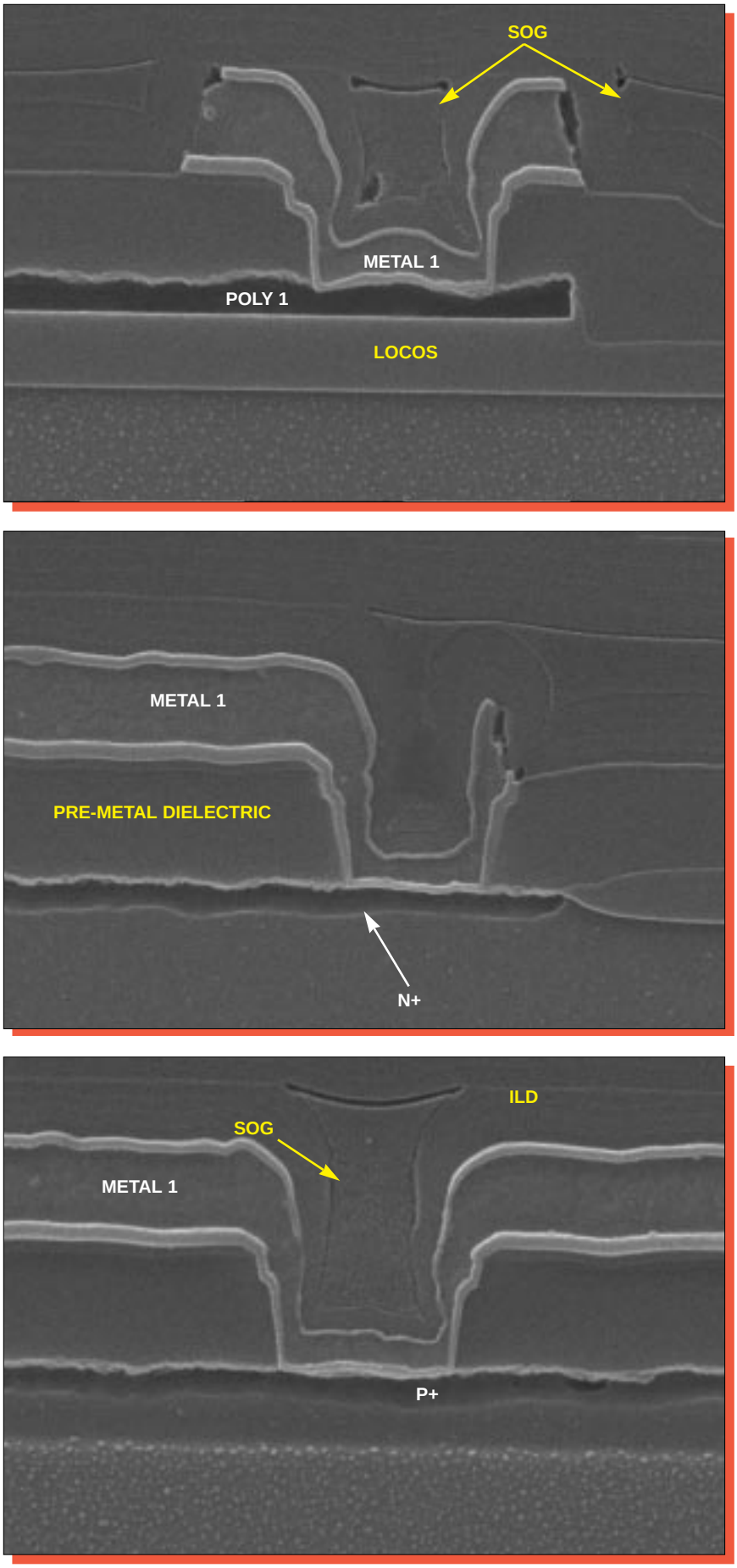
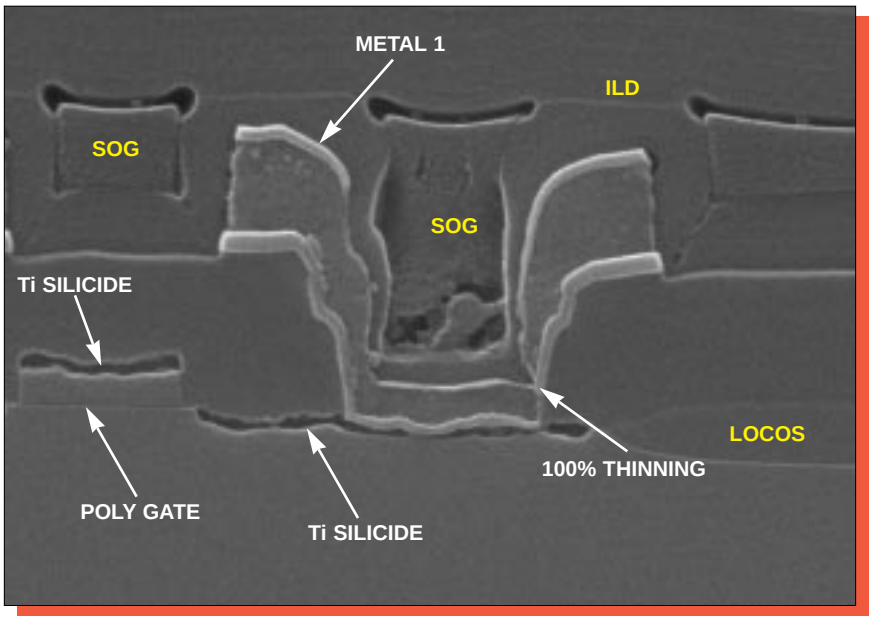
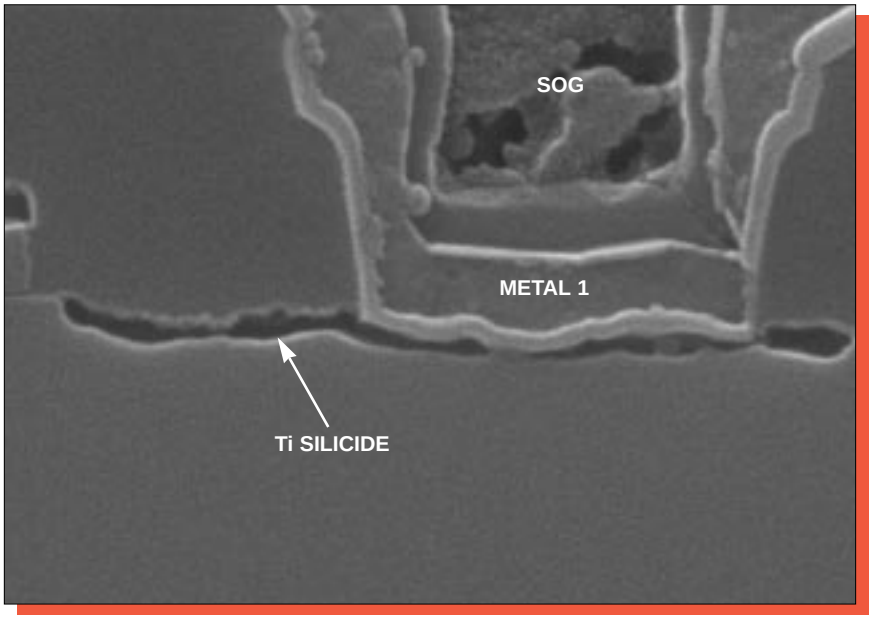


Figure 20. SEM section views of typical metal 1 contacts. Mag. 26,000x.



Mag. 26,000x



Mag. 52,000x

Figure 21. SEM section views of a typical metal 1 contact. Glass etch.

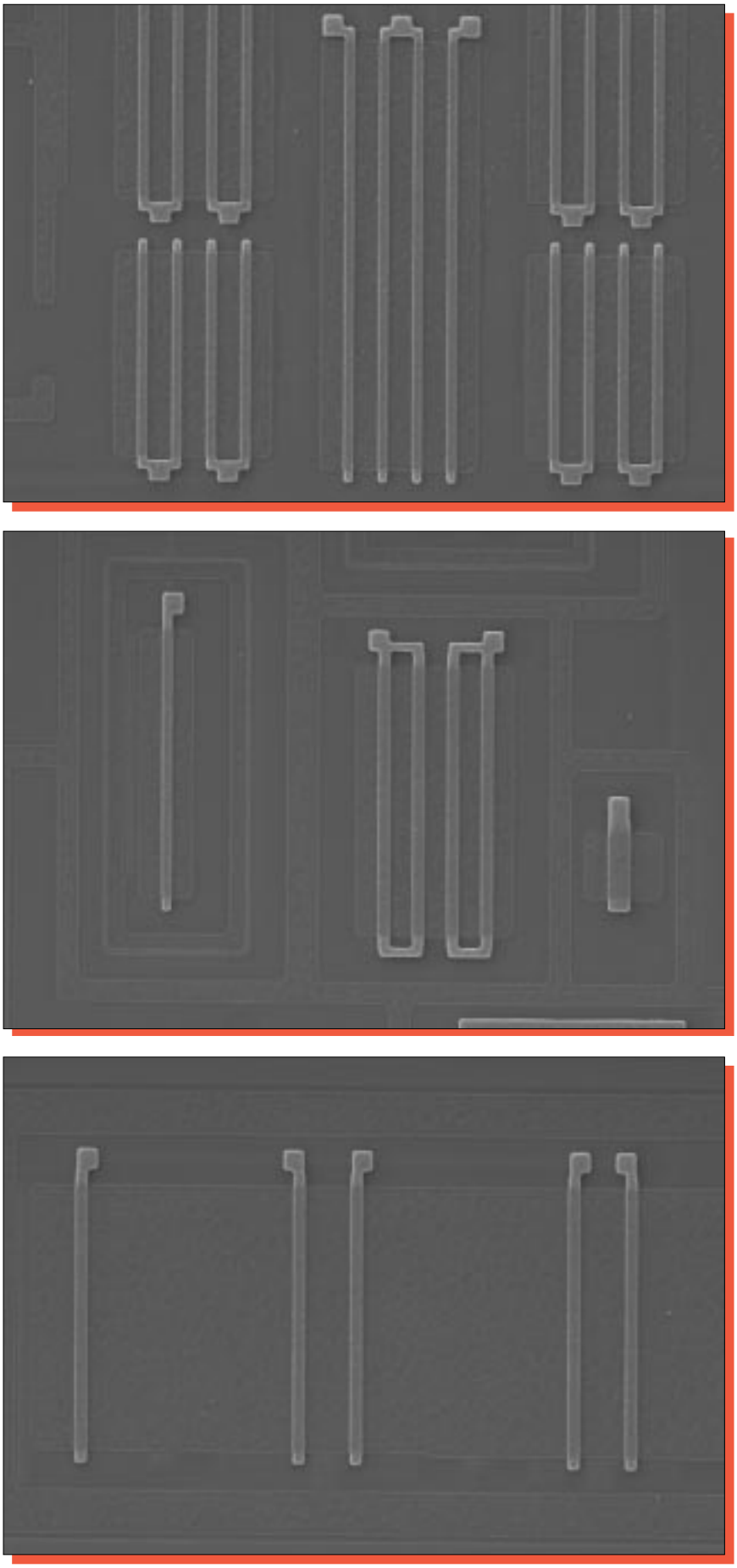
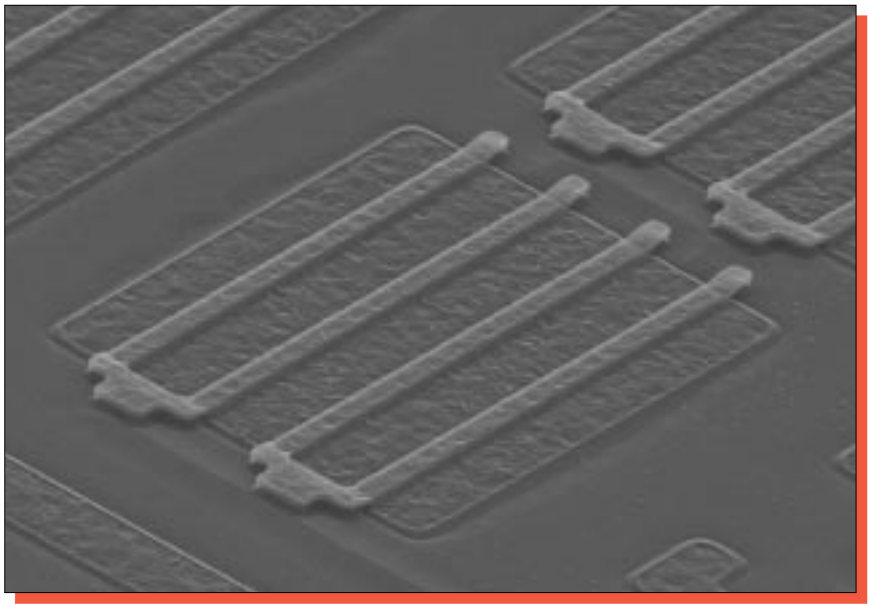
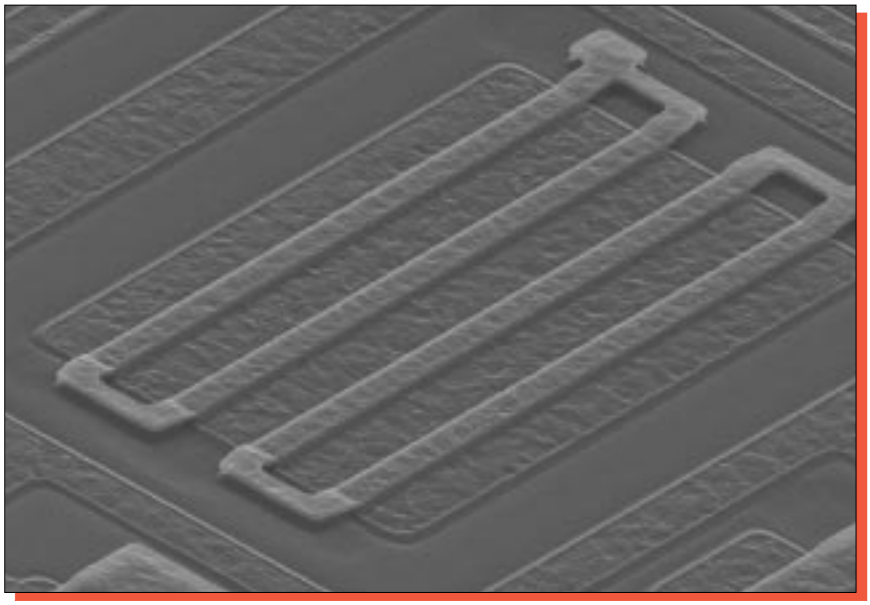


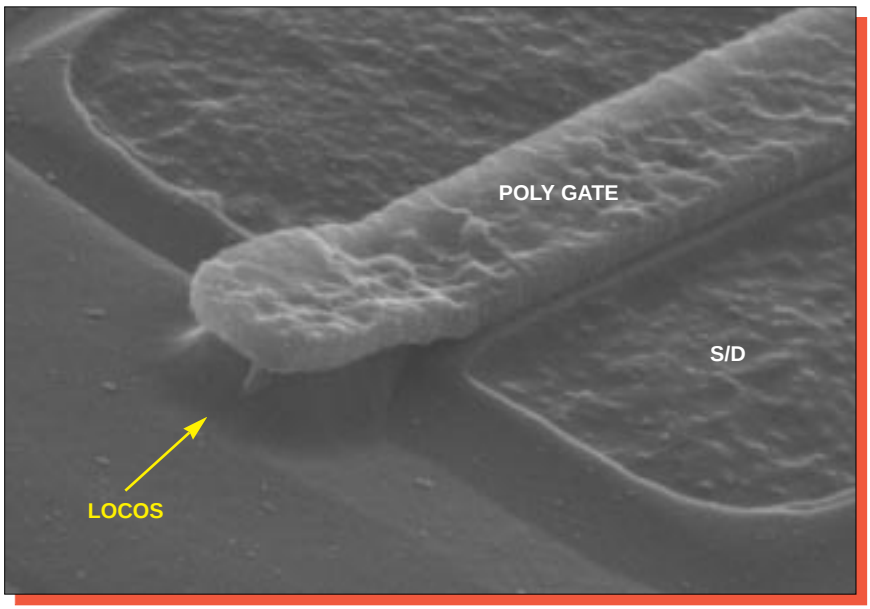
Figure 22. Topological SEM views of poly patterning. Mag. 1600x, 0°.



Mag. 4000x

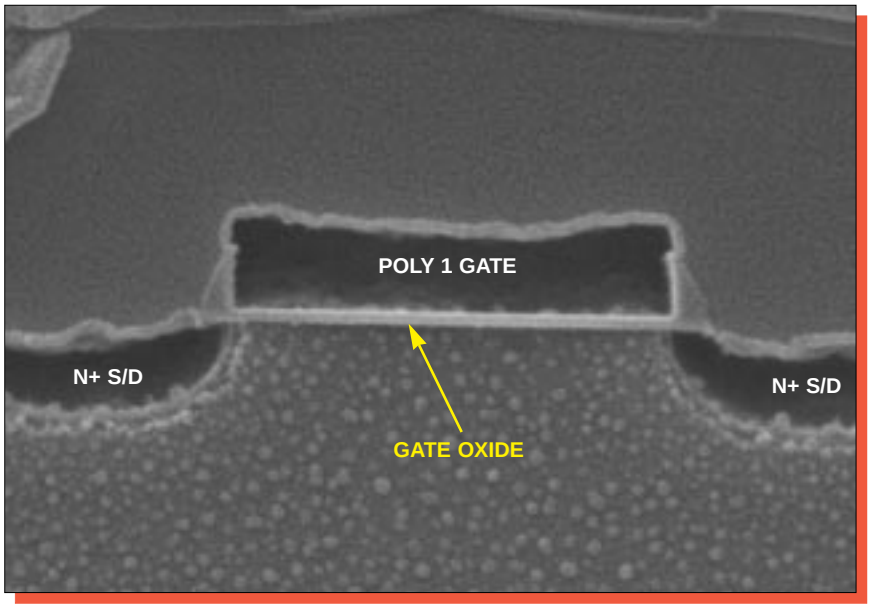


Mag. 4000x

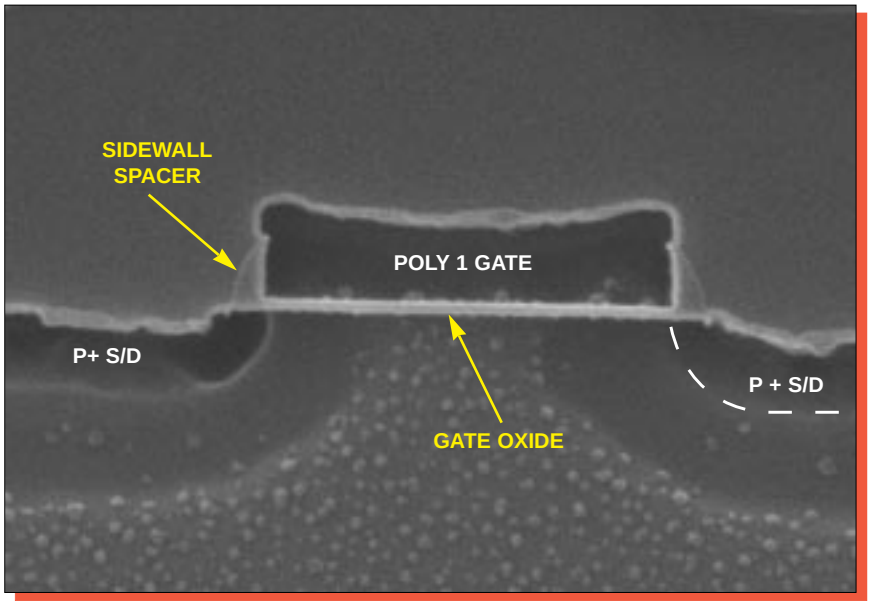


Mag. 28,000x

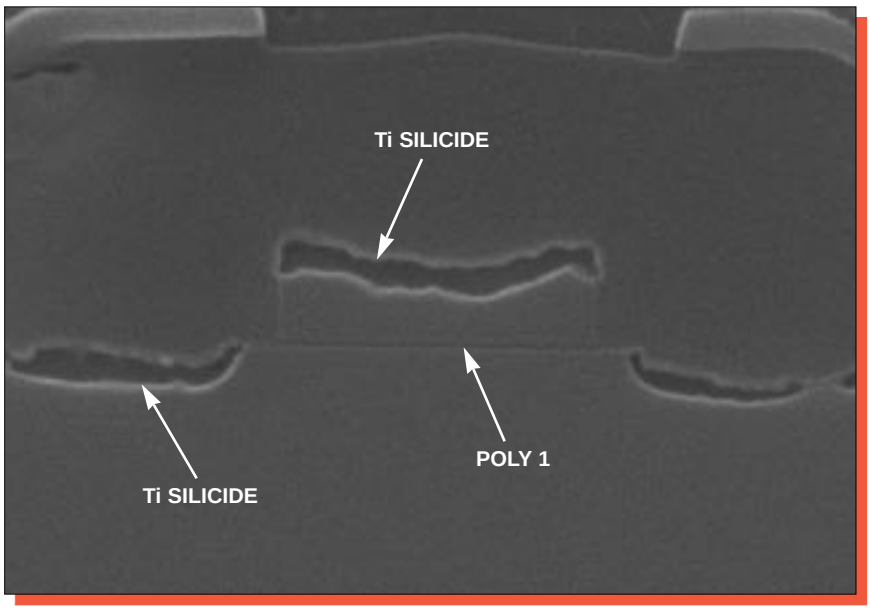
Figure 23. Perspective SEM views of poly coverage. 60°.



N-channel

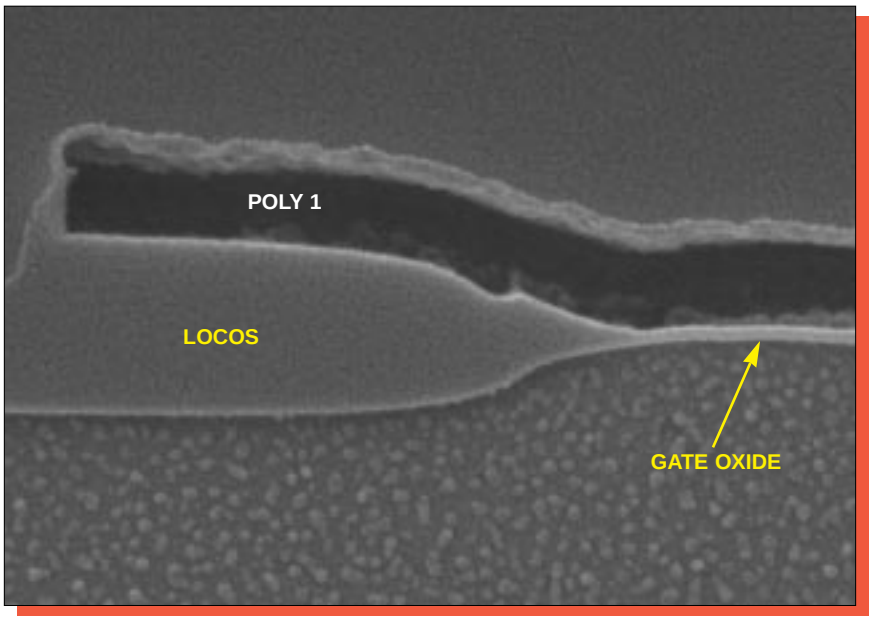


P-channel

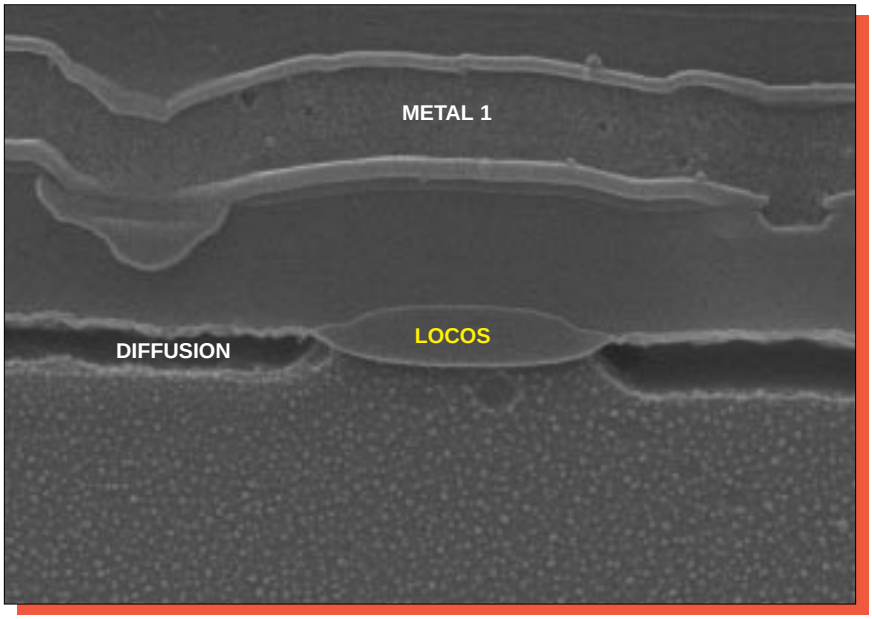


glass etch

Figure 24. SEM section views of typical transistors. Mag. 52,000x.

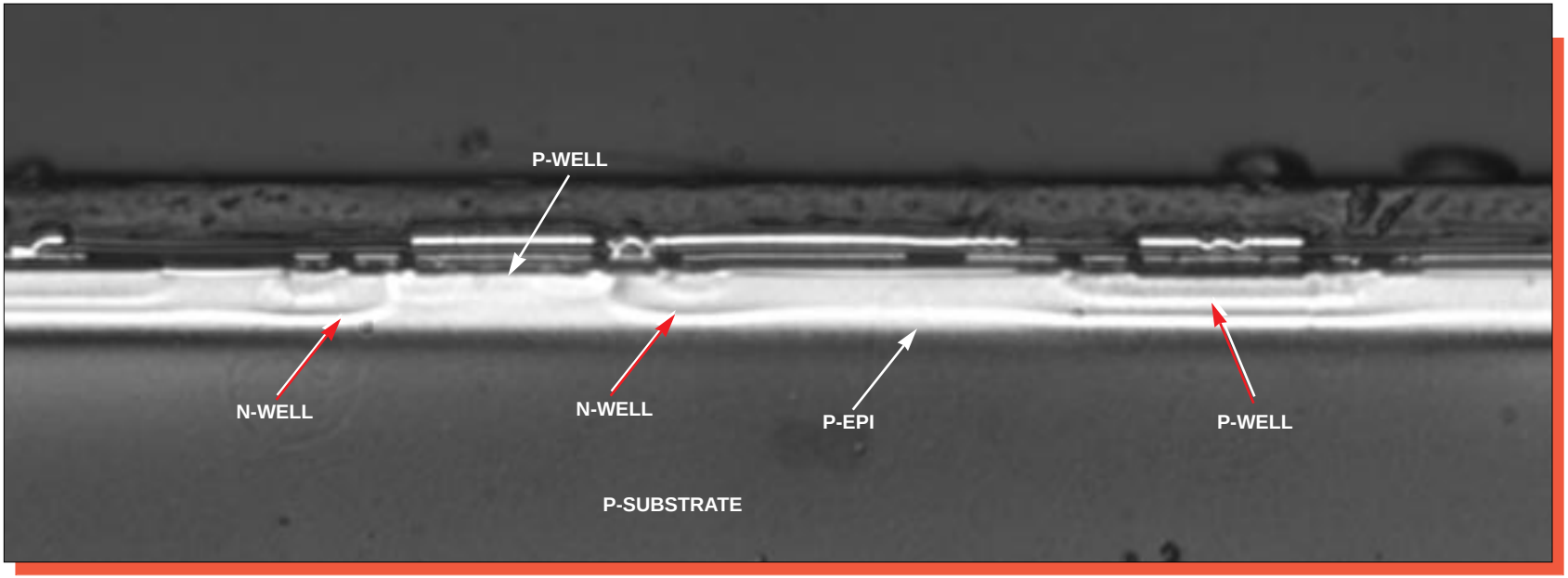


Mag. 52,000x

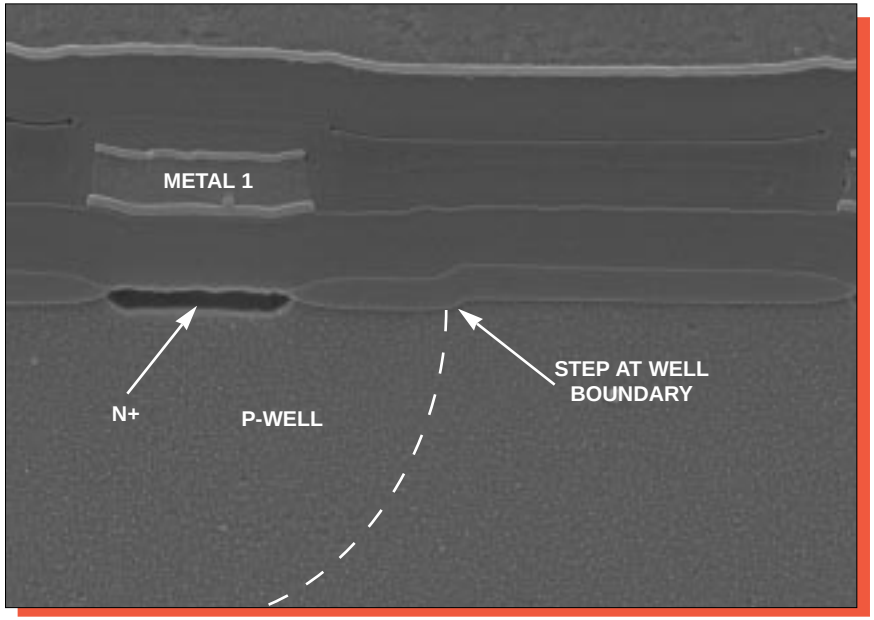


Mag. 26,000x

Figure 25. SEM section views of a typical birdsbeak and local oxide isolation.

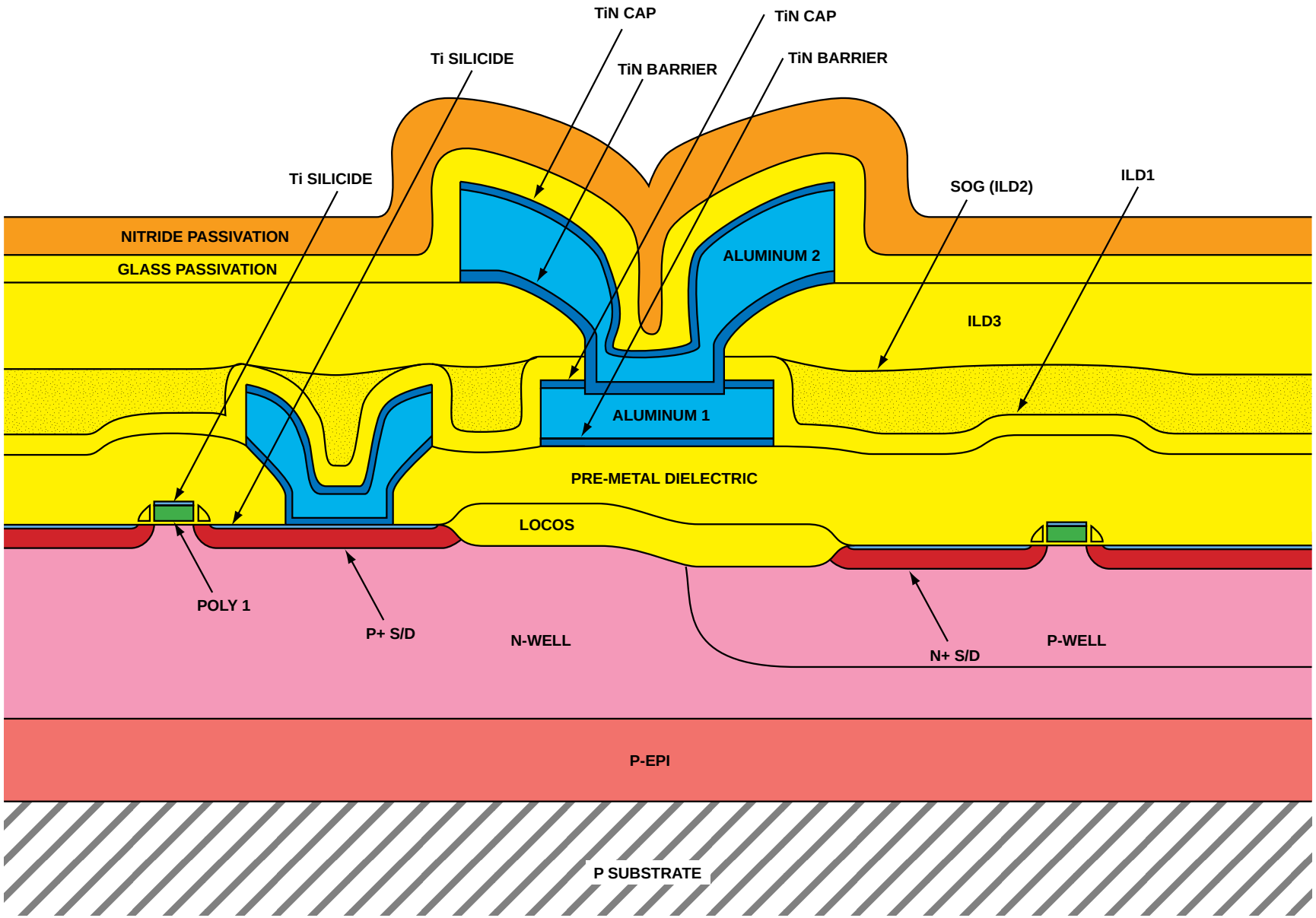


Mag. 1240x



Mag. 13,000x

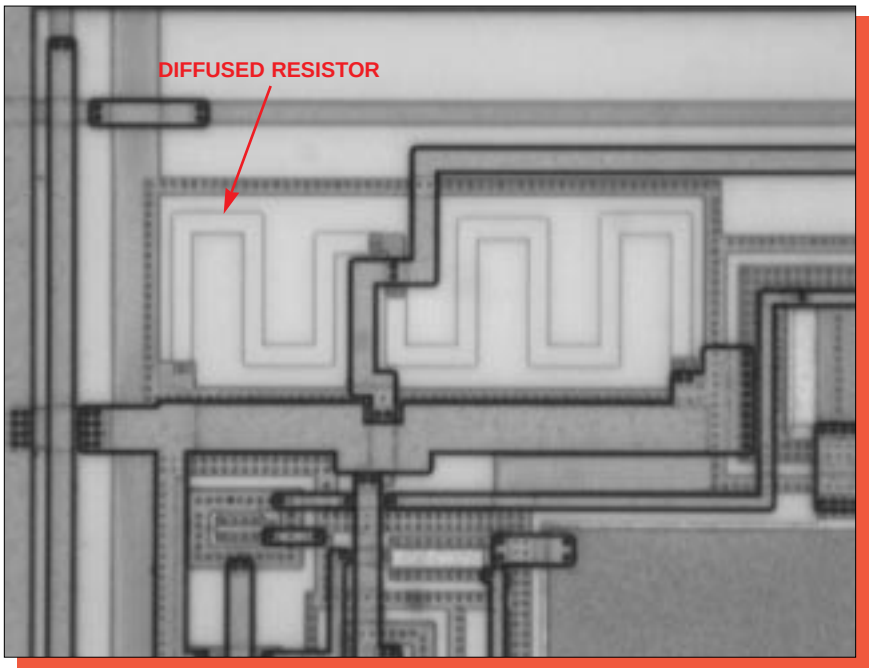
Figure 26. Section views illustrating well structure.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 27. Color cross section drawing illustrating device structure.



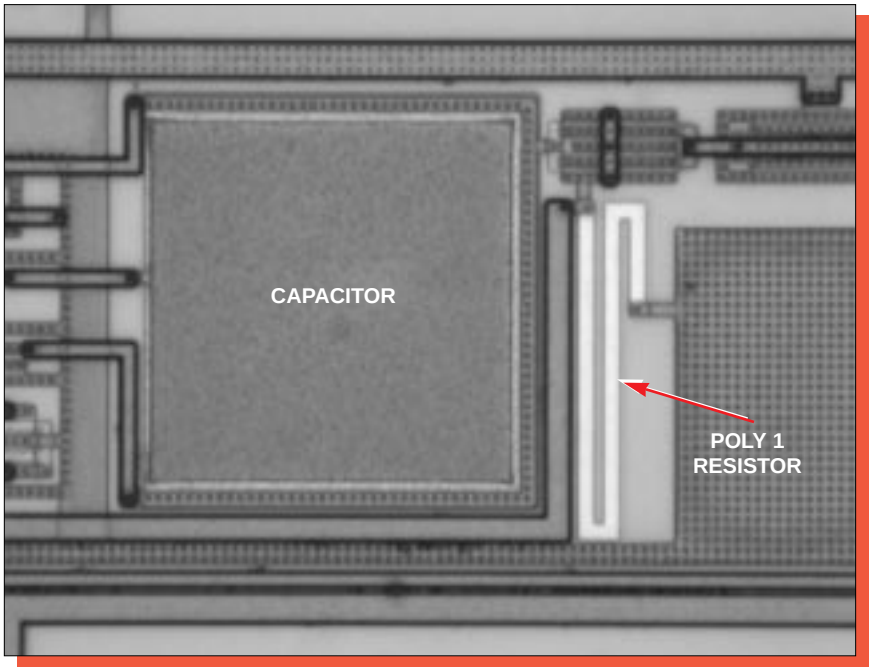
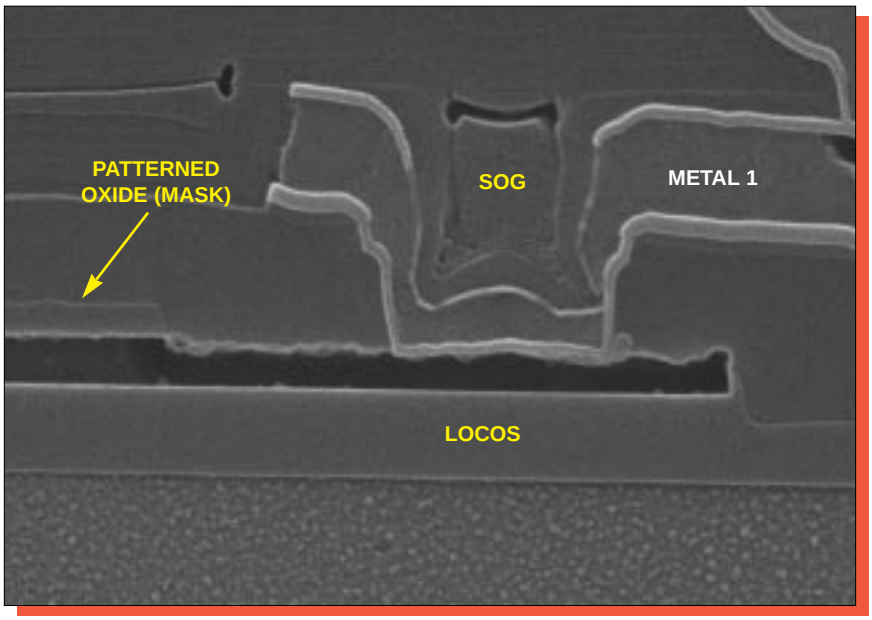
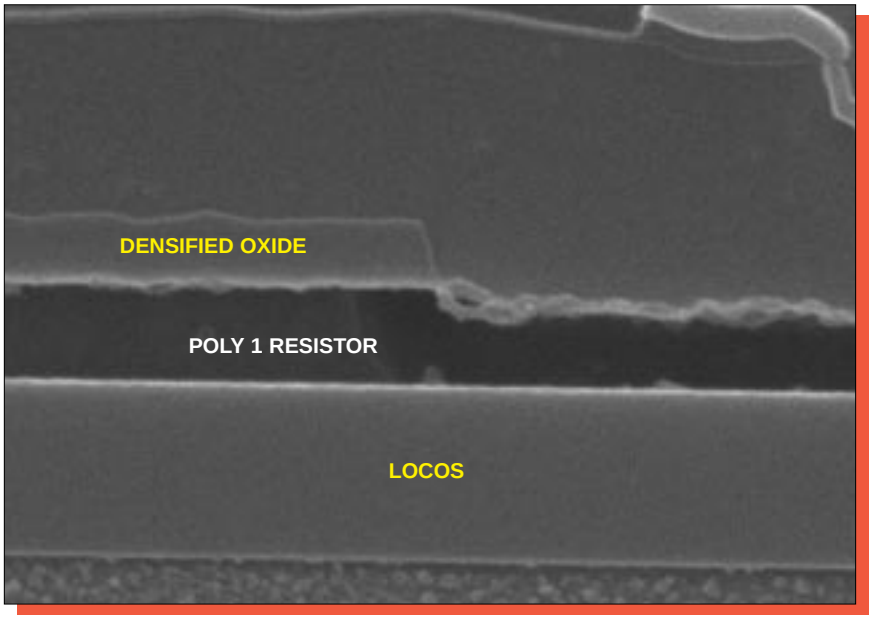


Figure 28. Optical views of resistors and a capacitor. Mag. 600x.

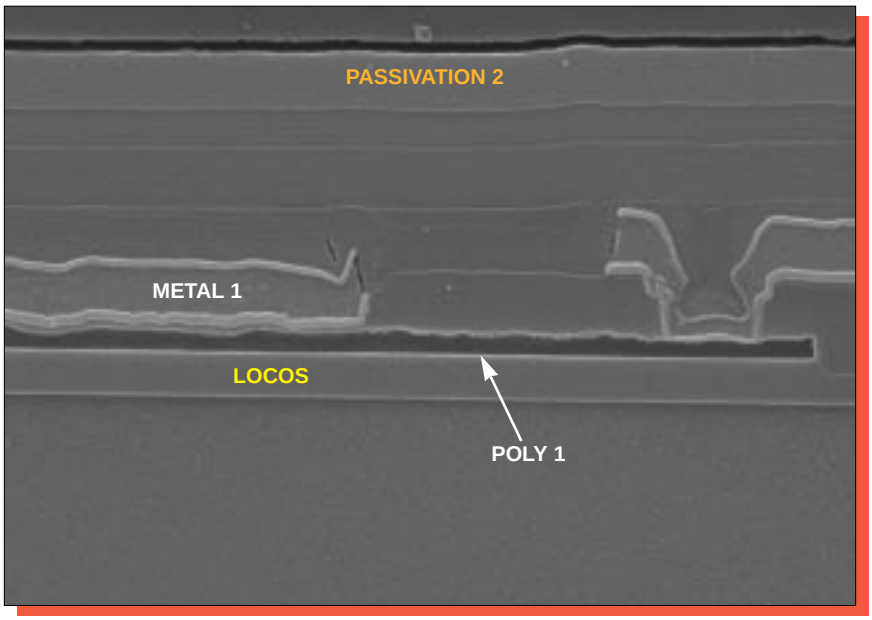


Mag. 26,000x

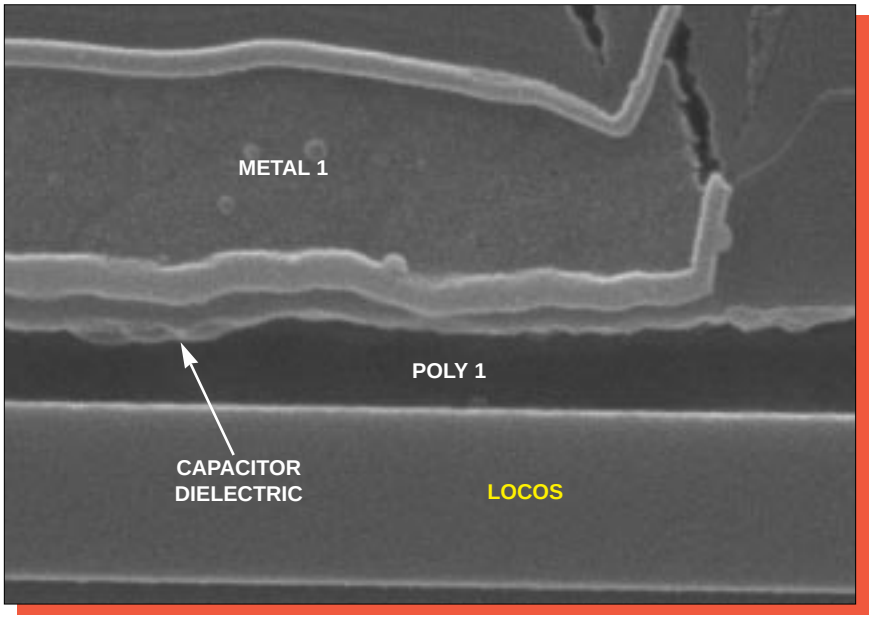


Mag. 52,000x

Figure 29. SEM section views of a poly 1 resistor.

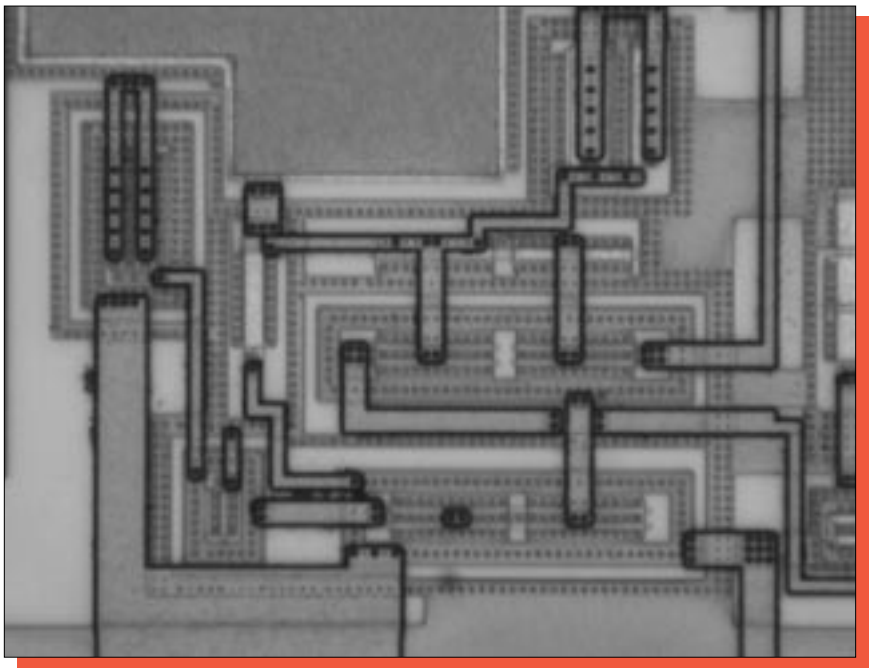


Mag. 13,000x

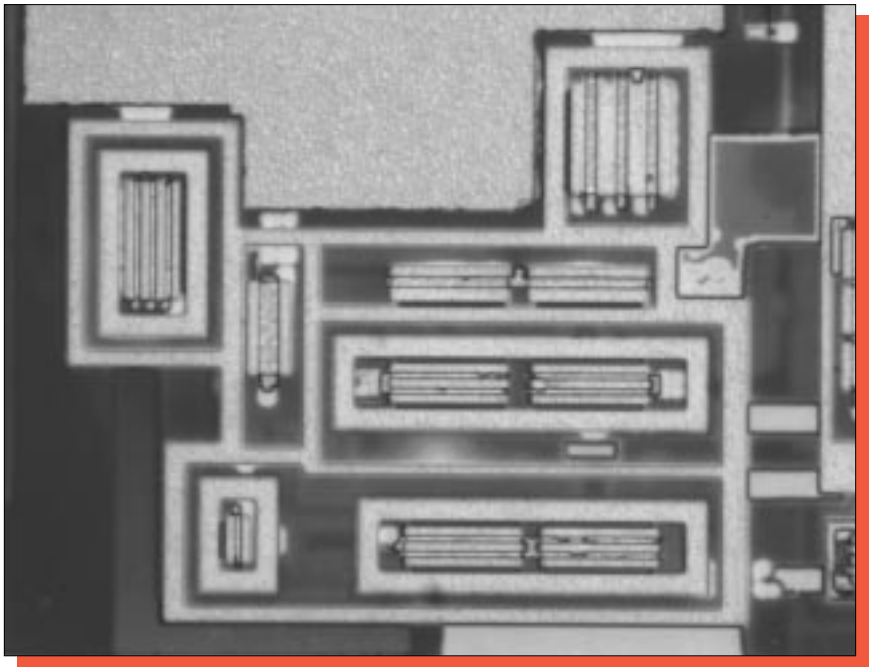


Mag. 52,000x

Figure 30. SEM section views illustrating a capacitor.

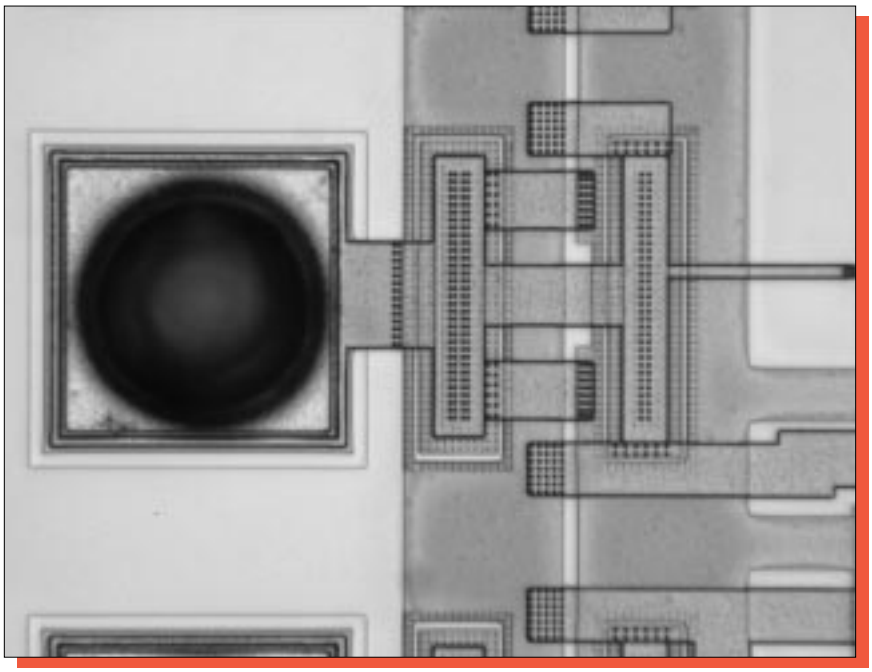


intact

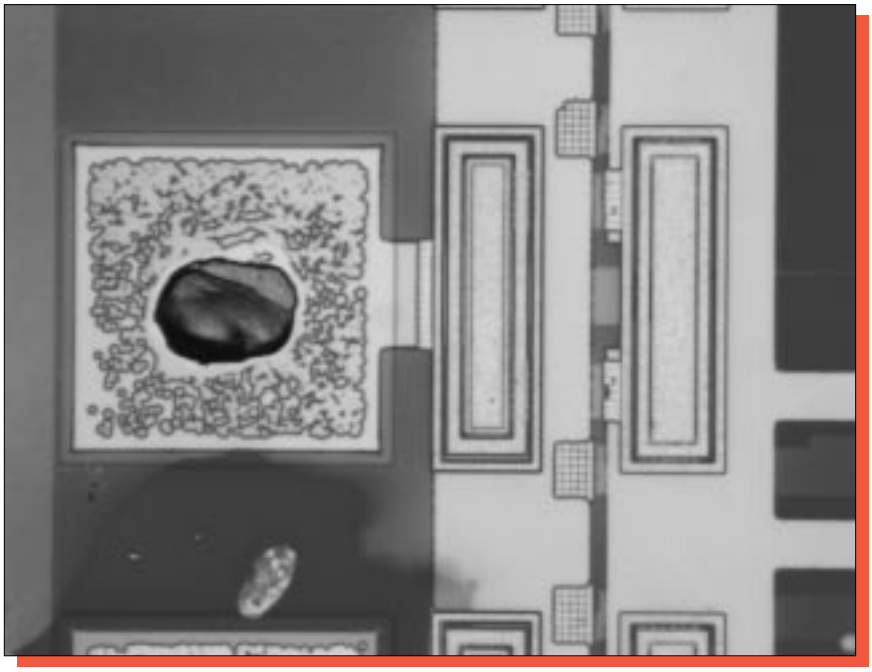


unlayered

Figure 31. Optical views of typical device circuit layout. Mag. 600x.



intact



unlayered

Figure 32. Optical views of typical input protection. Mag. 300x.

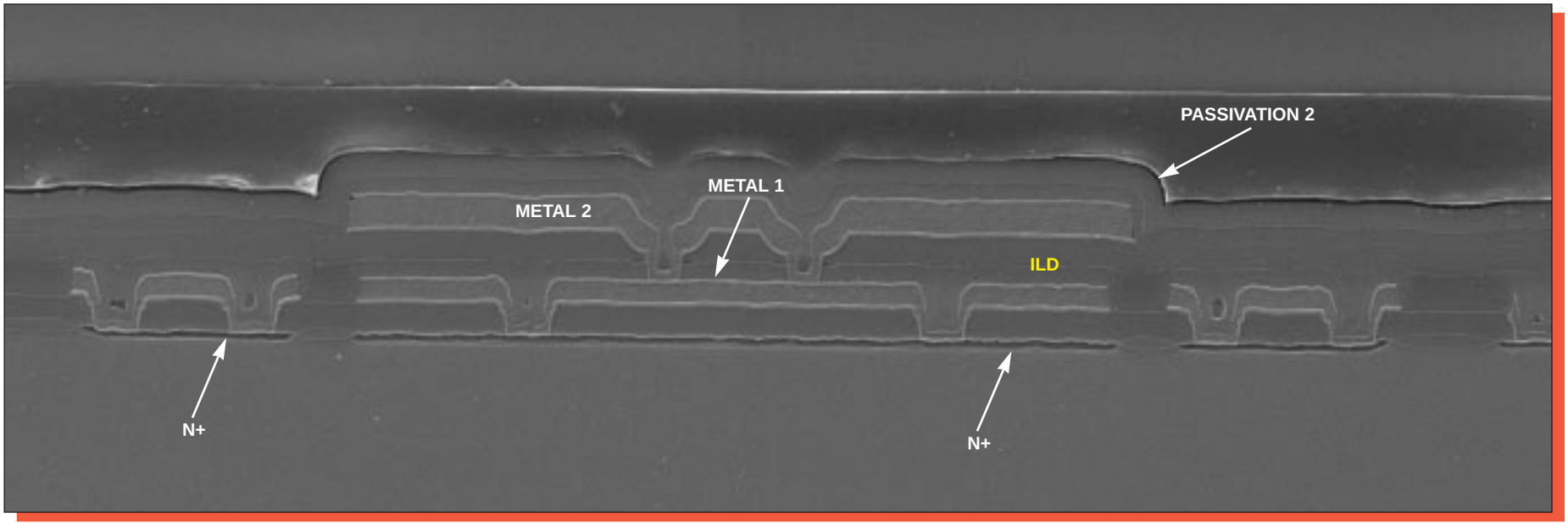


Figure 33. SEM section view of the I/O circuitry. Mag. 6500x.