Construction Analysis

VTC VM365830VSJ
Pre-Amp

Report Number: SCA 9708-549

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the VTC VM365830VSJ PRE-AMP. Four devices packaged in 32-pin Very Small Outline Packages (VSOPs) were received for the analysis. All samples were date coded 9637.

MAJOR FINDINGS

Questionable Items:[1]

- Aluminum 1 thinned up to 100 percent[2] at some emitter contact edges (barrier maintained continuity) (Figures 41a, 42 and 44).

Special Features:

- Aggressive feature sizes.
- Very thick metal 2.
- Complementary bipolar process.
- A selective epitaxial growth or a complex well process may have been used.
- PNP devices utilize a isolation tub (N ISO TUB), to isolate PNP devices from the substrate.

Design Features:

- Metal 2 employed isolated "octagon" shaped vias.
- Metal 1 employed elongated/oval shaped contacts.
- Poly-silicon is used to form one plate of the capacitors.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 32-pin Very Small Outline Plastic Packages (VSOPs).
- The leadframe was constructed of copper and plated externally with tin-lead solder.
- Internal leadframe plating was silver (spot).
- Die separation by sawn dicing (95+ percent).
- Wirebonding by the thermosonic ball bond method using 1.1 mil gold wire.
- All pins were connected.

Die Process

- Fabrication process: Complementary bipolar process which may have used a selective epitaxial growth or complex well process. All NPN devices were located in the N-epi/N+ buried layer. All PNP devices were located in the P-epi/P+ buried layer with an N-type doped region (N ISO TUB) beneath for collector isolation.
- Final passivation: A layer of nitride over multi-layers of silicon-dioxide. The silicon-dioxide appeared to have been doped.
- Metallization: Two levels of metal defined by dry-etch techniques. Metal 2 consisted of aluminum with a titanium-nitride cap and titanium barrier. Metal 2 “octagon” shaped vias were used and some were isolated. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Standard contacts were employed (no plugs). Some metal 1 elongated contacts were used with bipolar devices. Both

TECHNOLOGY DESCRIPTION (continued)

metal layers used an adhesion layer under the barrier. All contacts contained a platinum ($PtSi_2$) silicide. Platinum silicide would indicate that schottky devices may have been present but no schottky devices were identifiable on the die.

- Intermetal dielectric: Intermetal dielectric consisted of a multi-layered glass followed by two layers of a higher density glass (TEOS?). The second layer of glass had been subjected to an etchback for planarization.

- Pre-metal glass: A multi-layer of PSG (phosphosilicate glass) over a deposited glass and grown oxide.

- Polysilicon: A single layer of polysilicon was employed. Poly was used exclusively for the poly to N+ capacitor structures where it formed the upper plates.

- Isolation: Selective epitaxial growth may have been used for active device fabrication to isolate PNP devices from NPN devices. The step in the oxide at the epi boundary indicates this process.

- Transistors: NPN devices were located in the P-epi/P+ buried layer. PNP devices were located in the N-epi/N+ buried layer with a lightly N-doped region (N ISO TUB) beneath for collector isolation. Standard type diffusions appear to be used for emitters and bases (i.e., no polysilicon emitter sources). A Deep P+ sinker was used as the collector for PNP devices. All N+ emitter contacts contact silicon “mesas” at NPN devices and all N+ base contacts contact silicon “mesas” at PNP devices.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 10**

Questionable Items:[1] None.

Special Features: None.

General Items:

- The devices were encapsulated in a 32-pin Very Small Outline Plastic Packages (VSOPs) with "gull-wing" leads.

- Overall package quality: Good. No defects were found on the external or internal portions of the packages. No voids or cracks were noted in the plastic package. External pins were well formed and tinning of the leads was complete. No gaps were noted at lead exits.

- Leadframe: Copper (Cu) leadframe externally tinned with tin-lead (SnPb) solder and spot-plated internally with silver (Ag). No problems were found.

- Wirebonding: Thermosonic ball bond method using 1.1 mil gold wire. Bonds were well formed and placement was good. Good intermetallic formation was found at the ball bonds. All bond pull strengths were somewhat low (possibly due to the thick metal 2 used) but no bond lifts occurred (see page 10). In-board bonding was noted on three sides of the die.

- Die attach: Silver-epoxy die attach of normal quality. Some small voids were noted in the epoxy but no problems are foreseen.

- No die coat was used.

- Die dicing: Die separation was by sawing (95+ percent) and showed normal quality workmanship. No large chips or cracks were present at the die surface.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process and Design: **Figures 11 - 46**

Questionable Items:[1]

- Aluminum 1 thinned up to 100 percent[2] at some emitter contact edges (barrier maintained continuity) (Figures 41a, 42 and 44).

Special Features:

- Complementary bipolar process.
- A selective epitaxial growth or complex well process may have been used.
- Aggressive feature sizes.
- PNP devices utilize a isolation tub (N ISO TUB), to isolate PNP devices from the substrate.
- Very thick metal 2.

General Items:

- Fabrication process: Complementary bipolar process which may have used a selective epitaxial growth or complex well process. All NPN devices were located in the N-epi/N+ buried layer. All PNP devices were located in the P-epi/P+ buried layer with a lightly N- doped region (N ISO TUB) beneath for collector isolation. No significant problems were found in the complementary bipolar process.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Design implementation: Die layout was clean. Alignment was good at all levels.

- Surface defects: No toolmarks, masking defects, or contamination areas were found.

- Final passivation: A layer of nitride over a multi-layered silicon-dioxide. The silicon-dioxide appeared to have been doped. Edge seal was also good, as the passivation extended into the scribe lane to seal the metallization. Passivation integrity test indicated defect-free passivation.

- Metallization: Two levels of metal defined by dry-etch techniques. Metal 2 consisted of aluminum with a titanium-nitride cap and titanium barrier. Metal 2 "octagon" shaped vias were used and some were isolated. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Standard contacts were employed (no plugs). Some metal 1 elongated contacts were used with bipolar devices. Both metal layers used an adhesion layer under the barrier. All contacts contained a platinum ($PtSi_2$) silicide. Platinum silicide would indicate that schottky devices may have been present but no schottky devices were identifiable on the die.

- Metal patterning: Both metal layers were defined by a dry etch of normal quality. Metal 1 appeared slightly over-etched but no problems are foreseen.

- Metal defects: No notching or voiding of the metal layers was found.

- Metal step coverage: No metal 2 thinning occurred at vias or elsewhere due to the thick aluminum used. Metal 1 aluminum thinned up to 100 percent at some emitter contact edges (barrier maintained continuity). Typical metal 1 thinning was 65 percent including cap and barrier. MIL-STD-883D allows up to 70 percent metal thinning for contacts of this size.

ANALYSIS RESULTS II (continued)

- Vias and contacts: Via and contact cuts appeared to have been wet-etched. No over-etching was found at contacts. All contacts contained a platinum ($PtSi_2$) silicide.

- Intermetal dielectric: Intermetal dielectric consisted of a multilayered glass followed by two layers of higher density glass (TEOS?). The second layer of glass had been subjected to an etchback. No problems were found with these layers.

- Pre-metal glass: A multi-layer PSG (phosphosilicate glass) over a deposited glass and grown oxide. No problems were found.

- Polysilicon: Single layer of polysilicon was employed. Poly (no silicide) was used to form poly to N+ capacitor structures. No problems were found.

- Isolation: The step in the silicon surface at the epi boundary is taken to indicate that a selective epitaxial growth process may have been used for active device fabrication. The process appeared well implemented.

- Transistors: NPN devices were located in the P-epi/P+ buried layer. PNP devices were located in the N-epi/N+ buried layer with a lightly N-doped region (N ISO TUB) beneath for collector isolation. A standard P+ diffusion was used to form the base of NPN transistors and the N-epi was used to form the base for the PNP transistors. A Deep P+ sinker was used as the collector for PNP devices and also was used as an isolation. All N+ emitter contacts and all N+ base contacts were made to silicon “mesas.”

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Package section and material analysis

Decapsulate

Internal optical inspection

SEM inspection of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Delayer to metal 1

SEM inspection of metal 1

Aluminum removal (metal 1), inspect barrier

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	G
Die attach quality	N
Dicing quality	N
Die attach method	Silver-epoxy
Dicing method	Sawn (95+ percent)
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	P*
Metal registration	N
Contact coverage	G
Contact registration	G

**100 percent metal 1 aluminum thinning.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP	BOTTOM
VTC 003 VM365830VSJ 9637 AN	KOREA

WIREBOND STRENGTH

Wire material: 1.1 mil diameter gold
Die pad material: aluminum
Material at package lands: silver

Sample #	1	2
# of wires pulled:	28	28
Bond lifts:	0	0
Force to break - high:	5g	7g
- low:	2g	3g
- avg.:	3.3g	3.8g
- std. dev.:	0.65	0.87

PACKAGE MATERIAL ANALYSIS (EDX)

Leadframe:	Copper (Cu)
External pin plating:	Tin-lead (SnPb) solder
Internal plating:	Silver (Ag)
Die attach:	Silver-epoxy (Ag)

DIE MATERIAL ANALYSIS

Overlay passivation:	Nitride over a multi-layers of silicon-dioxide.
Metallization 2:	Aluminum with a titanium-nitride cap and a titanium barrier and adhesion layer.
Intermetal dielectric (IMD):	Intermetal dielectric consisted of a multilayered glass followed by two layers of higher density glass.
Metallization 1:	Aluminum with a titanium-nitride cap and barrier. A titanium adhesion layer was used under the barrier.
Pre-metal glass:	PSG glass containing 2.8 wt. percent phosphorus over grown/densified oxides.
Silicide:	Platinum ($PtSi_2$) silicide at all contacts.

HORIZONTAL DIMENSIONS

Die size:	1.6 x 2.95 mm (64.5 x 116 mils)
Die area:	4.7 mm^2 (7,482 $mils^2$)
Min pad size:	0.09 x 0.09 mm (3.9 x 3.9 mils)
Min pad window:	1 micron
Min pad space:	0.07 mm (2.9 mils)
Min metal 2 width:	1.2 micron
Min metal 2 space:	1.3 micron
Min metal 2 pitch:	2.5 microns
Min via size:	1.2 micron
Min via space:	1.45 micron
Min metal 1 width:	0.6 micron
Min metal 1 space:	1.2 micron
Min metal 1 pitch:	1.8 micron
Min contact size:	0.65 micron
Min P+ emitter size:	2 x 4 microns
Min N+ emitter size:	1.5 x 1.5 micron
Min P+ base to ISO:	2.0 microns

VERTICAL DIMENSIONS

Die thickness:	0.24 mm (9.5 mils)

Layers

Passivation 2:	0.65 micron
Passivation 1:	0.6 micron
Metal 2 - cap:	0.08 micron (approximate)
- aluminum:	2.0 microns
- barrier:	0.2 micron
Intermetal dielectric (IMD) - glass 2:	0.15 micron
- glass 1:	0.25 micron
- multilayered glass:	0.15 micron
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.5 micron
- barrier:	0.15 micron
Pre-metal glass:	0.6 micron
Poly:	0.2 micron
Silicon “mesa” height:	0.3 micron
N+ buried layer:	1.6 micron
P+ buried layer:	1.6 micron
N-epi:	1.5 micron
P-epi:	1.0 micron
P+ base:	0.7 micron
N+ emitter:	0.15 micron
P+ sinker:	1.0 micron

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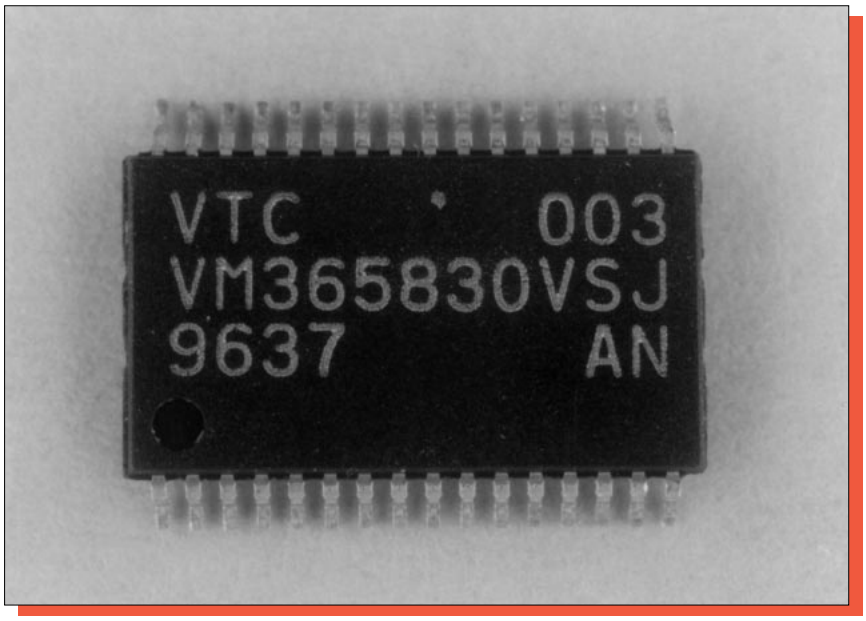
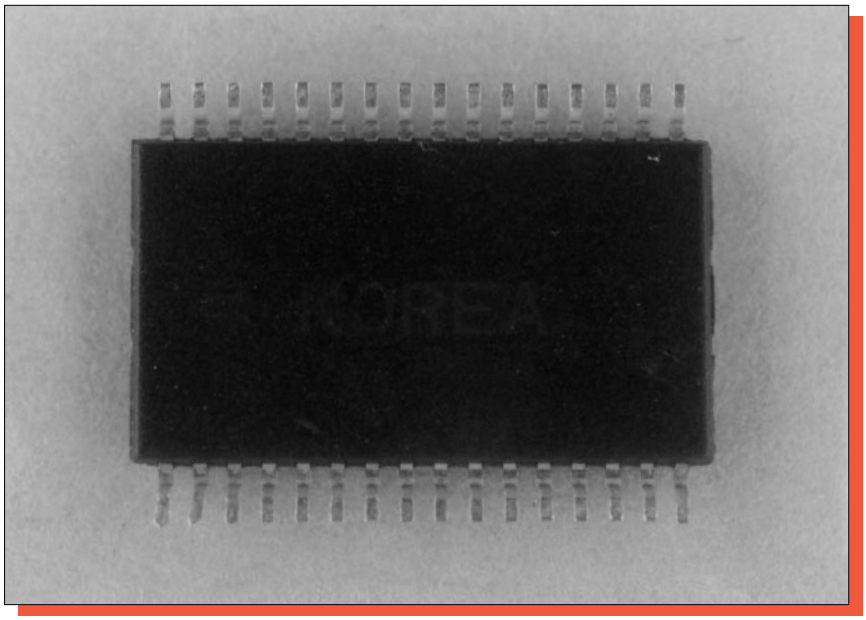




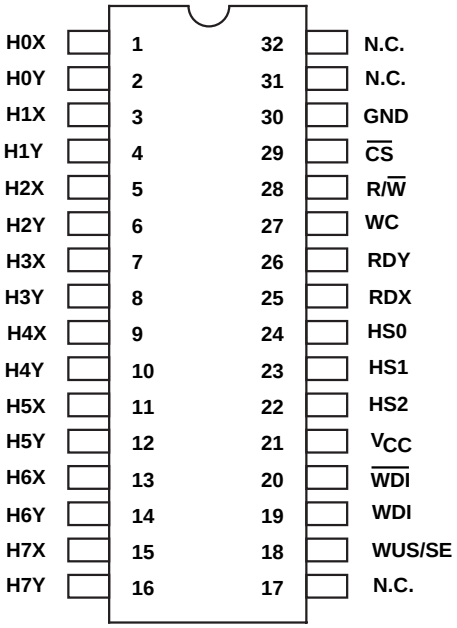
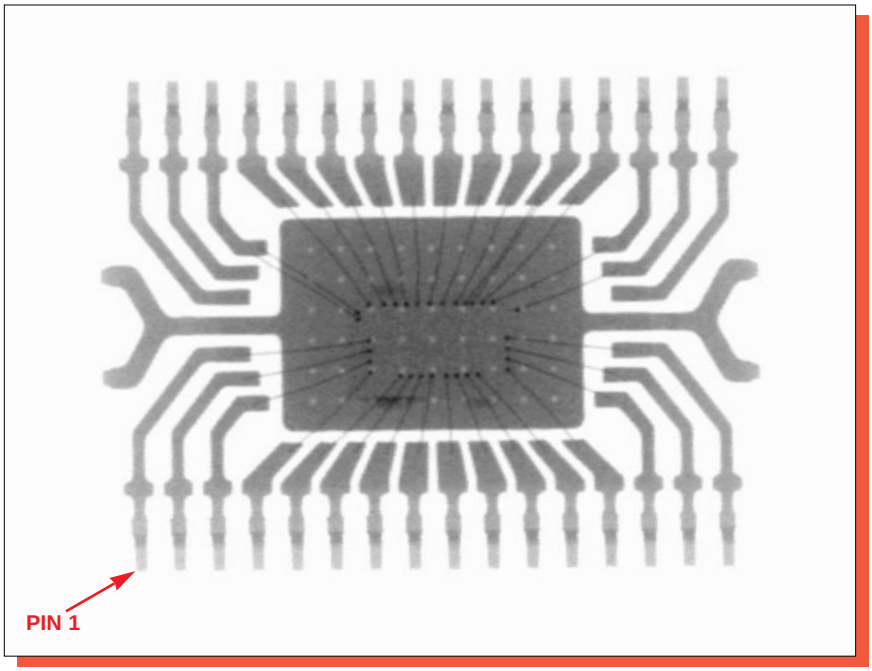


Figure 1. Package photographs and pinout of the VTC VM365830VSJ device.
Mag. 7x.



top view

side view

Figure 2. X-ray views of the package. Mag. 8x.

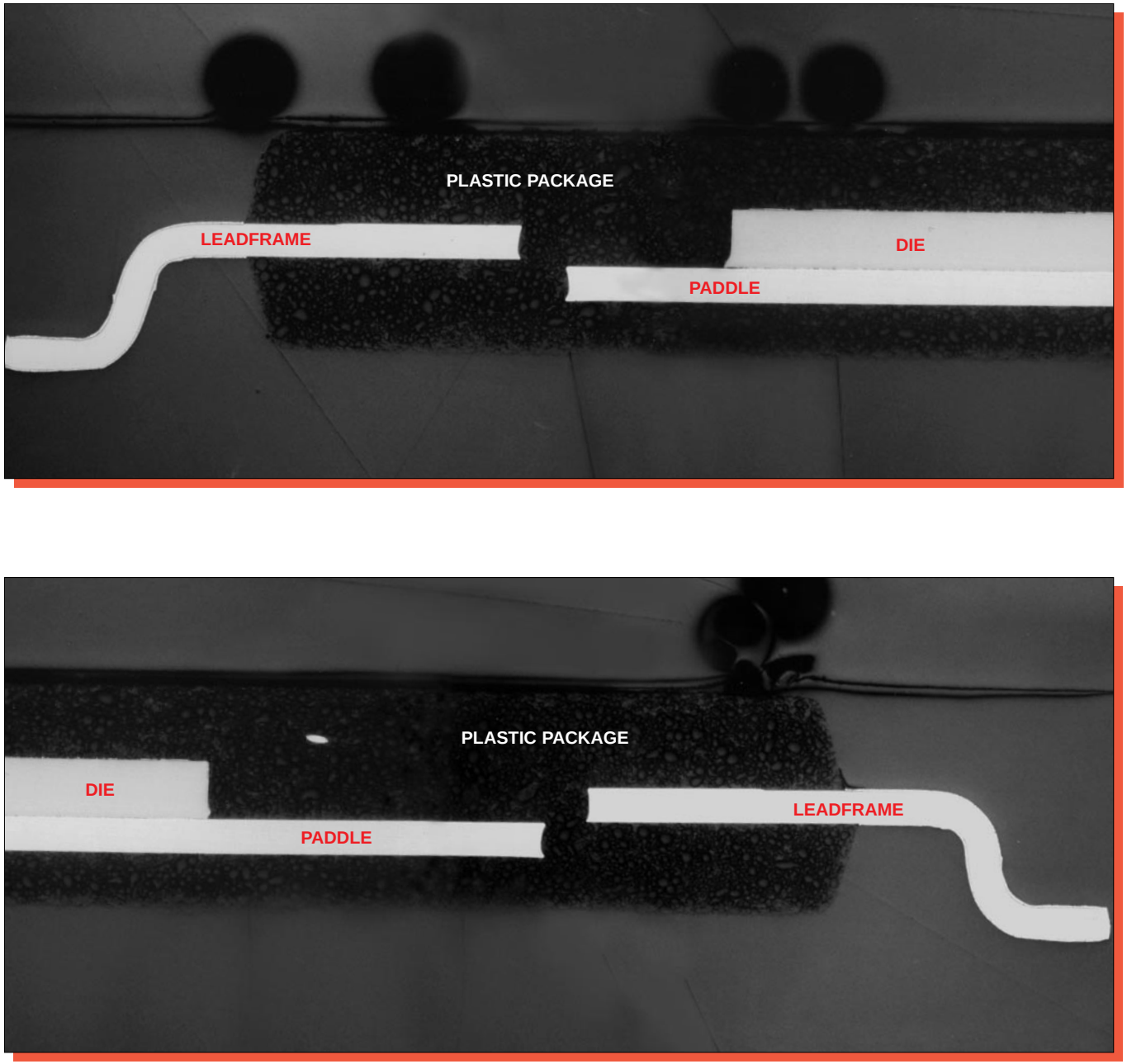
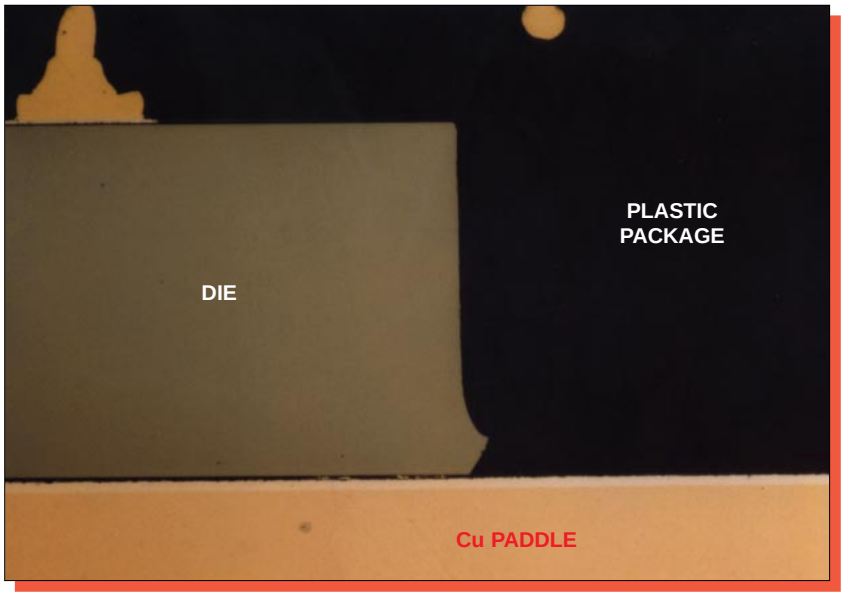
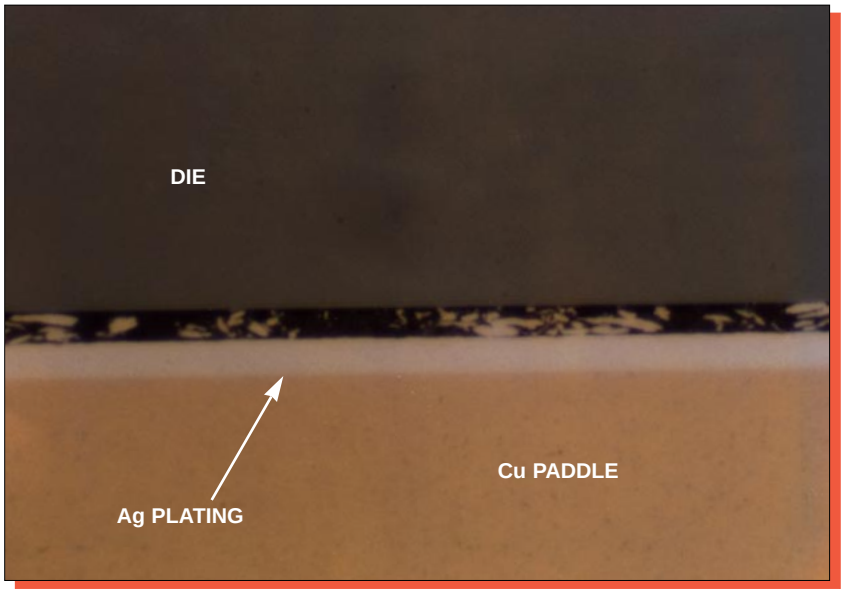


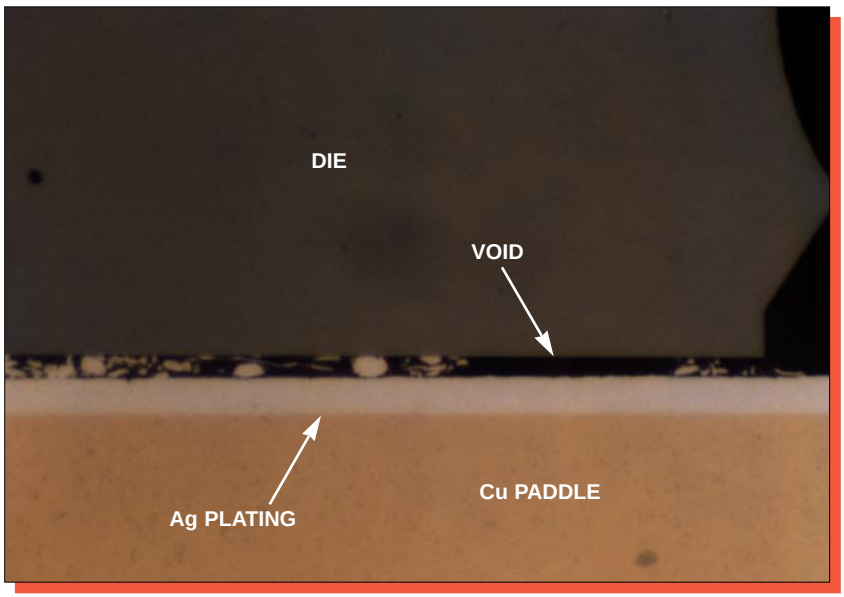
Figure 3. Package section views illustrating general construction. Mag. 40x.



Mag. 200x



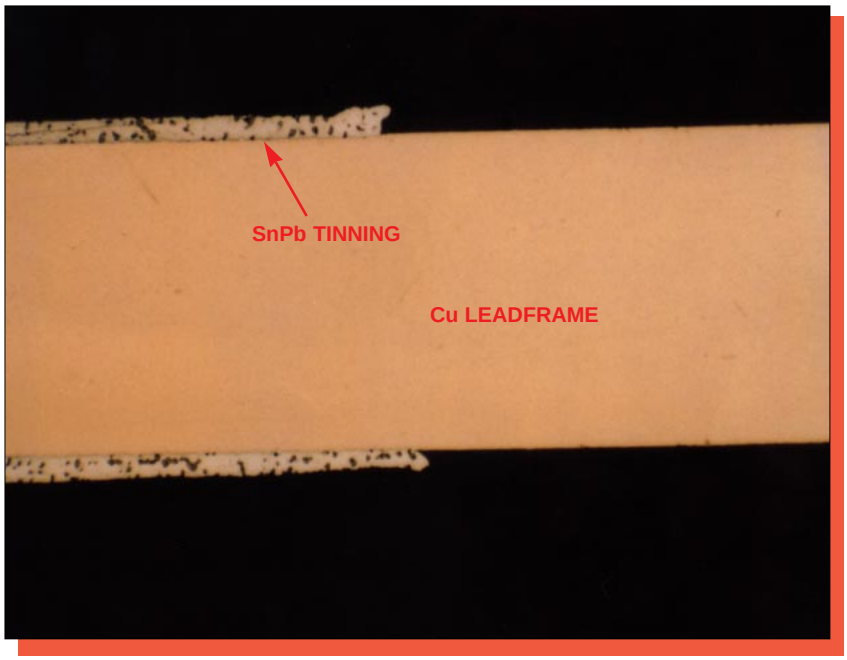
Mag. 800x



Mag. 800x

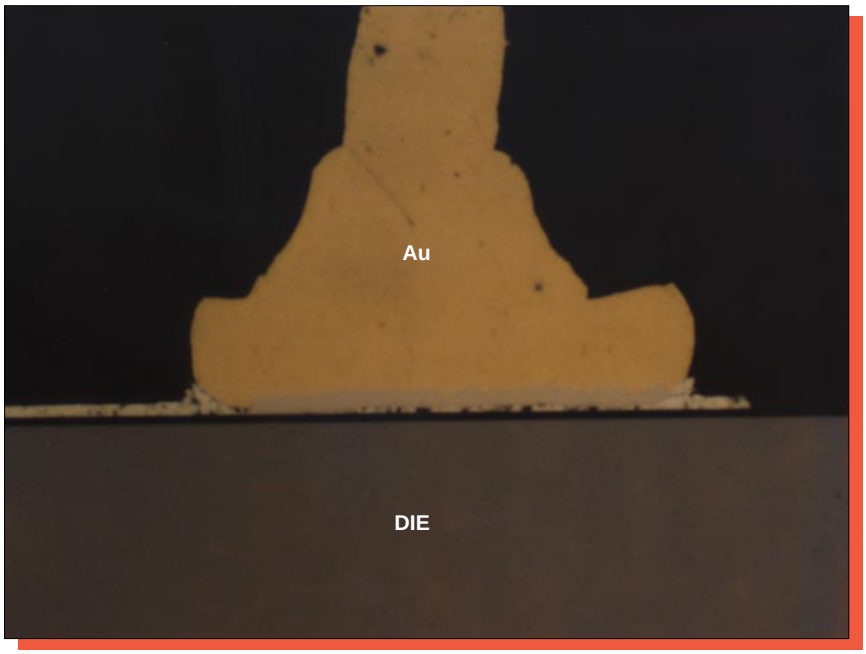
Figure 4. Package section views illustrating dicing and die attach.

Mag. 100x

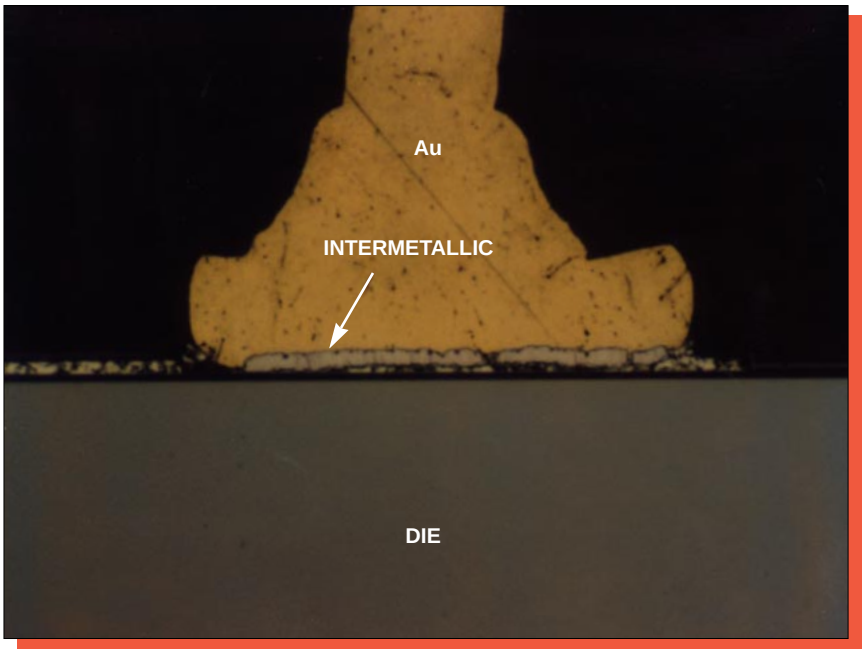


Mag. 320x

Figure 5. Package section views of the leadframe and leadframe exit.

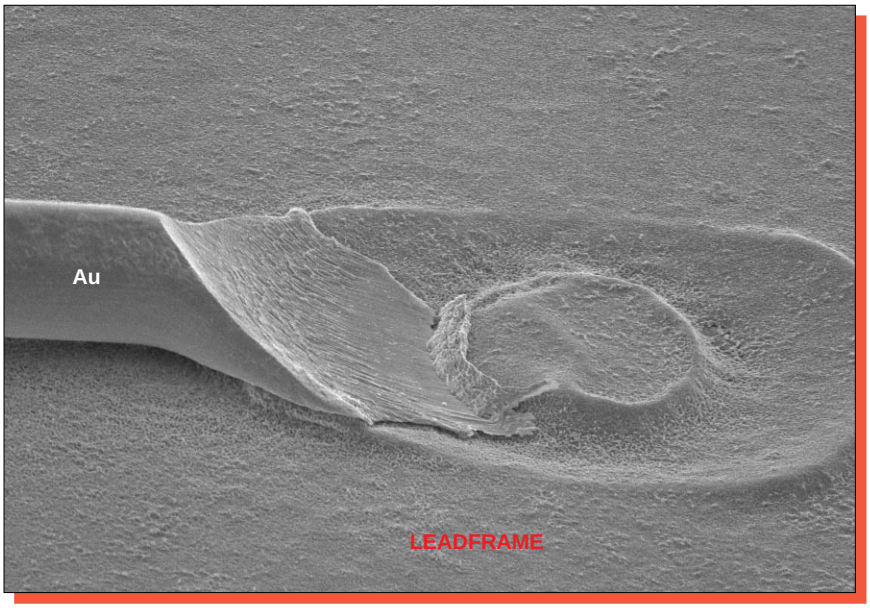


as polished

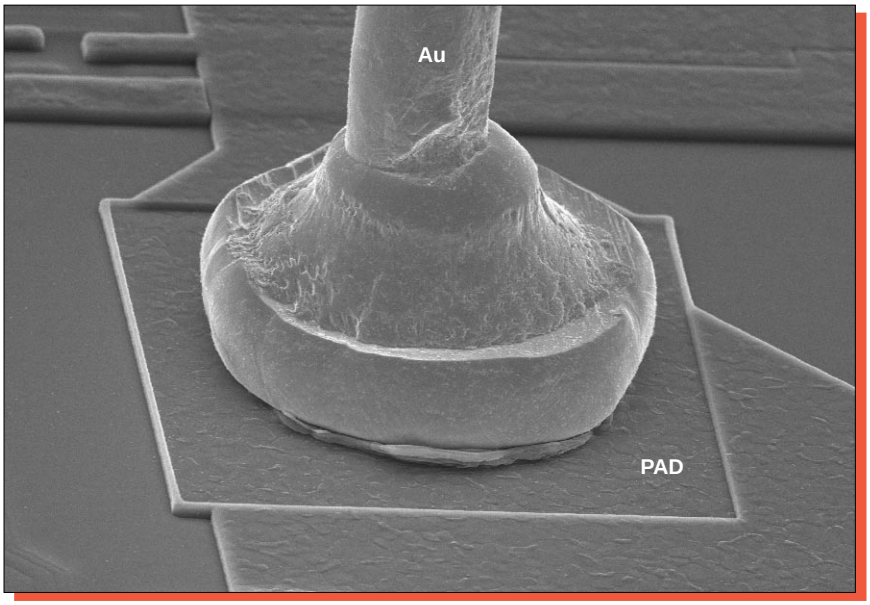


delineation etch

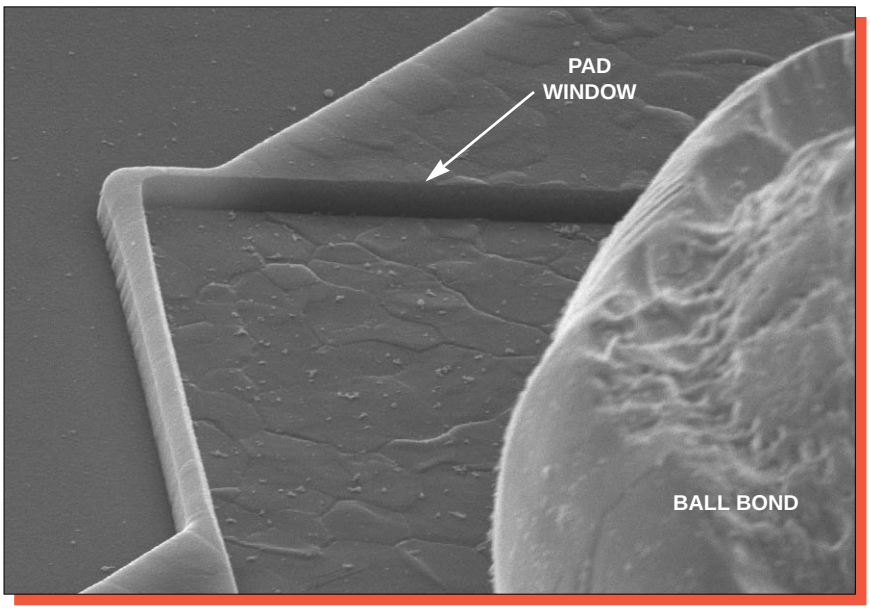
Figure 6. Optical views illustrating typical ball bonds. Mag. 800x.



Mag. 700x

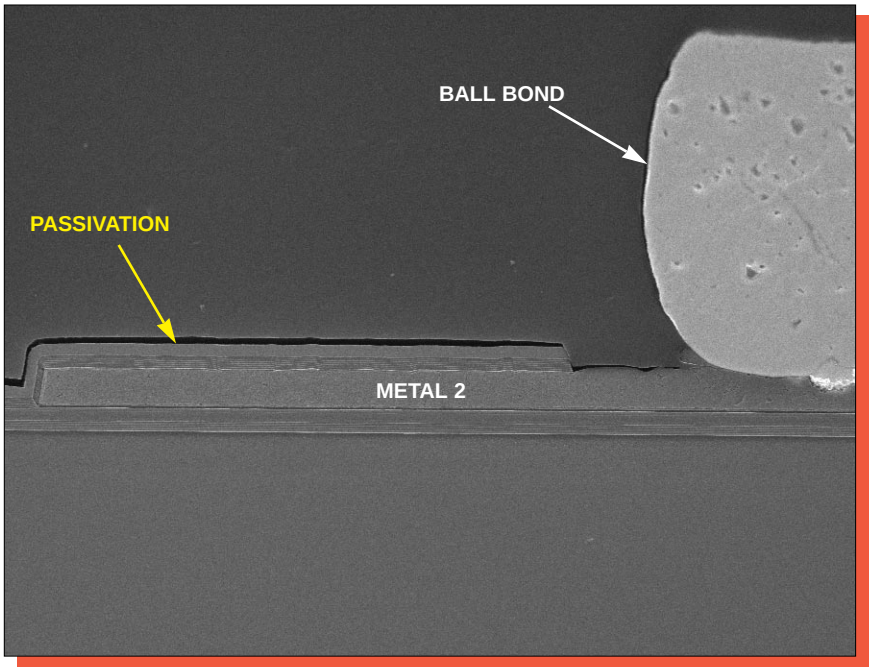


Mag. 800x

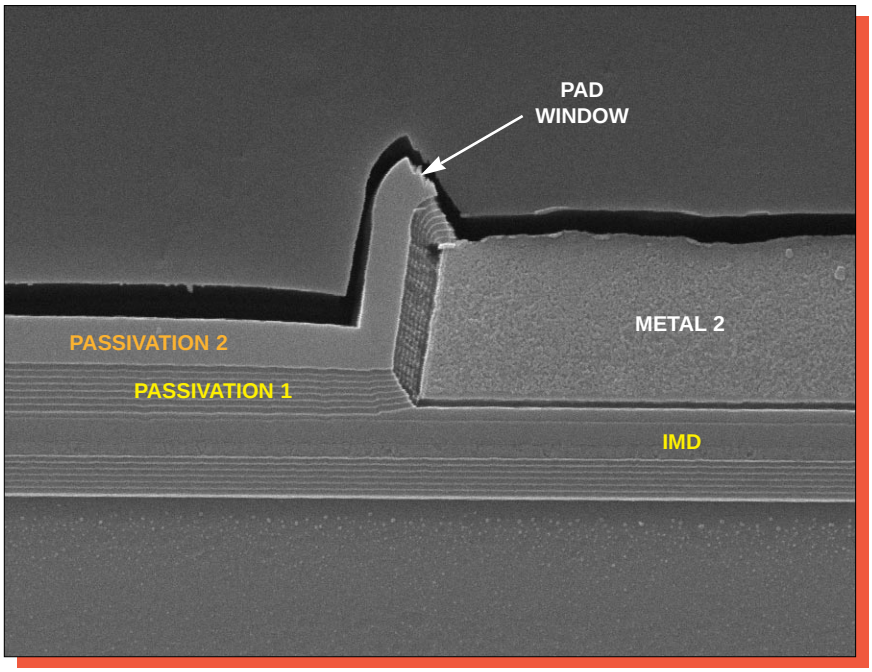


Mag. 3000x

Figure 7. SEM views of typical wirebonds and pad window. 60°.

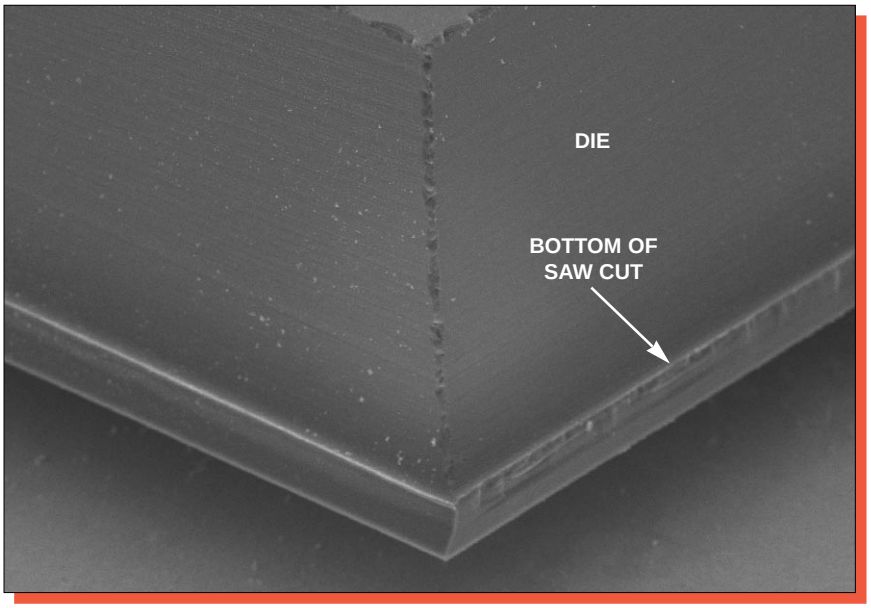


Mag. 2500x

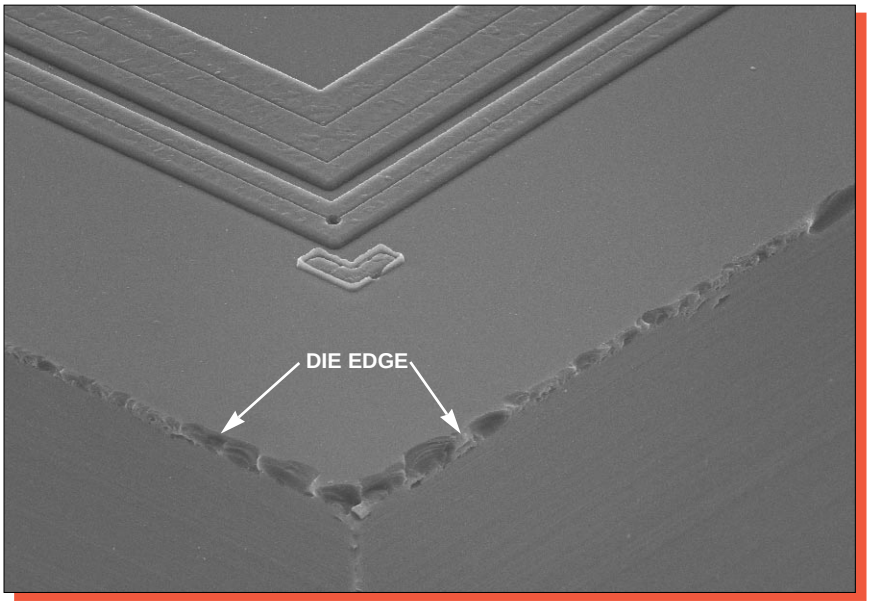


Mag. 10,000x

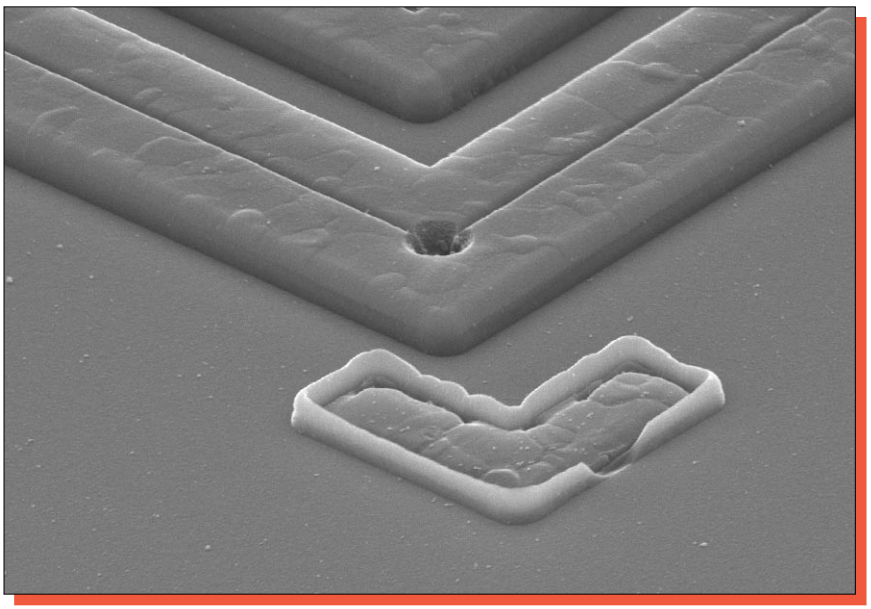
Figure 8. SEM section views of the bond pad structure.



Mag. 300x

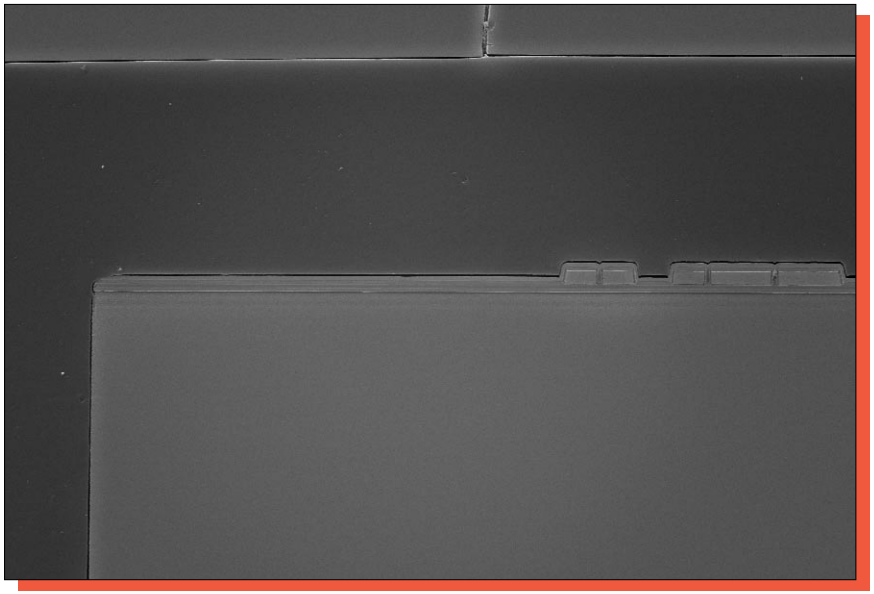


Mag. 600x

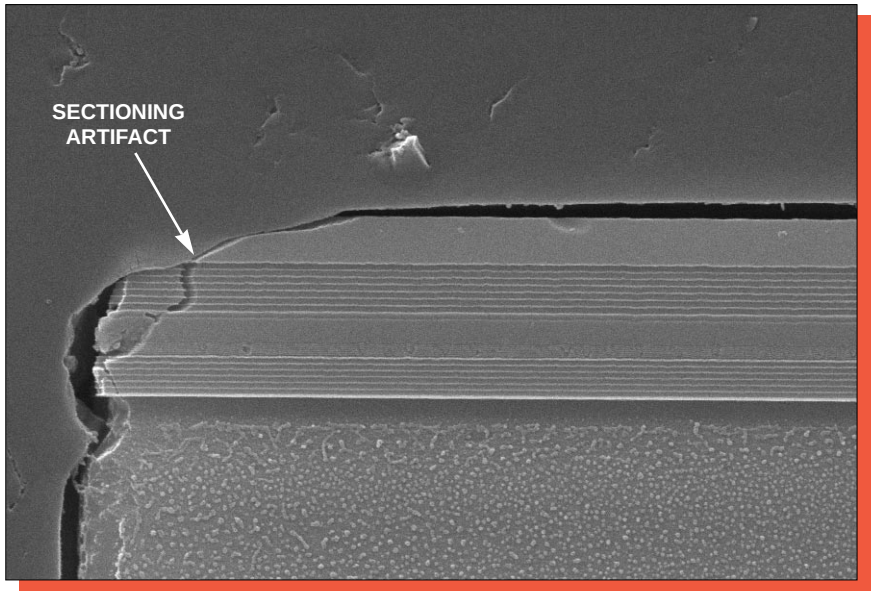


Mag. 2500x

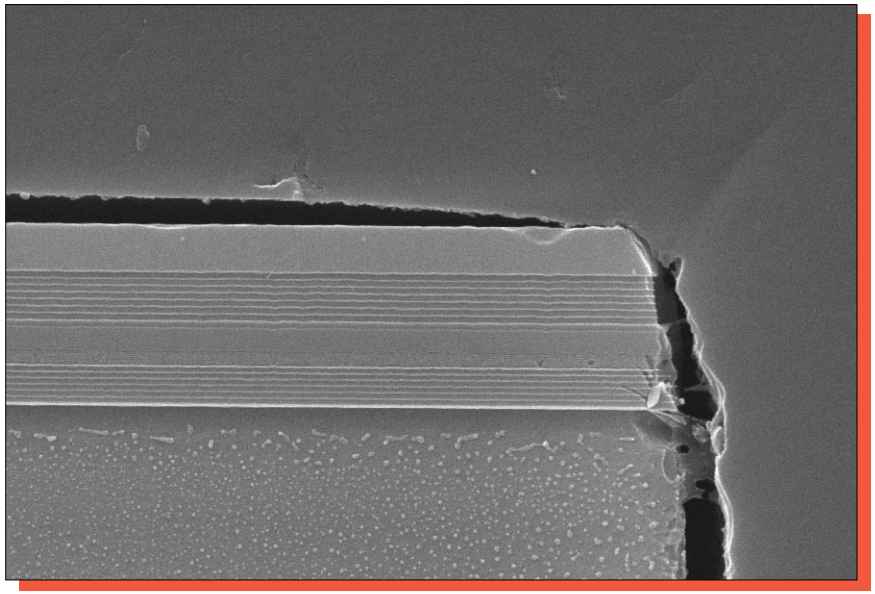
Figure 9. SEM views of dicing and edge seal. 60°.



Mag. 800x



Mag. 10,000x



Mag. 10,000x

Figure 10. SEM section views of the die edge seal.

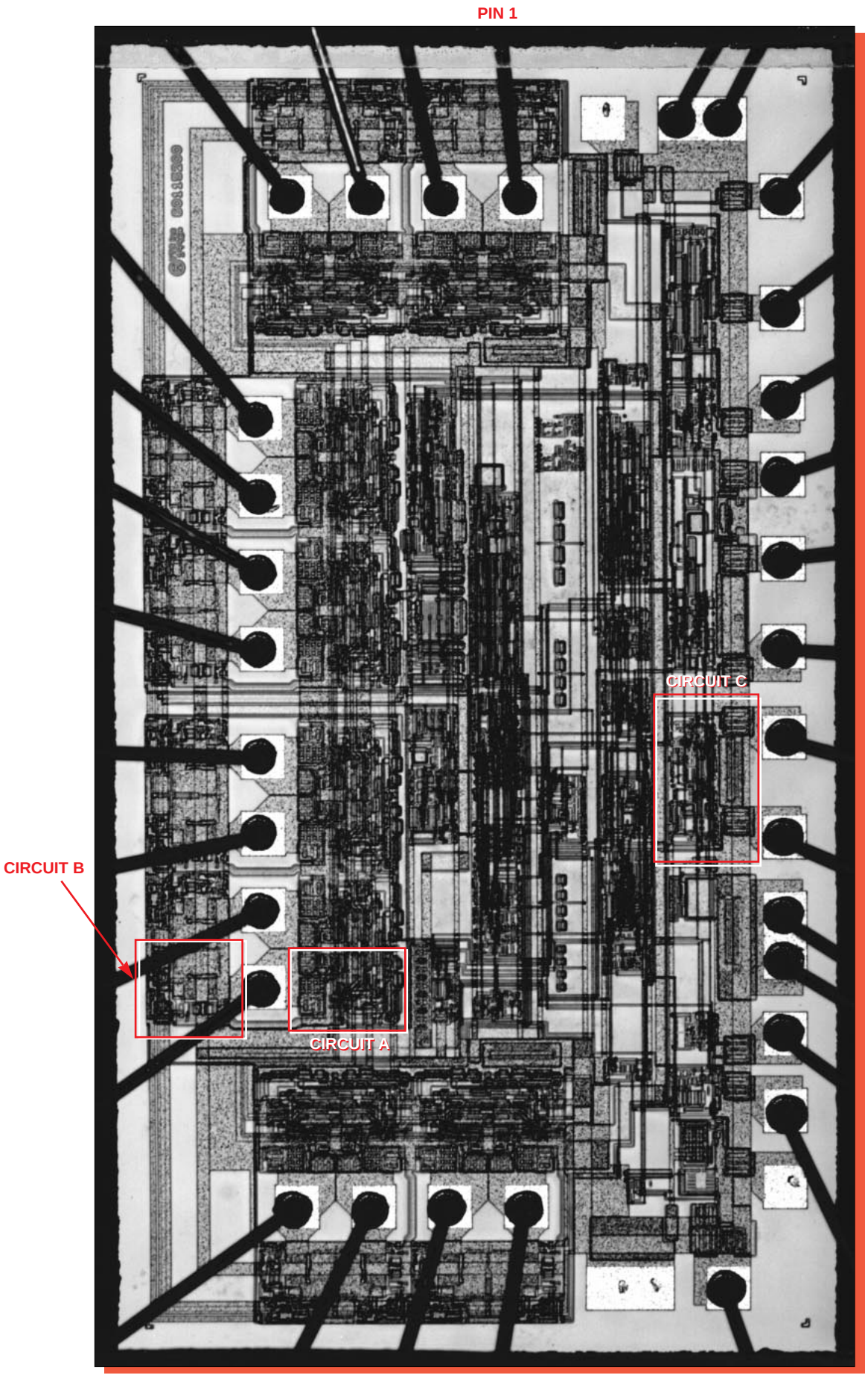
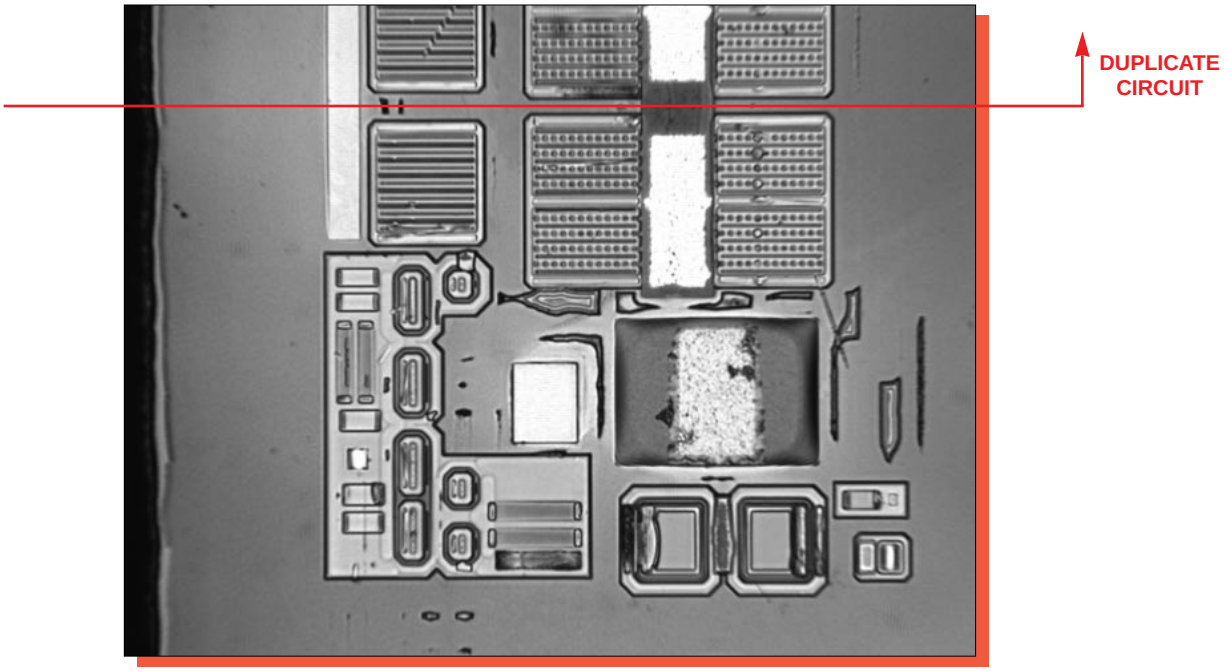
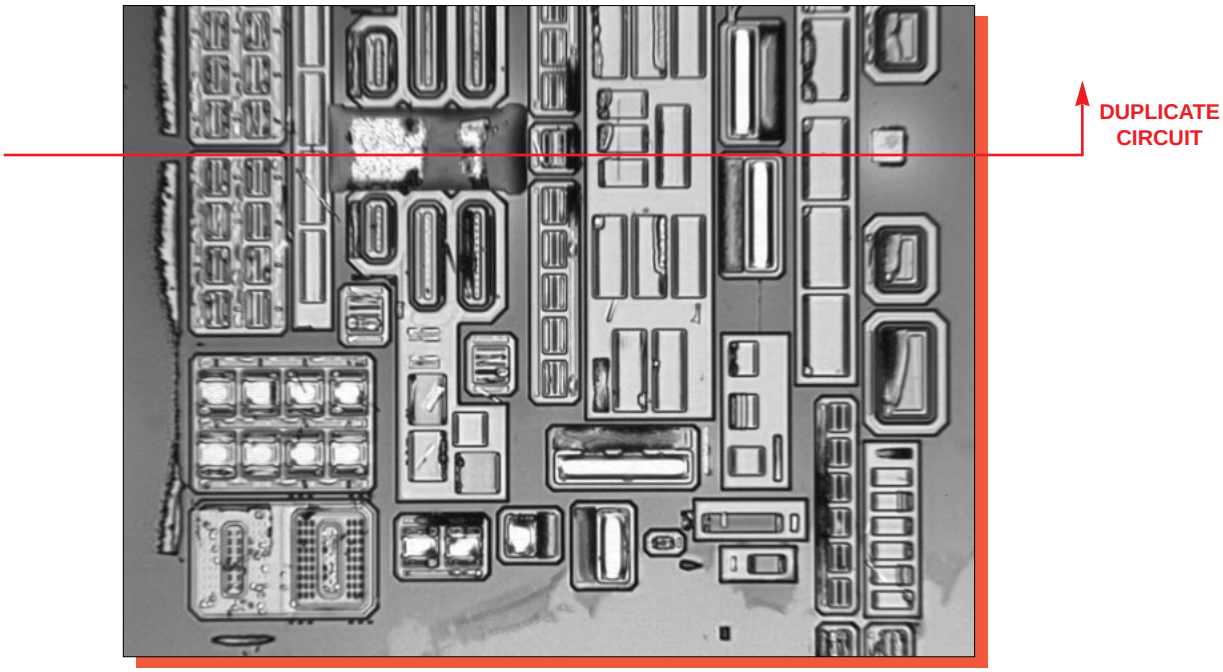


Figure 11. Whole die photograph of the VTC VM365830VSJ device. Mag. 80x.



Circuit B



Circuit A

Figure 11a. Delayered optical views of circuits A and B. Mag. 400x.

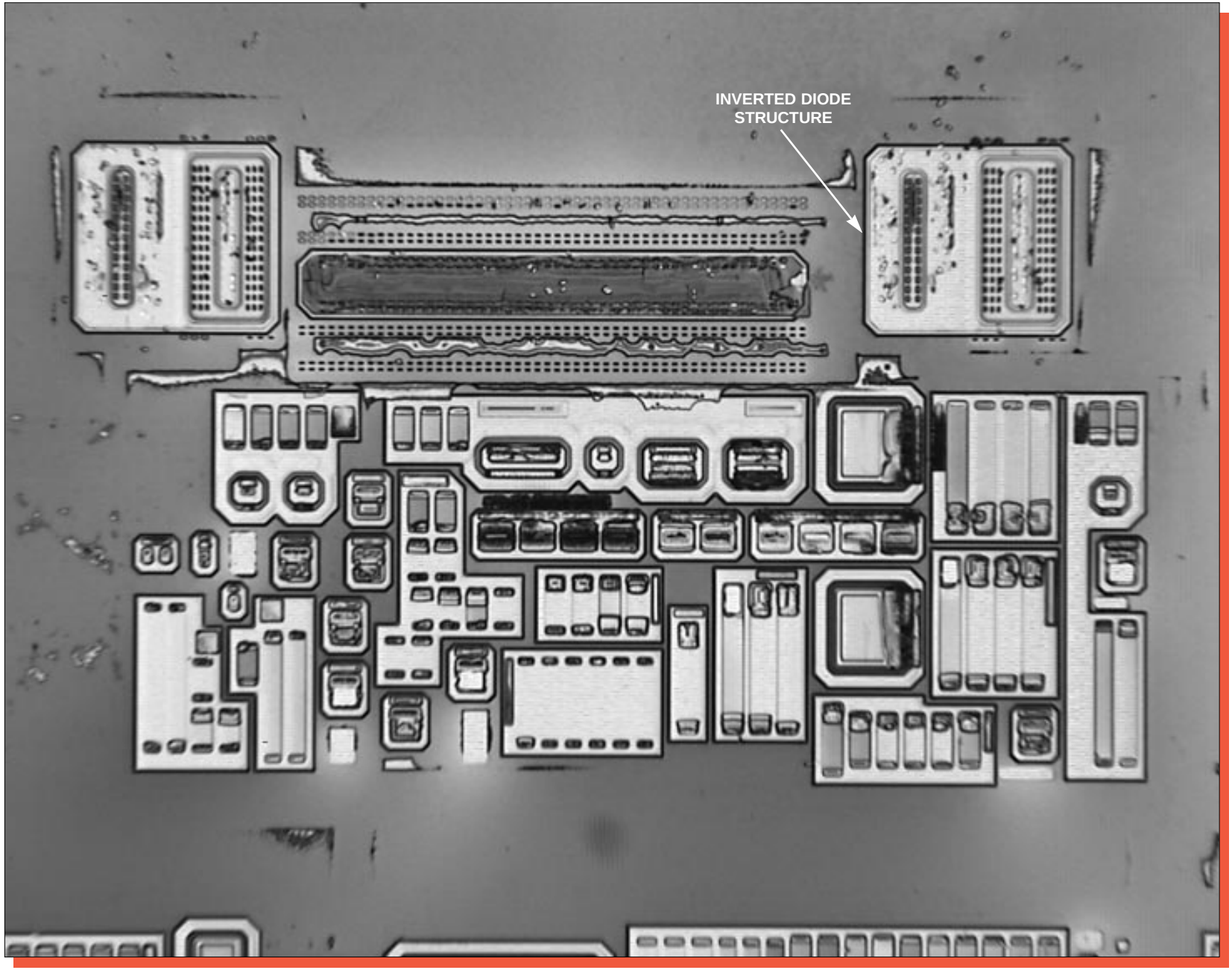


Figure 11b. Delayered optical view of circuit C. Mag. 540x.

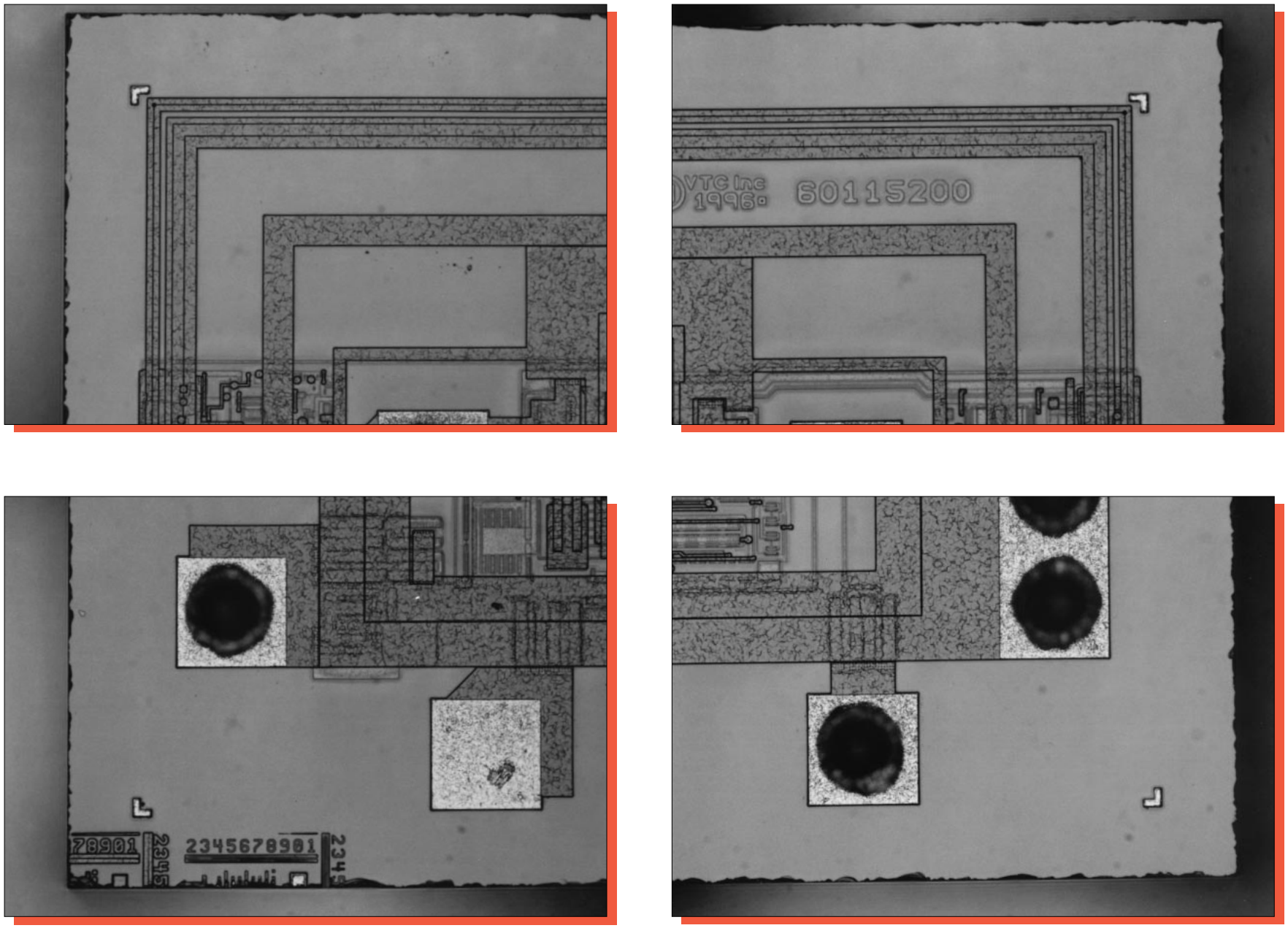
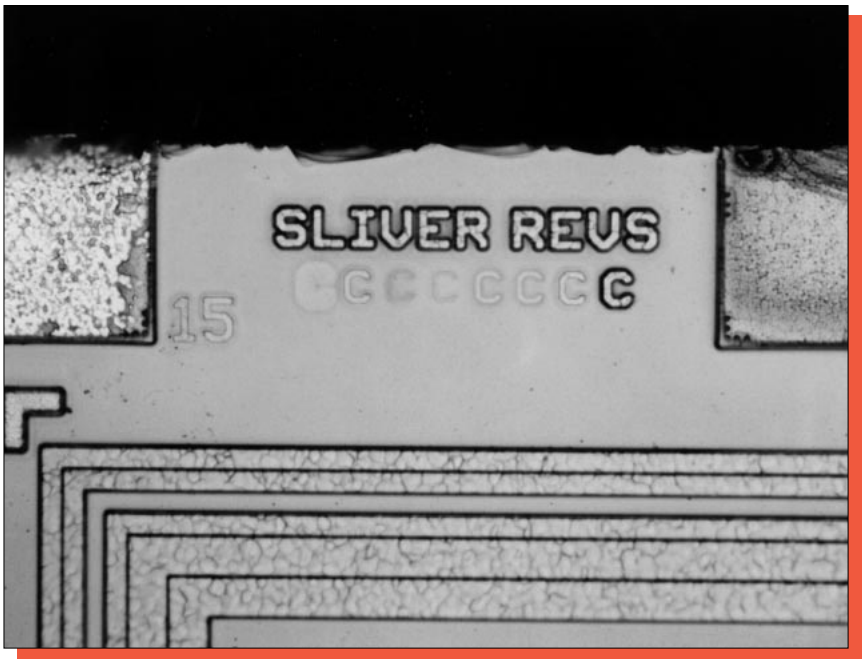


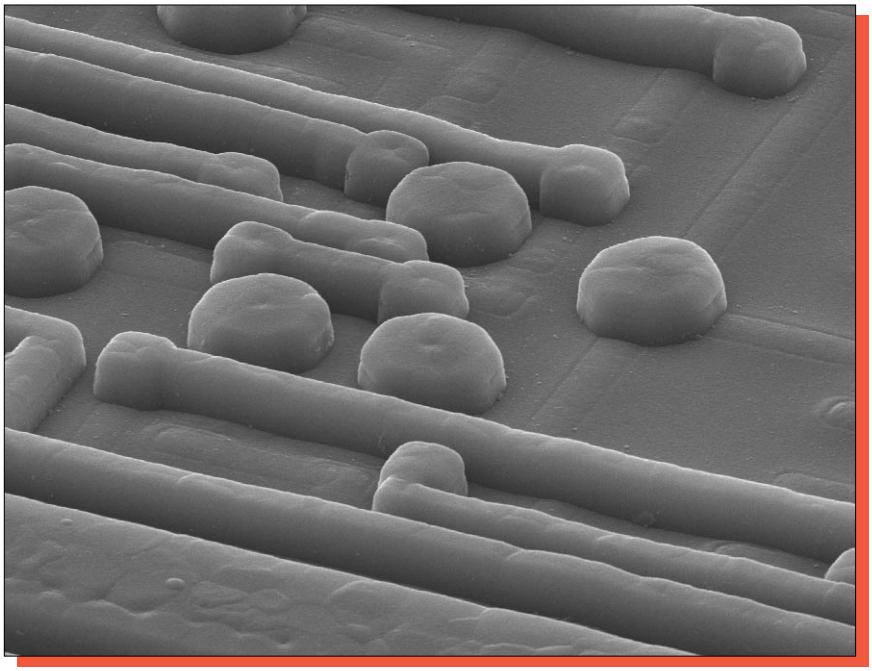
Figure 12. Optical views of the die corners on the VTC VM365830VSJ device. Mag. 200x.

Mag. 320x

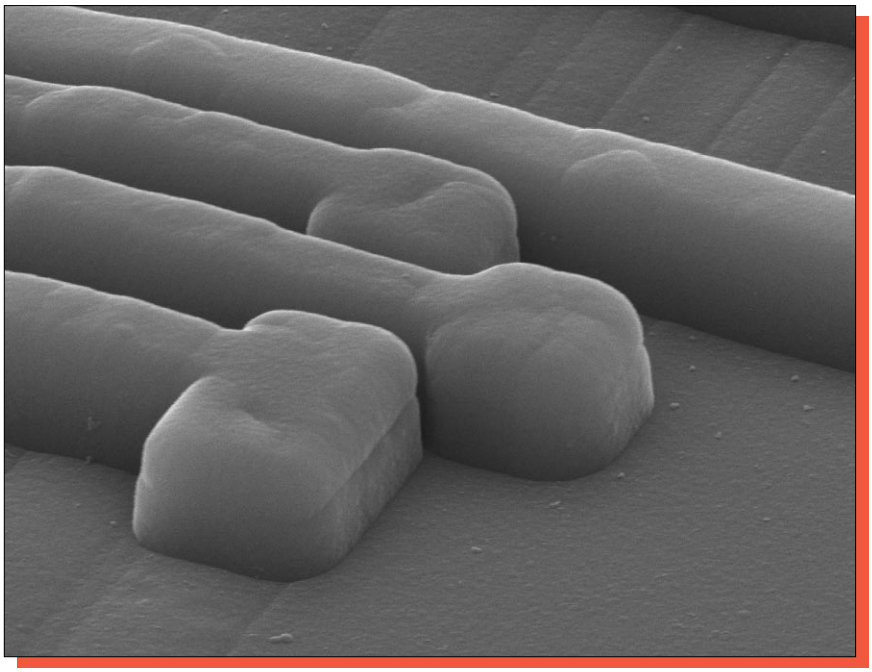


Mag. 500x

Figure 13. Die identification markings from the surface.



Mag. 2600x



Mag. 7100x

Figure 14. SEM views illustrating passivation coverage. 60°

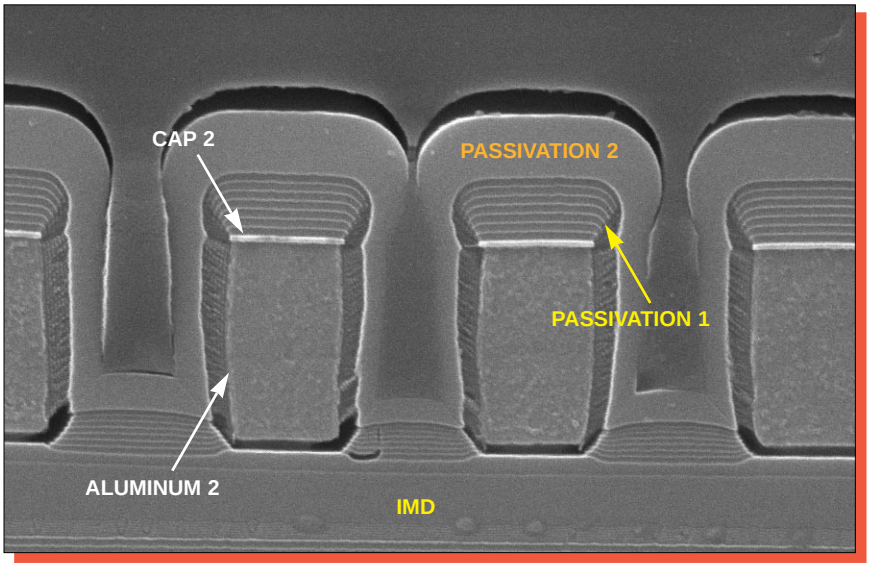
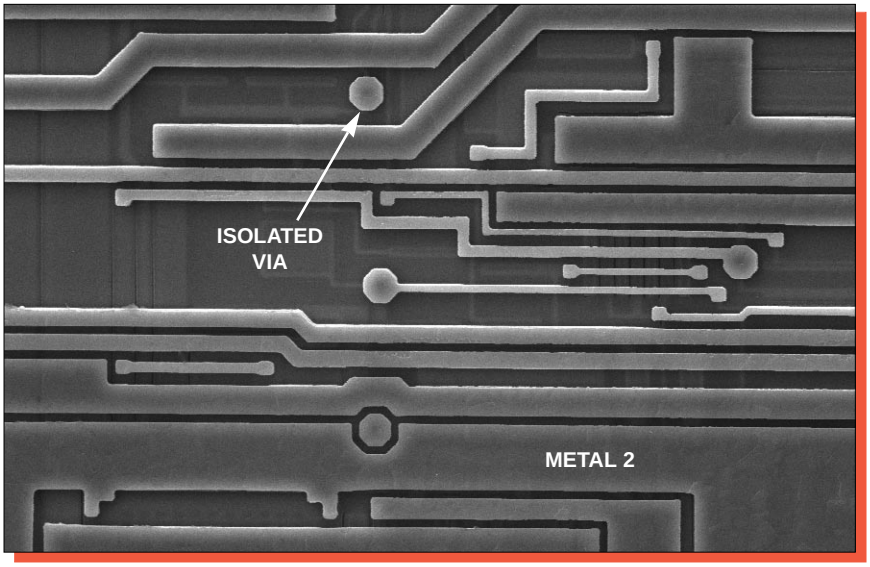
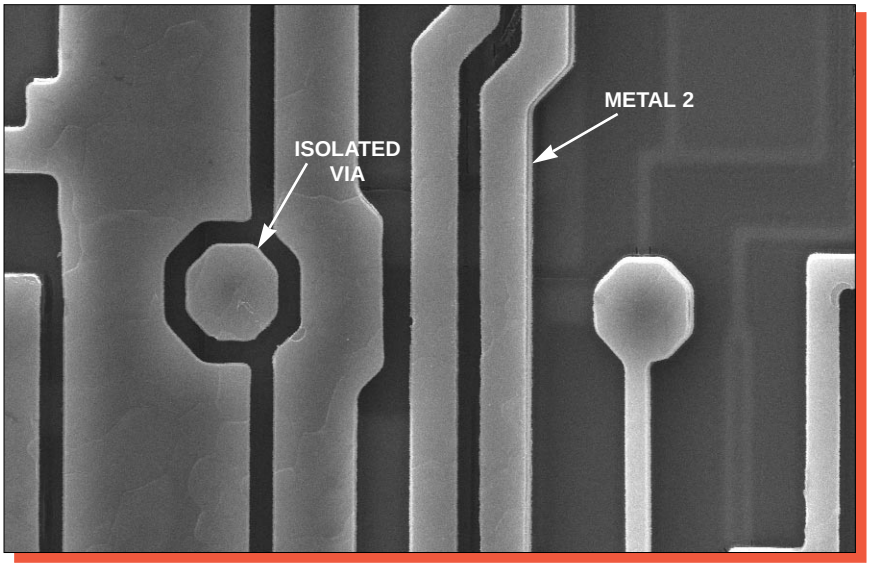


Figure 15. SEM section view of metal 2 line profiles. Mag. 13,000x.

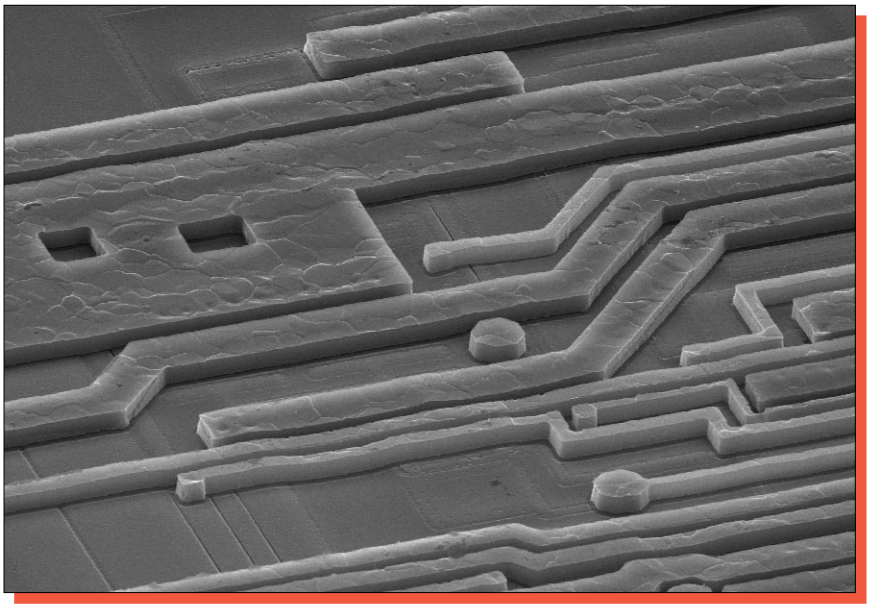


Mag. 800x

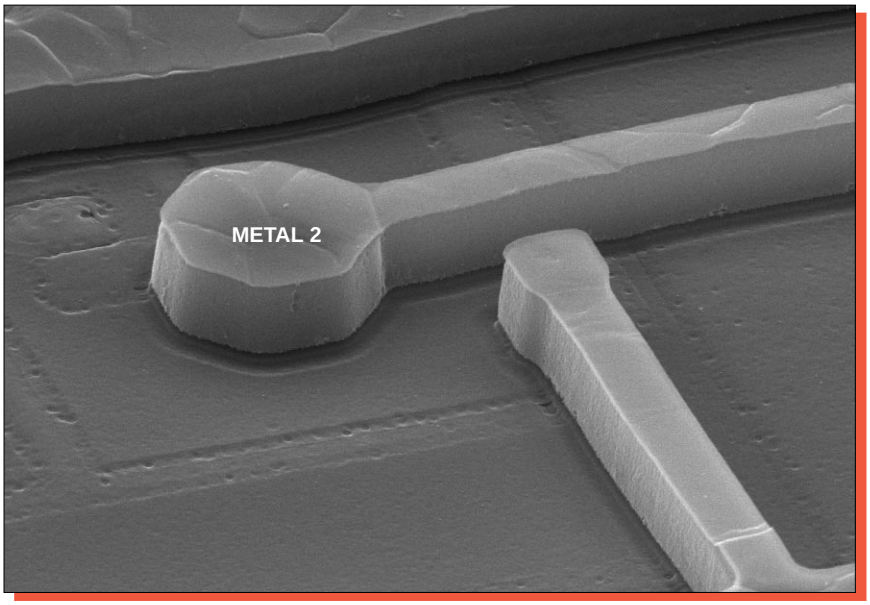


Mag. 2500x

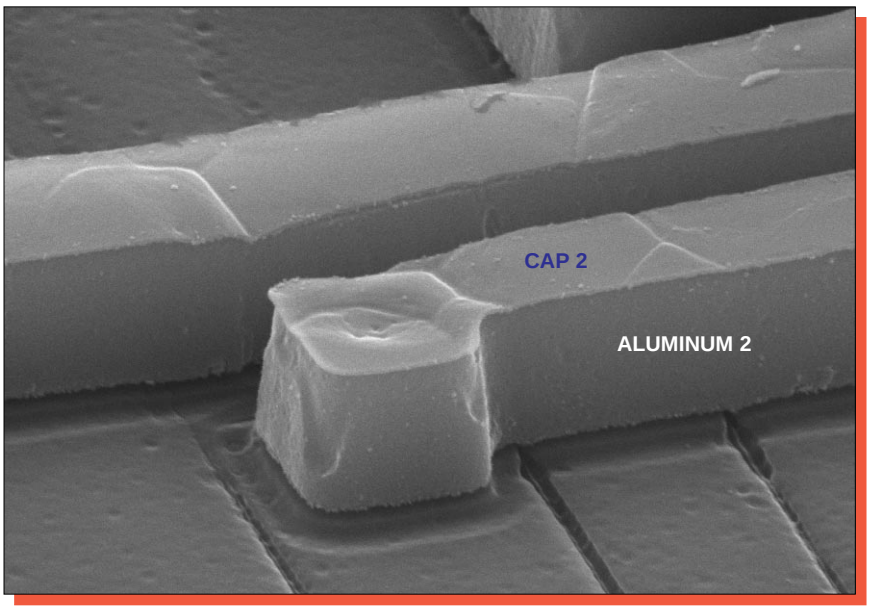
Figure 16. Topological SEM views illustrating metal 2 patterning. 0°.



Mag. 1300x

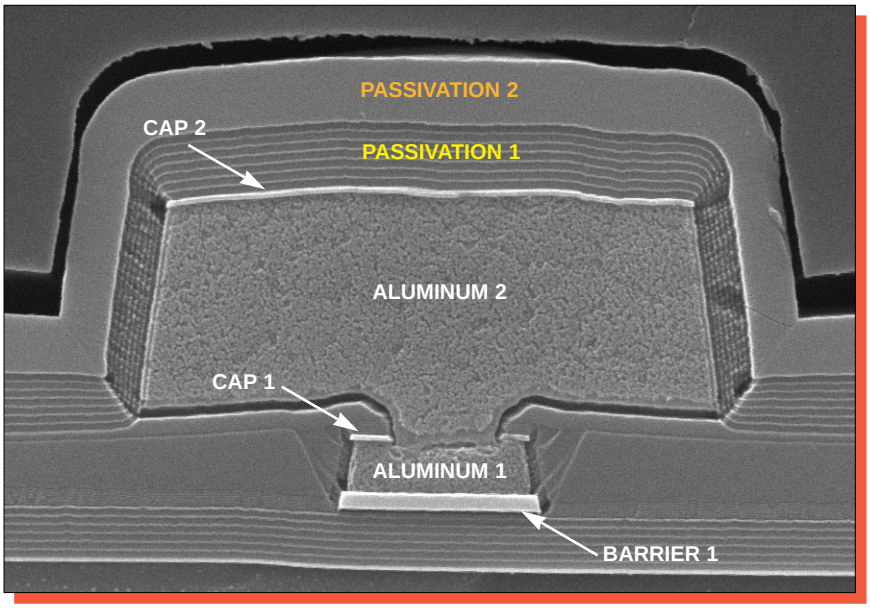


Mag. 5000x

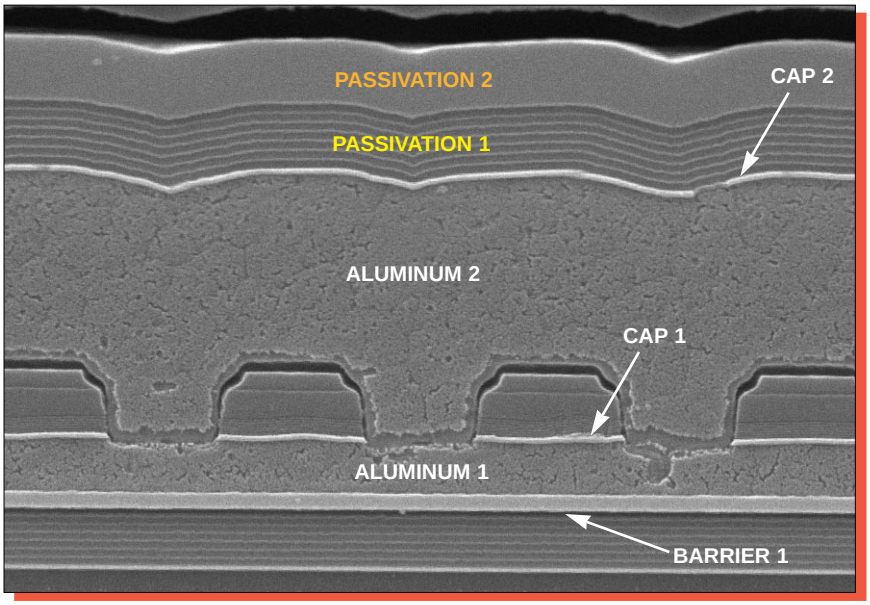


Mag. 10,000x

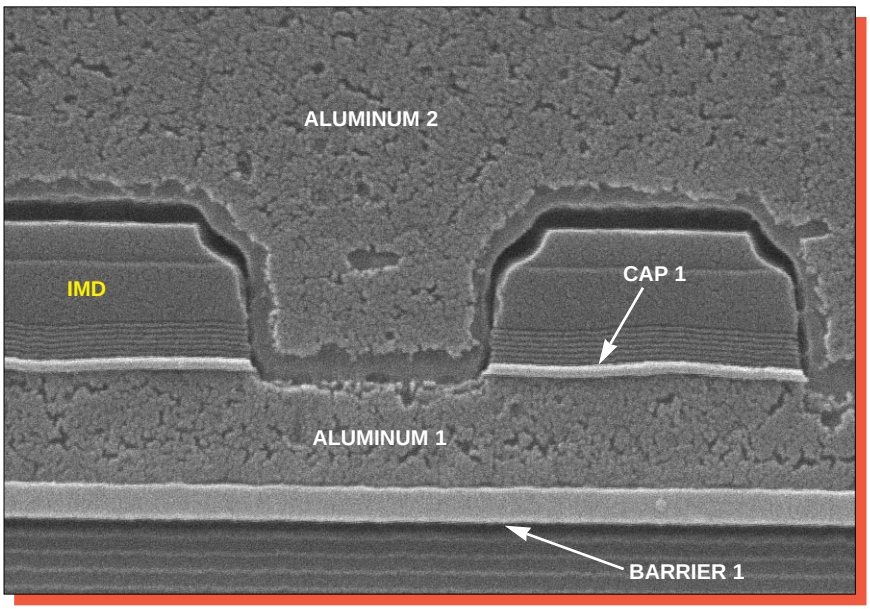
Figure 17. Perspective SEM views of metal 2 coverage. 60°.



Mag. 13,000x

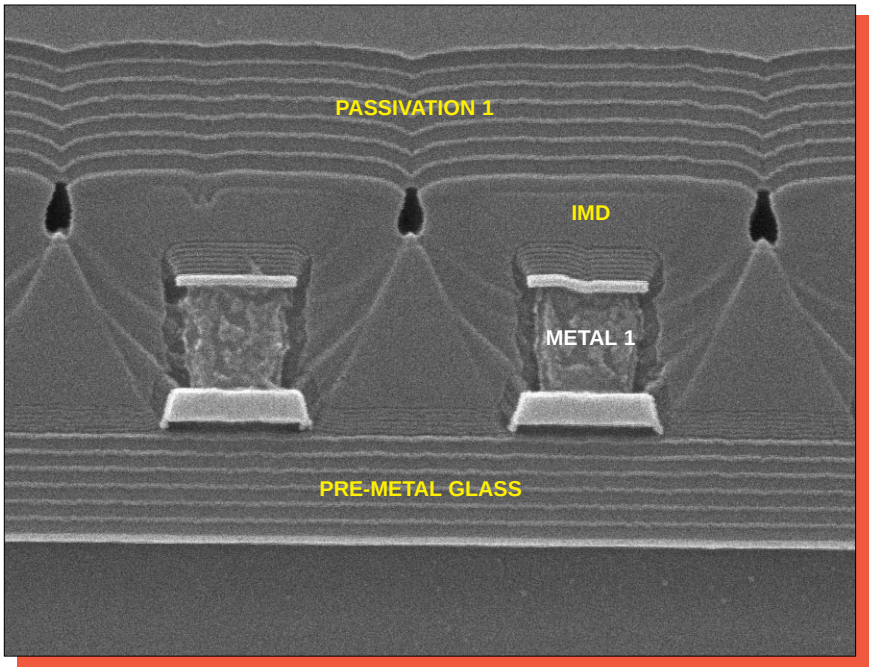


Mag. 13,000x

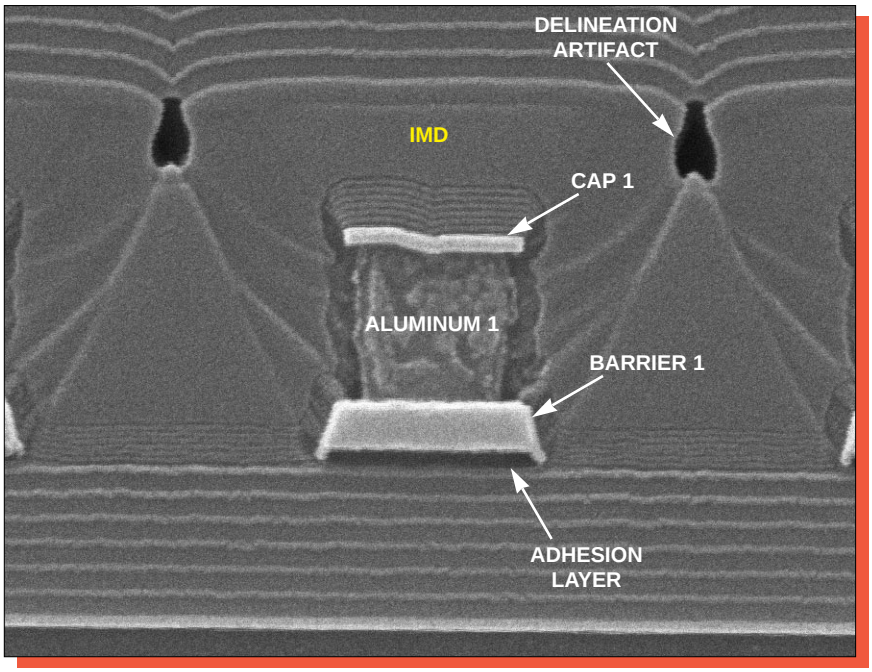


Mag. 30,000x

Figure 18. SEM section views of metal 2 vias.

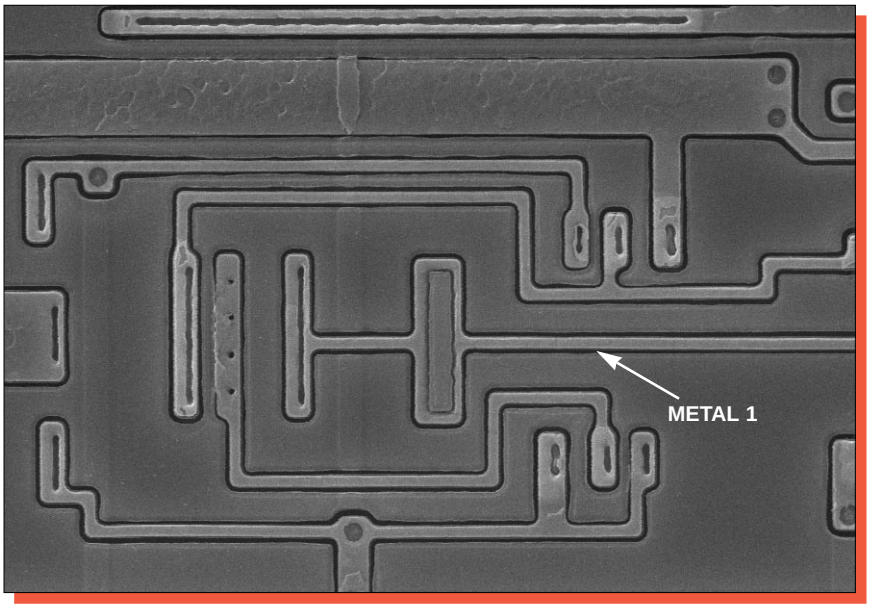


Mag. 26,000x

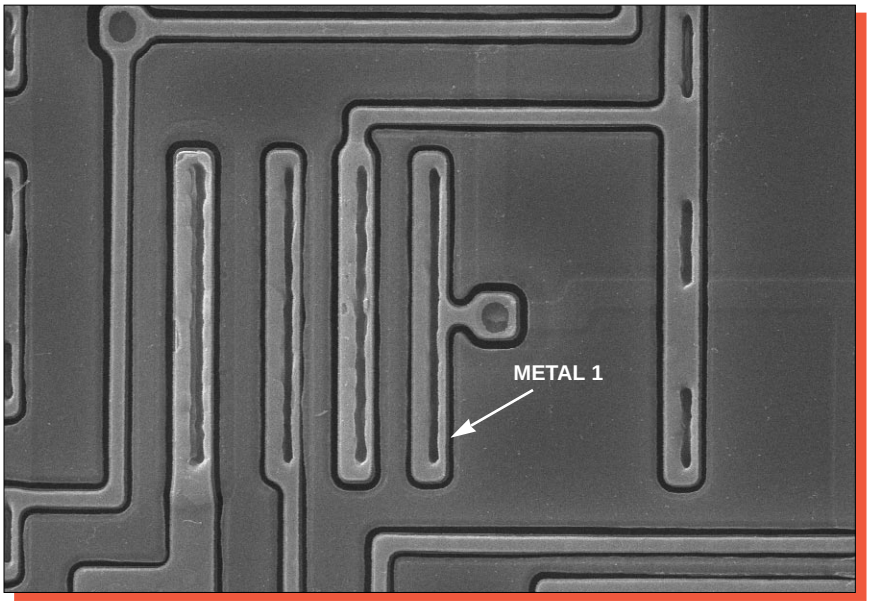


Mag. 40,000x

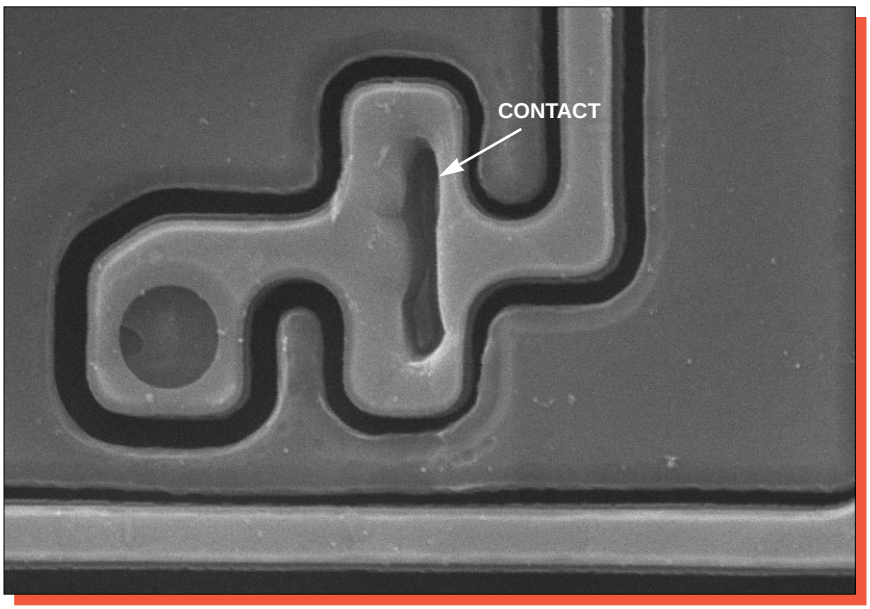
Figure 19. SEM section views of metal 1 line profiles.



Mag. 2300x

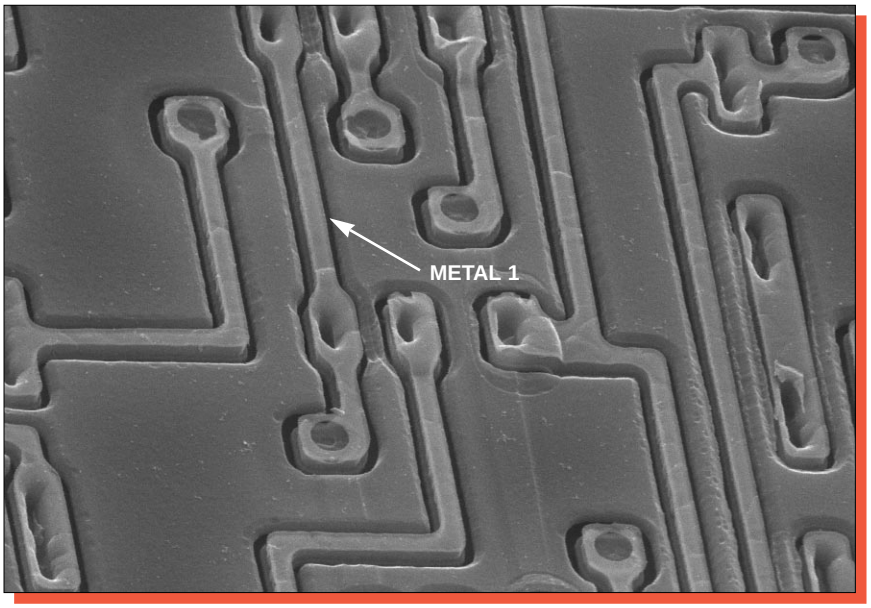


Mag. 3000x

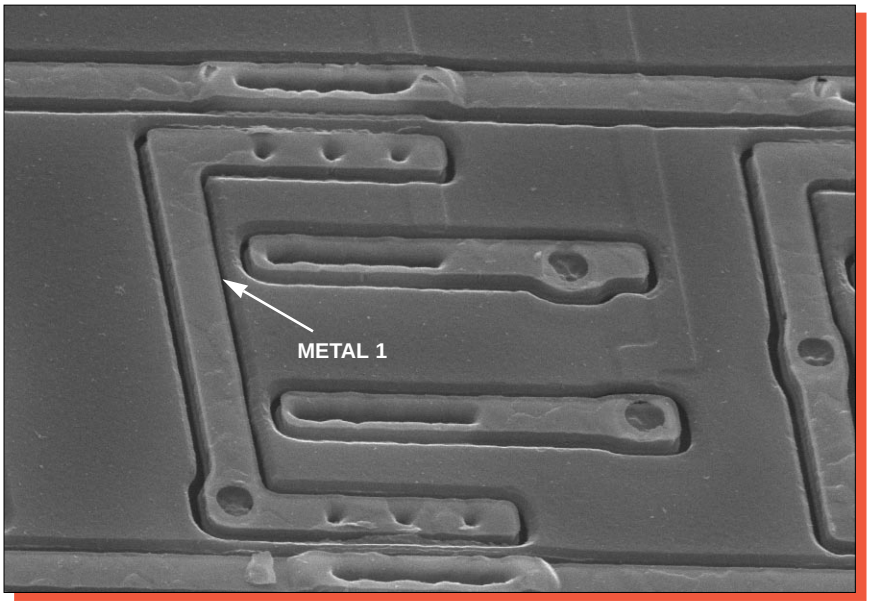


Mag. 12,000x

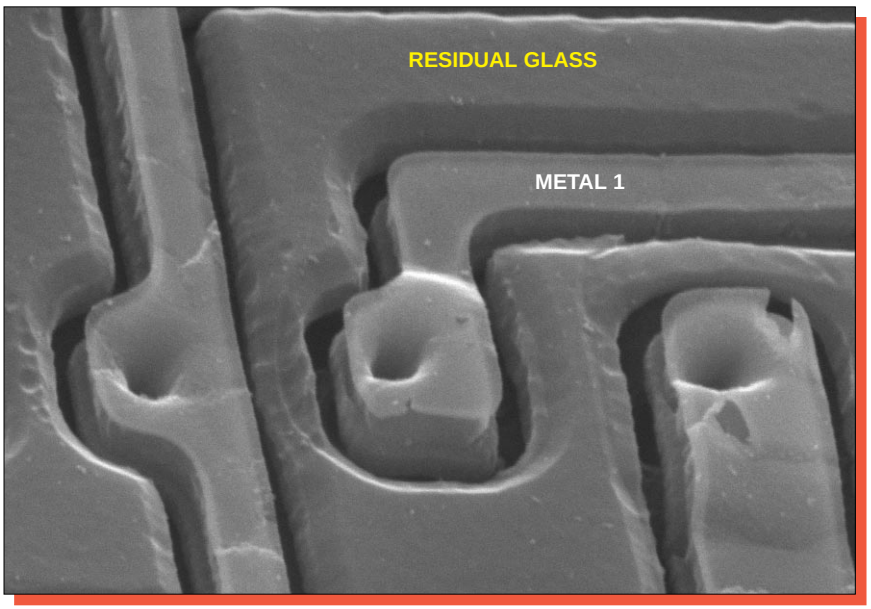
Figure 20. Topological SEM views illustrating metal 1 patterning. 0°.



Mag. 4000x

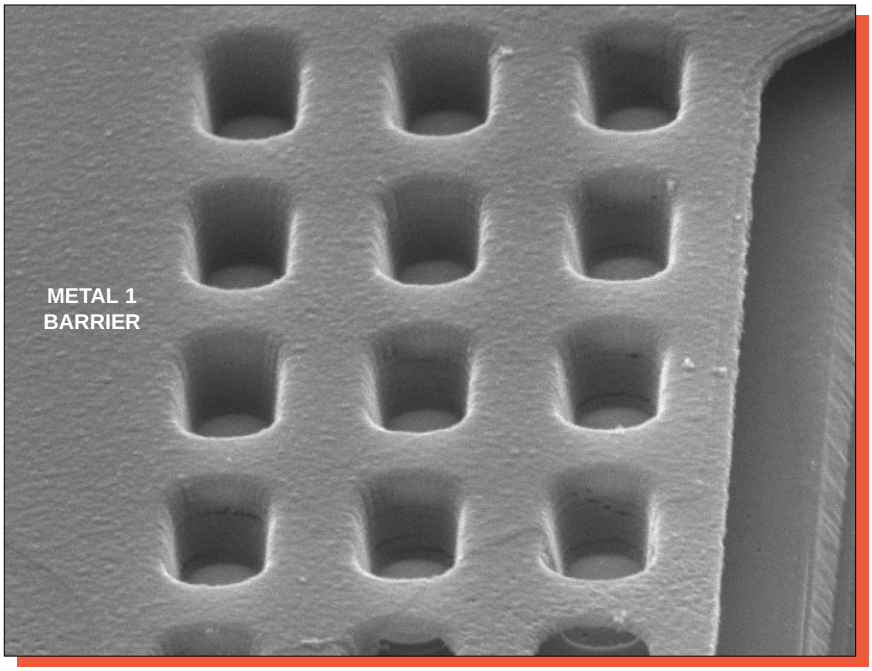


Mag. 4000x

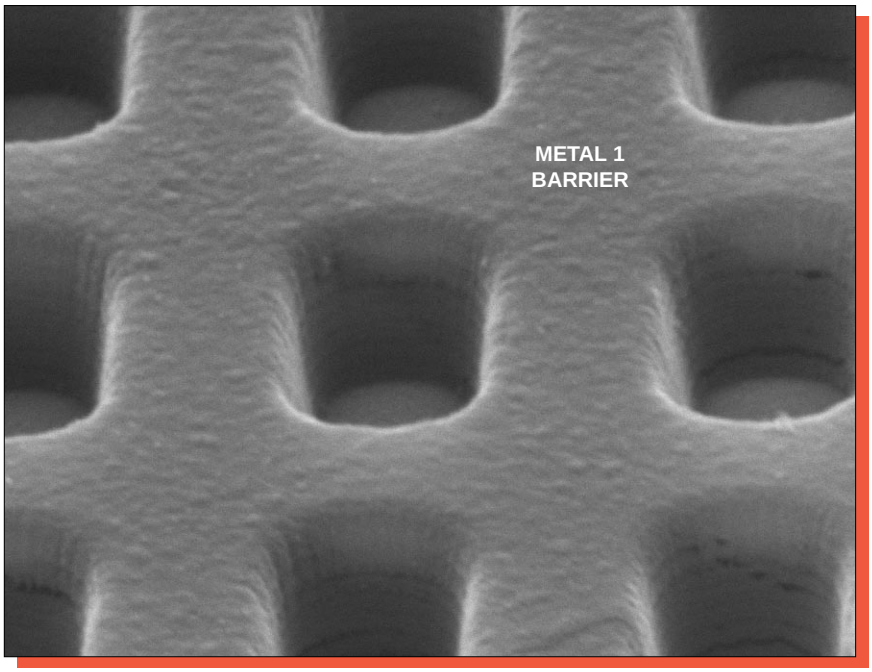


Mag. 13,000x

Figure 21. Perspective SEM views of metal 1 coverage. 60°.

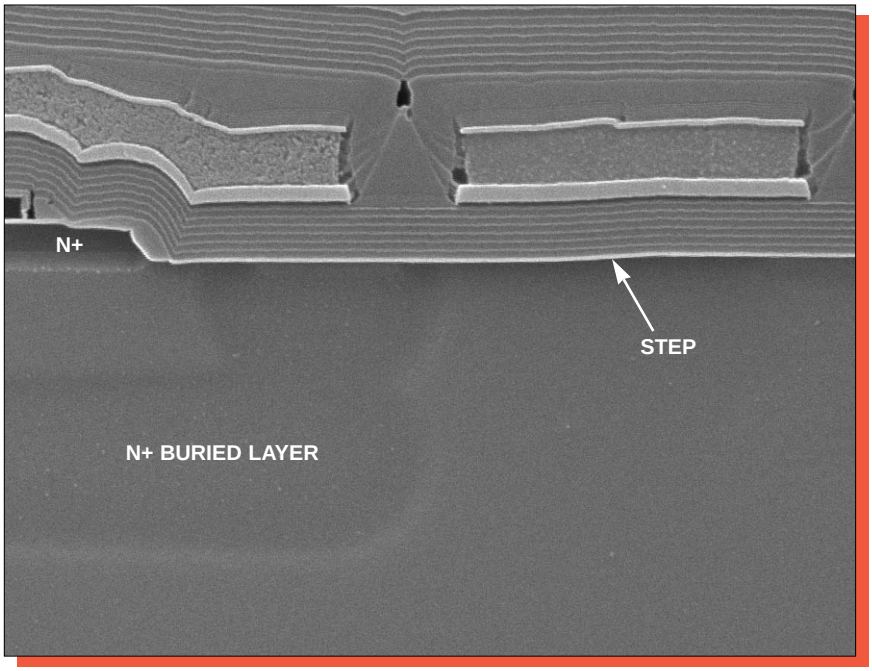


Mag. 13,500x

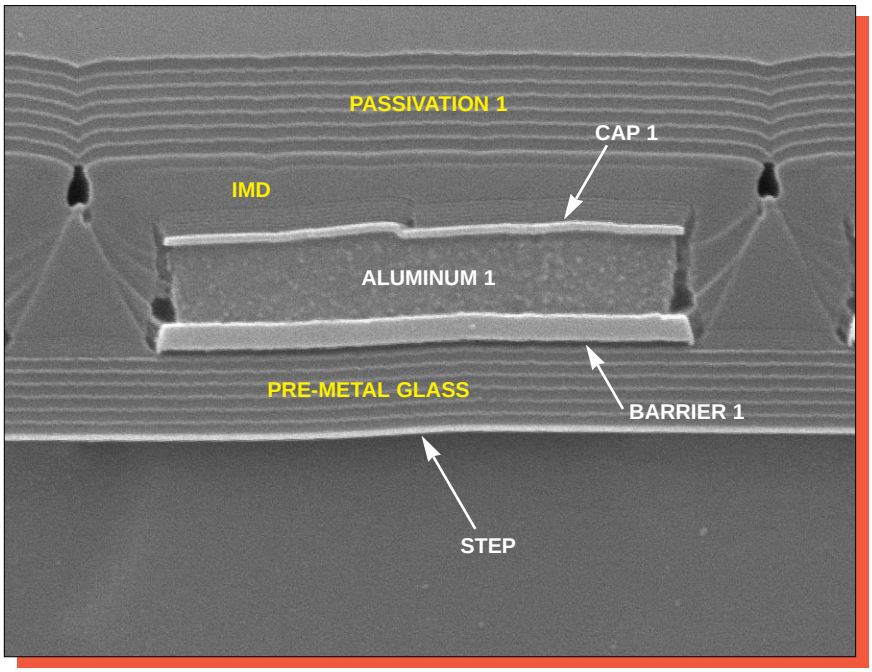


Mag. 27,000x

Figure 22. Perspective SEM views of metal 1 barrier. 60°.



Mag. 13,000x



Mag. 20,000x

Figure 23. SEM section views of the step in the oxide at epi boundary.

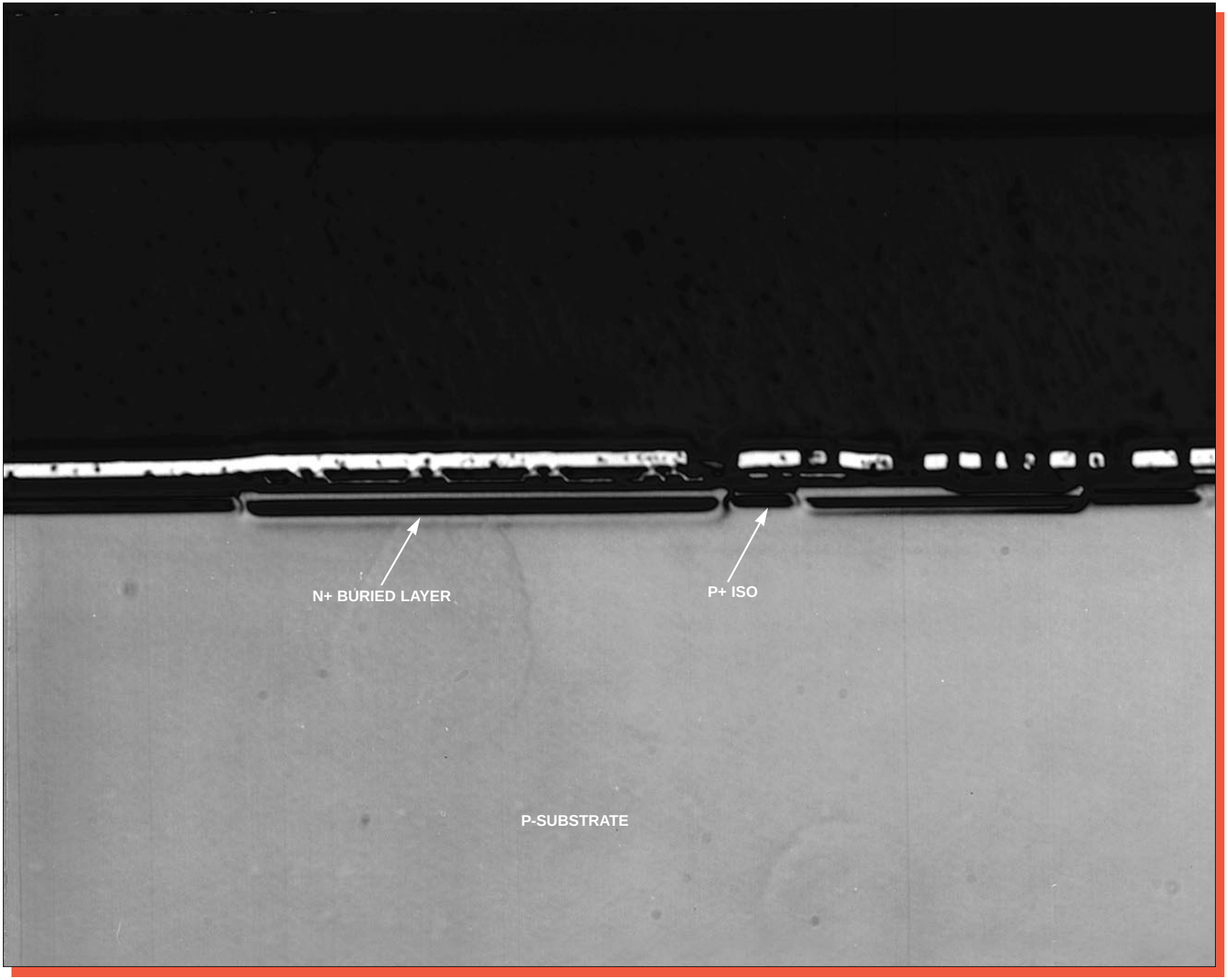
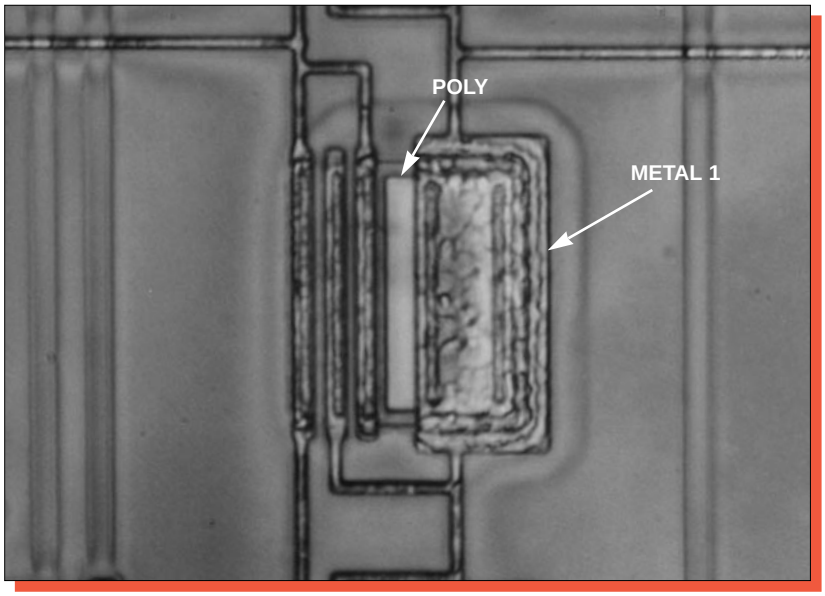
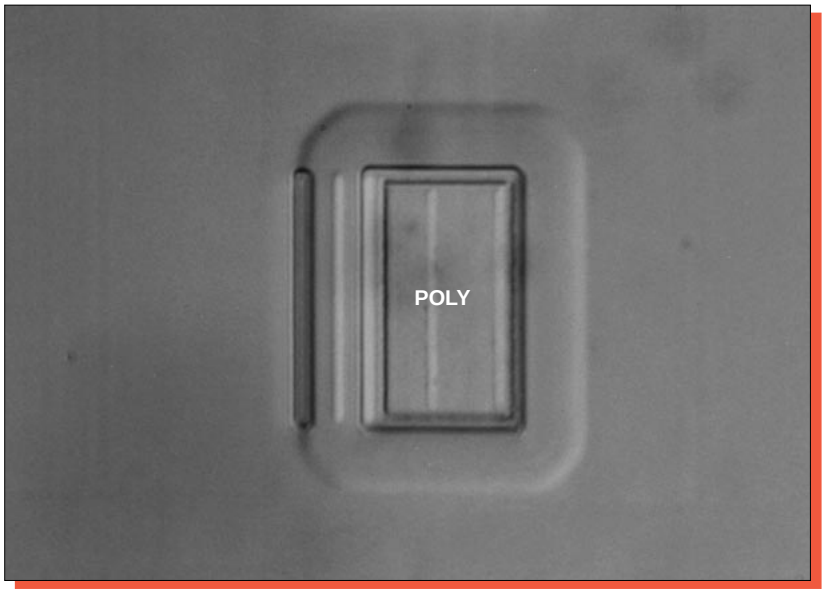


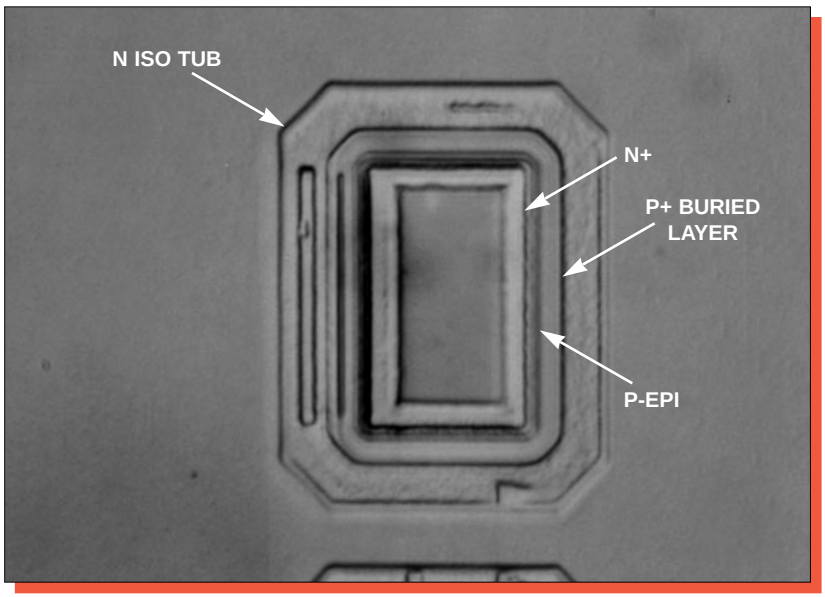
Figure 23a. Optical view illustrating general bipolar structure. Mag. 1600x.



metal 1

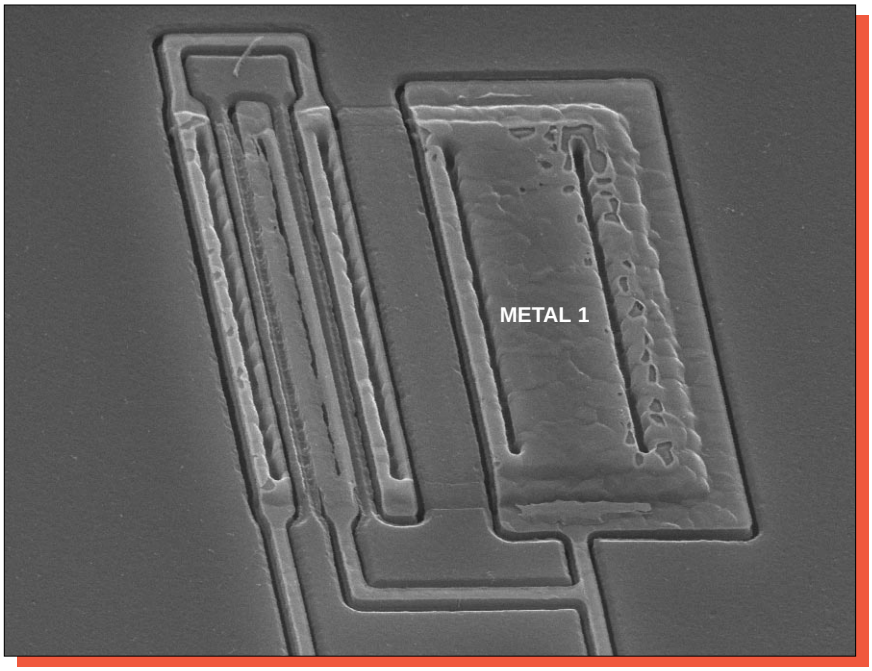


unlayered

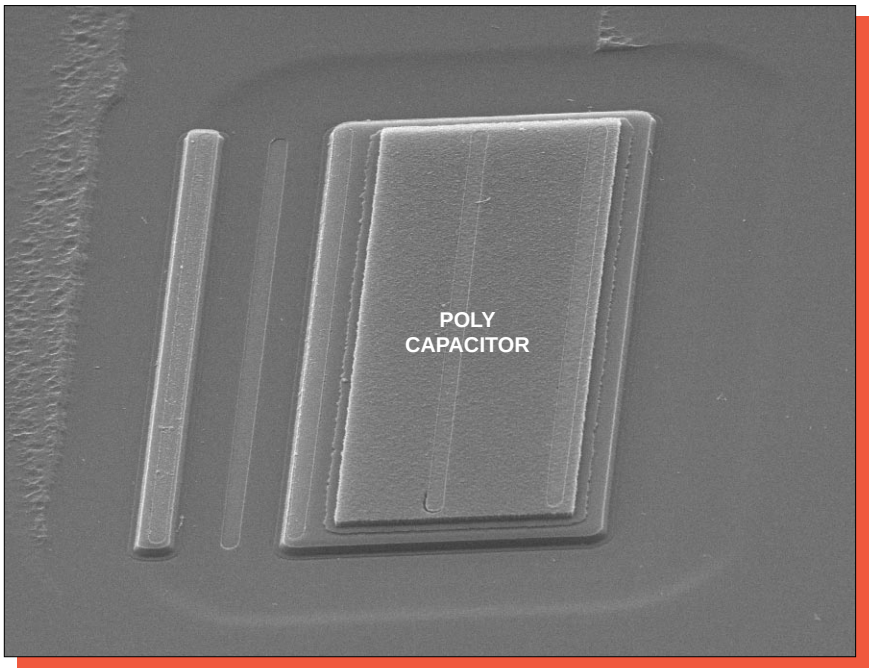


stained

Figure 24. Optical views of a capacitor and diode structure. Mag. 1600x.

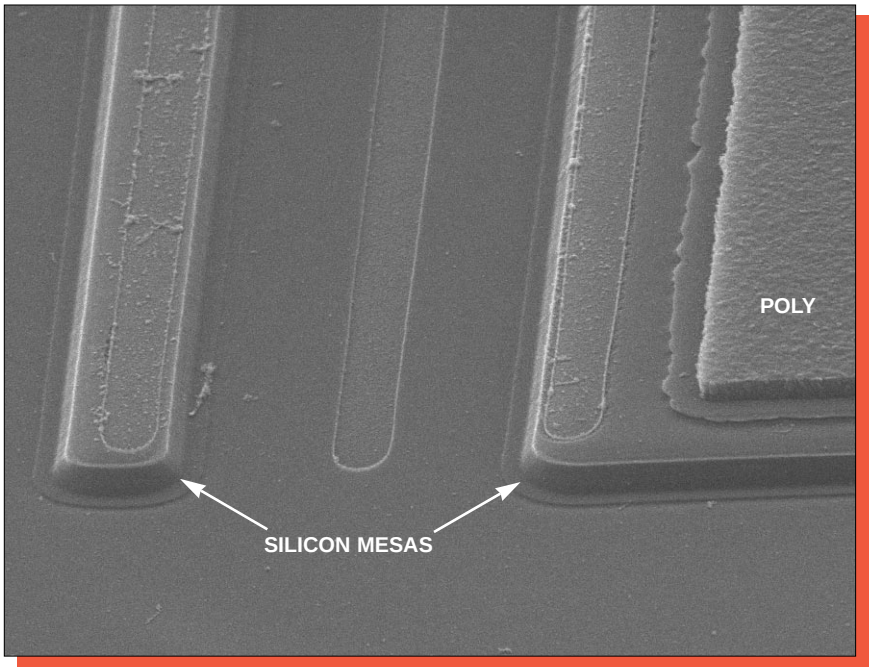


metal 1

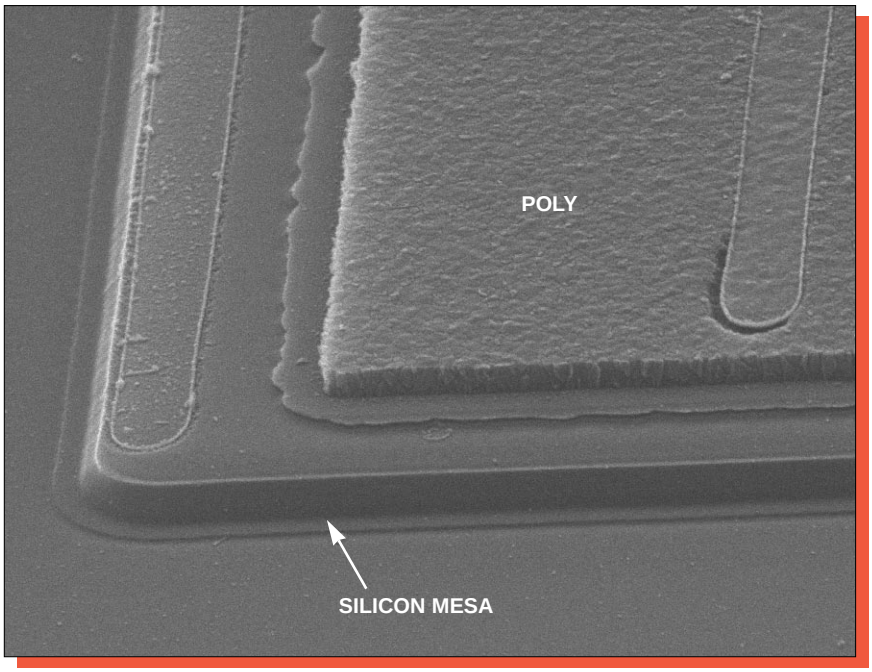


unlayered

Figure 25. Perspective SEM views of a capacitor and diode structure. Mag. 3000x, 60°.

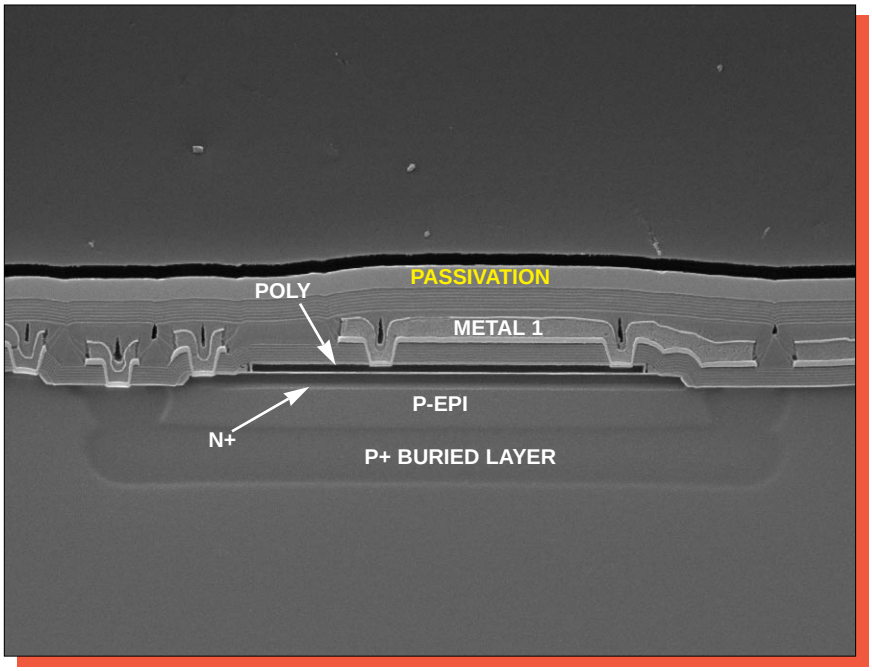


Mag. 11,000x

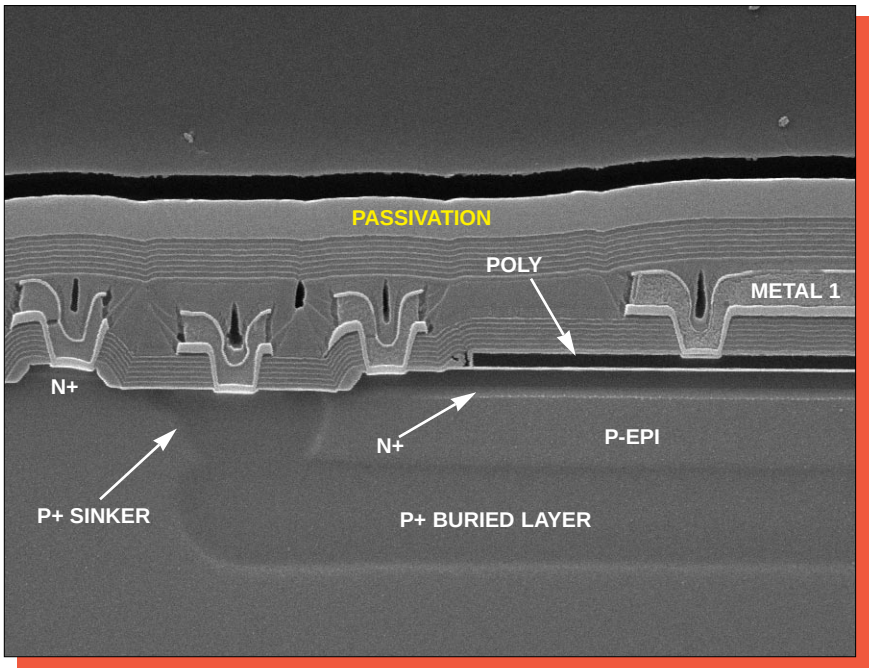


Mag. 15,000x

Figure 26. Detailed SEM views of the capacitor and diode structure. 60°.

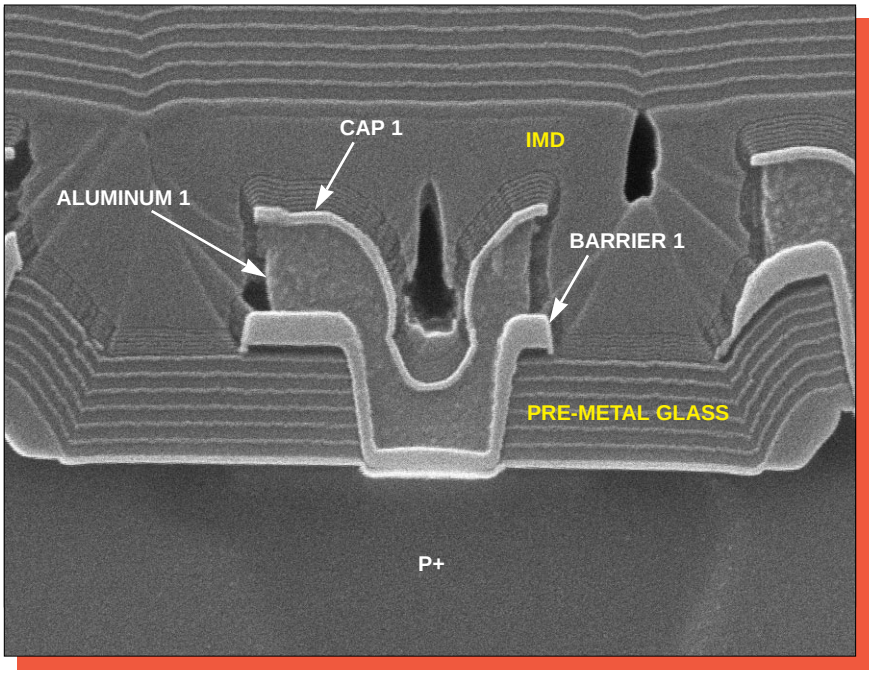


Mag. 4500x



Mag. 8000x

Figure 27. SEM section views of a capacitor and diode structure.



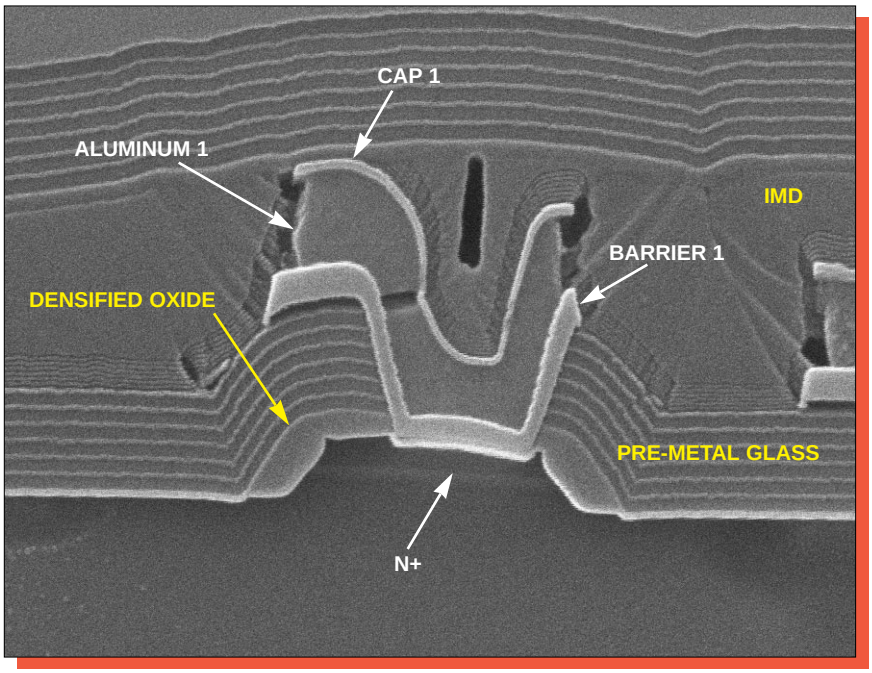
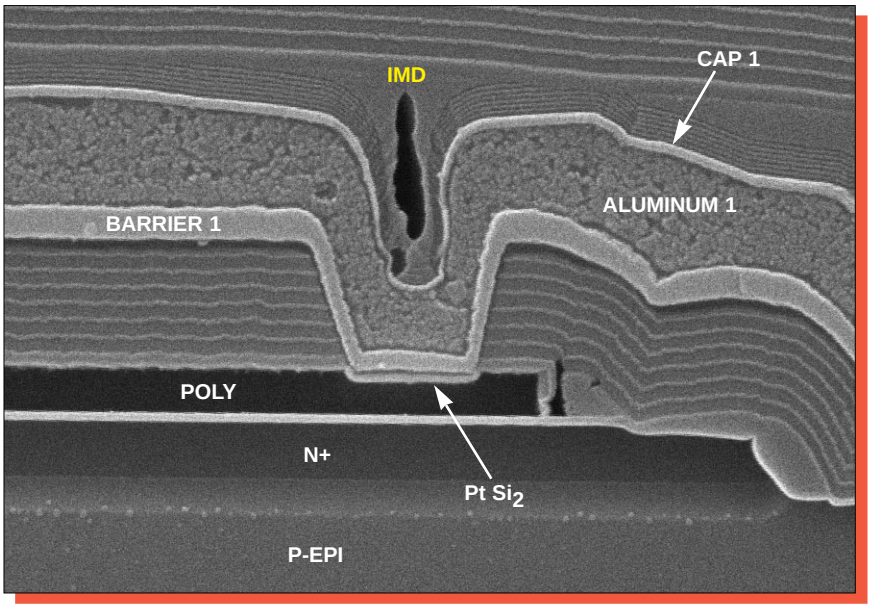
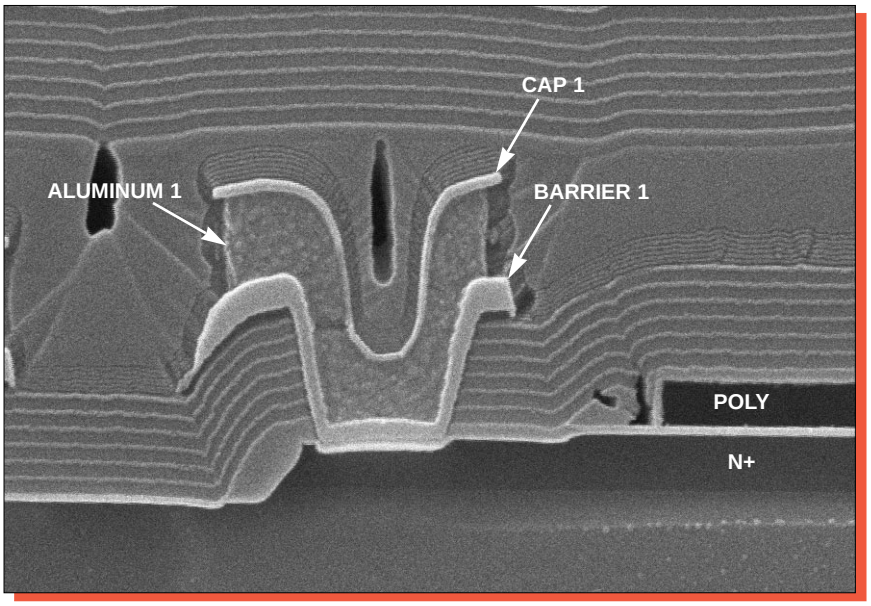


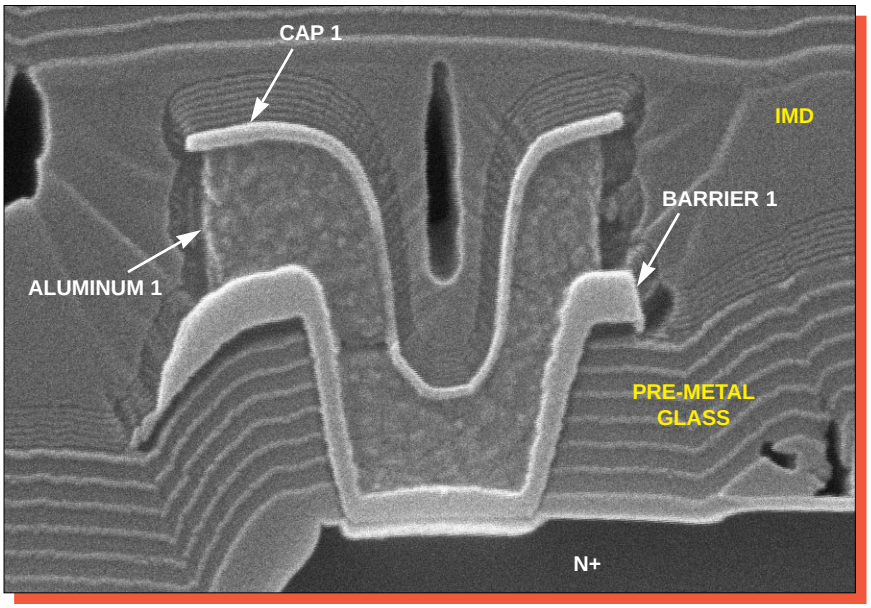
Figure 28. Detailed SEM section views through the capacitor and diode contacts.
Mag. 26,000x.



Mag. 26,000x

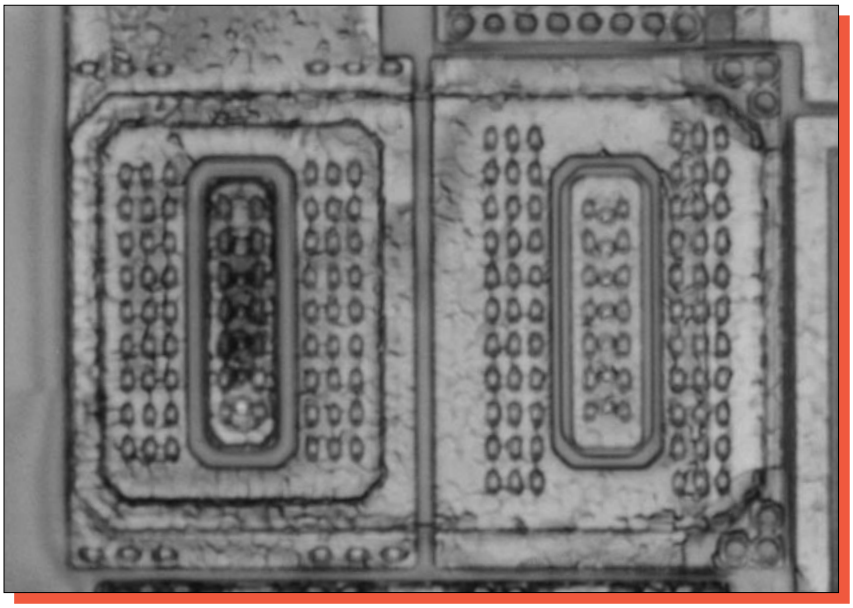


Mag. 26,000x

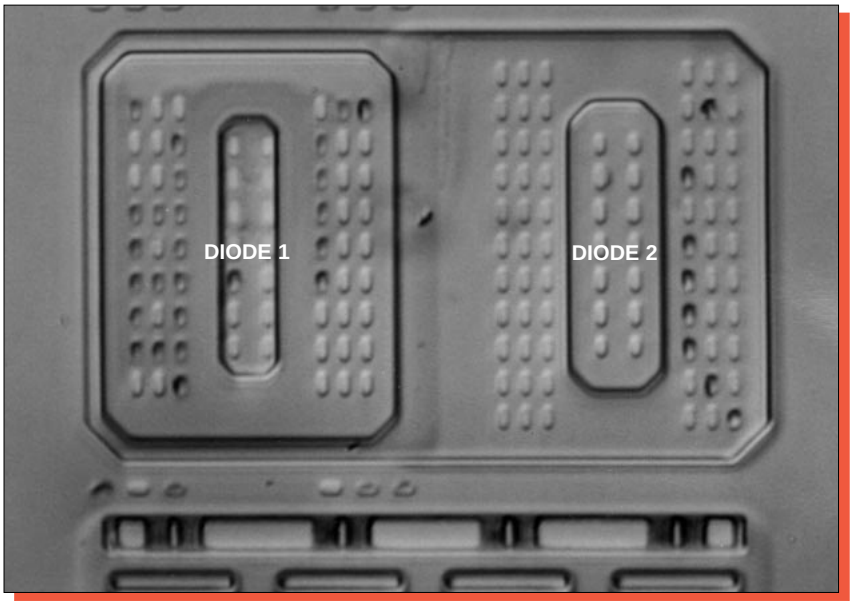


Mag. 40,000x

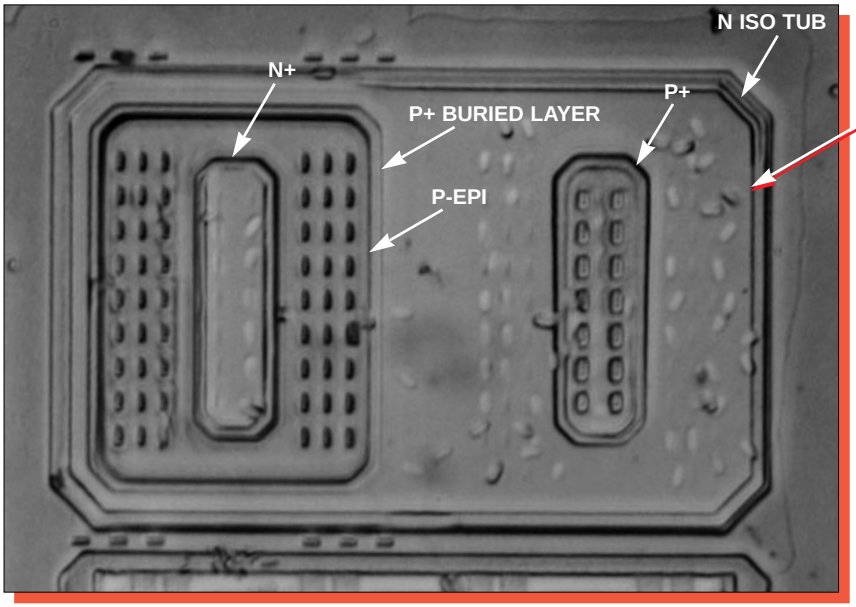
Figure 29. Additional detailed SEM section views through the capacitor and diode region.



metal 1



delayered



stained

Figure 30. Optical views of an inverted diode structure.

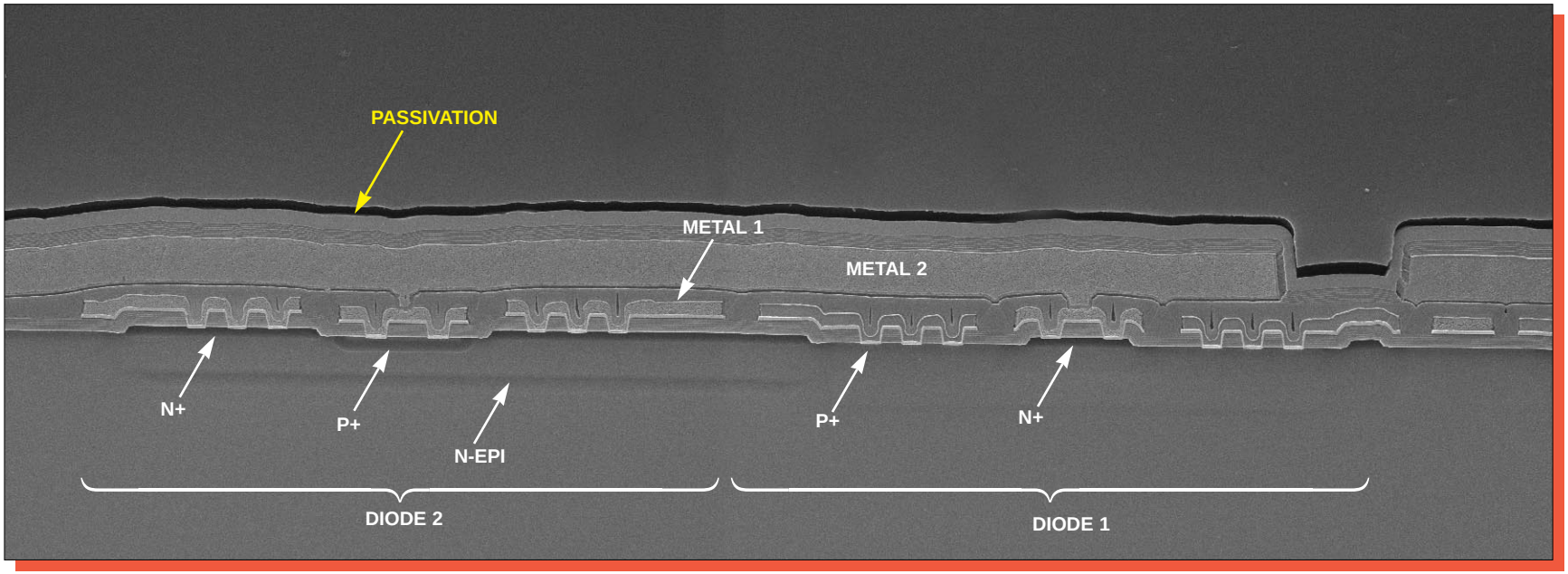
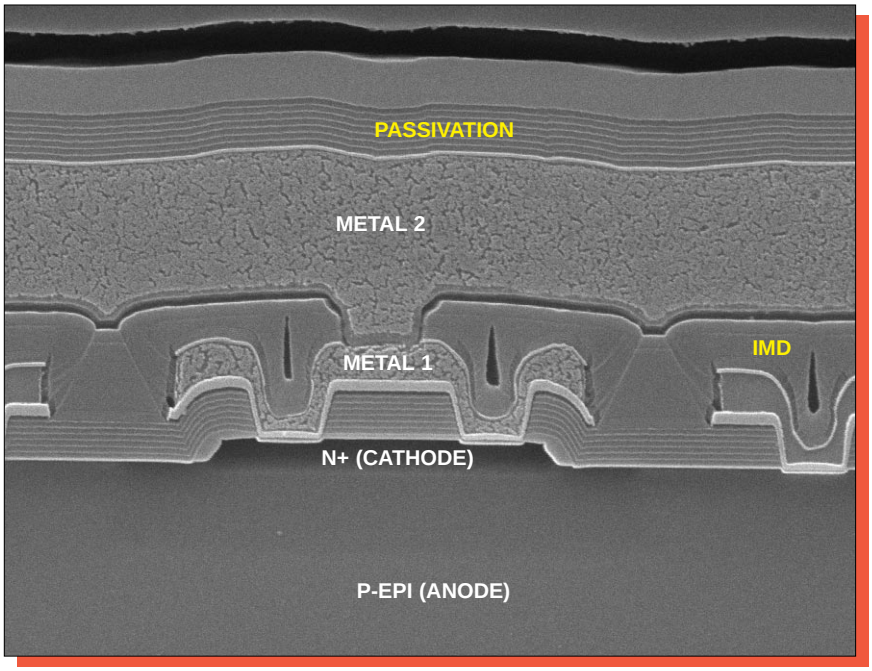
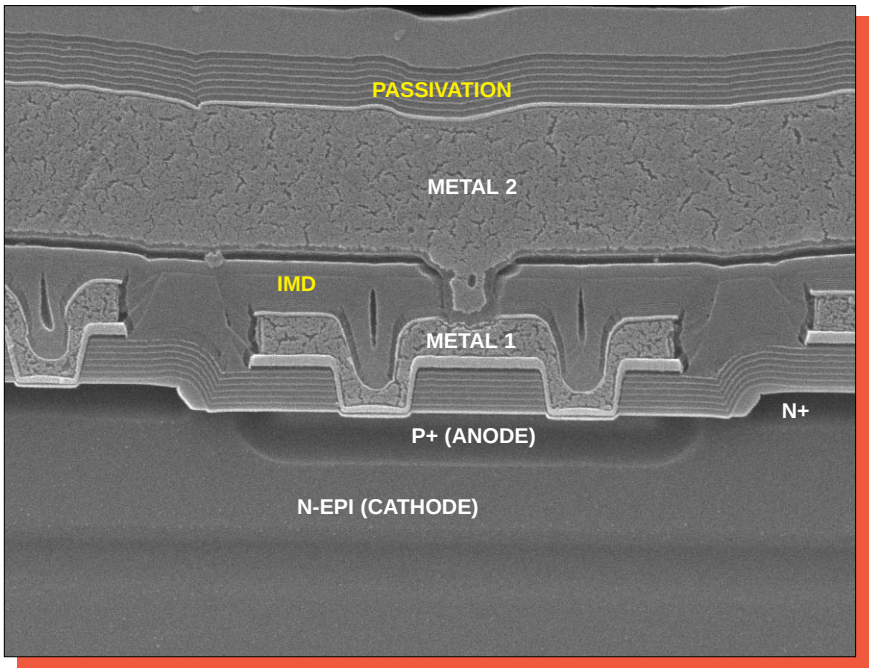


Figure 31. SEM section views illustrating an inverted diode structure. Mag. 3000x.

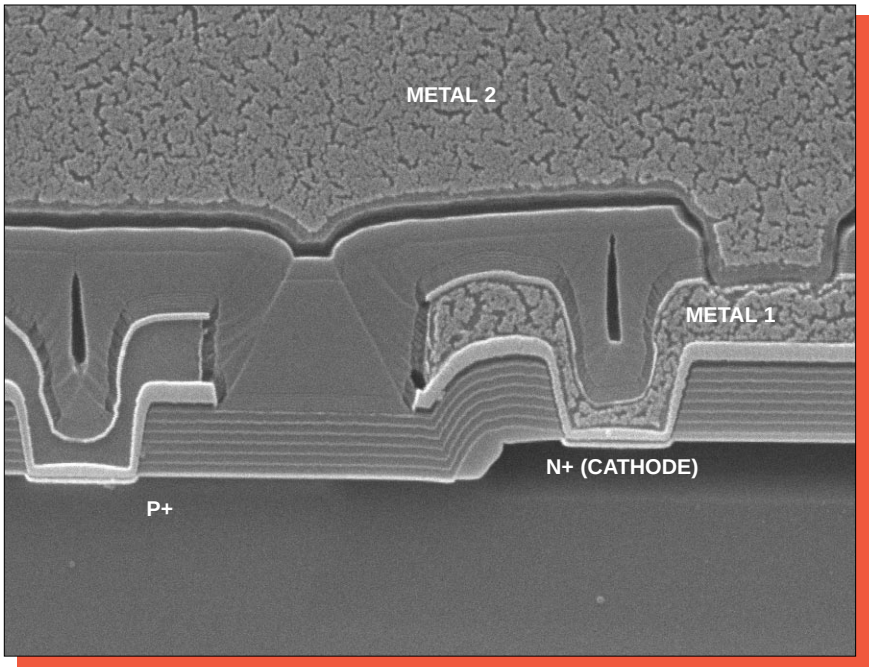


diode 1

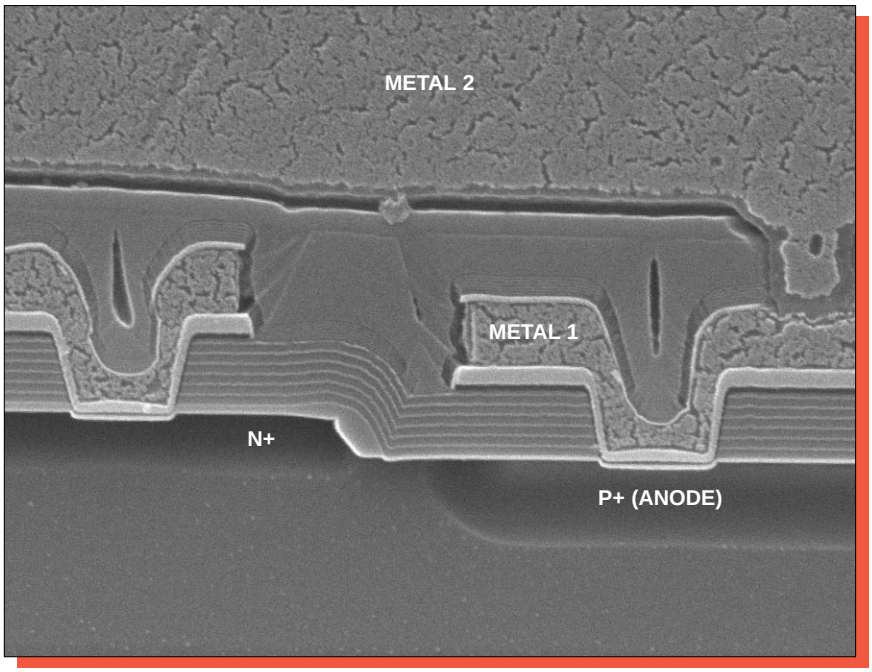


diode 2

Figure 32. SEM section details of an inverted diode structure. Mag. 10,000x.



diode 1



diode 2

Figure 33. Additional SEM section details of an inverted diode structure. Mag. 16,000x.

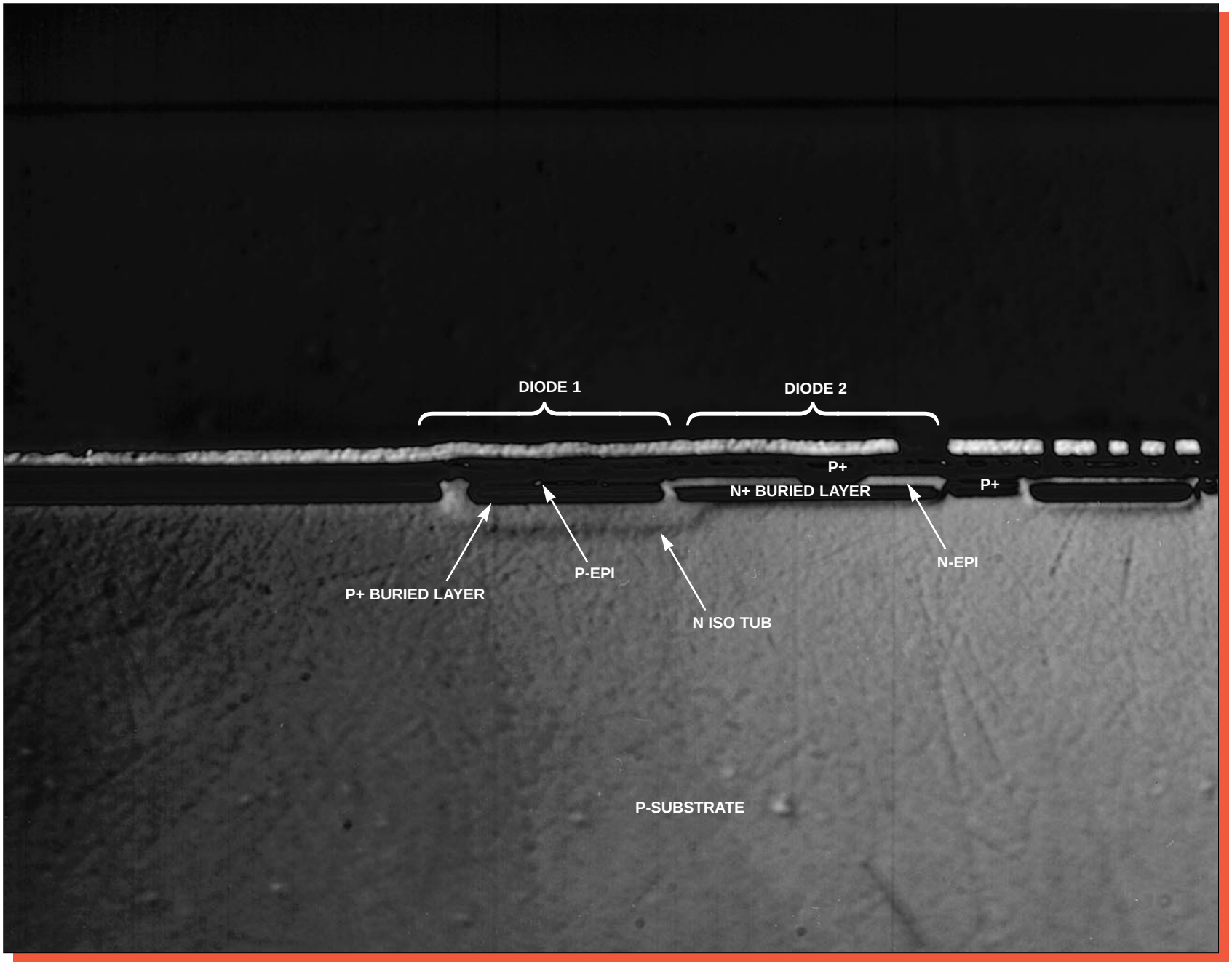
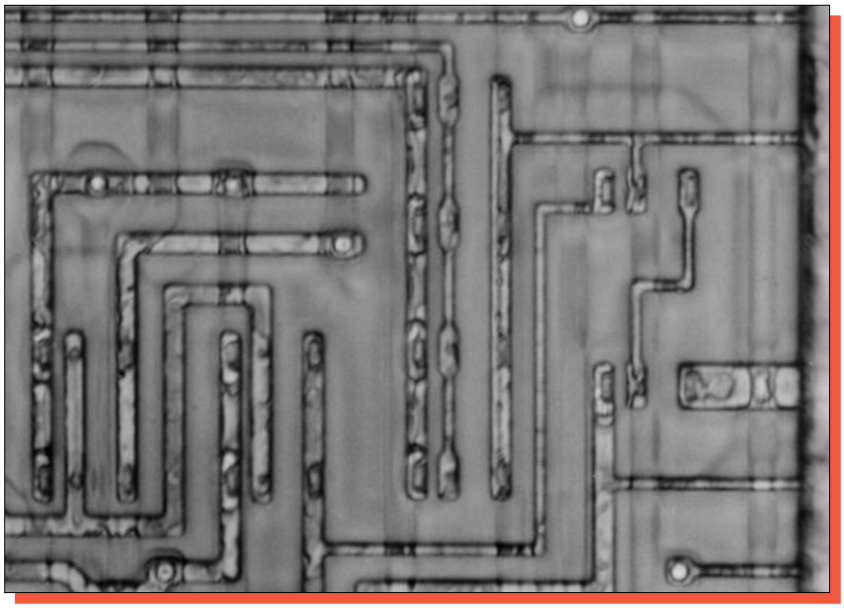
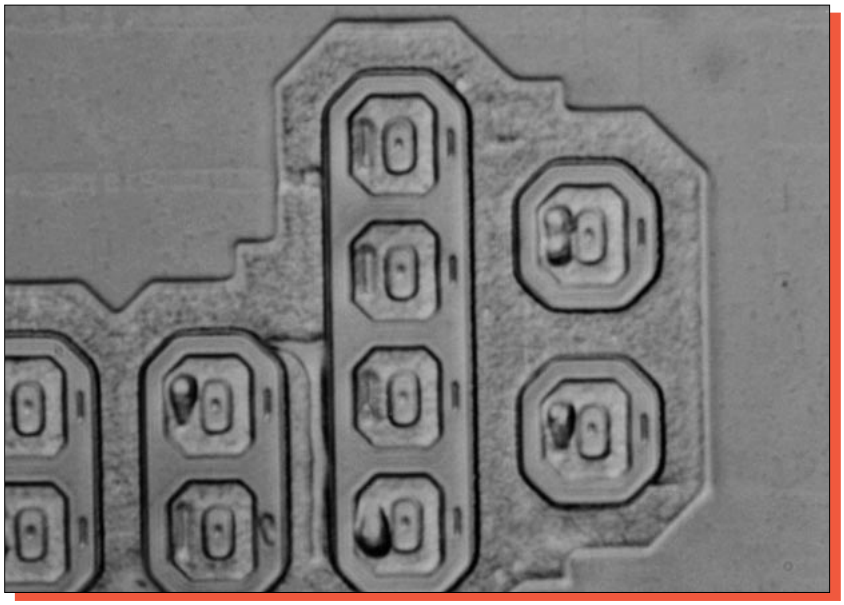


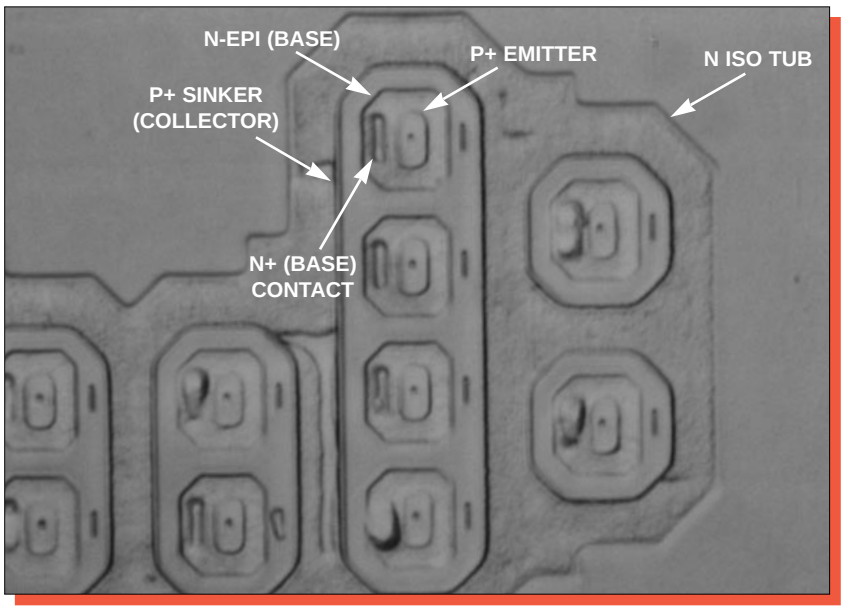
Figure 34. Optical view illustrating the inverted diode structure. Mag. 1600x.



metal 1

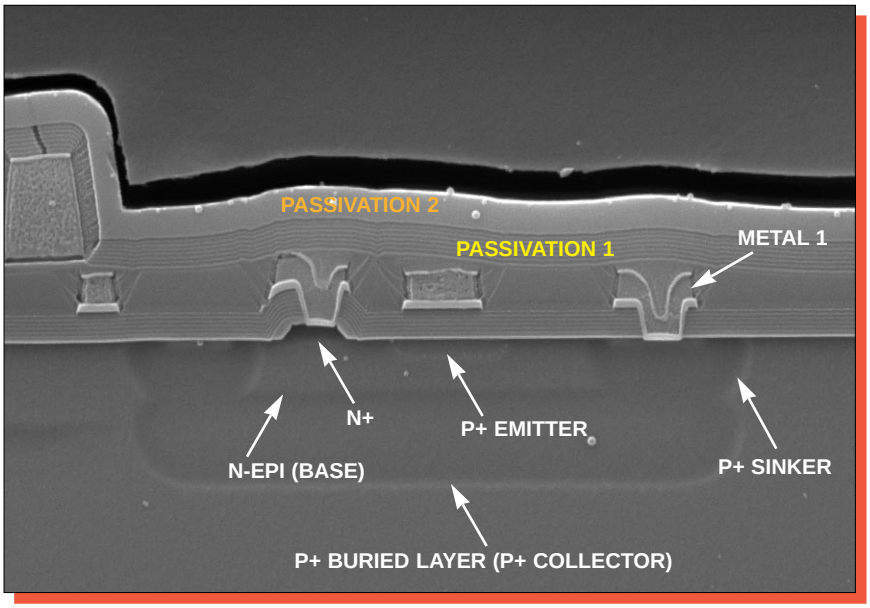


unlayered

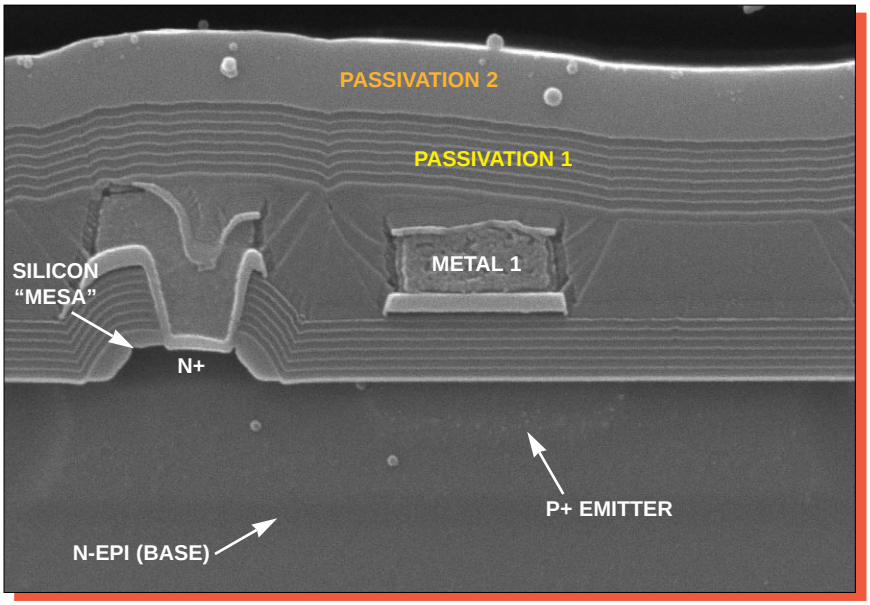


stained

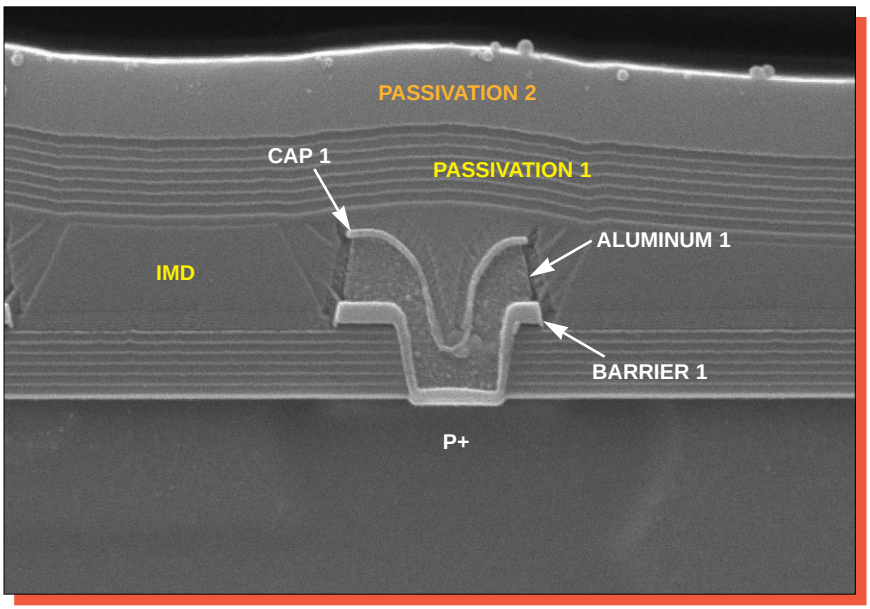
Figure 35. Optical views of PNP transistors.



Mag. 6500x



Mag. 15,000x



Mag. 16,000x

Figure 36. SEM section views of a PNP transistor.

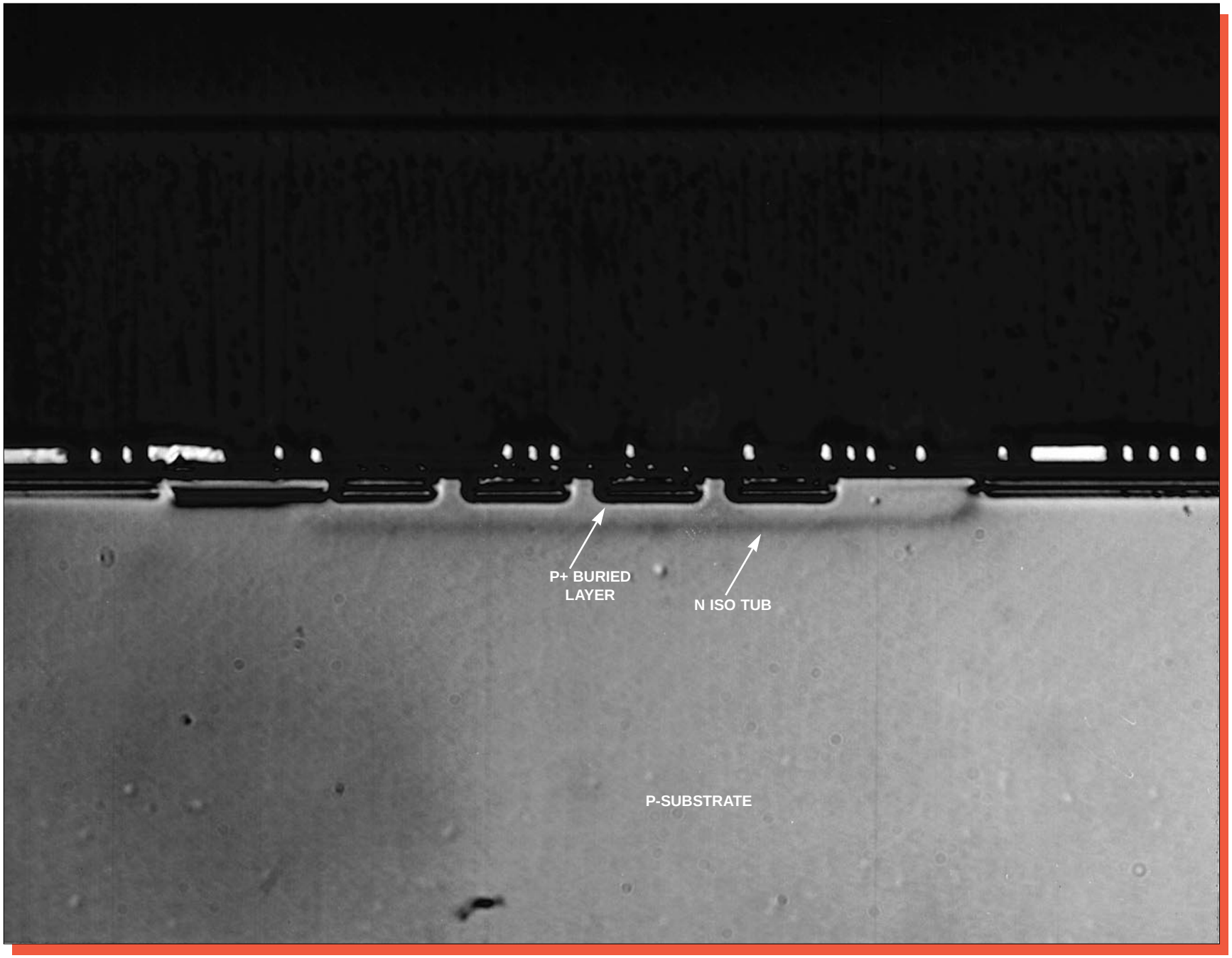
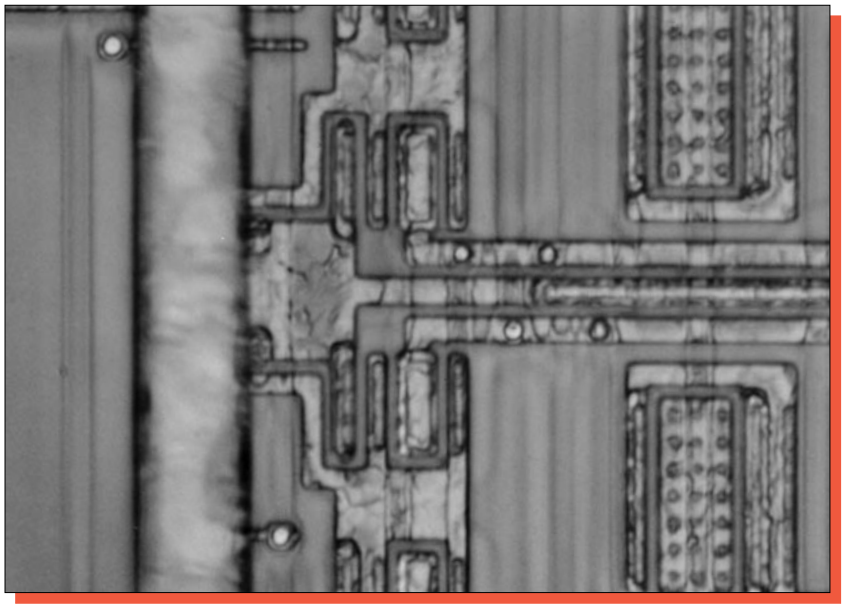
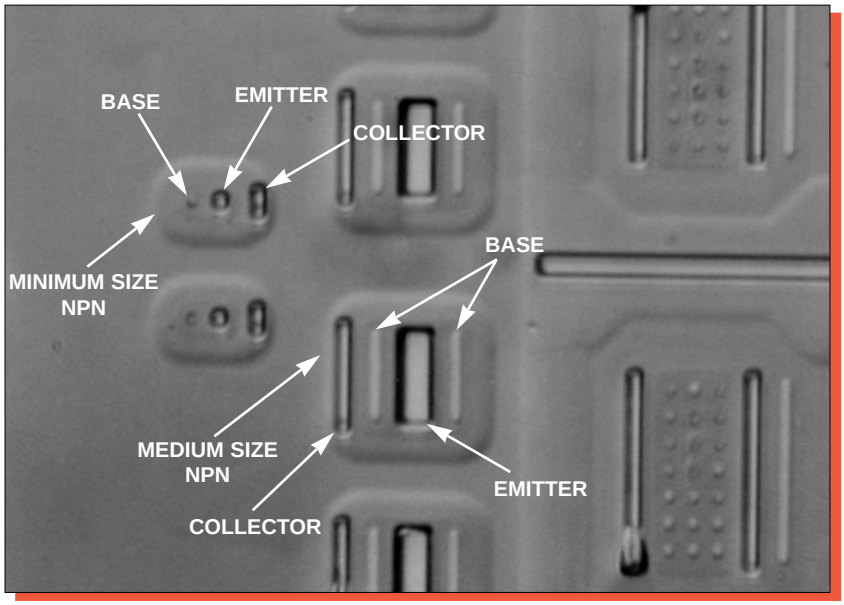


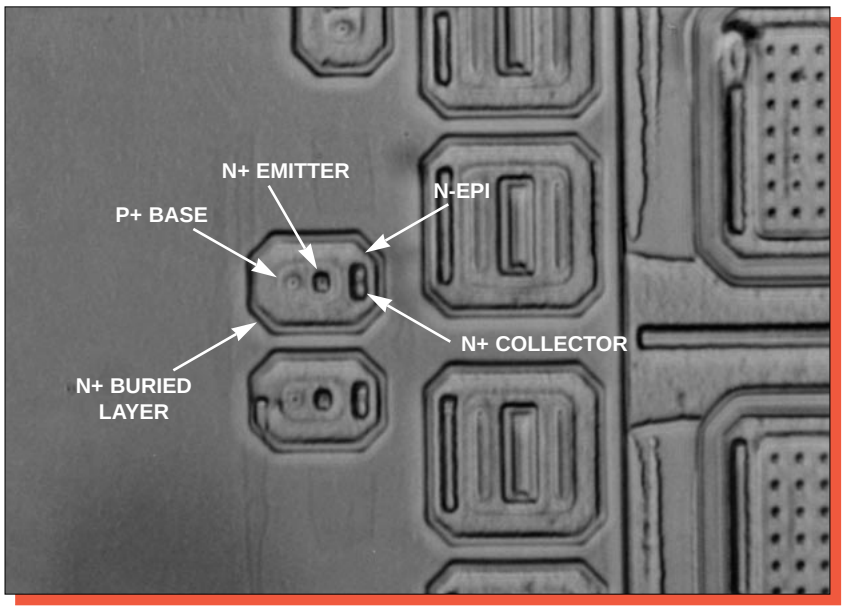
Figure 37. Optical section view illustrating the PNP transistors structure. Mag. 1600x.



metal 1

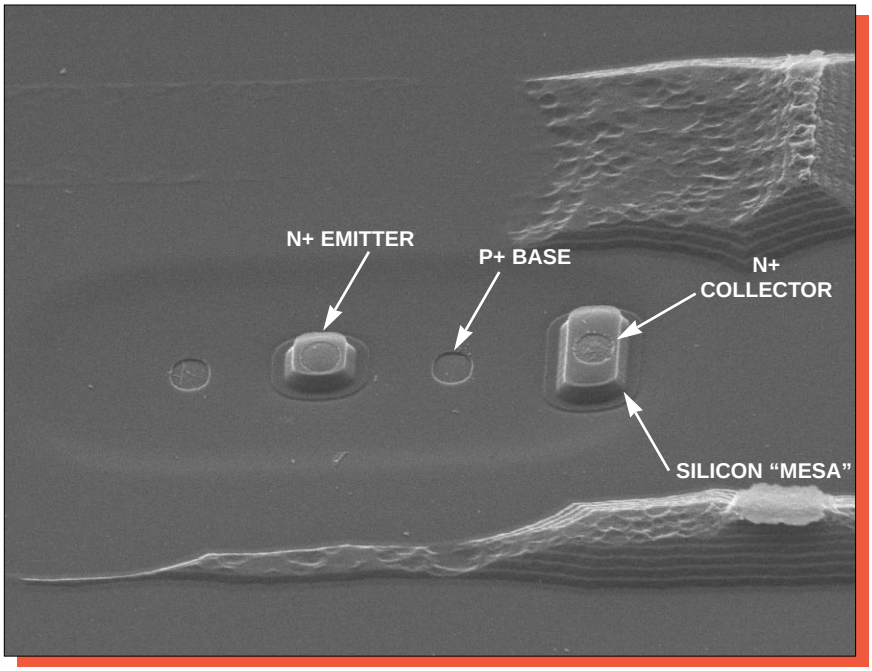


unlayered

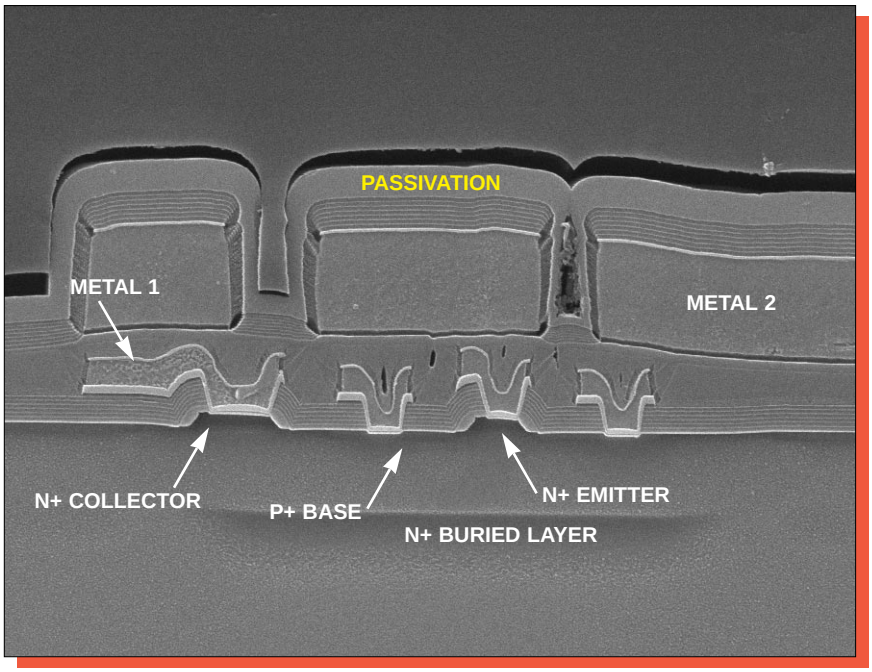


stained

Figure 38. Optical views of NPN transistors. Mag. 1600x.

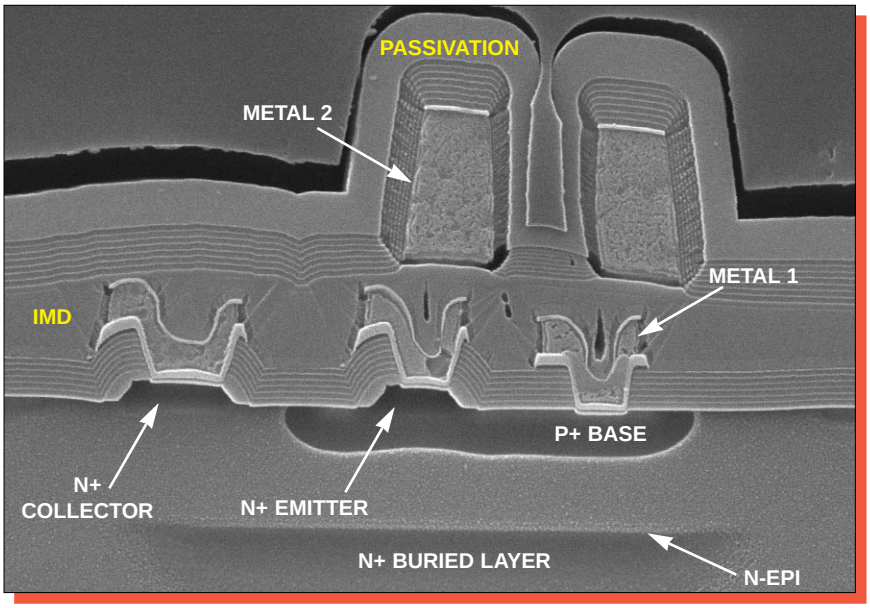


Mag. 7000x, 60°

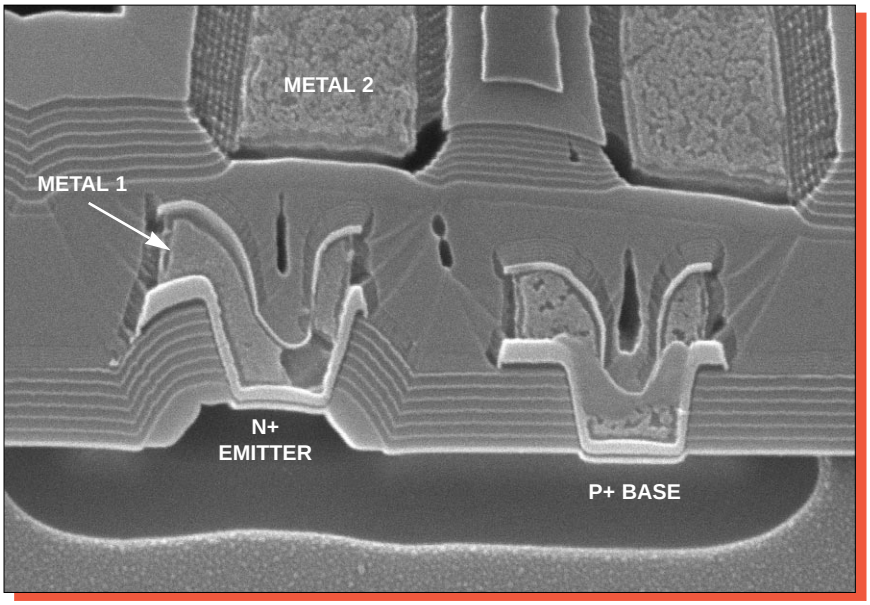


Mag. 6500x

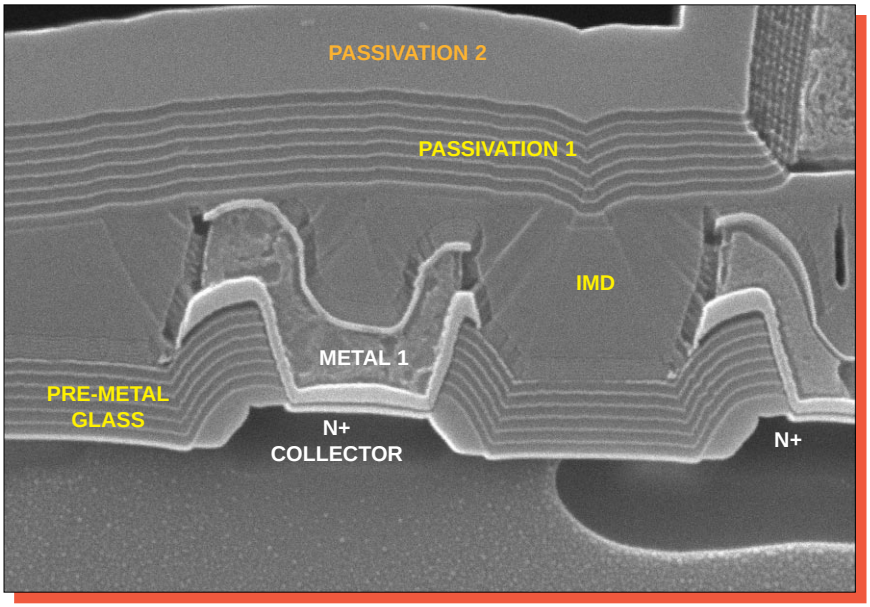
Figure 39. Perspective and SEM section views of a minimum size NPN transistor.



Mag. 10,000x



Mag. 20,000x



Mag. 20,000x

Figure 39a. SEM section views of a medium size NPN transistor.

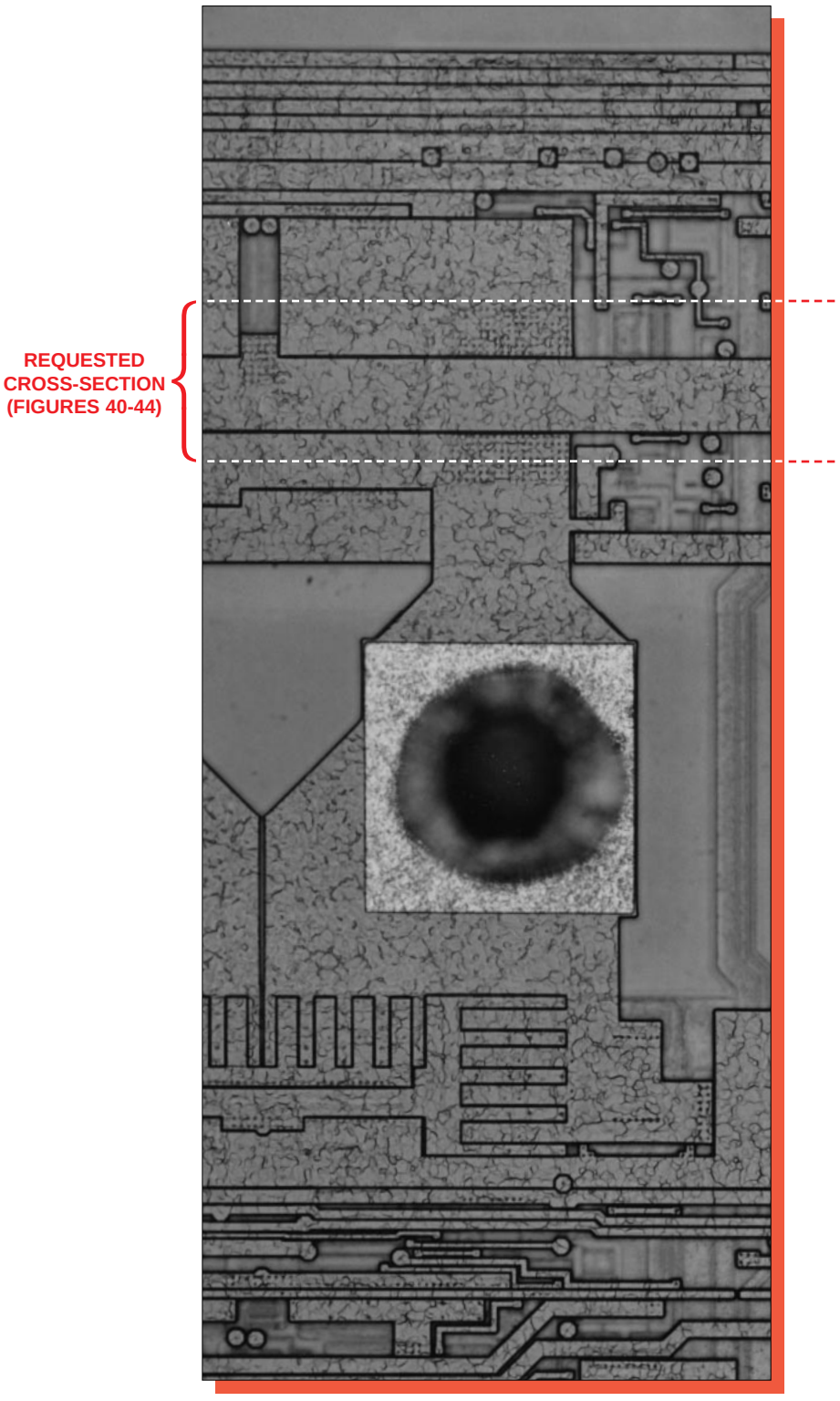
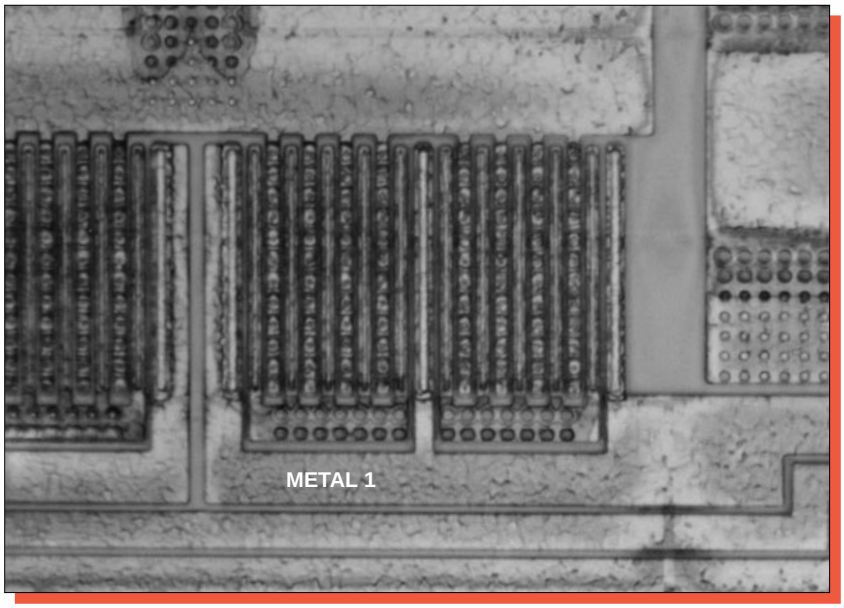
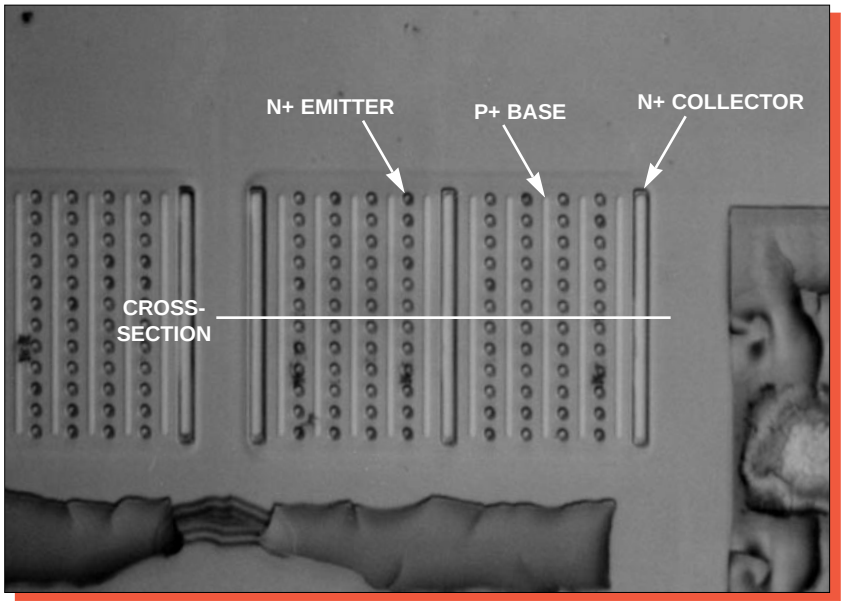


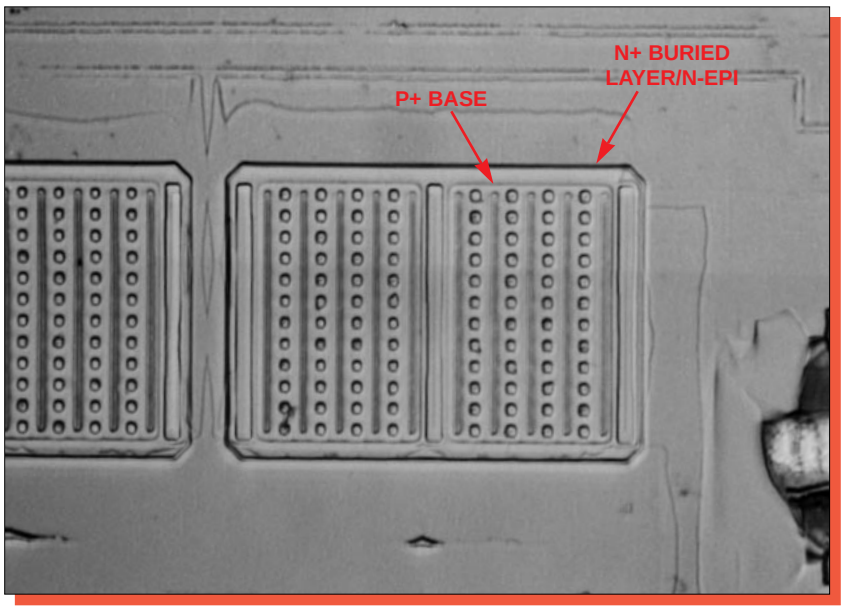
Figure 40. Optical view of a typical input structure. Mag. 400x.



metal 1



unlayered



stained

Figure 41. Optical views of a large input device (requested section). Mag. 1000x.

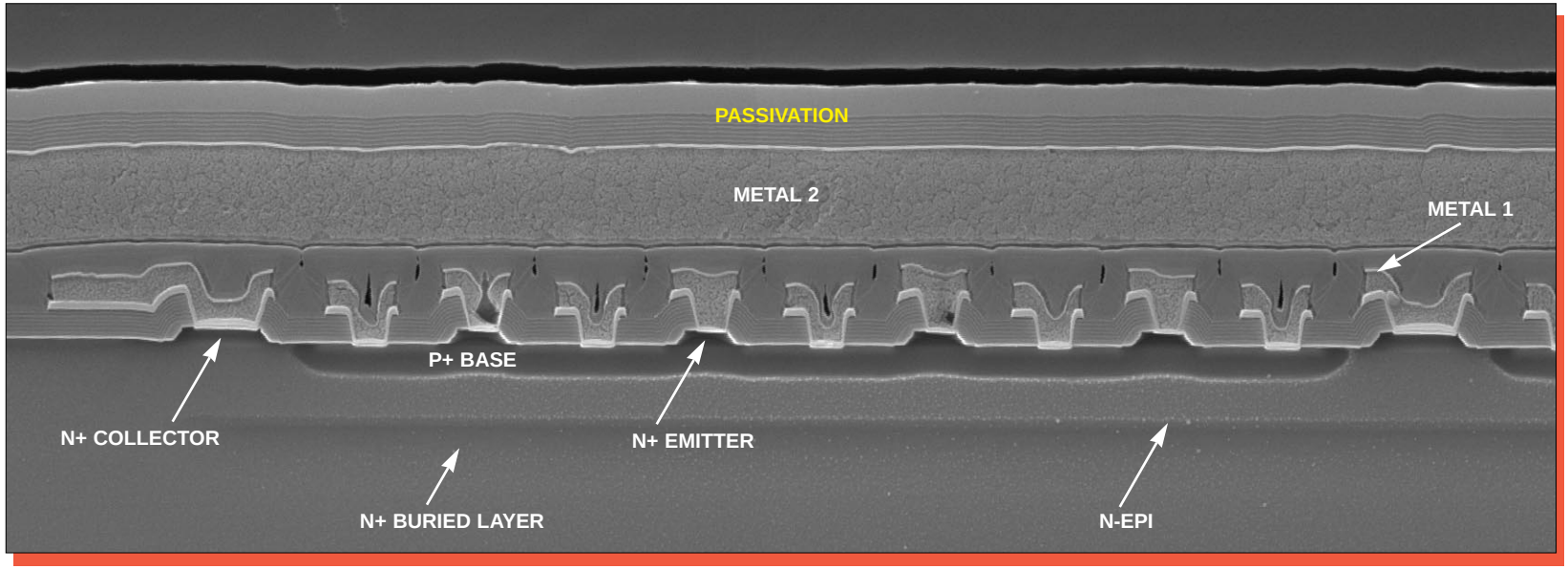
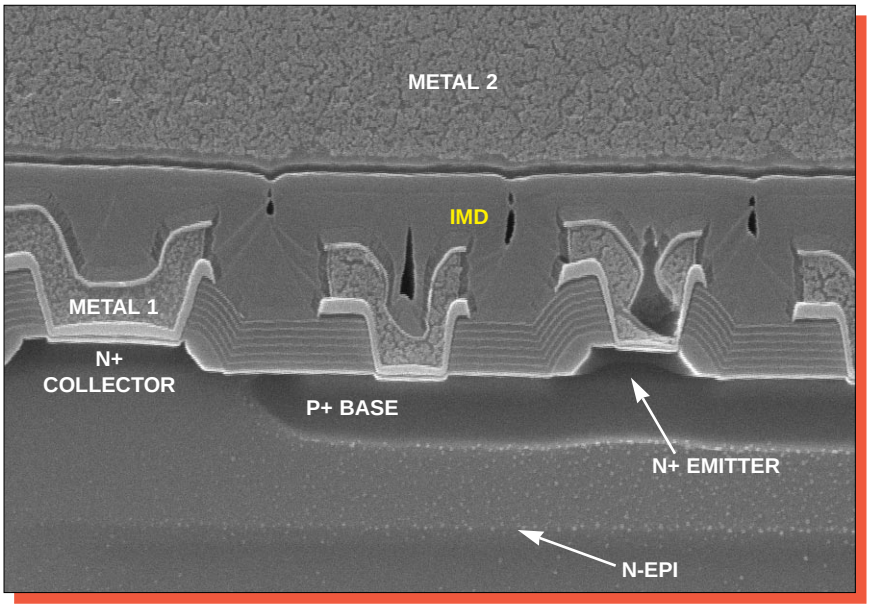
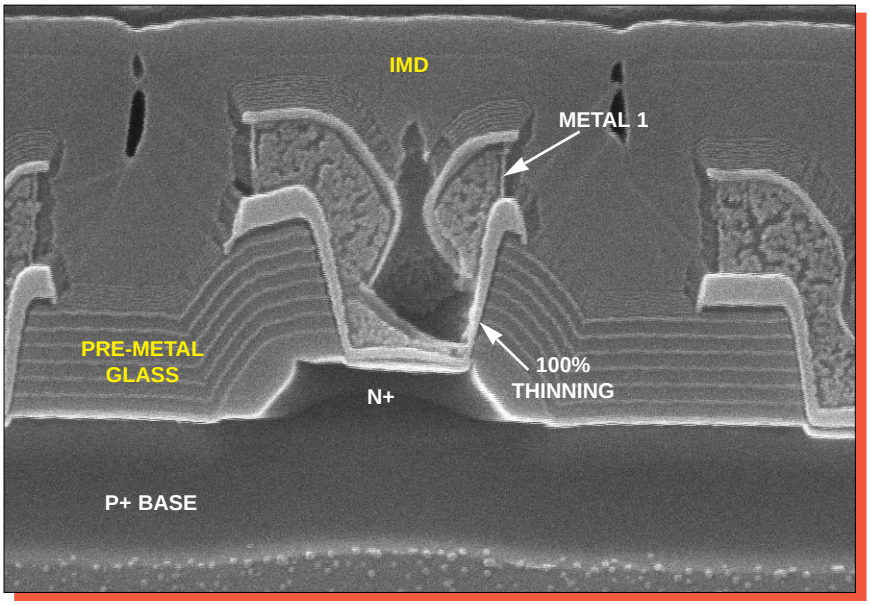


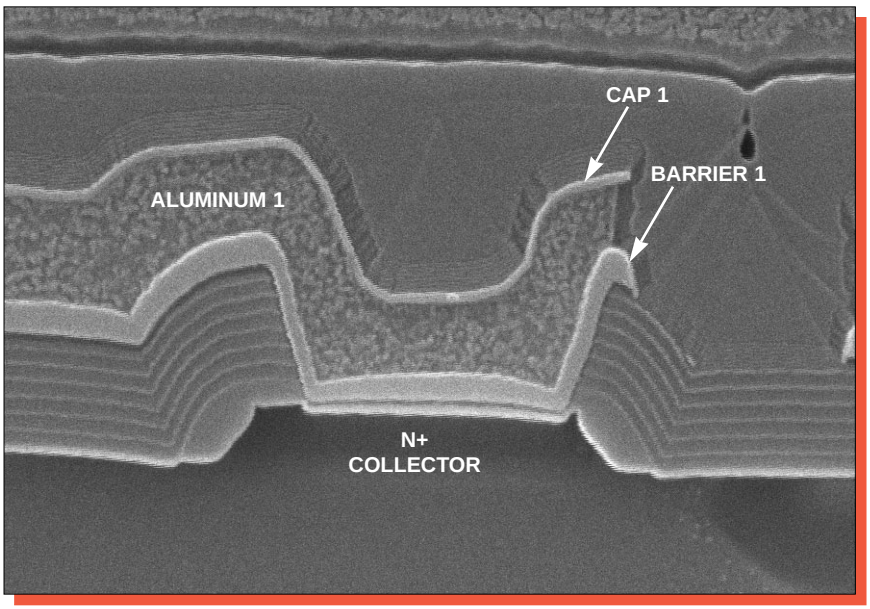
Figure 41a. SEM section view of a large input device with multiple emitter and base contacts (requested section). Mag. 6500x.



Mag. 13,000x



emitter,
Mag. 26,000x



collector,
Mag. 26,000x

Figure 42. Detailed views of the input device (requested section). Mag. 26,000x.

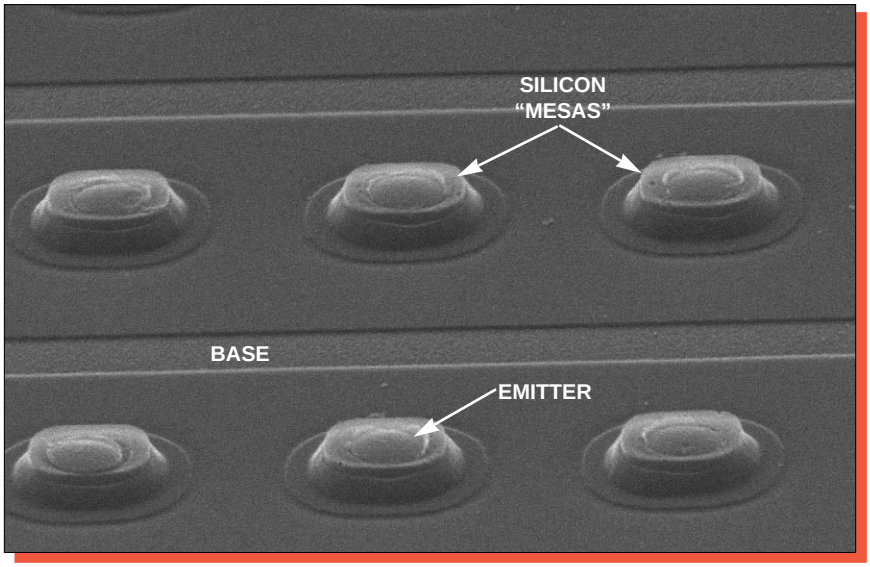


Figure 43. Perspective SEM view of the silicon "mesas". Mag. 13,500x.

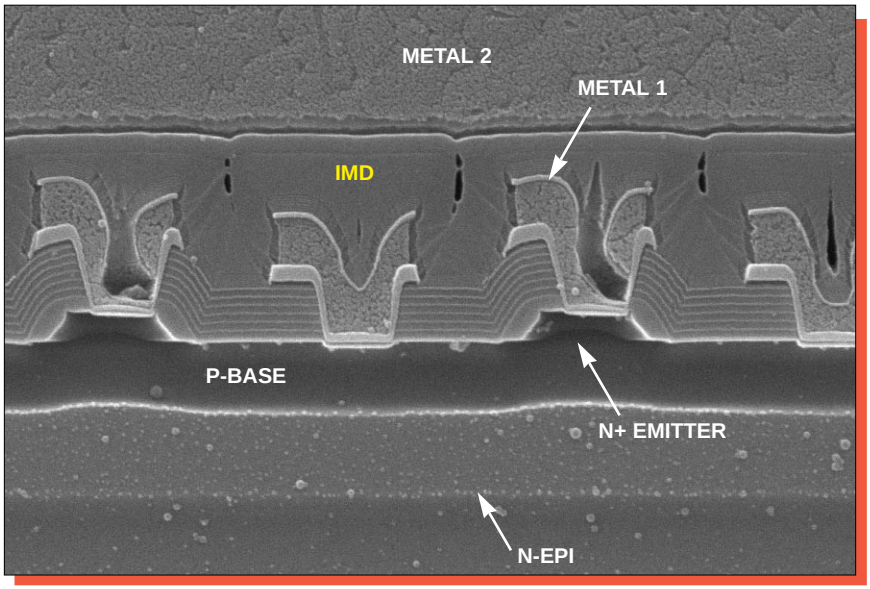
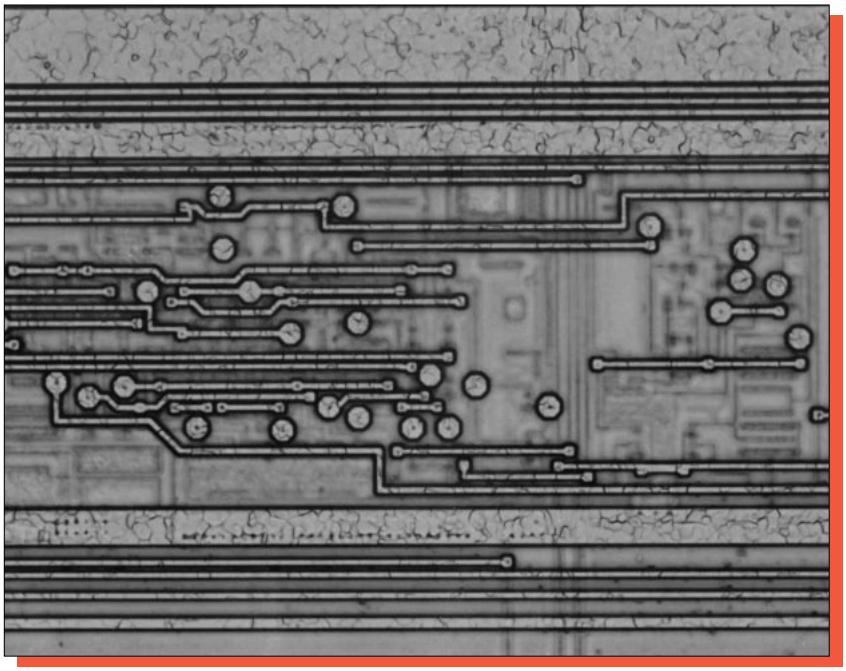
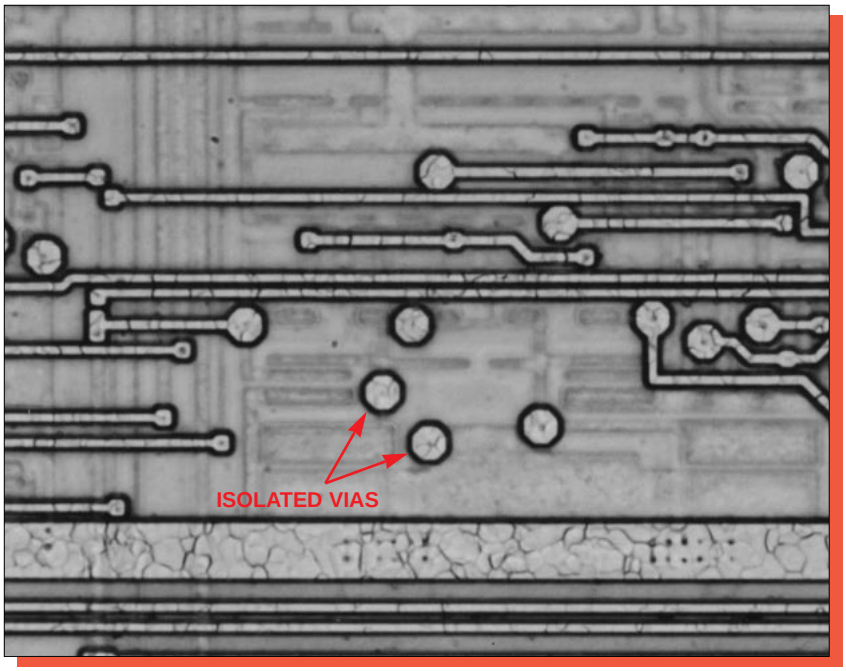


Figure 44. Additional SEM section view of the mesa emitter contacts. Mag. 13,000x.

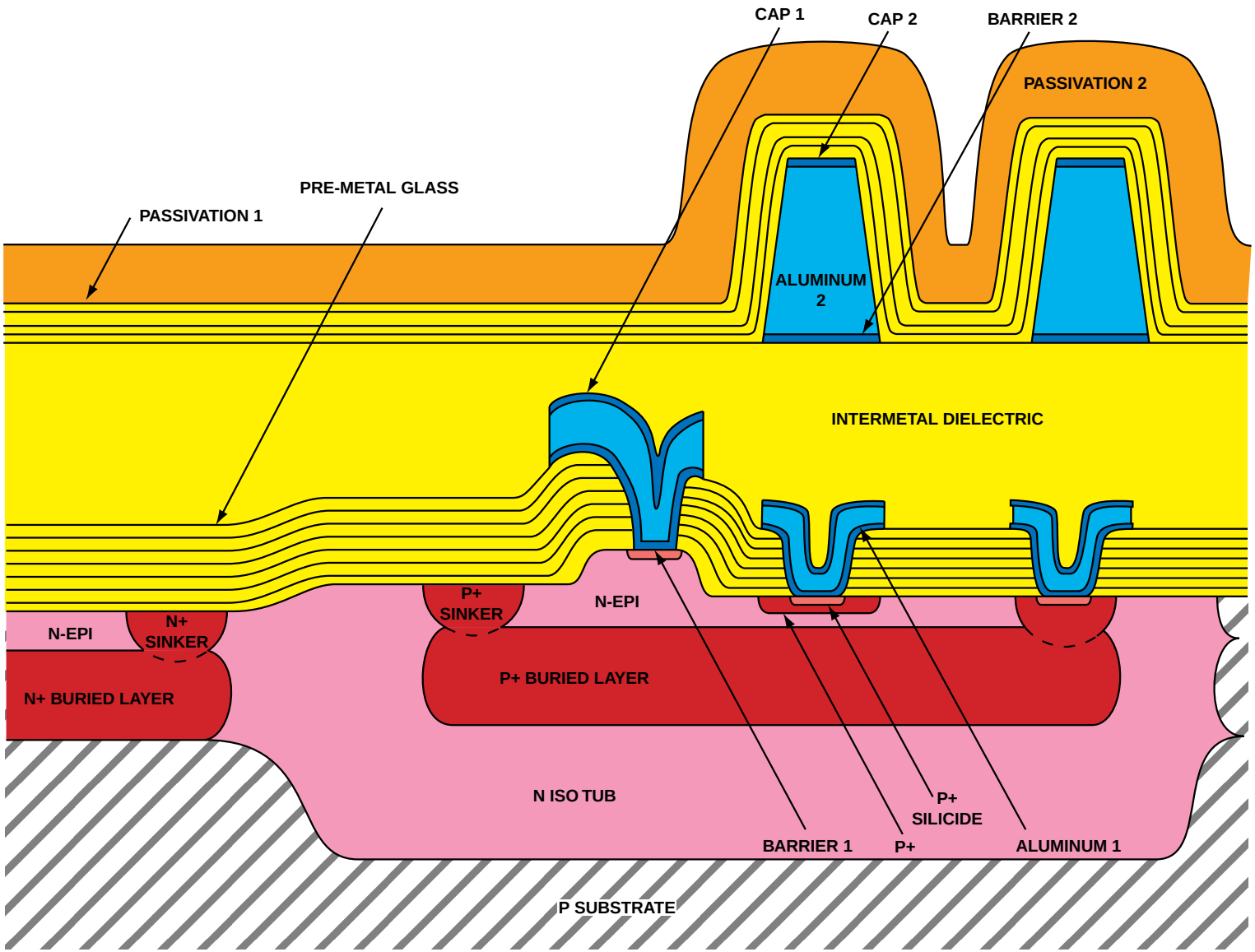


Mag. 500x



Mag. 800x

Figure 45. Optical views of general circuit layout.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 46. Color cross section drawing illustrating device structure.