# Construction Analysis

# Rockwell 11577-11
# Digital Correlator

Report Number: SCA 9707-546


INTEGRATED CIRCUIT ENGINEERING

17350 N. Hartford Drive
Scottsdale, AZ 85255
Phone: 602-515-9780
Fax: 602-515-9781
e-mail: ice@ice-corp.com
Internet: http://www.ice-corp.com

# INDEX TO TEXT

## INTRODUCTION

This report describes a competitive analysis of the Rockwell 11577-11 digital correlator. One device packaged in a 144-pin Square Quad Flat Package (SQFP) was received for the analysis. The device was taken from a GPS receiver chipset manufactured by IST. The IC was date coded 9636.

## MAJOR FINDINGS

**Questionable Items:[1]**

- Metal 2 aluminum thinned up to 100 percent[2] at some locations of some vias. Barrier metal remained intact to provide continuity.

- Metal 1 aluminum thinned up to 100 percent[2] at some locations of some contacts. Barrier metal remained intact to provide continuity.

**Special Features:**

- Titanium silicided diffusion structures.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

## TECHNOLOGY DESCRIPTION

**Assembly:**

- Device was encapsulated in a 144-pin plastic Square Quad Flat Package (SQFP).
- Copper (Cu) leadframe was internally plated with silver (Ag).
- External pins were tinned with tin-lead (SnPb) solder.
- Lead-locking provisions (holes) at all pins.
- Thermosonic ball bonding using 1.1 mil O.D. gold wire.
- Pins 139 - 143 were not connected.
- Sawn dicing (full-depth).
- Silver-filled epoxy die attach.

**Die Process:**

- Fabrication process: Selective oxidation CMOS process employing P-wells in an N-epi on a P-substrate.
- Final passivation: A layer of nitride over a layer of glass.
- Metallization: Two levels of metal defined by standard dry-etch techniques. Both consisted of aluminum with a titanium-nitride cap and barrier. Standard vias and contacts were used (no plugs).
- Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them.

**TECHNOLOGY DESCRIPTION (continued)**

- Polysilicon: A single layer of polycide (titanium silicide on poly) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Wells: P-well CMOS process in an N-epi on a P-substrate. No step was present at well boundaries.

- Memory cells: On-board MROM memory design used metal 2 “piggy-back” word lines via metal 1 links. Metal 1 was used to form the bit lines. Polycide was used to form the word lines. Programming is achieved at the field (local) oxide cut.

- Redundancy: Fuses were not used.

- Design features: Slotted and beveled Metal 2 bus lines were employed for stress relief. Both metals one and two were used in the bond pads.

## ANALYSIS RESULTS I

**Assembly:** **Figures 1 - 4**

**Questionable Items:** None.

**General items:**

- The device was encapsulated in a 144-pin plastic Square Quad Flat Package (SQFP).
- Overall package quality: Good. Internal plating of the copper leadframe was silver. The leadframe was dimpled to add structural integrity. External pins were tinned with tin-lead (SnPb). No cracks or voids present. No gaps were noted at lead exits.
- Lead-locking provisions (holes) were present at all pins.
- Wirebonding: Thermosonic ball method using 1.1 mil O.D. gold wire. No bond lifts occurred during wire pull tests and bond pull strengths were normal. No problems are foreseen.
- Pins 139 - 143 were not connected.
- Die attach: Silver-filled epoxy of good quality. No voids were noted in the die attach and no problems are foreseen.
- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

## ANALYSIS RESULTS II

**Die Process and Design:** **Figures 5 - 34**

**Questionable Items:[1]**

- Metal 2 aluminum thinned up to 100 percent[2] at some via locations. Barrier metal remained intact to provide continuity.

- Metal 1 aluminum thinned up to 100 percent[2] at some contact locations. Barrier metal remained intact to provide continuity.

**Special Features:**

- Titanium silicided diffusion structures.

**General items:**

- Fabrication process: Devices were fabricated using selective oxidation CMOS process employing P-wells in an N-epi on a P-substrate.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.

- Die coat: No die coat was present.

- Final passivation: A layer of nitride over a layer of glass. Overlay integrity test indicated defect-free passivation. Edge seal was good as the passivation extended

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

**ANALYSIS RESULTS II (continued)**

the metal at the edge of the die. The voids above metal 2 vias are not considered areas of concern.

- Metallization: Two levels of metal were used. Both consisted of aluminum with titanium-nitride caps and barriers. Standard vias and contacts were used (no plugs).

- Metal patterning: Both metal levels were patterned by a dry etch of normal quality.

- Metal defects: No voiding, notching, or neckdown was noted in either of the metal layers. No silicon nodules were noted following removal of either metal.

- Metal step coverage: Metal 2 aluminum thinned up to 100 percent at several via locations. Barrier metal maintained continuity. Metal 1 aluminum also thinned up to 100 percent at some contact locations. Typical metal 1 thinning was 90 percent.

- Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them. The SOG had been etched back.

- Pre-metal glass: A layer of reflow glass (BPSG) over densified oxide was used under metal 1. Reflow was performed prior to contact cuts only.

- Contact defects: Contact and via cuts were defined by a two-step process. No over-etching of the contacts or vias was noted. No problems were found, except for one instance found and shown in Figure 13.

- Polysilicon: A single layer of polycide (titanium silicide on poly) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry-etch of normal quality.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. Diffusions were silicided (salicide process) with titanium.

**ANALYSIS RESULTS II (continued)**

An LDD process was used with oxide sidewall spacers left in place. No problems were found.

- Isolation: LOCOS (local oxide isolation). No step was present at the well boundaries.

- Memory cells: An MROM was present on the die. Metal 2 provided "piggy-back" word lines via metal 1 links. Metal 1 was used to form the bit lines. Polycide formed the word lines and gates. Programming was achieved through field (local) oxide masking.

- Redundancy: Fuses were not present on the die.

## PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

| | |
|---|---|
| Package integrity | G |
| Package markings | N |
| Die placement | N |
| Die attach quality | G |
| Wire spacing | G |
| Wirebond placement | G |
| Wirebond quality | G |
| Dicing quality | G |
| Wirebond method | Thermosonic ball bond method using 1.1 mil O.D. gold wire. |
| Die attach method | Silver-epoxy |
| Dicing method | Sawn (full depth) |
| | |
| Die surface integrity: | |
| Tool marks (absence) | G |
| Particles (absence) | G |
| Contamination (absence) | G |
| Process defects | G |
| General workmanship | N |
| Passivation integrity | G |
| Metal definition | N |
| Metal integrity | N |
| Metal registration | N |
| Contact coverage | N |
| Contact registration | N |

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

## PACKAGE MARKINGS

### TOP

11577-11
HONG KONG
9636
B24725.2 (LOGO)

## WIREBOND STRENGTH

| | |
|---|---|
| Wire material: | 1.1 mil O.D. gold |
| Die pad material: | aluminum |
| Material at package lands: | silver |

| **Sample #** | **1** |
|---|---|
| # of wires tested: | 20 |
| Bond lifts: | 0 |
| Force to break - high: | 13.0g |
| - low: | 6.0g |
| - avg.: | 8.1g |
| - std. dev.: | 1.7 |

## DIE MATERIAL ANALYSIS

| | |
|---|---|
| Overlay passivation: | A layer of silicon-nitride over a layer of glass. |
| Metallization 2: | Aluminum (Al) with a titanium-nitride (TiN) cap and barrier. |
| Metallization 1: | Aluminum (Al) with a titanium-nitride (TiN) cap and barrier. |
| Polycide: | Titanium (Ti) silicide on poly. |
| Diffusions: | Titanium (Ti) salicide. |

## HORIZONTAL DIMENSIONS

| | |
|---|---|
| Die size: | 8.5 x 8.45 mm (338 x 333 mils) |
| Die area: | 72.6 $mm^2$ (112,554 $mils^2$) |
| Min pad size: | 0.13 x 0.13 mm (5 x 5 mils) |
| Min pad window: | 0.11 x 0.11 mm (4.5 x 4.5 mils) |
| Min pad space: | 0.03 mm (1.1 mils) |
| Min metal 2 width: | 1.2 micron |
| Min metal 2 space: | 1.4 micron |
| Min metal 2 pitch: | 2.6 microns |
| Min metal 1 width: | 1 micron |
| Min metal 1 space: | 0.7 micron |
| Min metal 1 pitch: | 1.7 micron |
| Min via (M2-to-M1): | 0.9 micron (round) |
| Min contact: | 1 micron (round) |
| Min polycide width: | 0.6 micron |
| Min polycide space: | 0.4 micron |
| Min gate length* - (N-channel): | 0.7 micron |
| - (P-channel): | 0.6 micron |

**Physical gate length.*

## VERTICAL DIMENSIONS

| | |
|---|---|
| Die thickness: | 0.4 mm (15 mils) |

**Layers**

| | |
|---|---|
| Passivation 2: | 0.5 micron |
| Passivation 1: | 0.25 micron |
| Metal 2 - cap: | 0.06 micron (approx.) |
| - aluminum: | 0.7 micron |
| - barrier: | 0.1 micron |
| Intermetal dielectric - glass 2: | 0.35 micron (average) |
| - SOG: | 0 - 1.1 micron |
| - glass 1: | 0.3 micron (average) |
| Metal 1 - cap: | 0.06 micron (approx.) |
| - aluminum: | 0.5 micron |
| - barrier: | 0.1 micron |
| Pre-metal glass: | 0.55 micron (average) |
| Polycide - silicide: | 0.05 micron (approx.) |
| - poly: | 0.2 micron |
| Local oxide: | 0.4 micron |
| N+ S/D diffusion: | 0.3 micron (approx.) |
| P+ S/D diffusion: | 0.25 micron |
| P-well: | 4.5 micron (approx.) |
| N-epi: | 14 microns |

# INDEX TO FIGURES

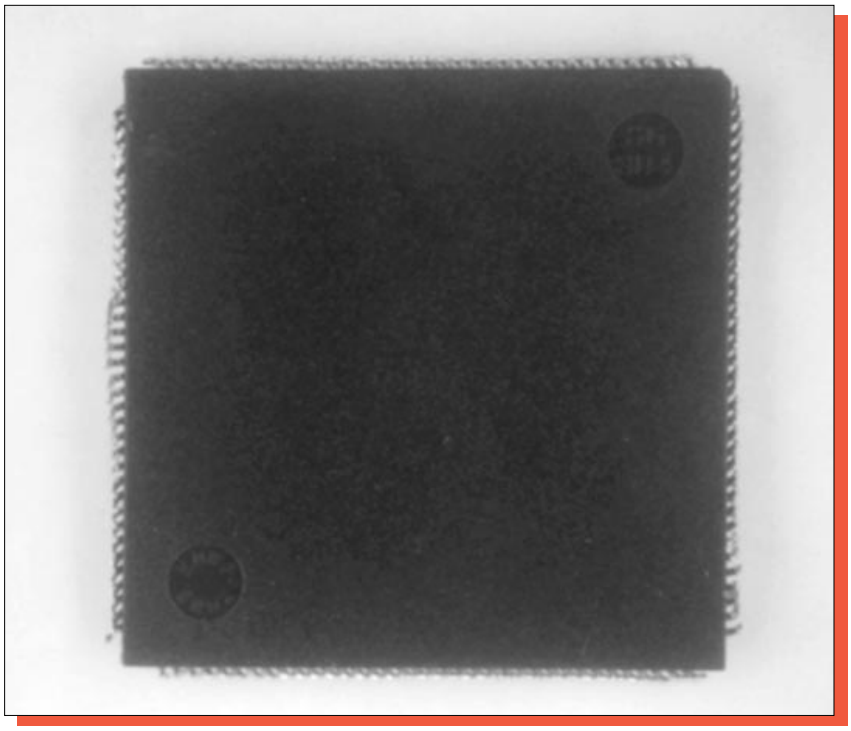



Figure 1. Package photographs of the Rockwell 11577-11. Mag. 4x.

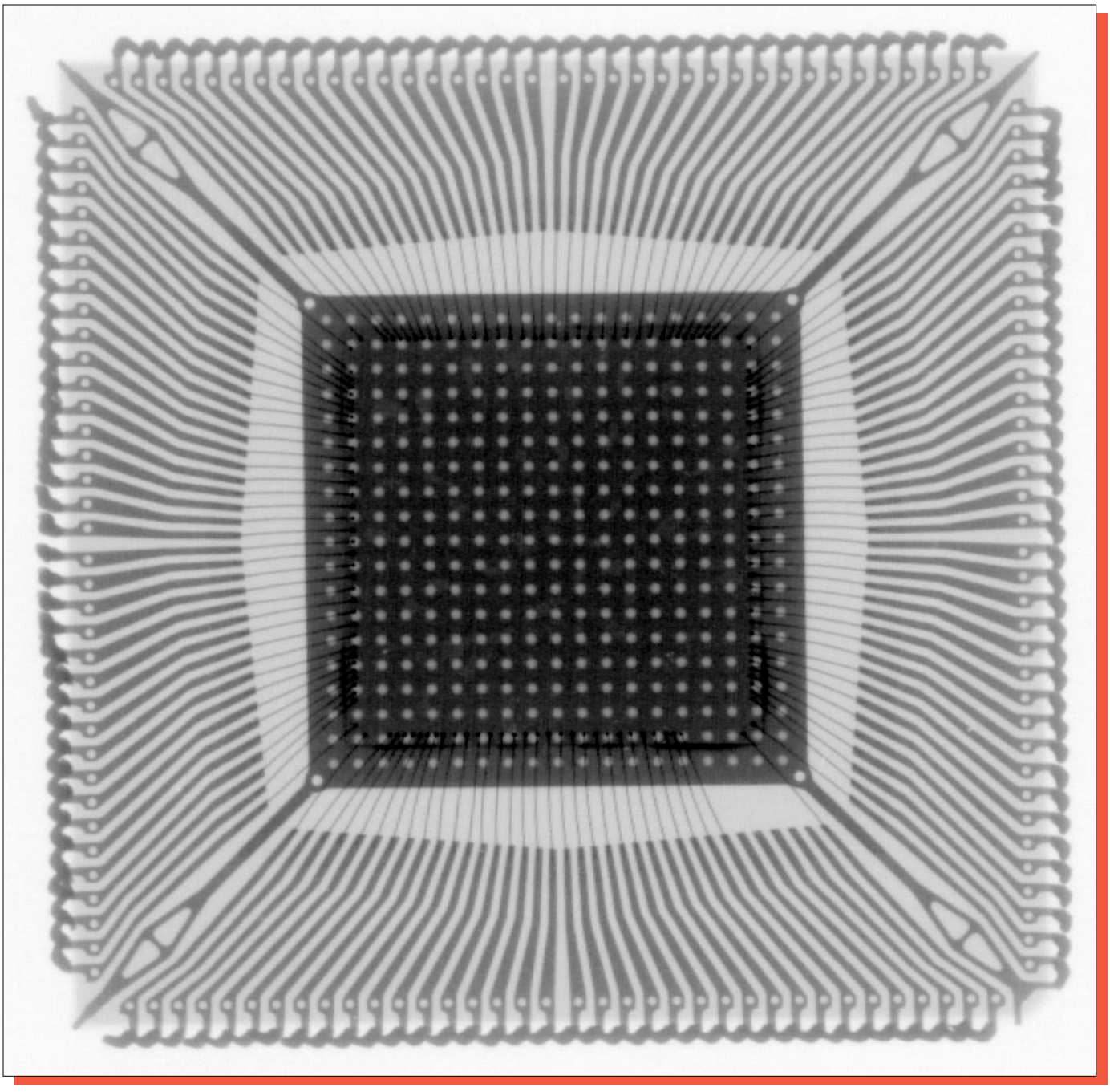
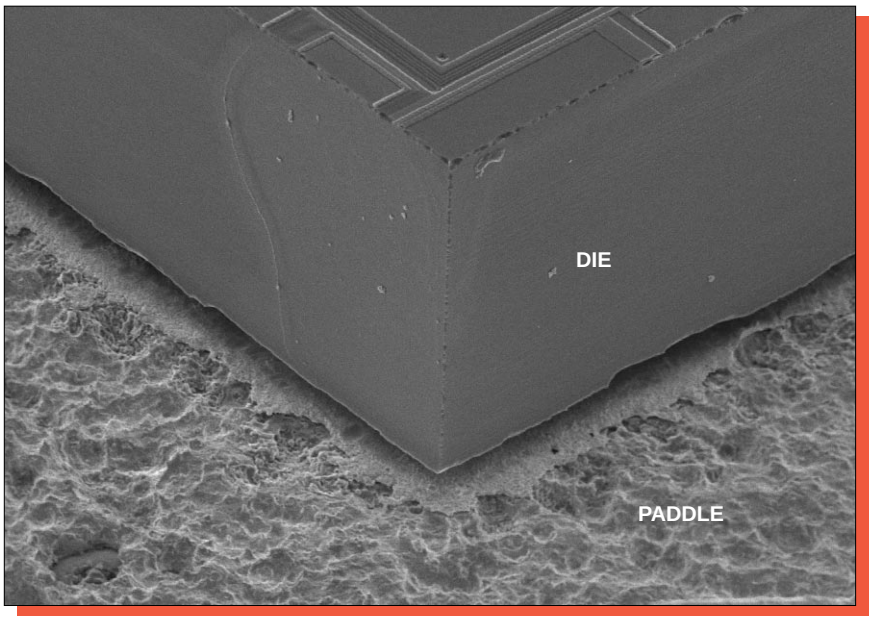
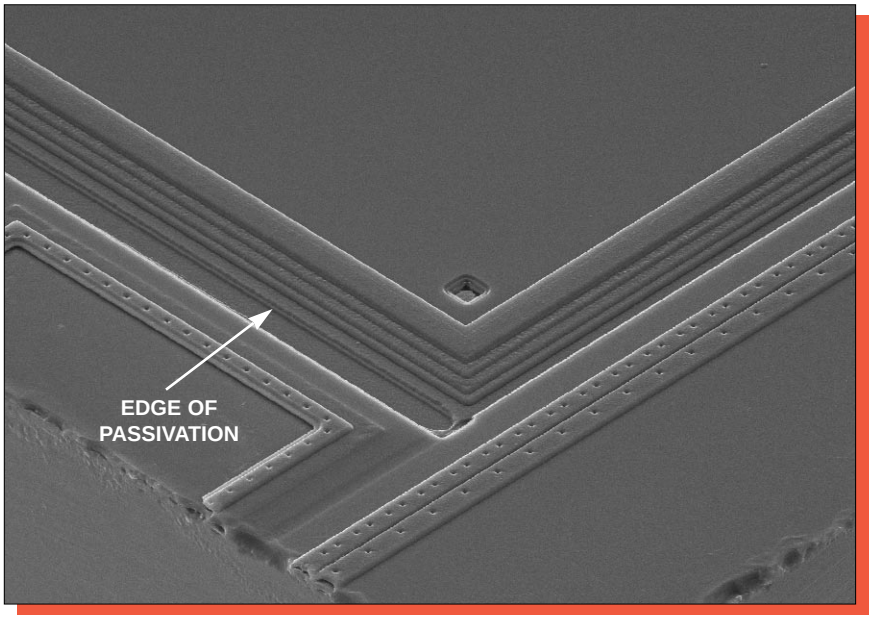


Figure 2. X-ray of the Rockwell 11577-11. Mag. 8x.

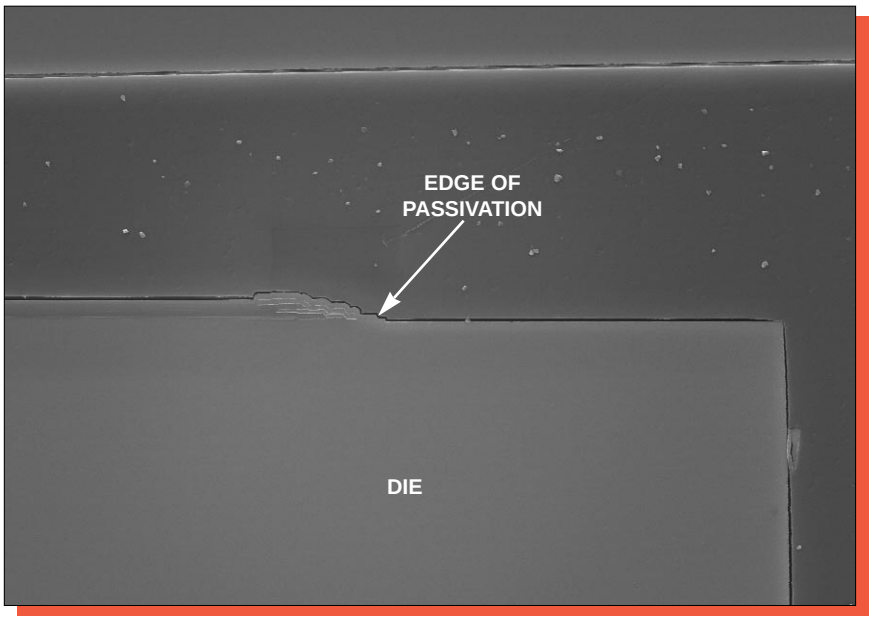



Mag. 160x

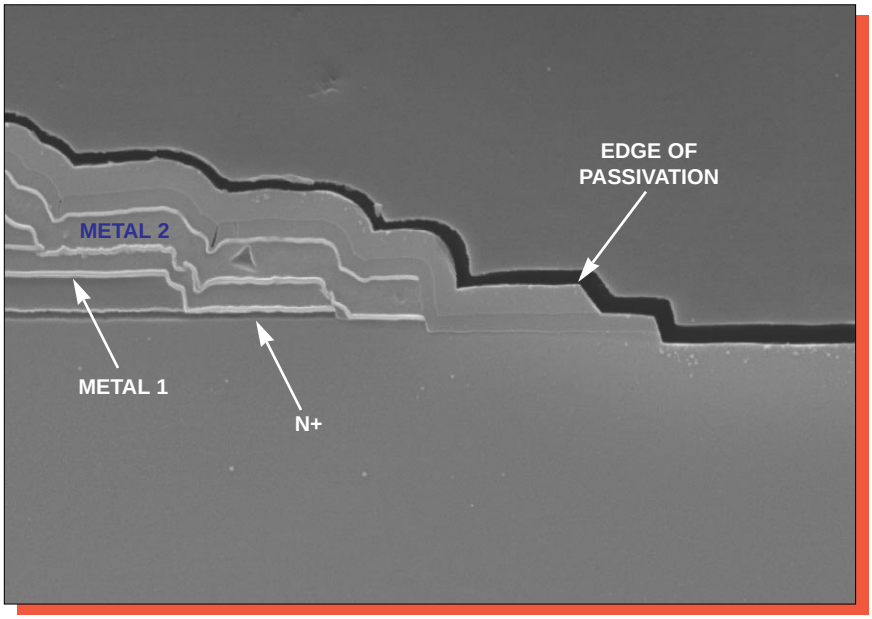



Mag. 650x

Figure 3. SEM views of dicing and edge seal. 60°.




Mag. 800x




Mag. 6500x

Figure 4. SEM section views of the edge seal.

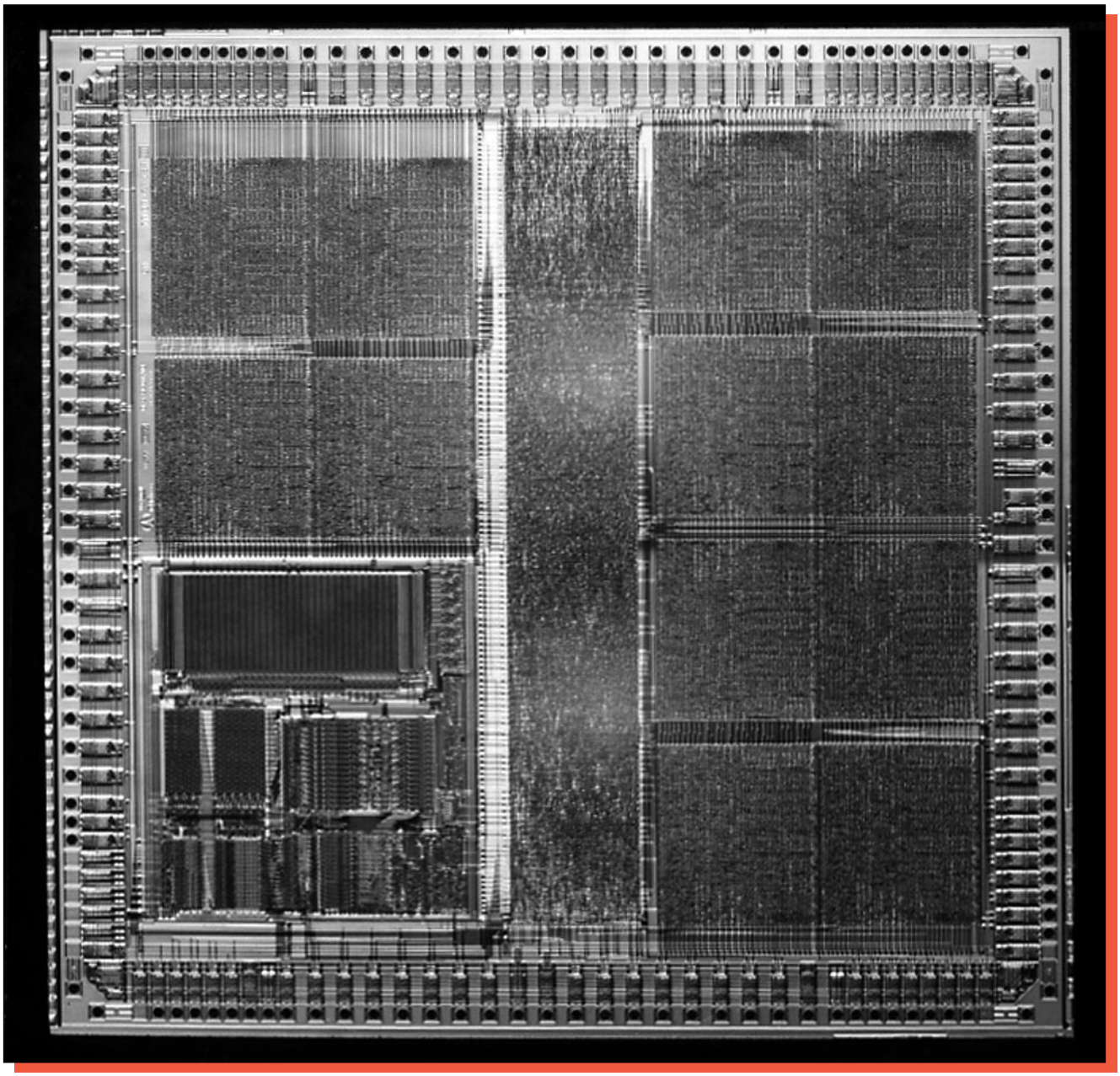


Figure 5. Whole die photograph of the Rockwell 11577-11. Mag. 20x.



Figure 6. Optical views of die markings. Mag. 155x.

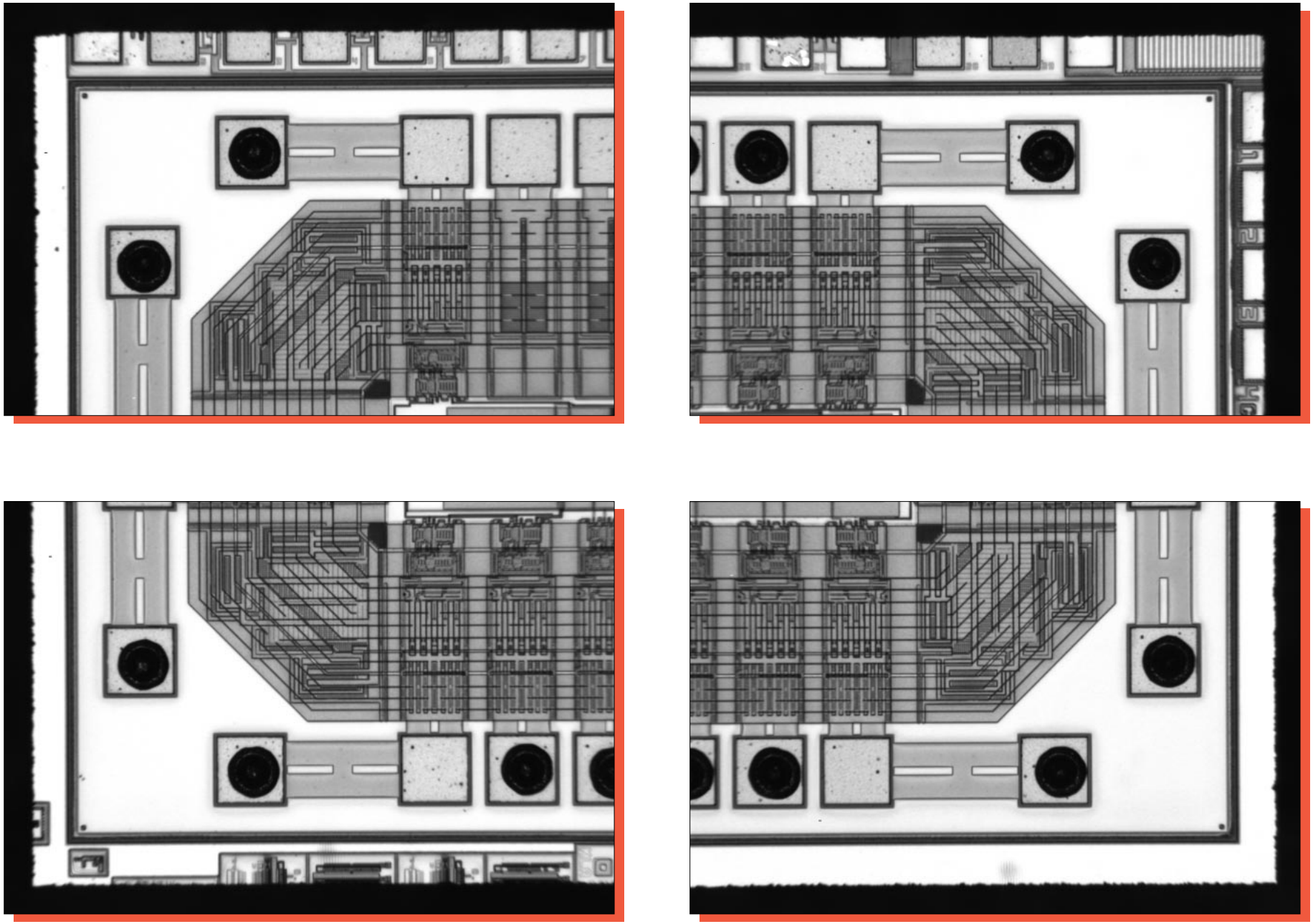
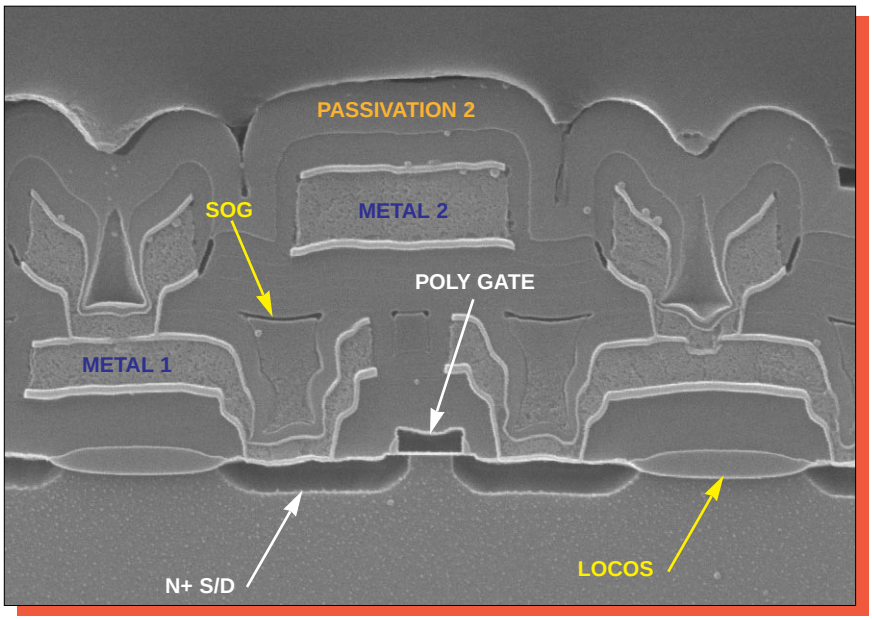
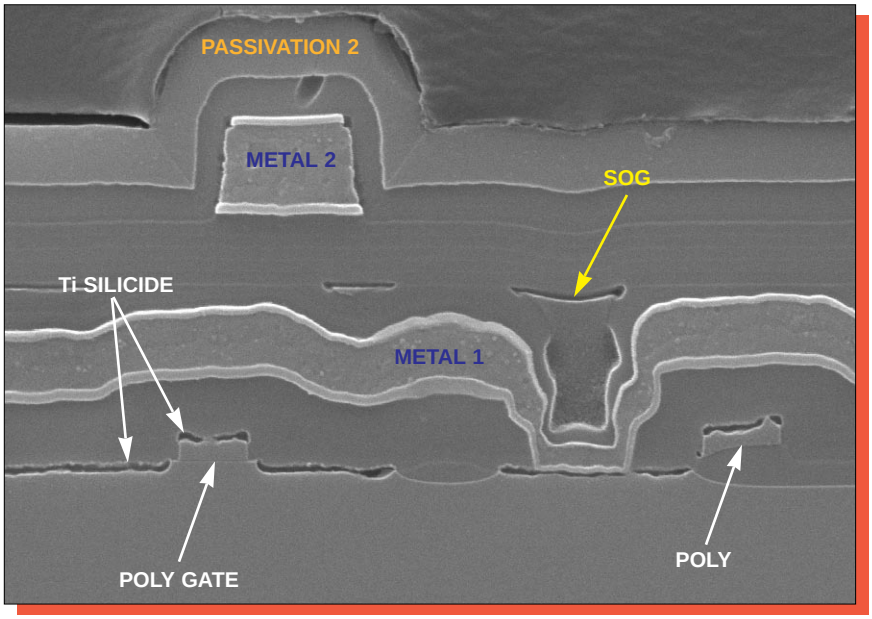


Figure 7. Optical views of die corners. Mag. 100x.




Mag. 12,000x




glass etch, Mag. 14,000x

Figure 8. SEM section views illustrating general structure.

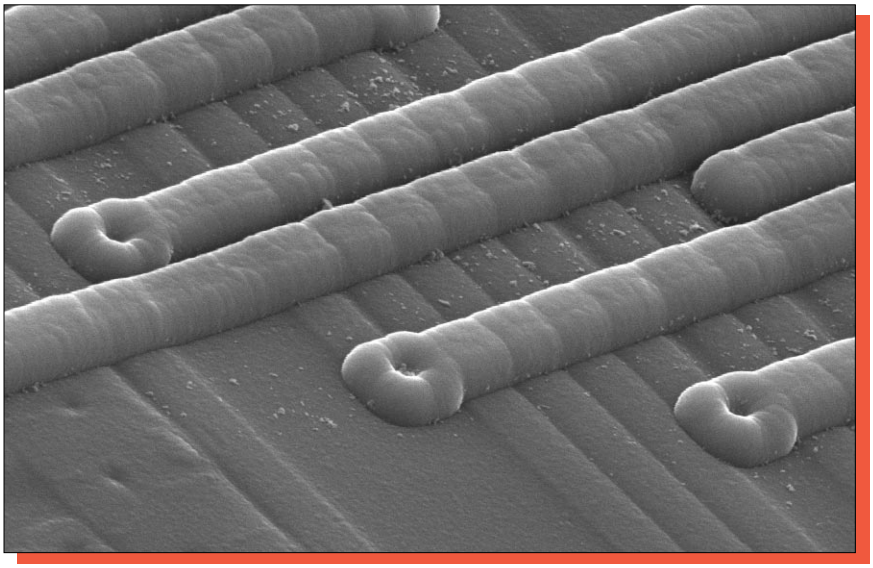
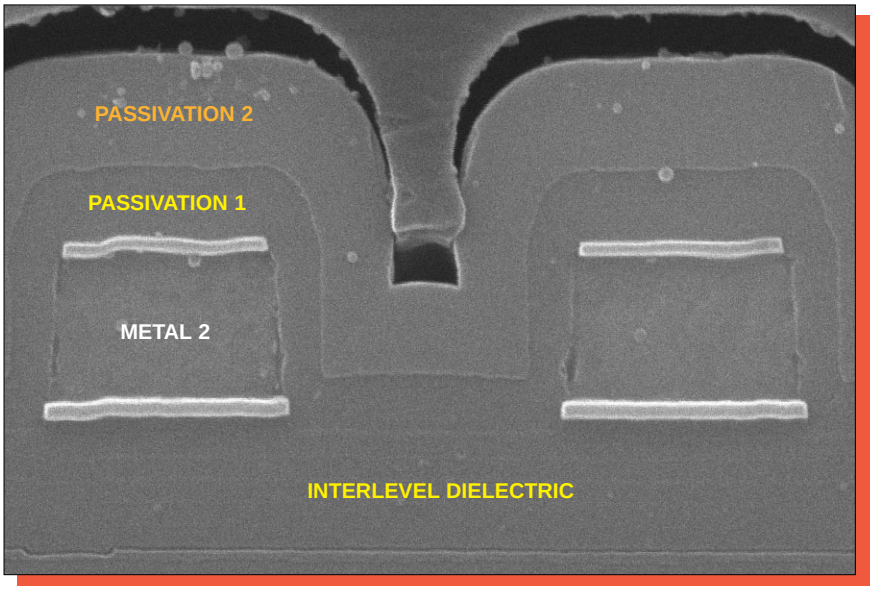
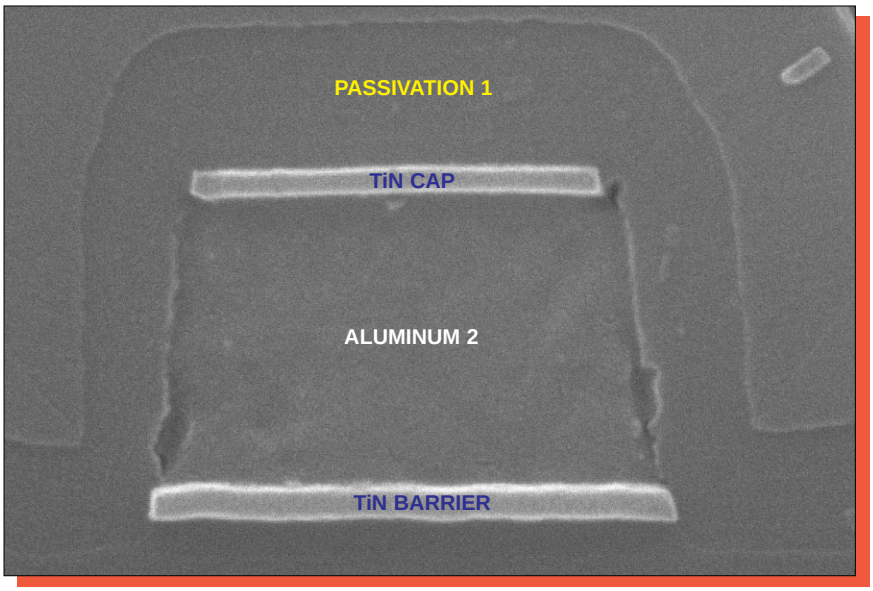


Figure 9. SEM view illustrating final passivation. Mag. 4800x, 60°.

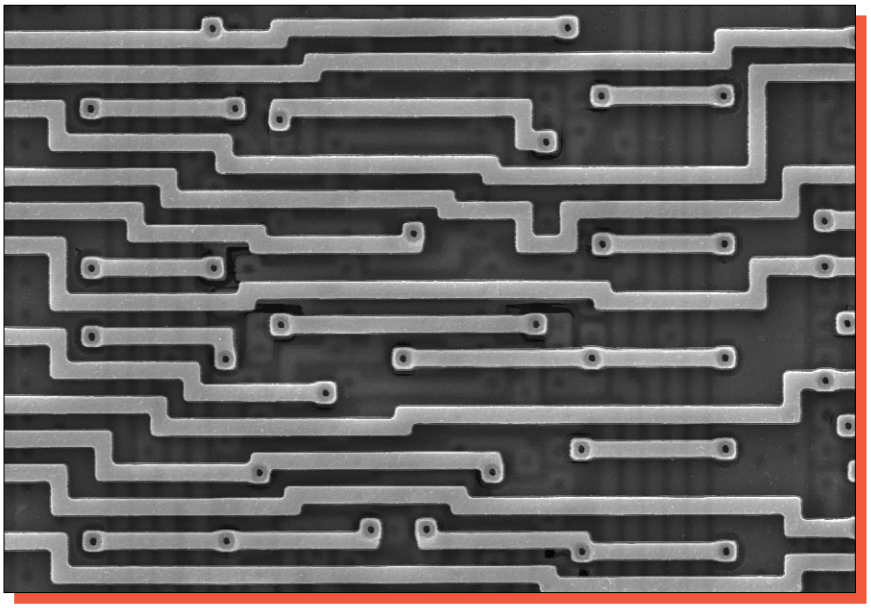



Mag. 26,000x

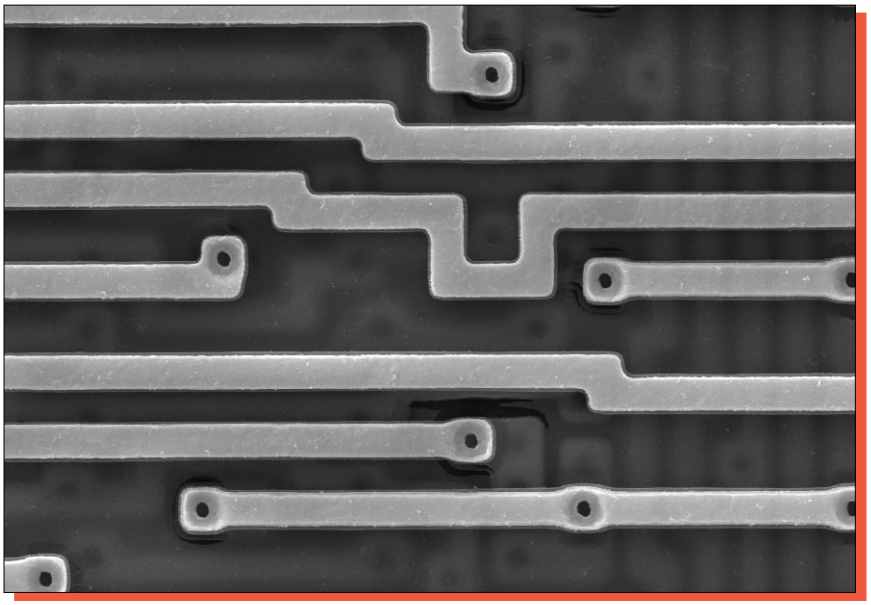



Mag. 52,000x

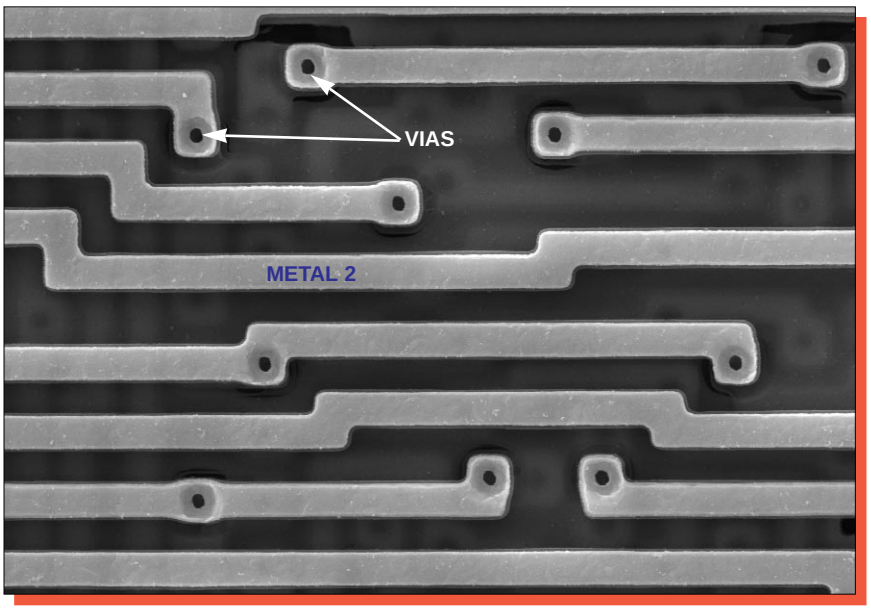
Figure 10. SEM section views of metal 2 line profiles.



Mag. 1600x

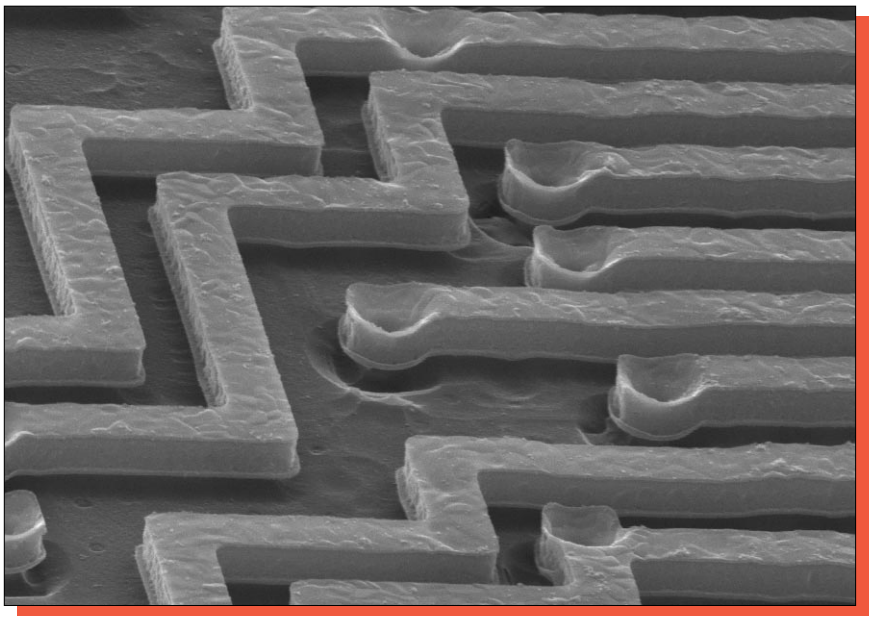


Mag. 3200x

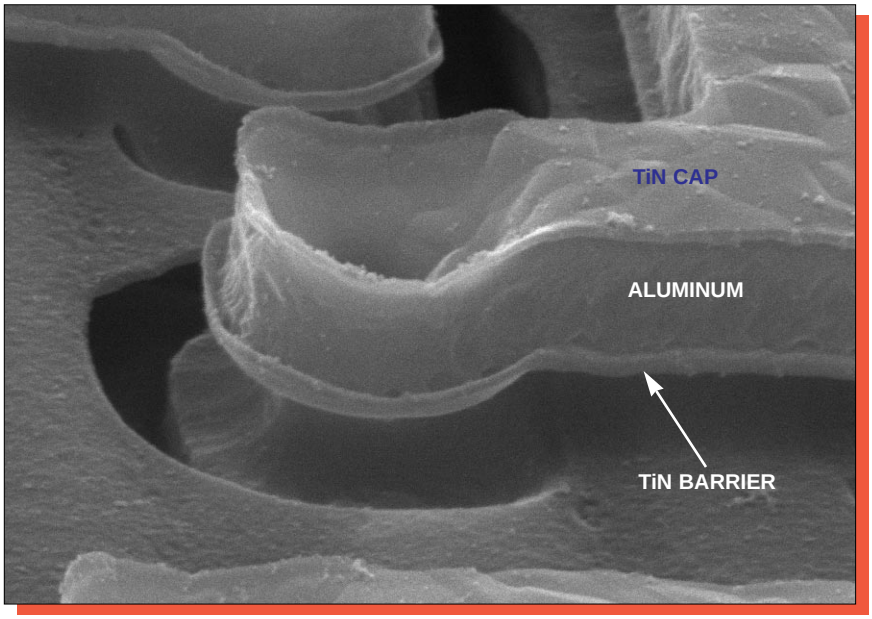



Mag. 3200x

Figure 11. Topological SEM views of metal 2 patterning. 0°.

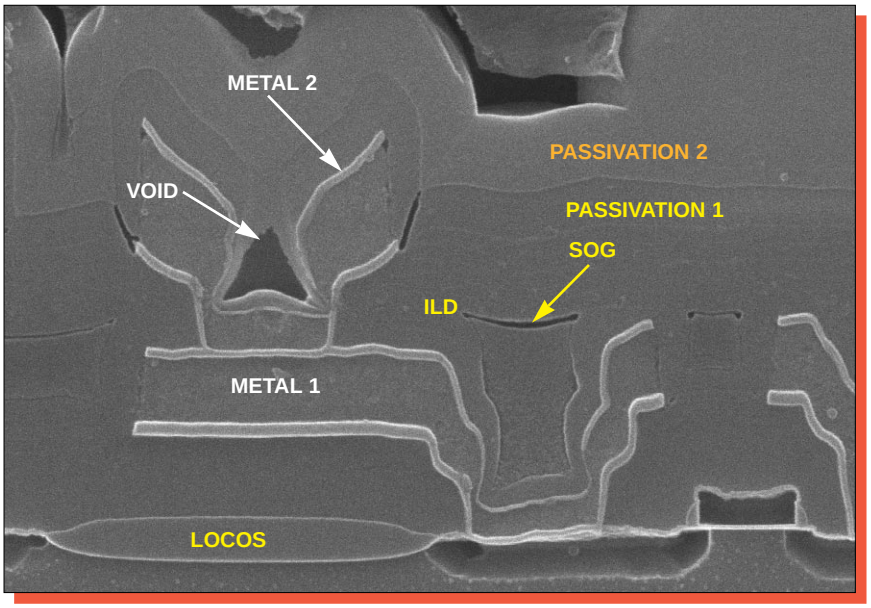


Mag. 6500x

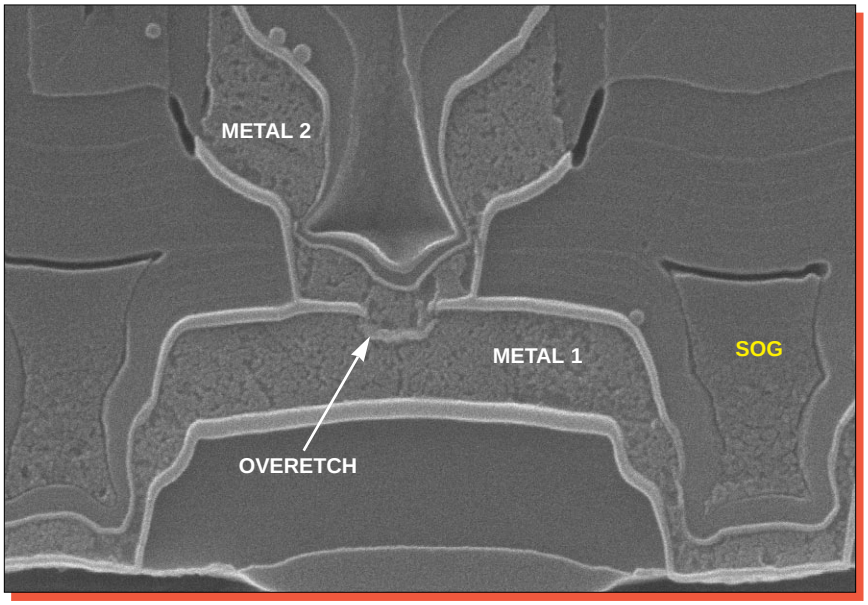



Mag. 23,000x

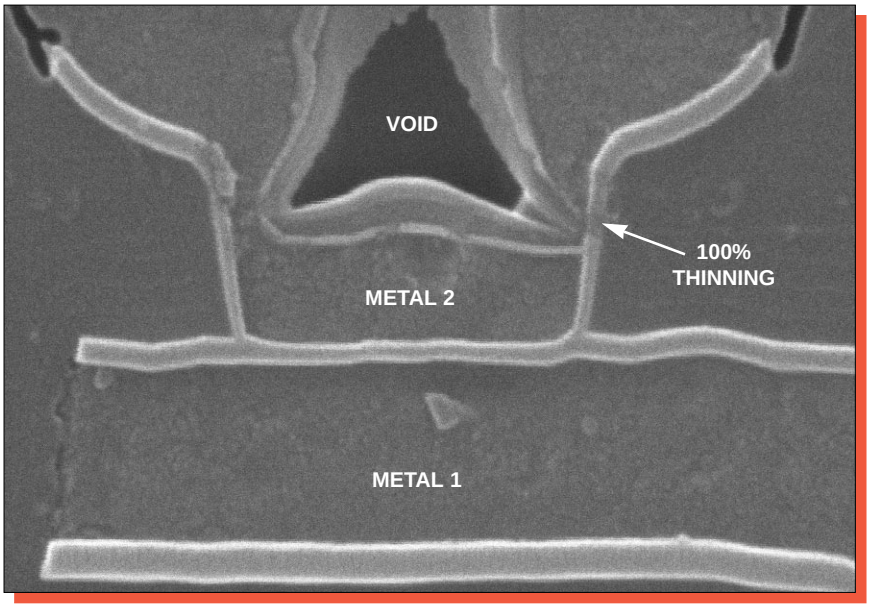
Figure 12. Perspective SEM views of metal 2 step coverage. 60°.




Mag. 19,000x

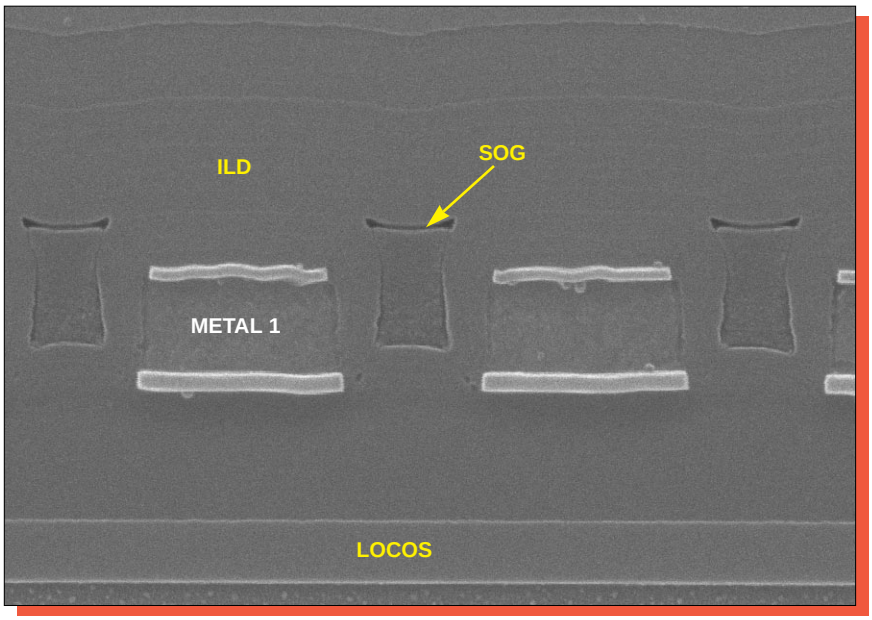



Mag. 52,000x

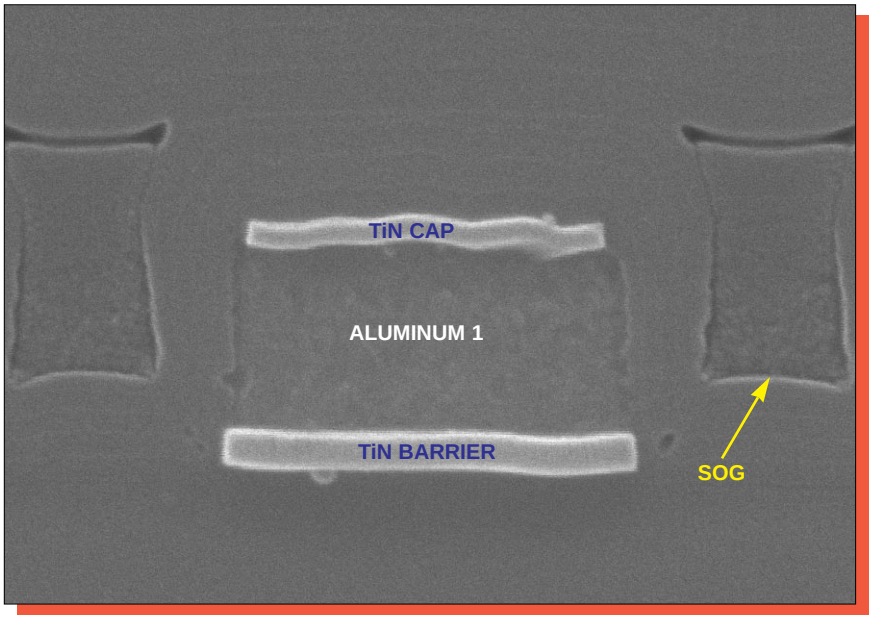



Mag. 52,000x

Figure 13. SEM section views illustrating typical vias.

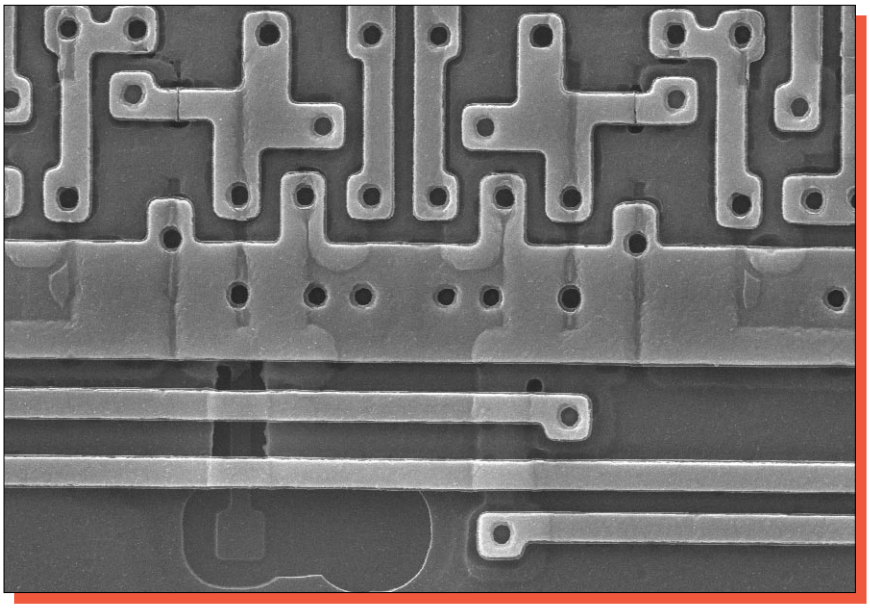



Mag. 26,000x

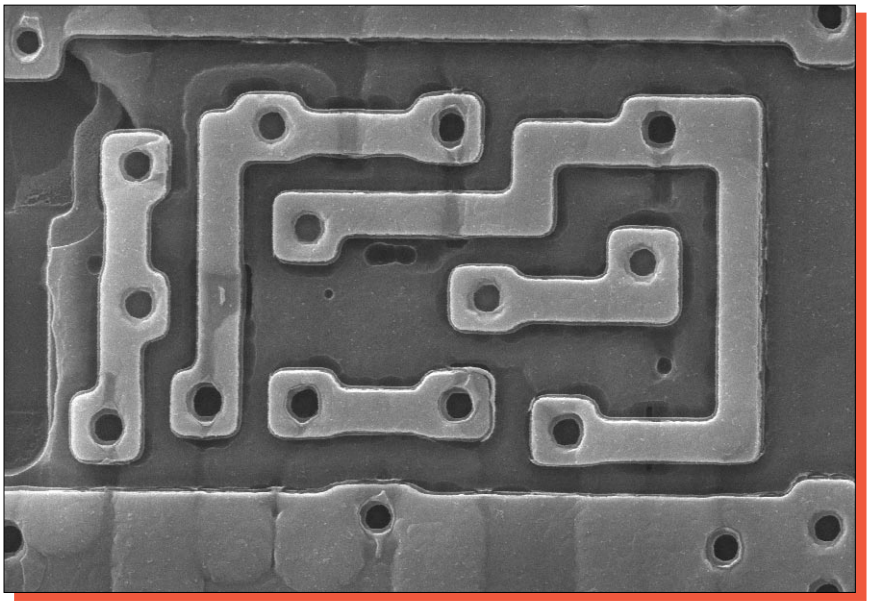



Mag. 52,000x

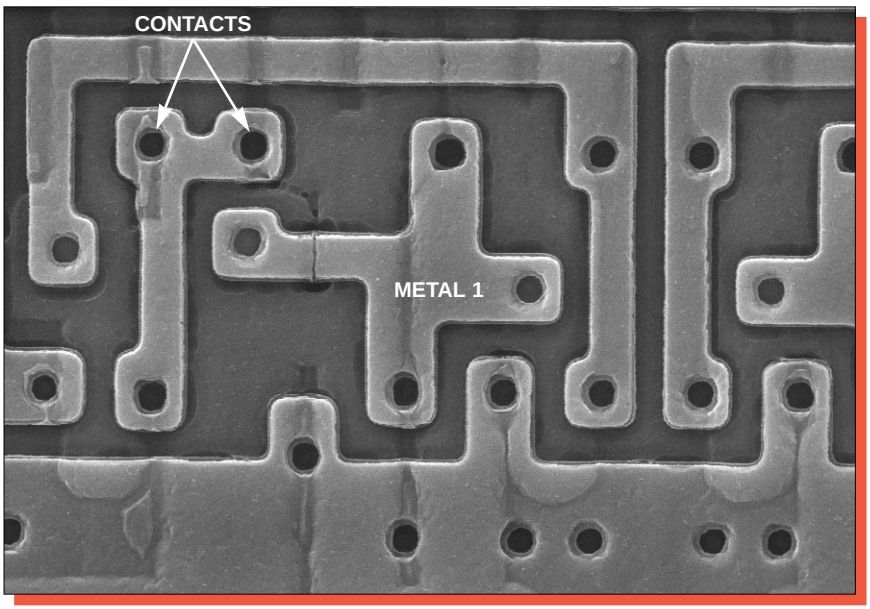
Figure 14. SEM section views of metal 1 line profiles.



Mag. 3200x

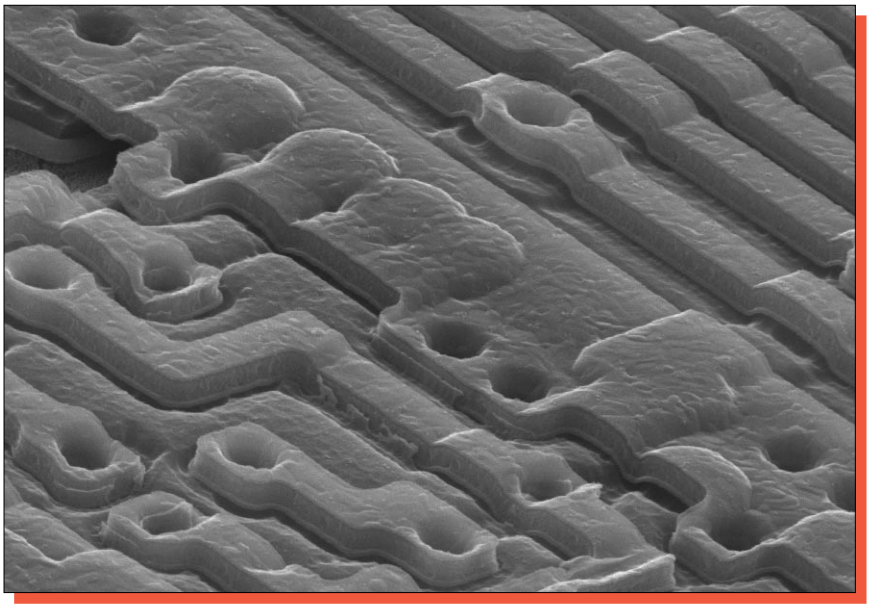


Mag. 5000x

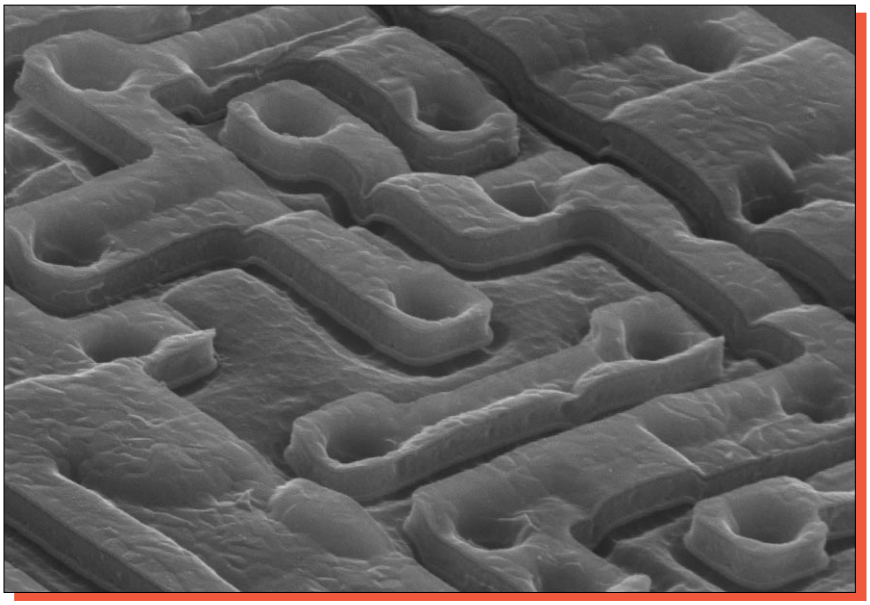



Mag. 5000x

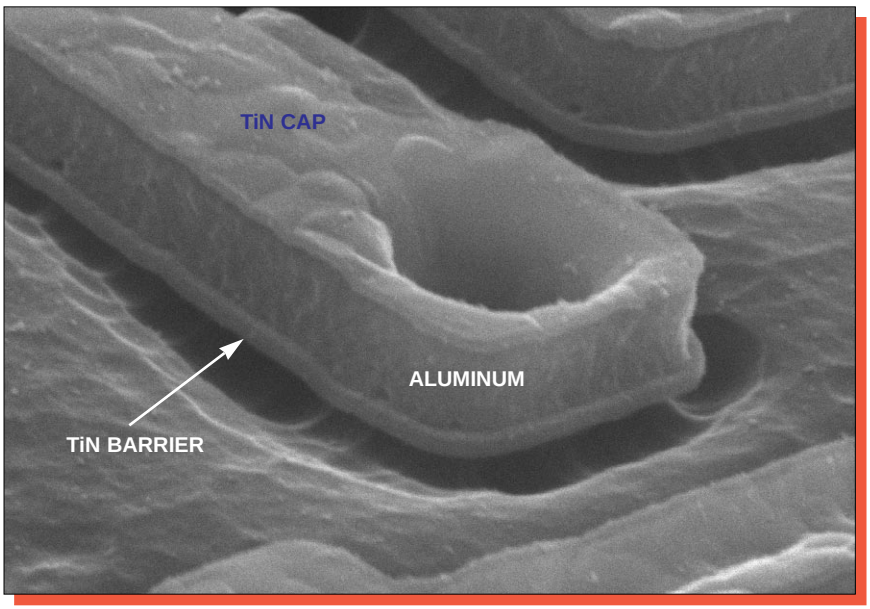
Figure 15. Topological SEM views of metal 1 patterning. 0°.



Mag. 6700x

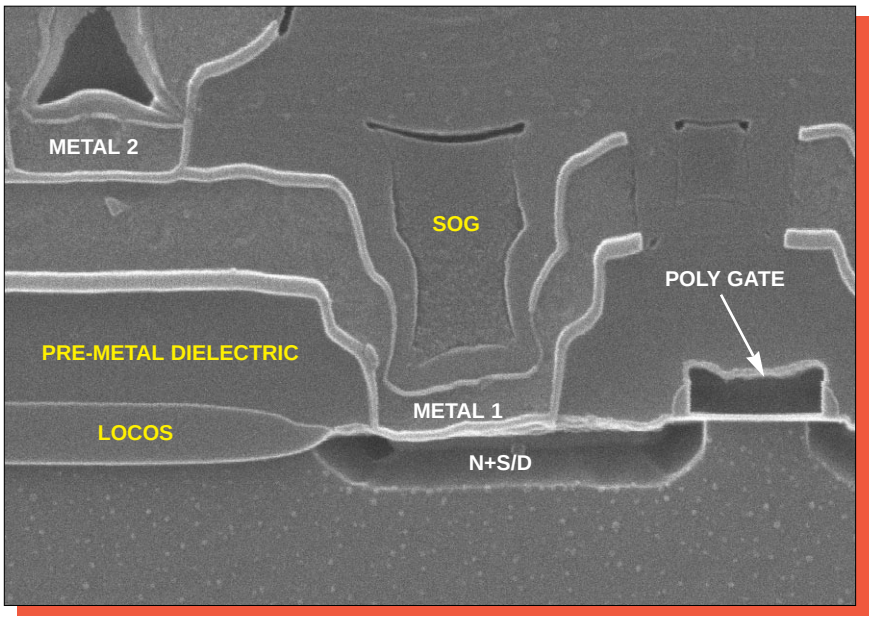


Mag. 8000x




Mag. 27,000x

Figure 16. Perspective SEM views of metal 1 step coverage. 60°.



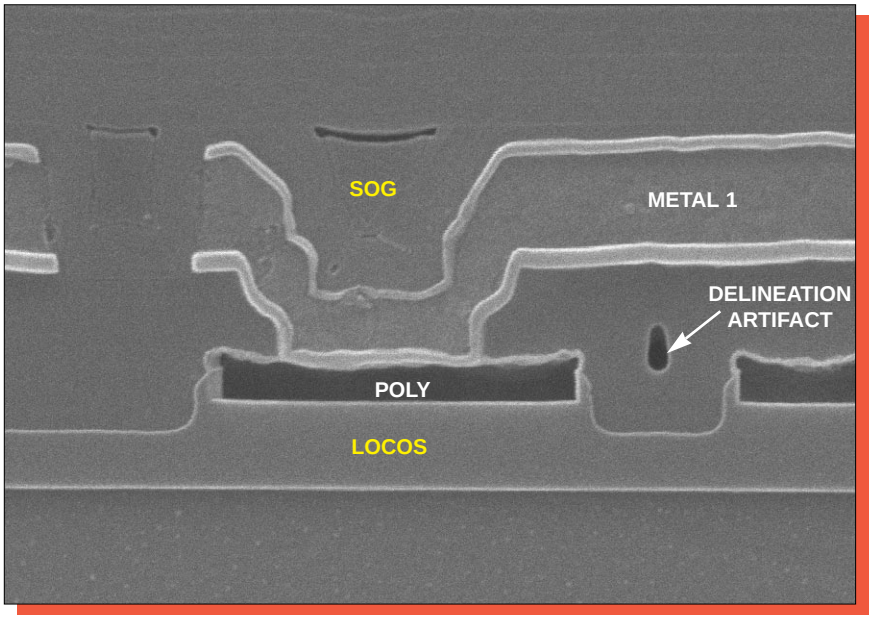
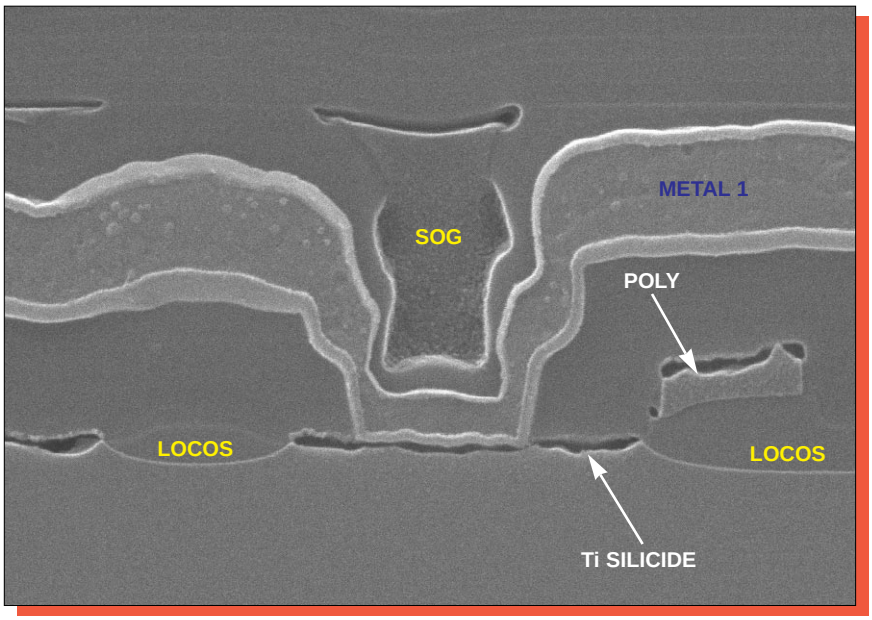
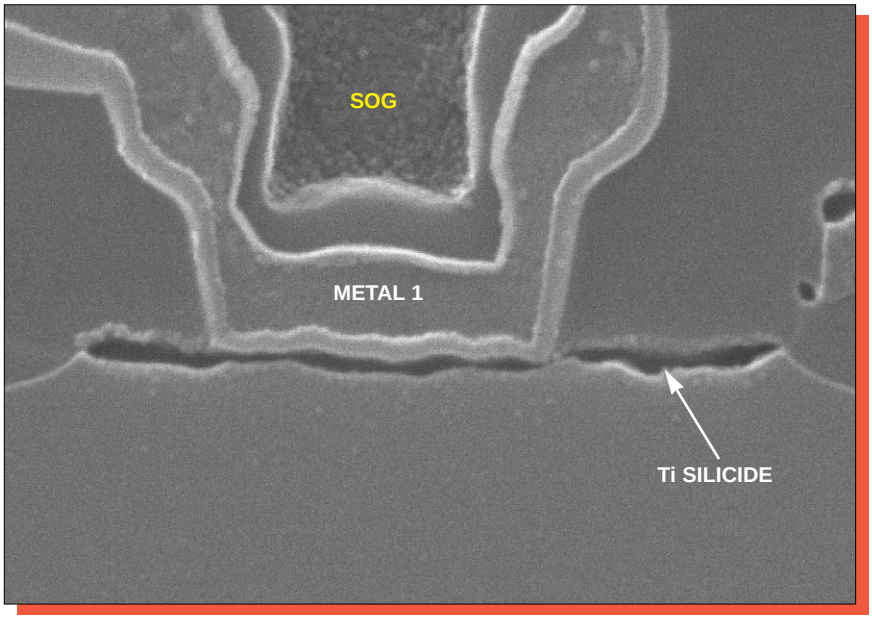




Figure 17. SEM section views of typical metal 1 contacts. Mag. 26,000x.

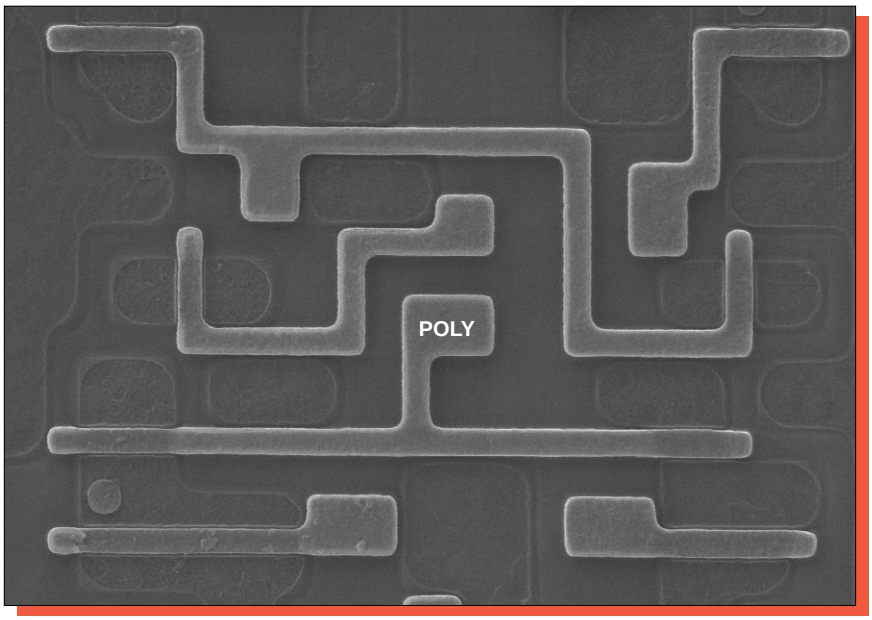



Mag. 26,000x

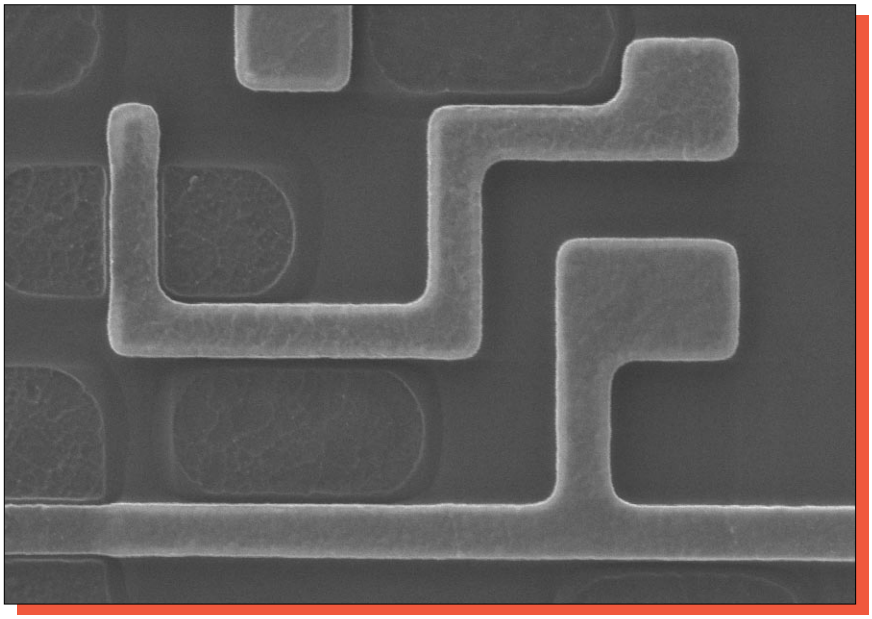



Mag. 52,000x

Figure 18. SEM section views illustrating silicided diffusion structures.

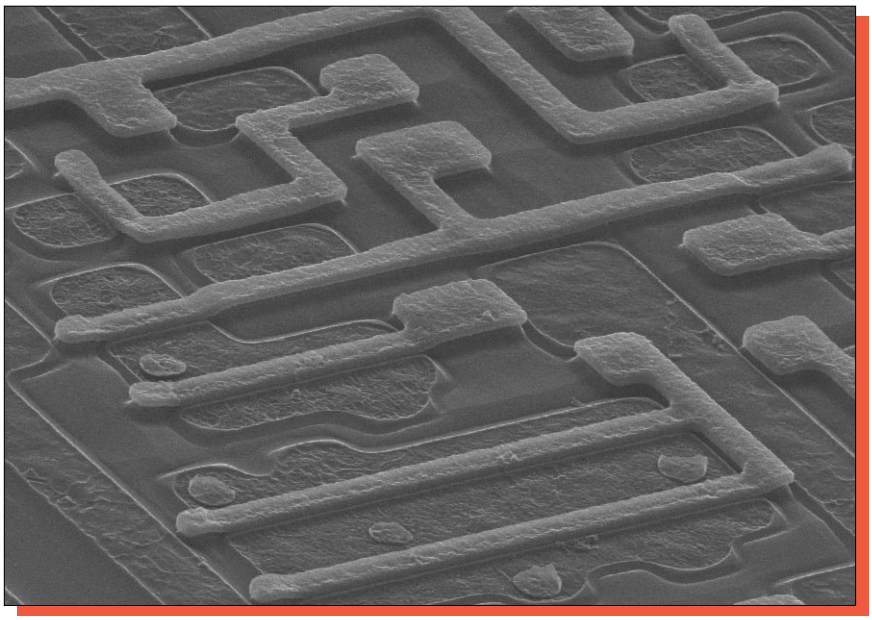



Mag. 5000x

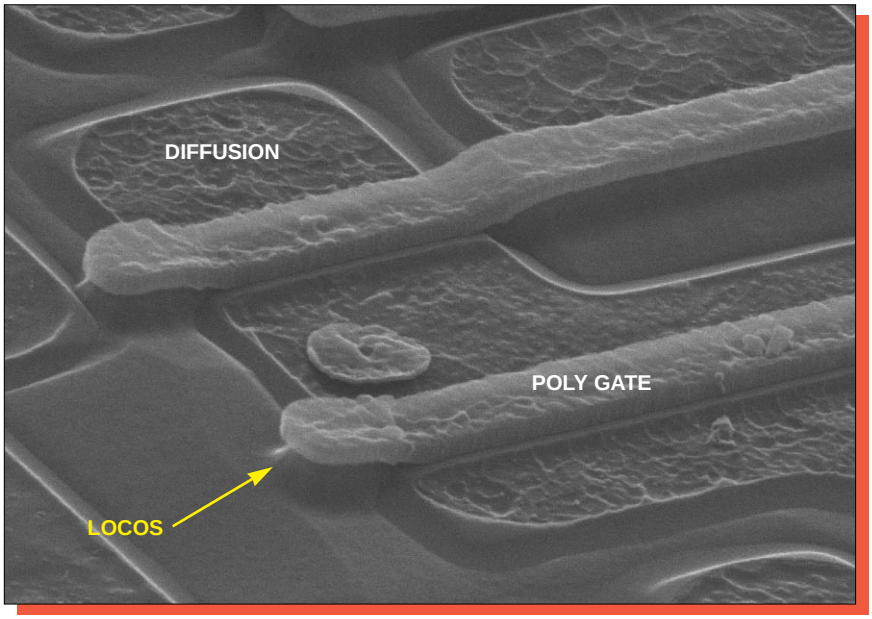


Mag. 10,000x

Figure 19. Topological SEM views of poly patterning. 0°.

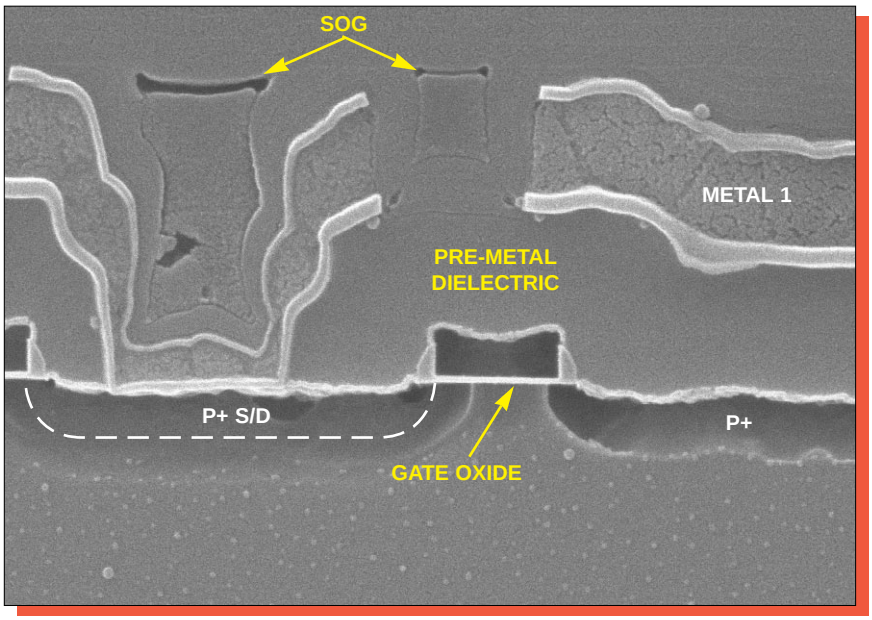


Mag. 6500x

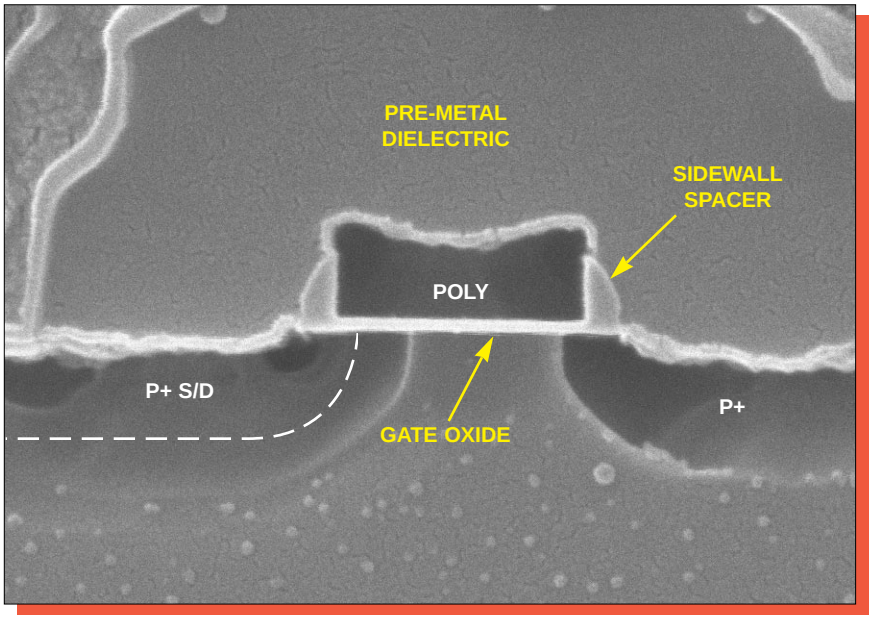



Mag. 17,600x

Figure 20. Perspective SEM views of poly coverage. 60°.

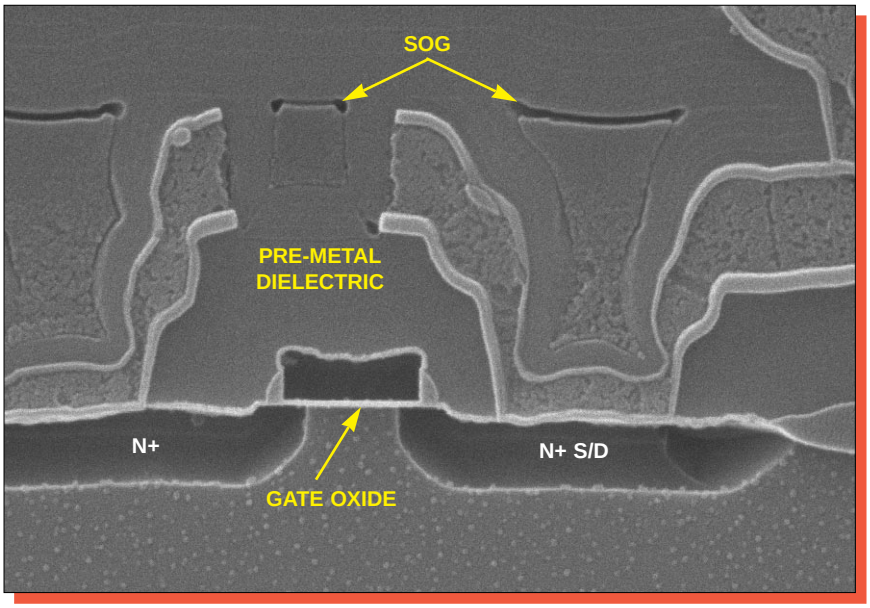



Mag. 26,000x

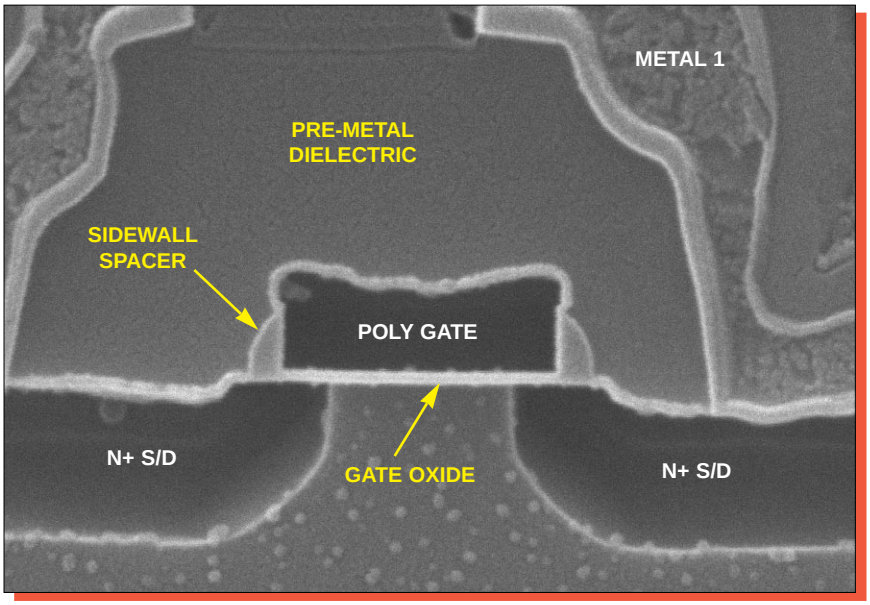



Mag. 52,000x

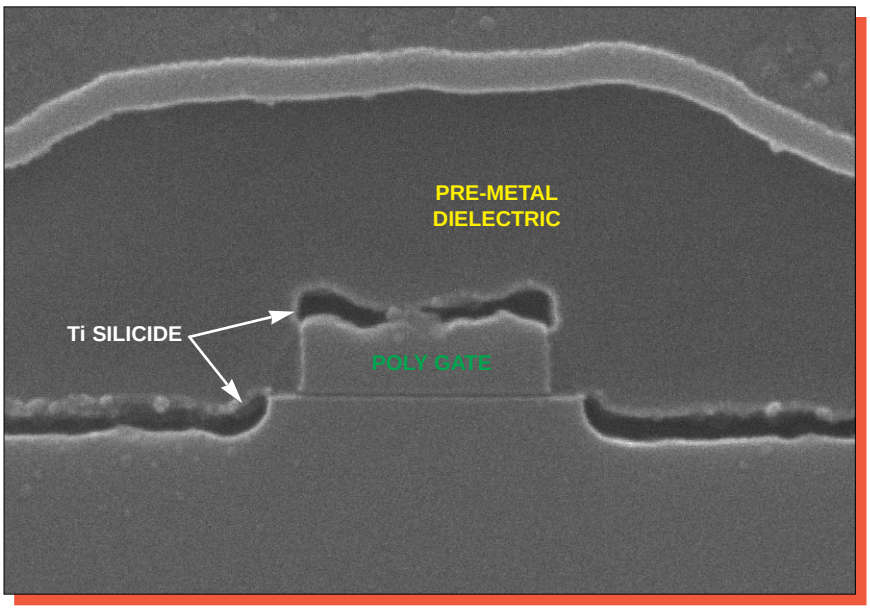
Figure 21. SEM section views of a typical P-channel transistor.




N-channel,
Mag. 26,000x

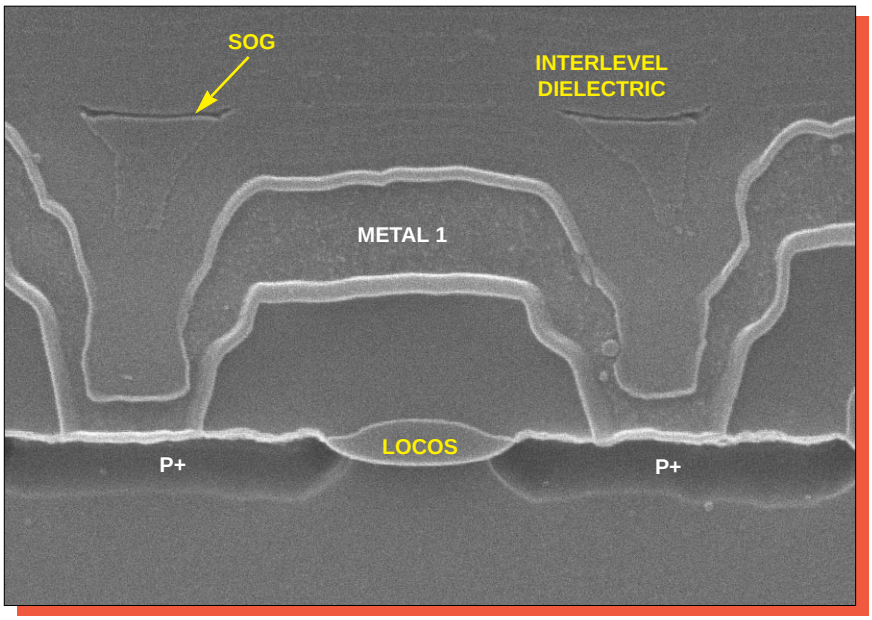



N-channel,
Mag. 52,000x

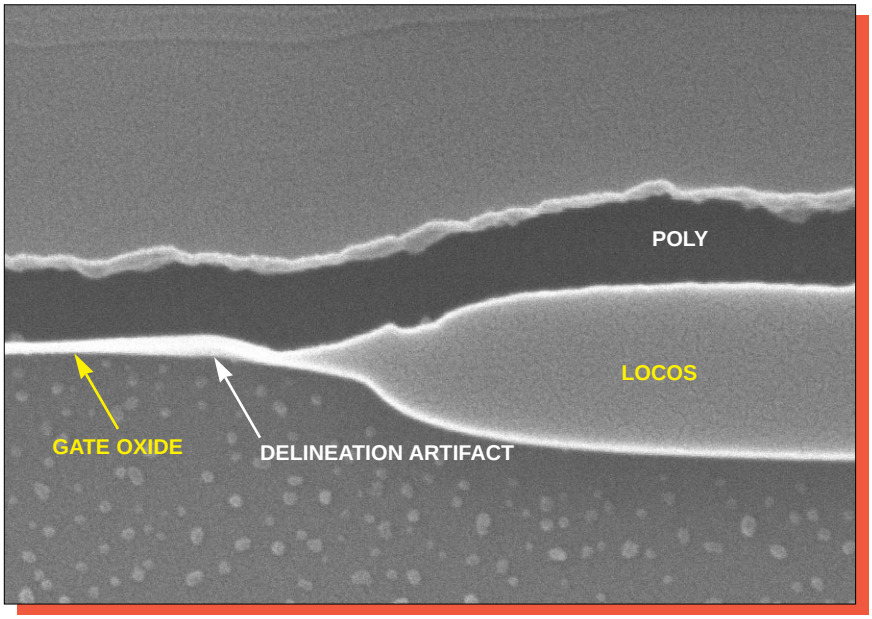



glass etch,
Mag. 52,000x

Figure 22. SEM section views of typical transistors.

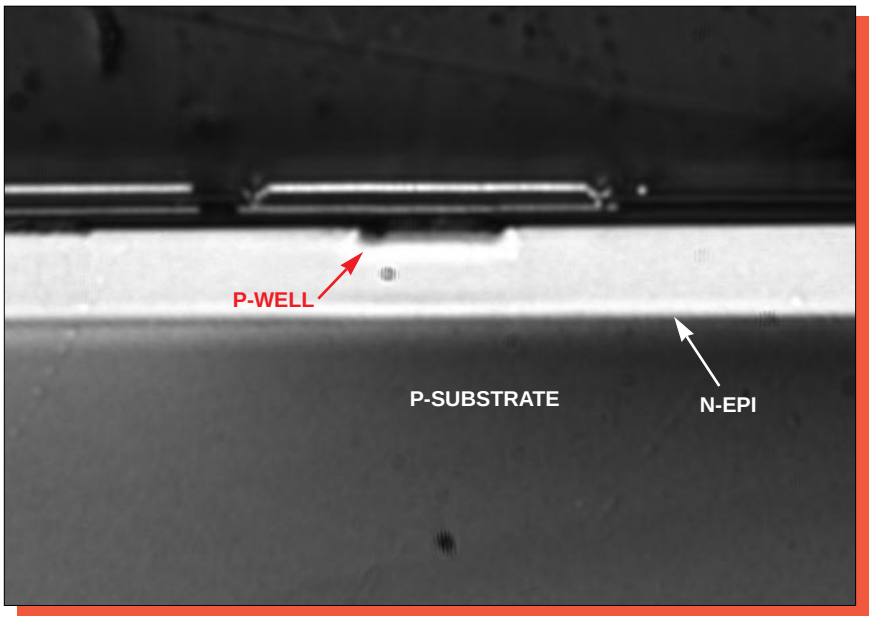



Mag. 26,000x

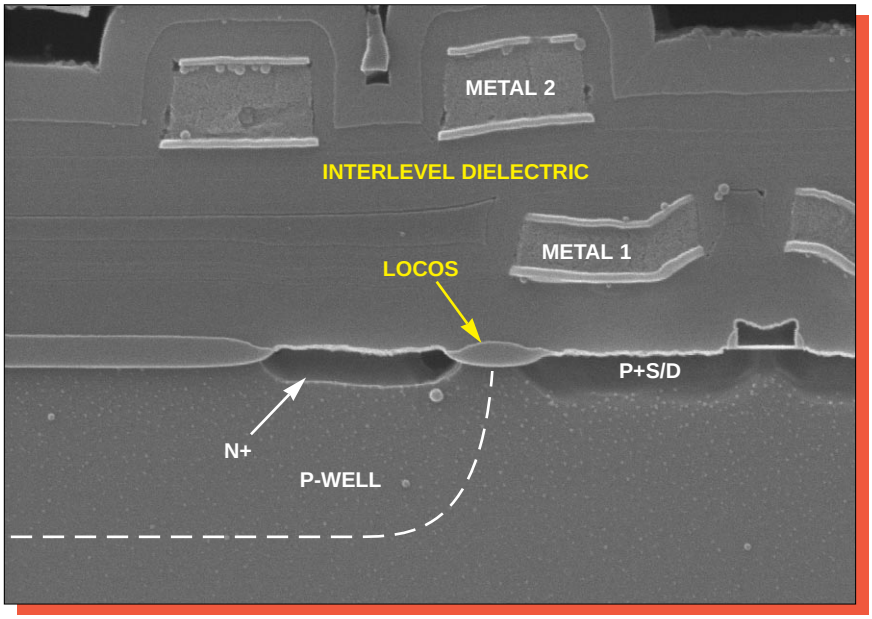



Mag. 52,000x

Figure 23. SEM section views of local oxide isolation and typical birdsbeak.

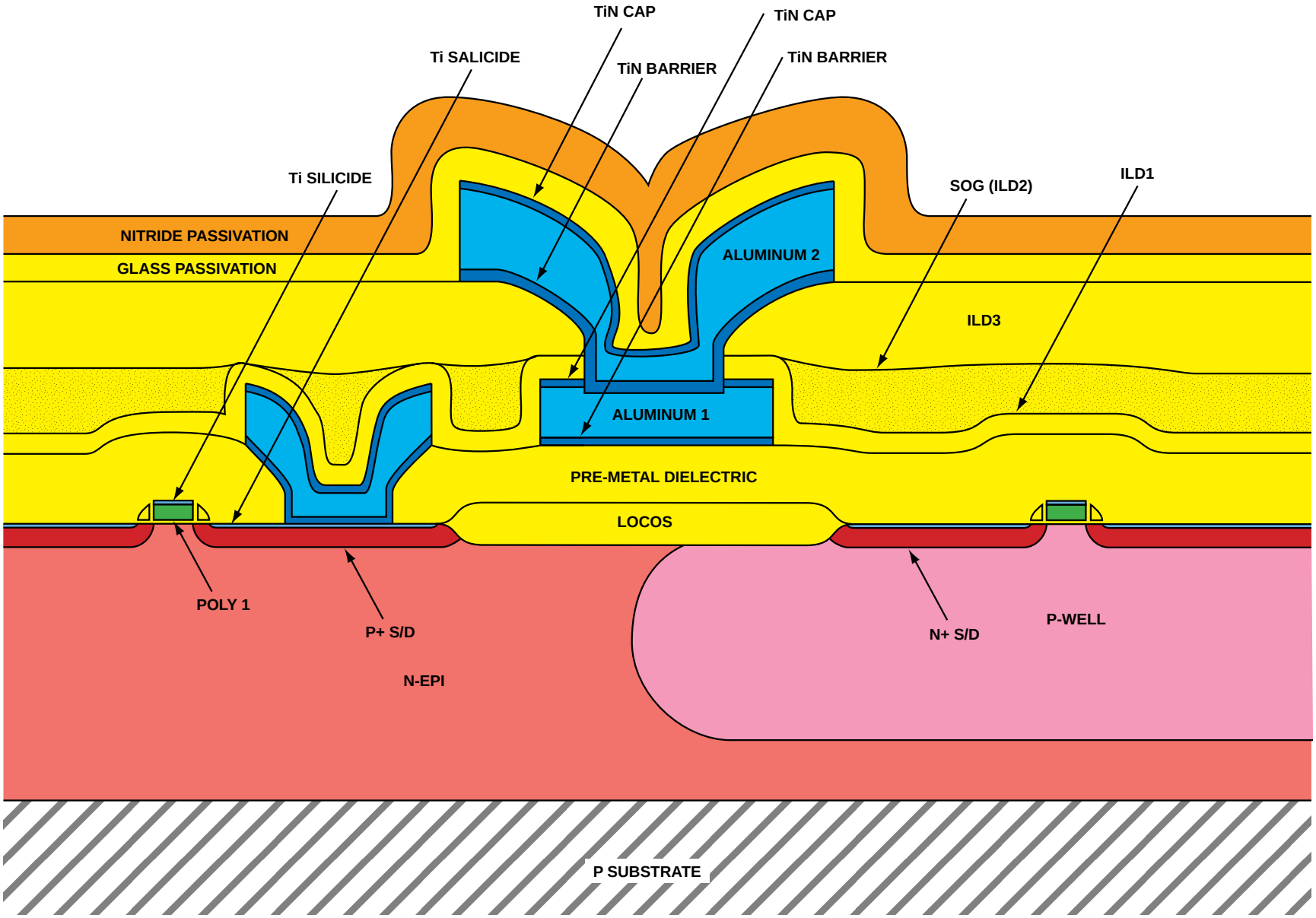



Mag. 825x




Mag. 13,000x

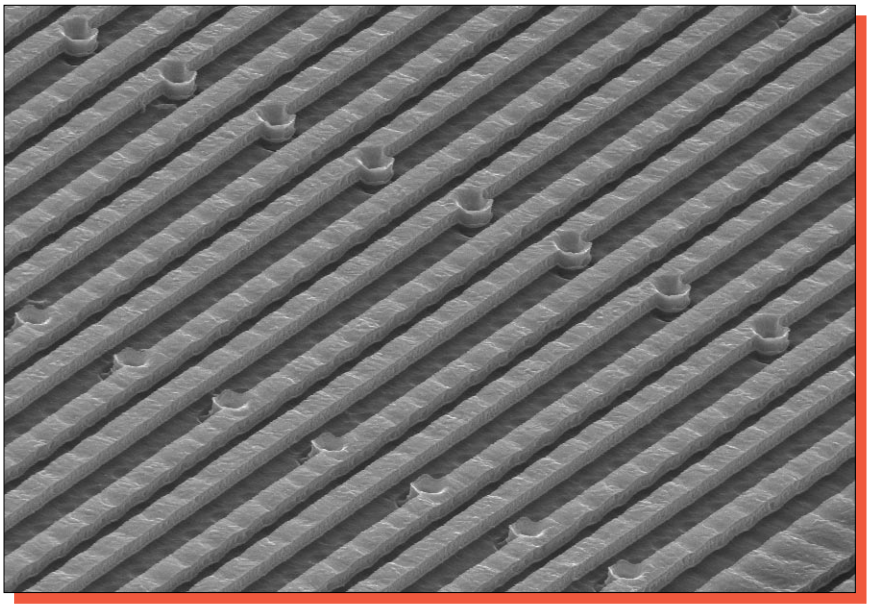
Figure 24. SEM section views illustrating well structure.



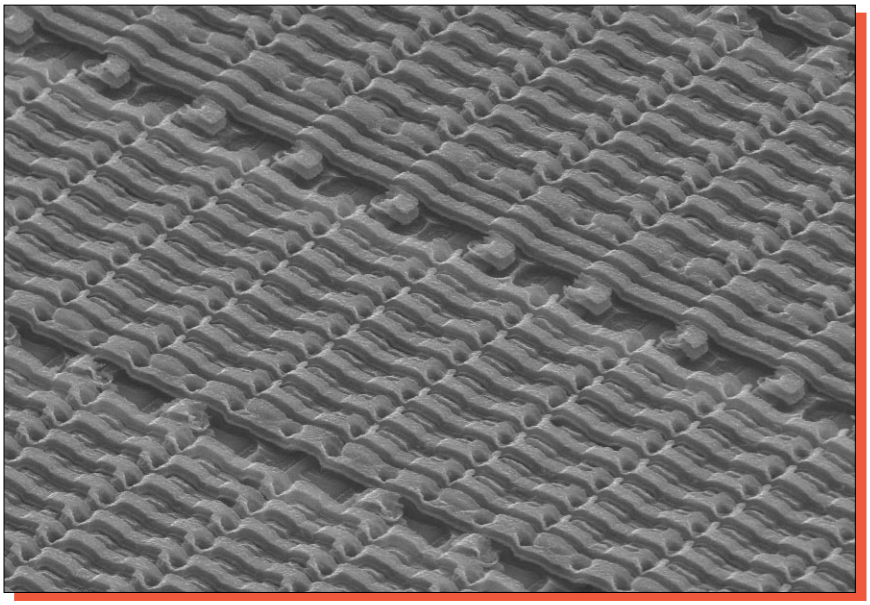

Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

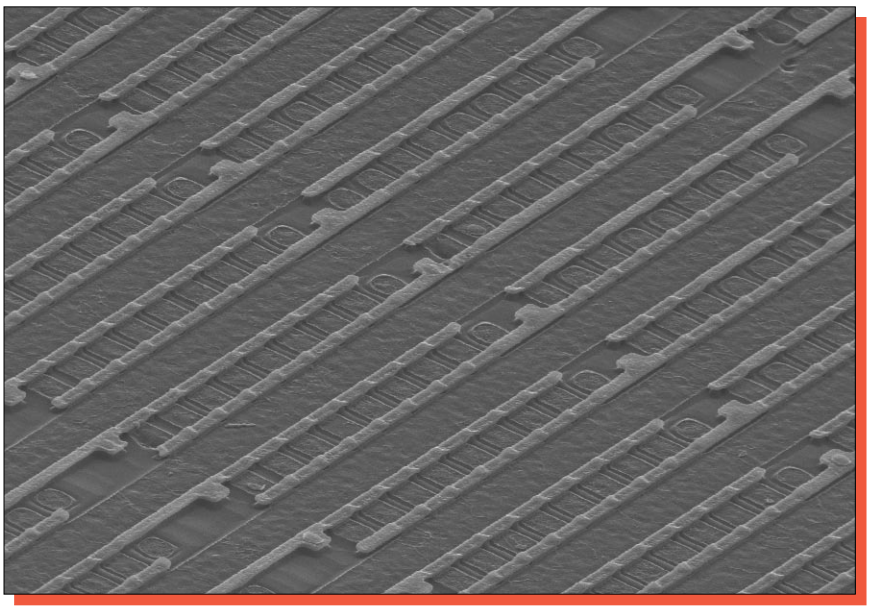
Figure 25. Color cross section drawing illustrating device structure.



metal 2



metal 1



unlayered

Figure 26. Perspective SEM views of the MROM array. Mag. 2500x, 60°.

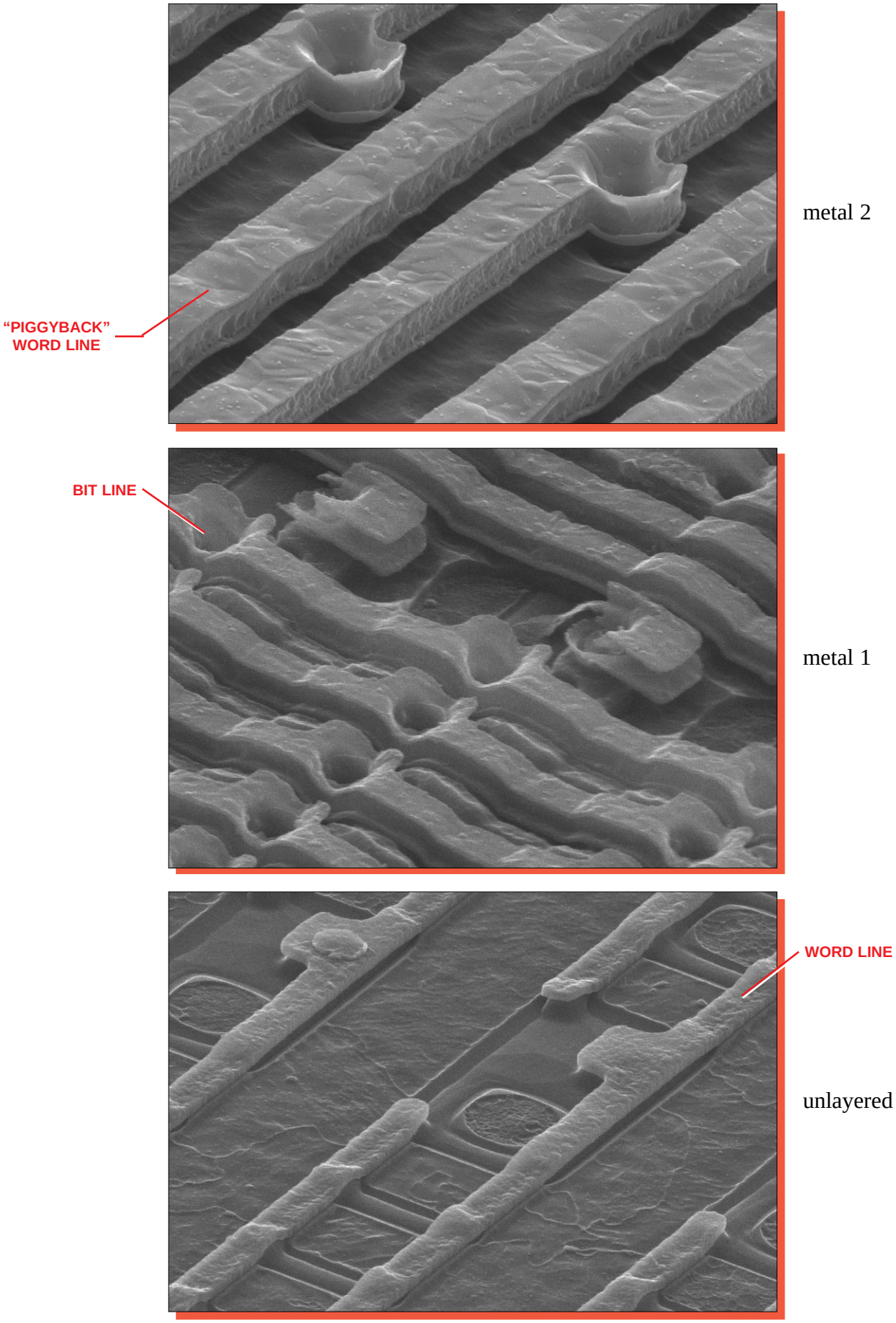
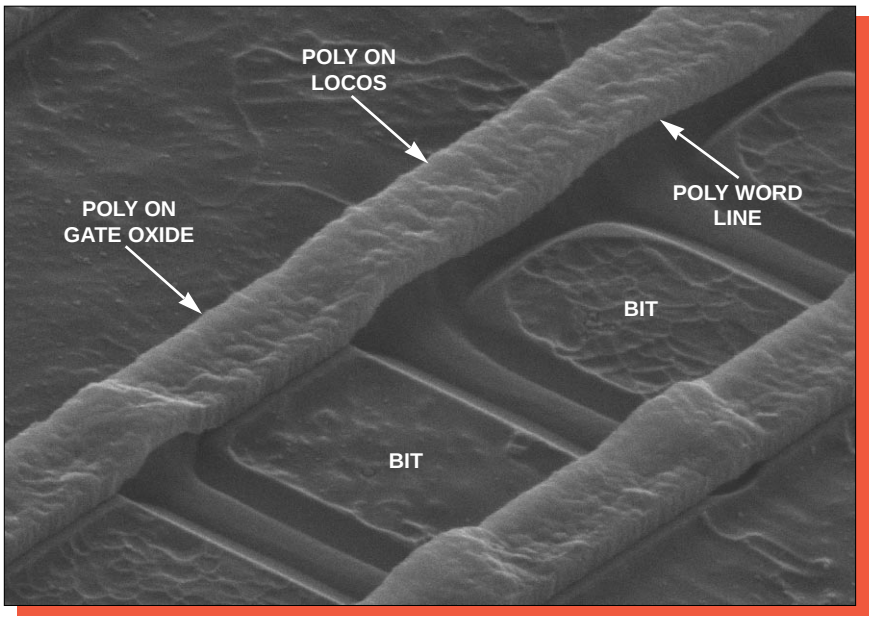
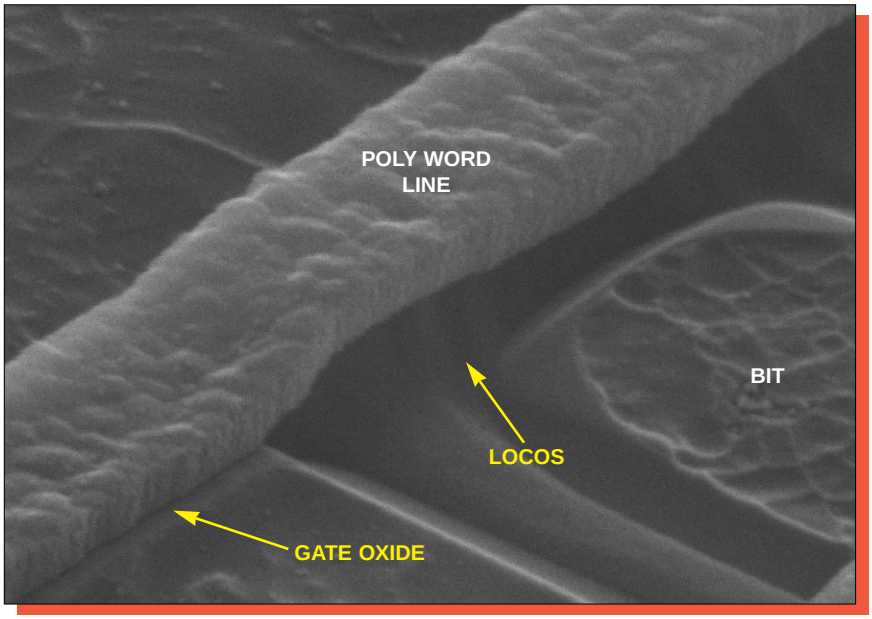



Figure 27. Detailed perspective SEM views of the MROM array. Mag. 10,000x, 60°.




Mag. 20,000x




Mag. 40,000x

Figure 28. Detailed SEM views of programmed cells. 60°.

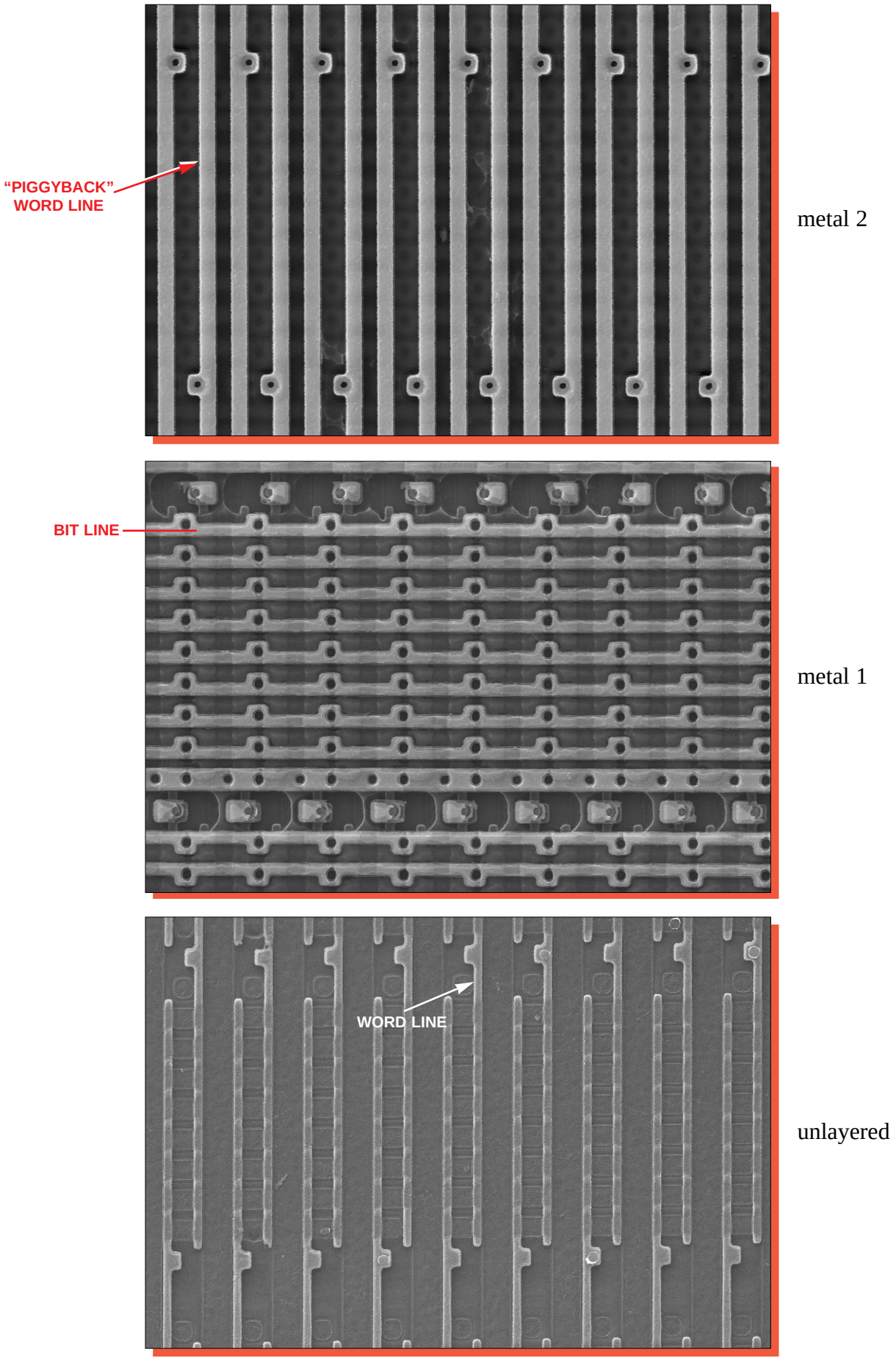
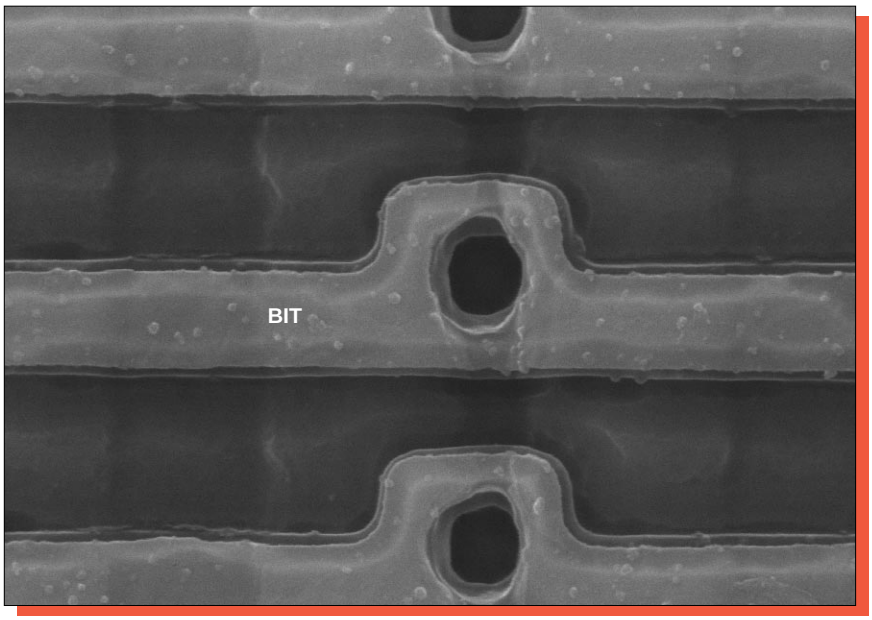
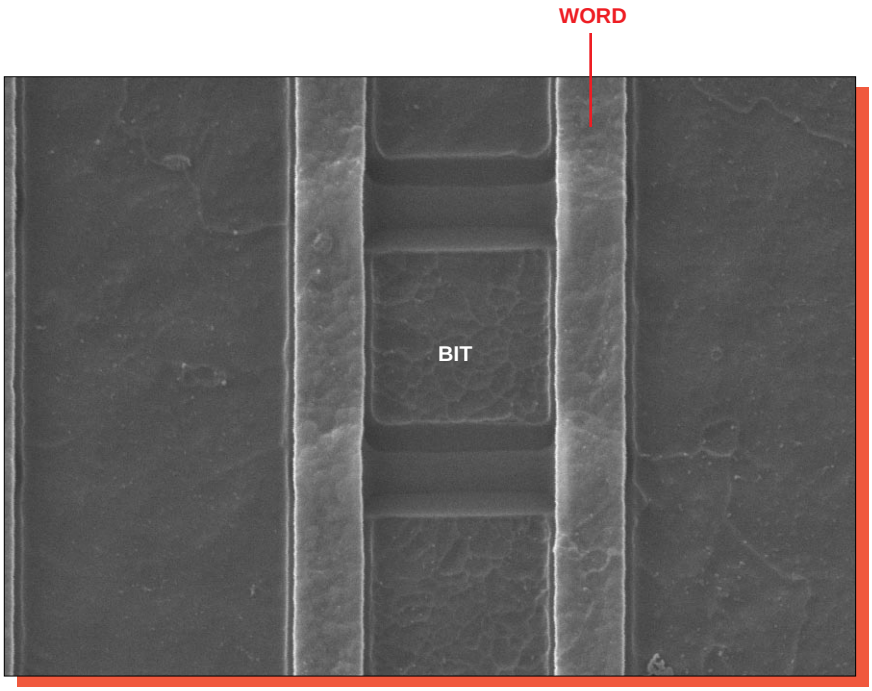



Figure 29. Topological SEM views of the MROM array. Mag. 2100x, 0°.

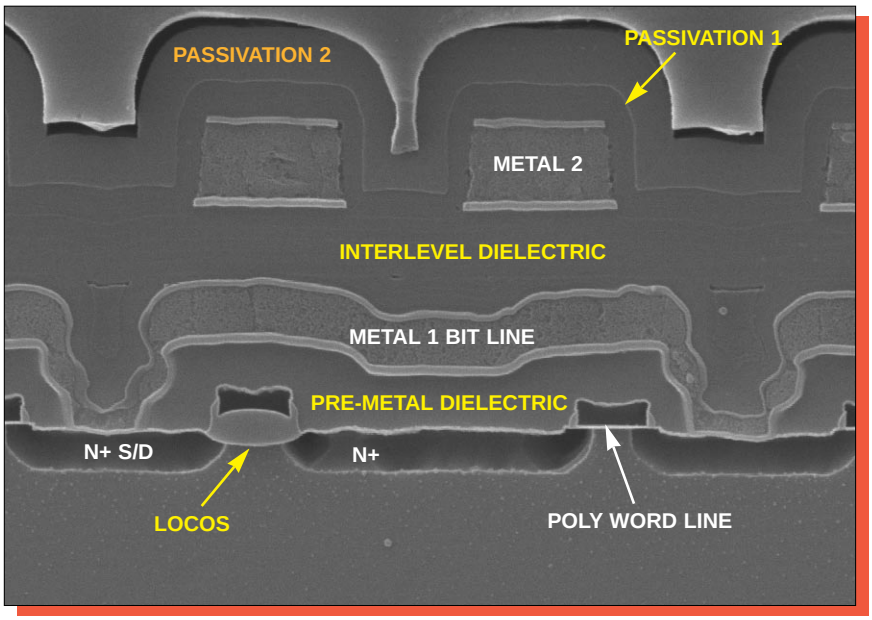



metal 1

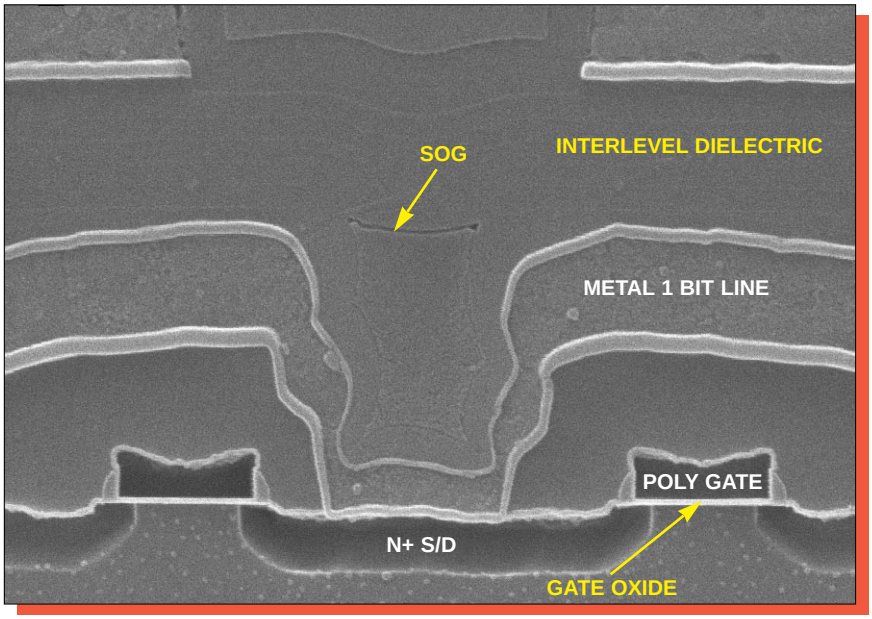



unlayered

Figure 30. Detailed topological views of the MROM cell array. Mag. 13,000x, 0°.

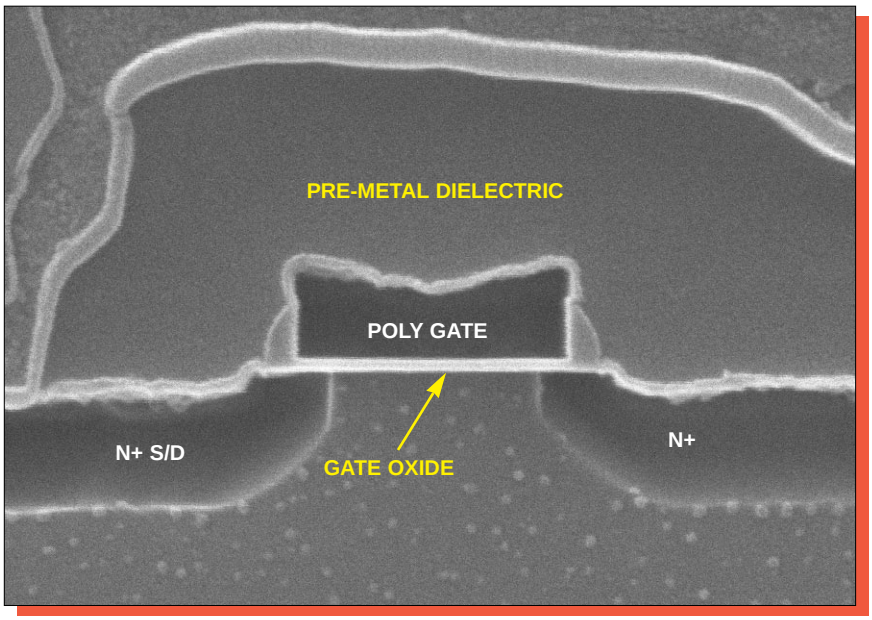



Mag. 13,000x




Mag. 26,000x

Figure 31. SEM section views of MROM array.



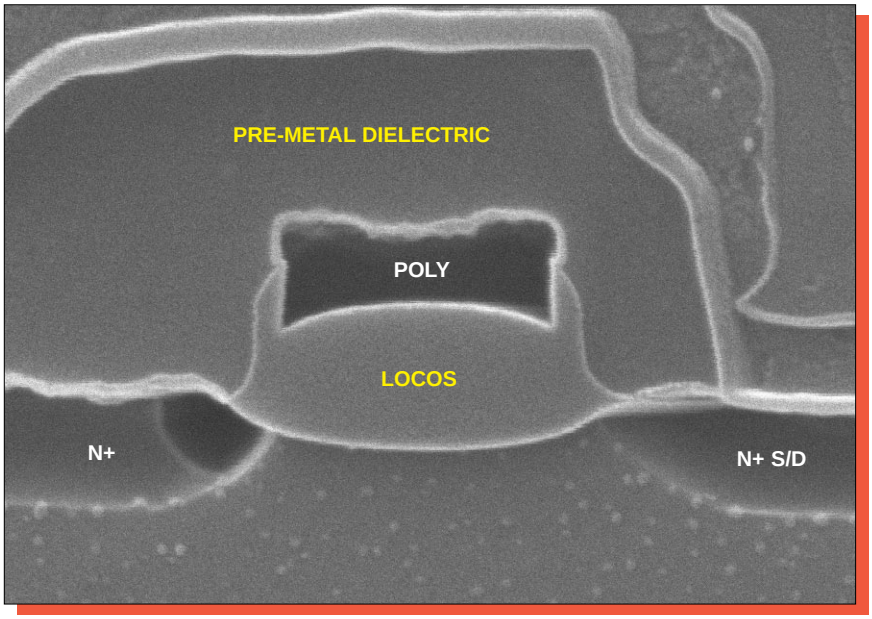
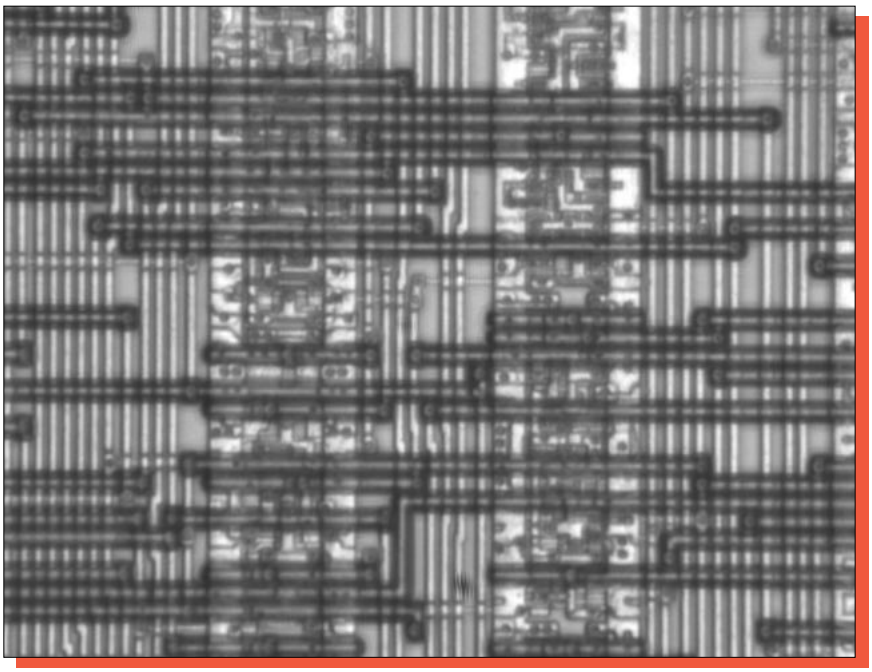
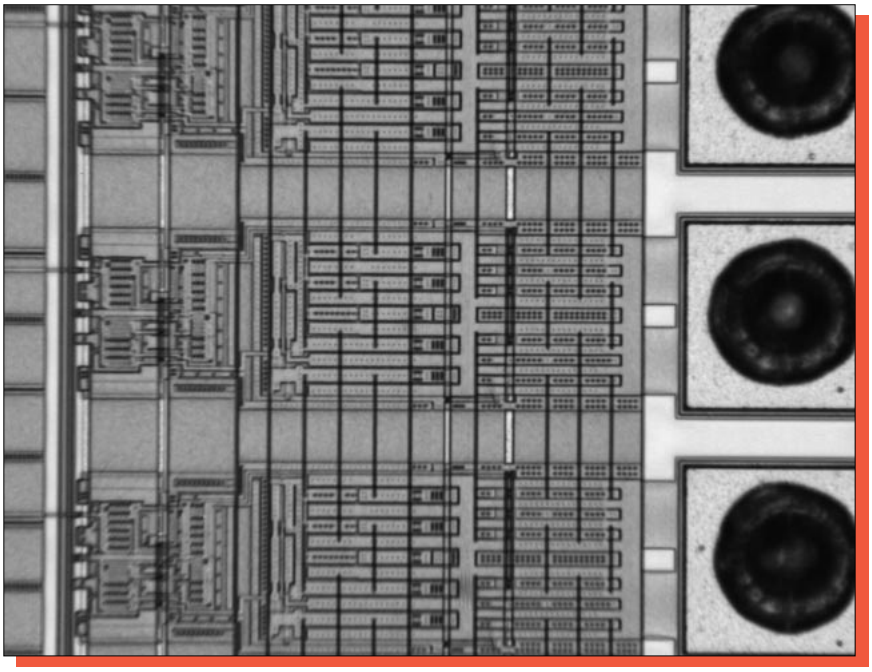




Figure 32. SEM section views of programmed cells. Mag. 52,000x.

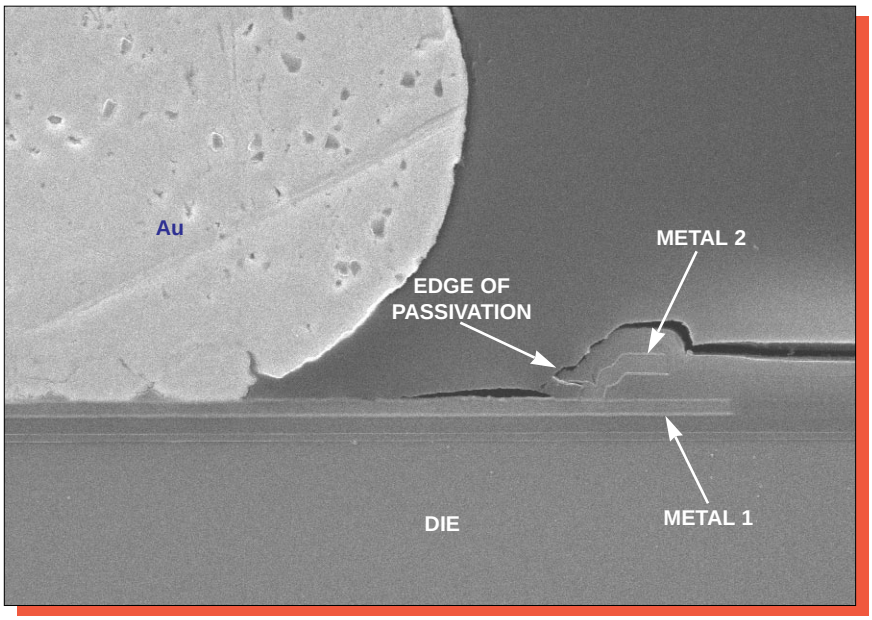


Mag. 860x

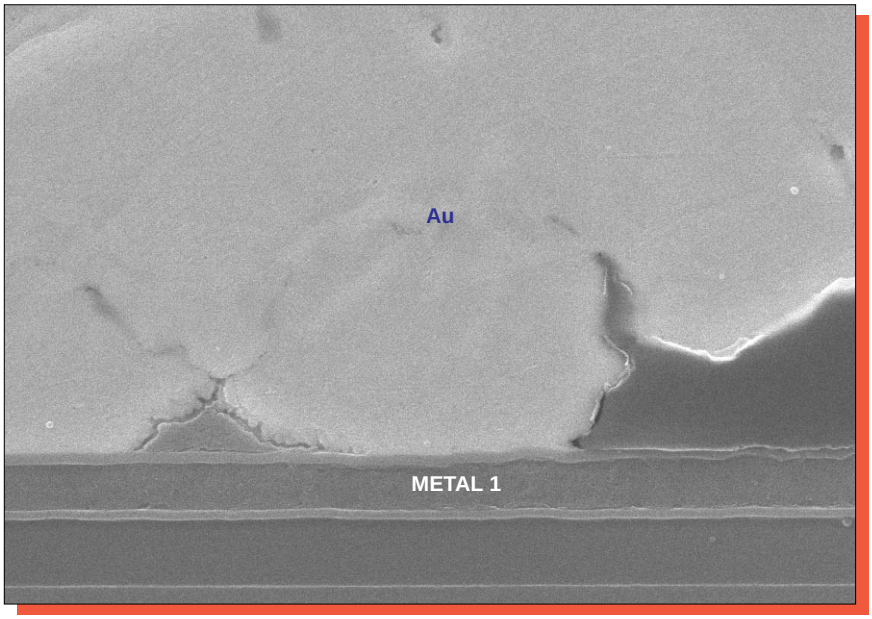


Mag. 220x

Figure 33. Optical views of typical circuitry and I/O structure.




Mag. 3200x




Mag. 13,000x

Figure 34. SEM section views illustrating bond pad structure.