Construction Analysis

Intel 266MHz 32-Bit Pentium II (Klamath) Processor

Report Number: SCA 9706-542

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INTRODUCTION

This report describes a construction analysis of the Intel 266MHz Pentium II (Klamath) Processor. Two samples were used for the analysis. The devices were received in 540-pin BGA (Ball Grid Array) packages with a metal heatsink.

MAJOR FINDINGS

Questionable Items:[1]

- Quality of die manufacturing was good and we found no areas of quality concerns.

Special Features:

- Four metal, P-epi, CMOS process (not BiCMOS).
- All metal levels employed stacked tungsten via/contact plugs.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium silicided diffusion structures.
- Aggressive feature sizes (reported 0.28 micron, measured 0.25 micron gates).
- Beveled die edges at top of die.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 540-pin BGA (Ball Grid Array) packages. A metal heatsink was employed on the top of the package. The die was mounted cavity down.

- Eight decoupling capacitors were present on top of the package.

- The BGA was constructed of fiberglass in which the package cavity was employed. The package was covered with a green conformal coating. The cavity was filled with black plastic material.

- Triple tier package lands plated with gold.

- Ultrasonic wedge wirebonding using gold wire. Wirebonds (to the die and package lands) had double "footprints."

- Sawn dicing (full depth). The edges of the die had been beveled at the surface.

- Silver-epoxy die attach. The backside of the die was plated with gold.

Die Process:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process apparently employing twin-wells in a P-epi on a P substrate.

- Die coat: A thin patterned polyimide die coat was present over the entire die.

- Final passivation: A single layer of nitride.

TECHNOLOGY DESCRIPTION (continued)

- Metallization: Four levels of metal defined by dry-etch techniques. All consisted of aluminum with titanium-nitride caps (except M4). Metal 4 employed a substantial titanium adhesion layer. There appeared to be evidence of very thin titanium adhesion layers under metals 1 - 3. Tungsten plugs were employed for all vertical interconnect. Metals 2 - 4 employed tungsten plugs with “stubs” underneath, for improved contact. The “stubs” penetrated into the metal below the tungsten plus. This is a unique processing feature. All plugs were lined with titanium-nitride. Stacked vias were employed at all levels.

- Interlevel dielectrics 1, 2 and 3: The interlevel dielectric between all metals consisted of the same structure. A very thin glass was deposited first, followed by two thick layers of glass. The second layer had rounded corners around metal sidewalls. The third layer of glass was planarized by CMP.

- Pre-metal glass: A thick layer of glass followed by a thin layer of glass. This dielectric was also planarized by CMP.

- Polysilicon: A single layer of dry-etched polycide (poly and titanium-silicide). This layer was used to form all gates on the die. Nitride sidewall spacers were used to provide the LDD spacing.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Titanium was sintered into the diffusions (salicide process). No bipolar devices appeared to be present.

- Isolation: Isolation consisted of oxide-filled shallow-trenches.

- Wells: Twin-wells in a P-epi on a P substrate.

- SRAM: On-chip Level 1 data and instruction Cache memory cell arrays (16KByte each) were employed. The memory cells used a 6T CMOS SRAM cell design.

- No redundancy fuses were found.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 8**

Questionable Items:[1] None.

Special Features:

- Beveled die edges.

- Unique double "footprint" wirebonding technique.

- Extremely tight bond pitch (80 microns).

General items:

- The devices were packaged in 540-pin BGAs. A metal heatsink was employed on top of the packages. The die was mounted cavity down. They were constructed of fiberglass and were covered with a green conformal coating. The cavity was filled with black plastic material. Eight decoupling capacitors were employed on top of the packages.

- Overall package quality: Good. No defects were found on the external or internal portions of the packages. Solder ball placement was good. No voids were noted in the plastic cavity fill.

- Wirebonding: Ultrasonic wedge bond method using 0.9 mil gold wire. All wirebonds had a double "footprint" which is the first time we've seen this type of bonding used on these types of devices. A three tier package land structure was used. Wire spacing and placement was good. Bond pitch was very close (80 microns); however, no problems were noted.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS I (continued)

- Die attach: Silver-epoxy die attach of good quality. No voids were noted in the die attach. The backside of the die was plated with gold.

- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges. The top edges of the die had been beveled (see Figures 7 and 8). This is highly unusual and it is not apparent why it is done.

ANALYSIS RESULTS II

Die Process and Design: **Figures 9 - 49**

Questionable Items:[1]

- No items of concern were found in the area of die fabrication.

Special Features:

- Four metal, twin-well, P-epi, CMOS process.
- All vertical interconnect employed tungsten via/contact plugs.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium salicided diffusion structures.
- Aggressive feature sizes (0.25 micron gates).

General Items:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process apparently employing twin-wells in a P-epi on a P substrate. No problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Design features: Slotted bus lines were employed to relieve stress. Anti-dishing patterns were employed for planarization purposes. Numerous unconnected metal 4 vias (which appear to be used for probing purposes) were present.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.

ANALYSIS RESULTS II (continued)

- Die coat: A patterned polyimide die coat was present over the entire die surface.

- Final passivation: A single layer of nitride. Coverage was good. Edge seal was also good as the passivation extended to the scribe lane to seal the metallization.

- Metallization: Four levels of metallization. All consisted of aluminum with titanium-nitride caps (except M4). Metal 4 employed a fairly thick titanium adhesion layer. The other levels probably used a titanium layer too thin to detect. Tungsten plugs were employed under all metals. Holes (voids) were noted in the center of some tungsten plugs (mainly metals 3 and 4). Although this indicates incomplete fill of the via holes no problems are foreseen. All plugs were lined with titanium-nitride underneath and the presumed titanium layer over top.

- Metal patterning: All metal levels were defined by a dry etch of good quality. Metal lines were widened (where needed), where vias made contact to them from above.

- Metal defects: None. No voiding, notching or cracking of the metal layers was found. No silicon nodules were found following removal of the metal layers.

- Metal step coverage: No metal (aluminum) thinning was present at the connections to the tungsten via plugs. The absence of thinning is due to the good control of plug height and the planarization technique employed.

- Vias and contacts: All via and contact cuts were defined by a dry etch of good quality. Again, alignment of the metals and plugs was good. Metals 2 - 4 employed tungsten “stubs” at the bottom of the tungsten plugs. These unique features consisted of stubs of tungsten metallization that penetrate into the underlying aluminum. The profiles of the “stubs” varied quite a lot indicating inconsistency in the processing. Vias and contacts were placed directly over one another (stacked vias). No problems were noted.

<u>ANALYSIS RESULTS II</u> (continued)

- Interlevel dielectrics: The interlevel dielectric between metal levels consisted of the same oxide structure. A very thin glass was deposited first, followed by two thick layers of glass. The third layer of glass was subjected to CMP which left the surface very planar. The appearance of the second glass layer on ILD 1 was somewhat unusual; however, it does not appear to present a problem. No problems were found with any of these layers.

- Pre-metal glass (under metal 1): A thick layer of silicon-dioxide followed by a thin layer of glass. This layer also appeared to have been planarized by chemical-mechanical-planarization. No problems were found.

- Polysilicon: A single level of polycide (poly and titanium-silicide) was used. It formed all gates and word lines in the array. Definition was by dry etch of good quality. Nitride sidewall spacers were used throughout and left in place. No problems were found.

- Isolation: The device used oxide-filled shallow-trench isolation. The step at the oxide transition was somewhat larger than normally seen.

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Titanium was sintered into the diffusions (salicide process) to reduce series resistance. An LDD process was used employing nitride sidewall spacers. No problems were found. No bipolar devices were found on these parts which makes them the first non BiCMOS Pentium parts we've seen.

- Wells: Apparent twin-wells were used in a P-epi on a P substrate. Definition was normal.

- Buried contacts: Not used.

ANALYSIS RESULTS II (continued)

- SRAM: On-chip Level 1 data and instruction Cache memory cell arrays (16KByte each) were employed. The memory cells used a 6T CMOS SRAM cell design. Metal 4 distributed GND and Vcc to Metal 3. Metal 3 distributed GND and Vcc (via metals 1 and 2) and formed “piggyback” word lines. Metal 2 formed bit lines and metal 1 provided cell interconnect and provided GND and Vcc throughout the cells. Polycide formed the N-channel select and storage transistors and the P-channel pull-up transistors. Cell pitch was 4.1 x 4.8 microns (19 microns^2).

- No redundancy fuses were noted.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Inspect assembly features

Die optical inspection

Wirepull test

Delayer to metal 4 and inspect

Aluminum removal (metal 4) and inspect tungsten plugs

Delayer to metal 3 and inspect

Aluminum removal (metal 3) and inspect tungsten plugs

Delayer to metal 2 and inspect

Aluminum removal (metal 2) and inspect tungsten plugs

Delayer to metal 1 and inspect

Aluminum removal (metal 1) and inspect tungsten plugs

Delayer to polycide/substrate and inspect

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

*_Delineation of cross-sections is by silicon etch unless otherwise indicated._

<u>OVERALL QUALITY EVALUATION</u>: Overall Rating: Normal

<u>DETAIL OF EVALUATION</u>

Package integrity	G
Package markings	N
Die placement	G
Wirebond placement	G (tight wirebond pitch)
Wirebond quality	G (double footprints)
Dicing quality	G (beveled edges)
Die attach quality	G
Die attach method	Silver-epoxy
Dicing method	Sawn
Wirebond method	Ultrasonic wedge bonds using 0.9 mil gold wire.

Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	G
Metal registration	N
Contact coverage	N
Via/contact registration	N
Etch control (depth)	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP (heatsink)

Sample 1	C70609 14-0257 (plus coded markings)
Sample 2	(only coded markings)

WIREBOND STRENGTH

# of wires pulled:	90 (30 each tier)
Bond lifts:	0
Force to break - high:	10g
- low:	5g
- avg.:	6.7g
- std. dev.:	0.9

DIE MATERIAL ANALYSIS

Overlay passivation:	Single layer of nitride.
Metallization 4:	Aluminum with a titanium adhesion layer.
Interlevel dielectrics 1, 2 and 3:	A thin layer of glass followed by two thick layers of glass.
Metallization 1 - 3: a	Aluminum with a titanium-nitride cap and probably very thin titanium adhesion layer.
Via/contact plugs (M1 - M4)	Tungsten (lined with titanium-nitride).
Pre-metal dielectric:	Thick layer of silicon-dioxide followed by a thin glass. (No reflow glass).
Polycide:	Titanium-silicide on polysilicon.
Salicide on diffusions:	Titanium-silicide.

HORIZONTAL DIMENSIONS

Die size:	13.3 x 14.6 mm (525 x 575 mils)
Die area:	195 mm^2 (301,875 $mils^2$)
Min pad size:	0.07 x 0.15 mm (3 x 5.9 mils)
Min pad window:	0.06 x 0.14 mm (2.4 x 5.3 mils)
Min pad space:	4 microns
Min metal 4 width:	1.6 micron
Min metal 4 space:	1.1 micron
Min metal 3 width:	0.6 micron
Min metal 3 space:	0.55 micron
Min metal 2 width:	0.55 micron
Min metal 2 space:	0.5 micron
Min metal 1 width:	0.4 micron
Min metal 1 space:	0.55 micron
Min via (M4-to-M3):	0.6 micron
Min via (M3-to-M2):	0.6 micron
Min via (M2-to-M1):	0.5 micron
Min contact:	0.5 micron
Min diffusion space:	0.4 micron
Min polycide width:	0.25 micron
Min polycide space:	0.5 micron
Min gate length* - (N-channel):	0.25 micron
- (P-channel):	0.25 micron
Min gate-to-contact space:	0.3 micron
SRAM cell size:	19.7 $microns^2$
SRAM cell pitch:	4.1 x 4.8 microns

*****_Physical gate length_

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (20 mils)

Layers:

Passivation:	0.7 micron
Metal 4 - aluminum:	1.7 micron
- barrier:	0.1 micron
- plugs:	0.9 micron (not including "stub")
Interlevel dielectric 3 - glass 3:	0.45 - 1.4 micron
- glass 2:	0.4 micron
- glass 1:	0.1 micron
Metal 3 - cap:	0.05 micron (approximate)
- aluminum:	0.75 micron
- plugs:	0.7 micron (not including "stub")
Interlevel dielectric 2 - glass 3:	0.4 - 1.3 micron
- glass 2:	0.35 micron
- glass 1:	0.1 micron
Metal 2 - cap:	0.05 micron (approximate)
- aluminum:	0.8 micron
- plugs:	0.6 micron (not including "stub")
Interlevel dielectric 1 - glass 3:	0.2 - 0.9 micron
- glass 2:	0.25 micron
- glass 1:	0.1 micron
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.55 micron
- plugs:	0.55 - 0.85 micron
Pre-metal glass - glass 2:	0.13 micron
- glass 1:	0.3 - 0.7 micron
Polycide - silicide:	0.07 micron (approximate)
- poly:	0.27 micron
Trench oxide:	0.4 micron
N+ S/D:	0.2 micron
P+ S/D:	0.25 micron
N-well:	0.8 micron (approximate)
P-epi:	1.6 micron

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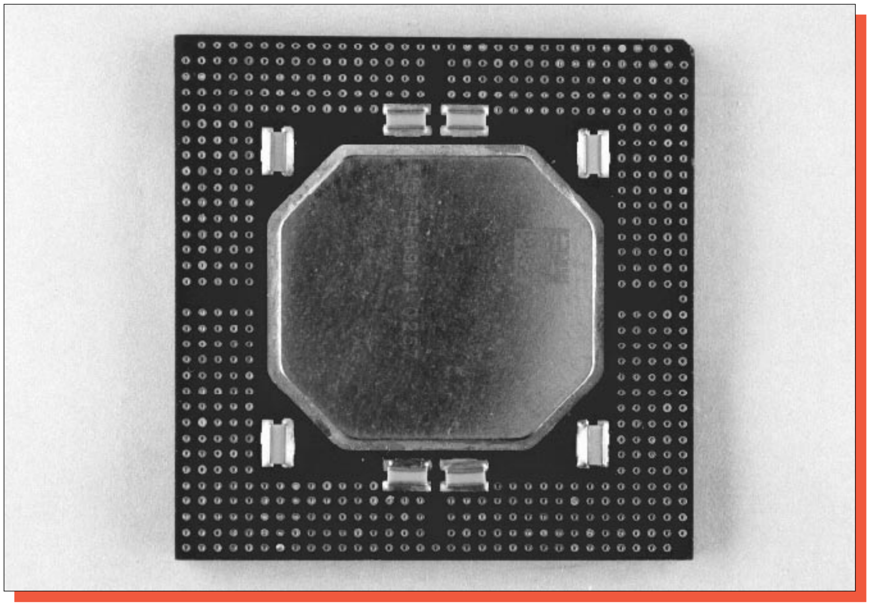
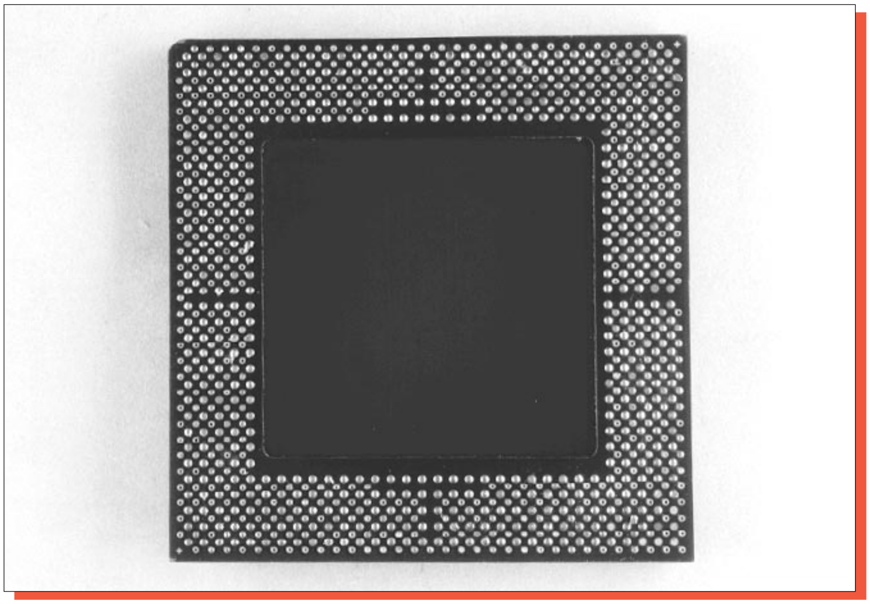
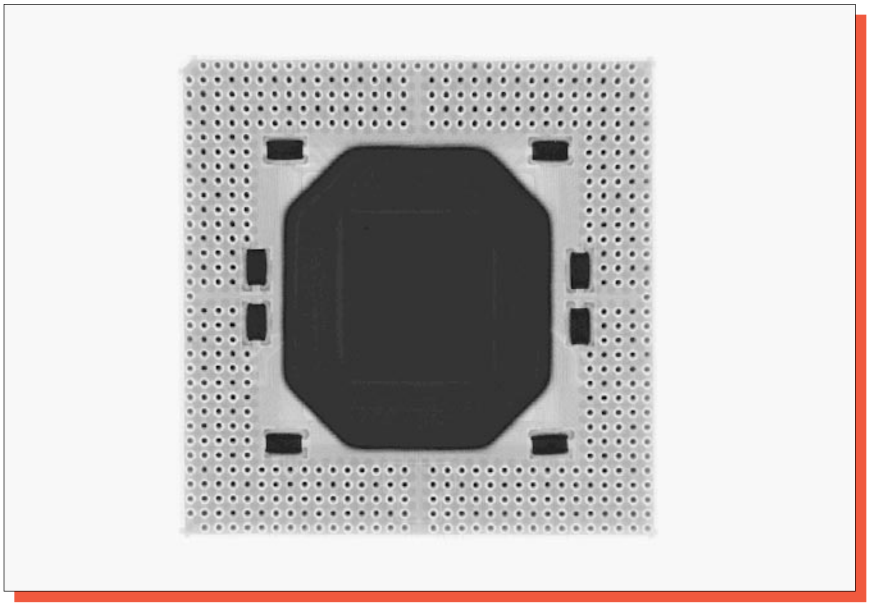


Mag. 1.3x

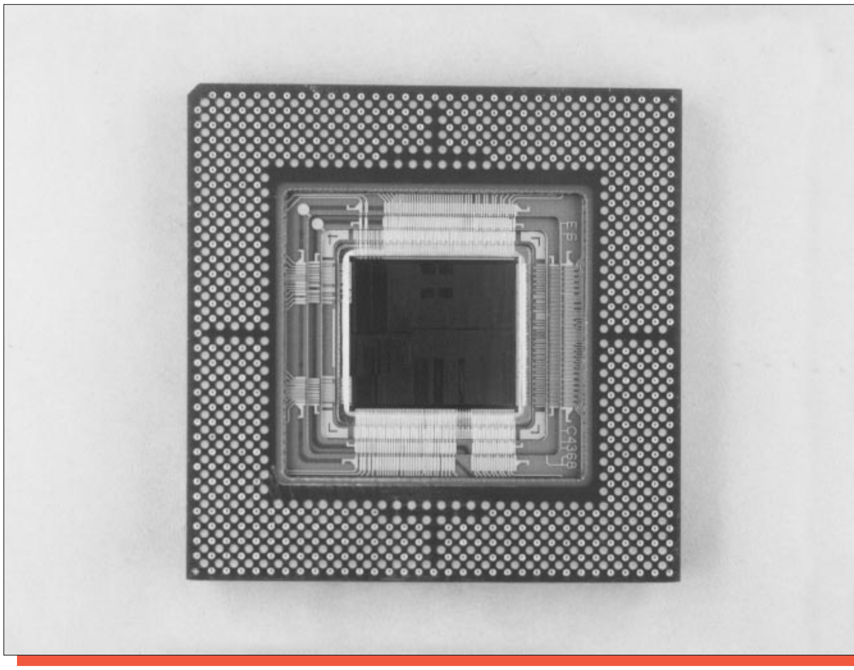


Mag. 1.3x

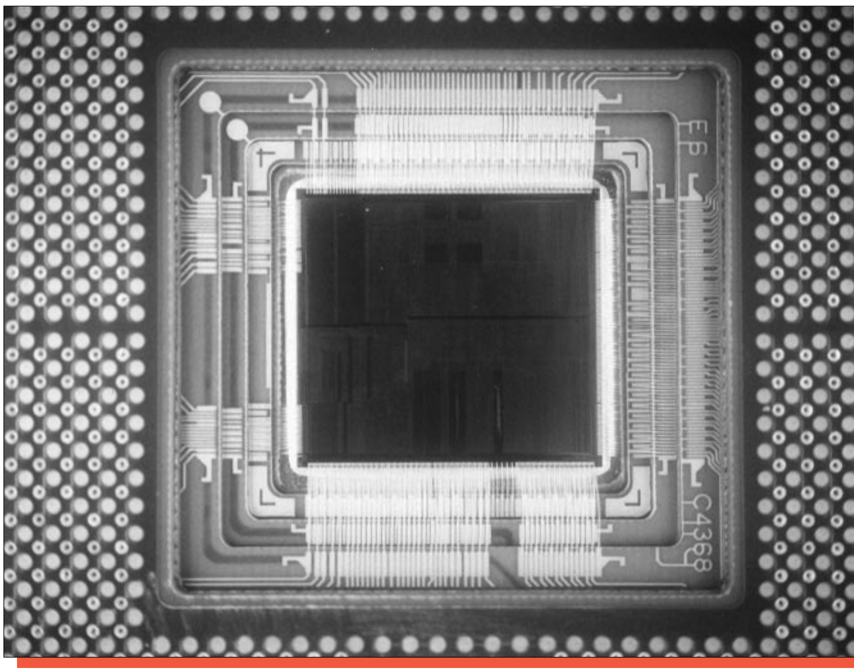


Mag. 1.2x

Figure 1. Package photographs and x-ray view of the Intel Pentium II Processor.

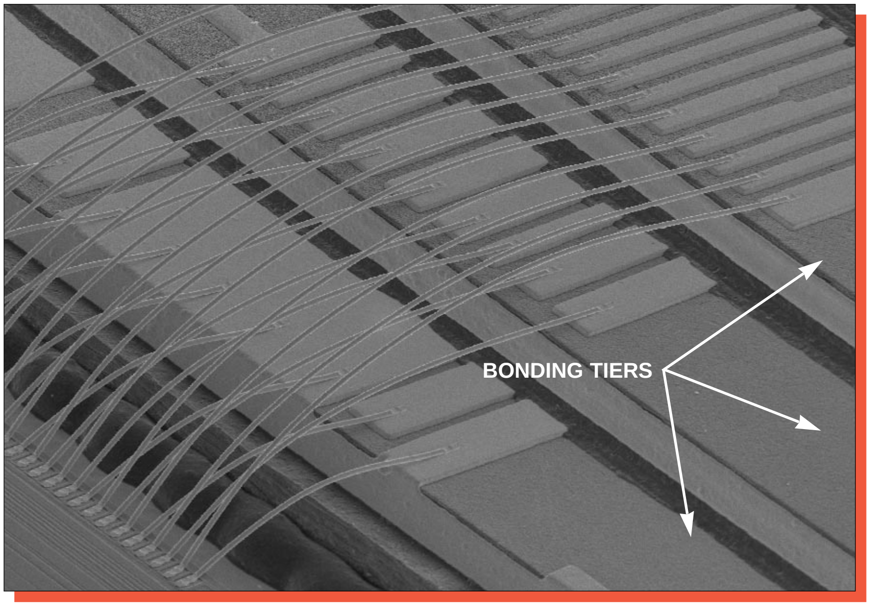


Mag. 1.25x

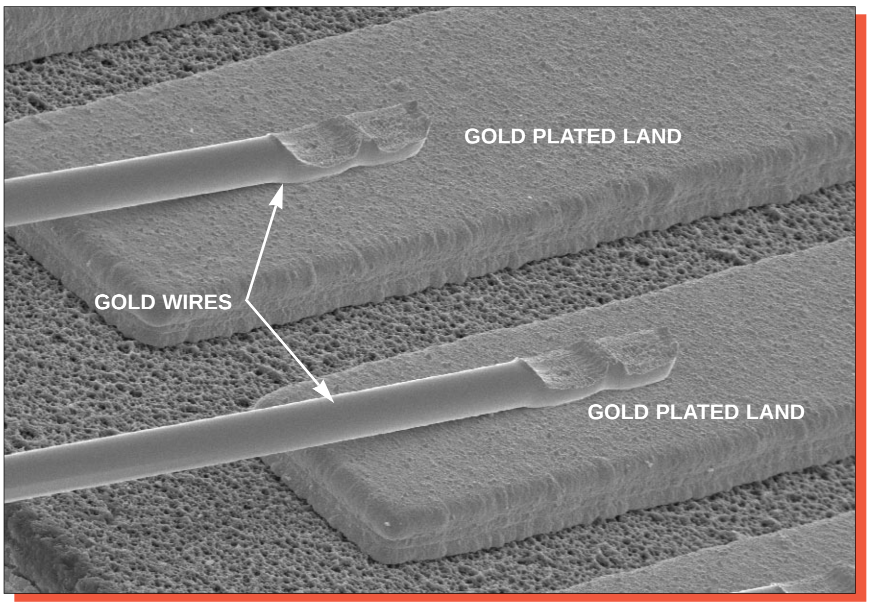


Mag. 3x

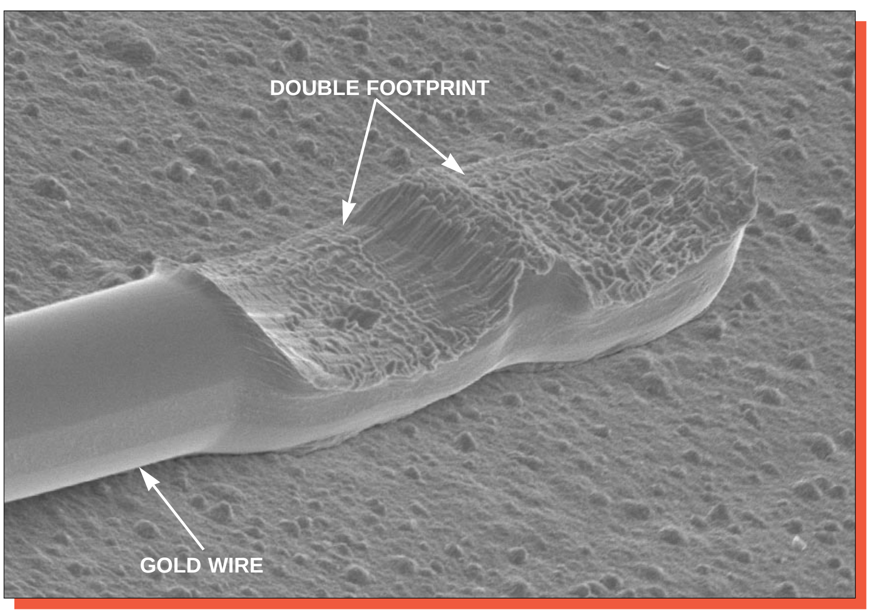
Figure 2. Cavity views of the package.



Mag. 30x

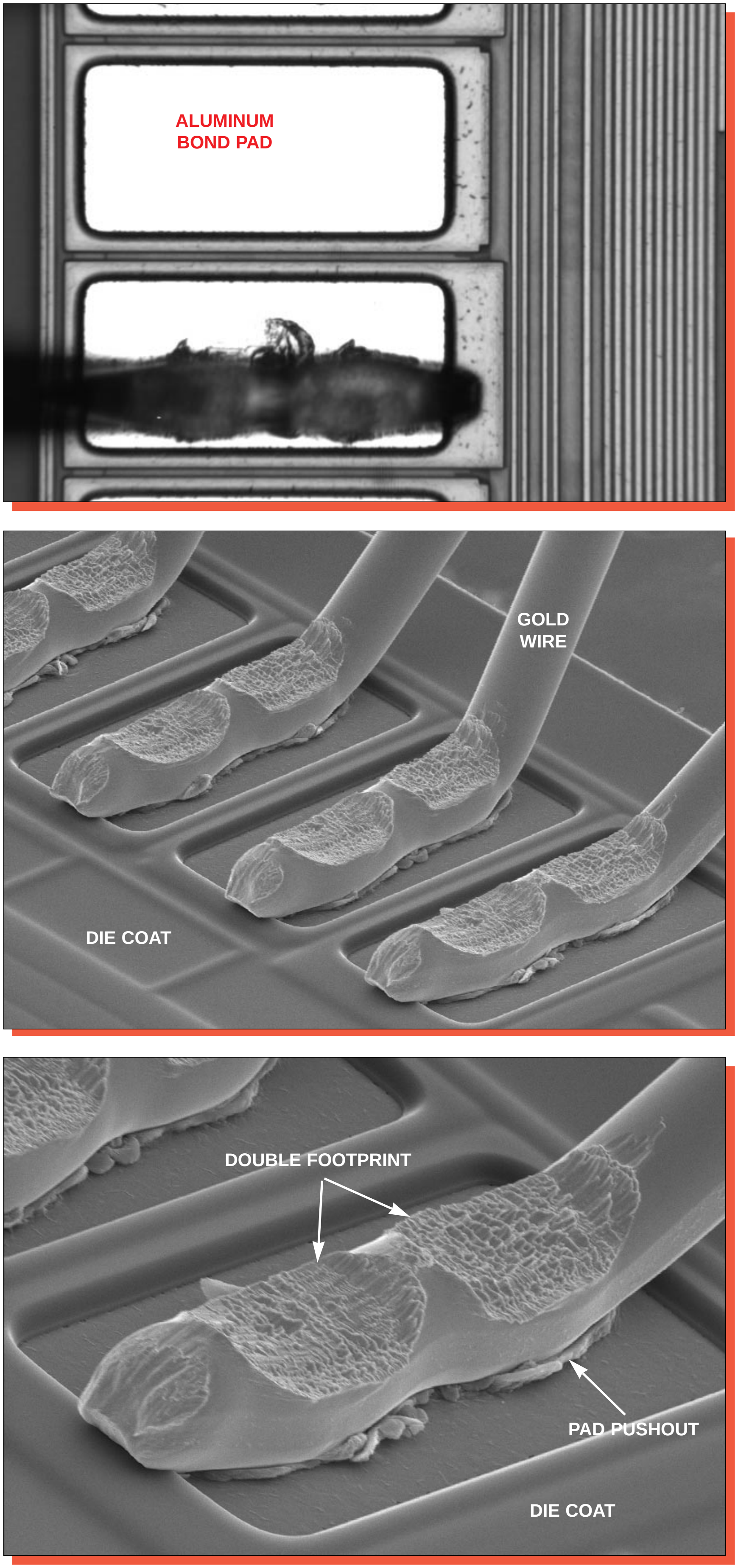


Mag. 260x



Mag. 1000x

Figure 3. SEM views of typical wirebonding. 60°.

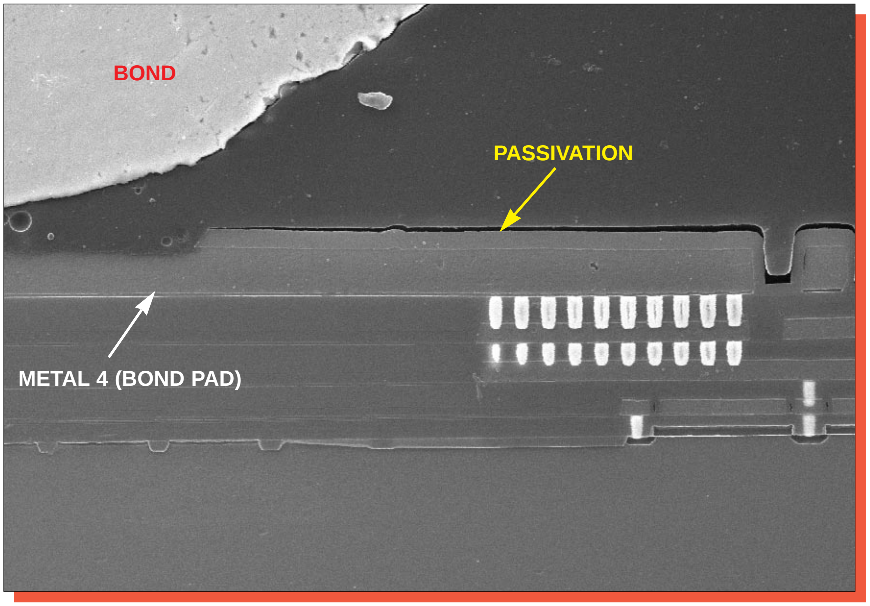


Mag. 410x

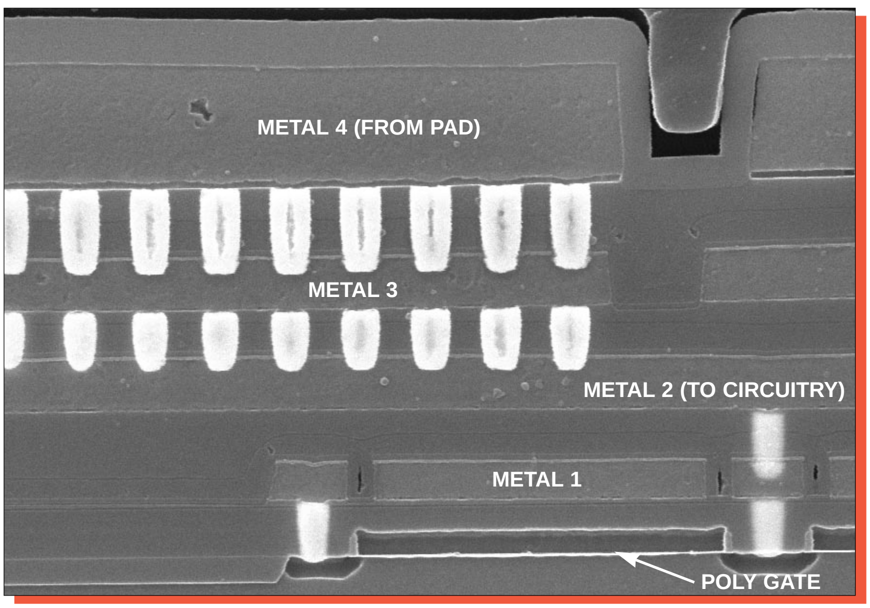
Mag. 500x, 60°

Mag. 1000x, 60°

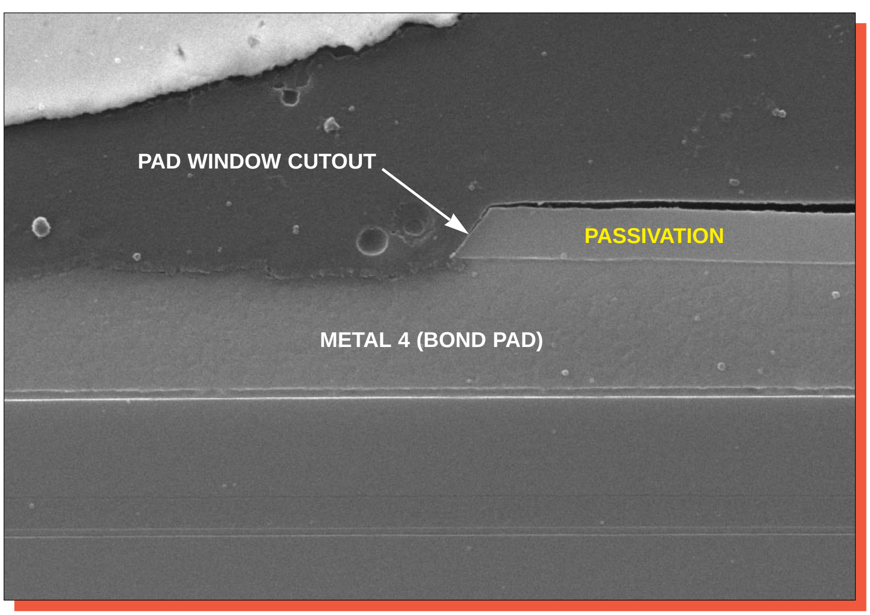
Figure 4. Optical and SEM views illustrating bond pad pitch and typical bonds.



Mag. 3500x



Mag. 9000x



Mag. 10,000x

Figure 5. SEM section views of the pad structure.

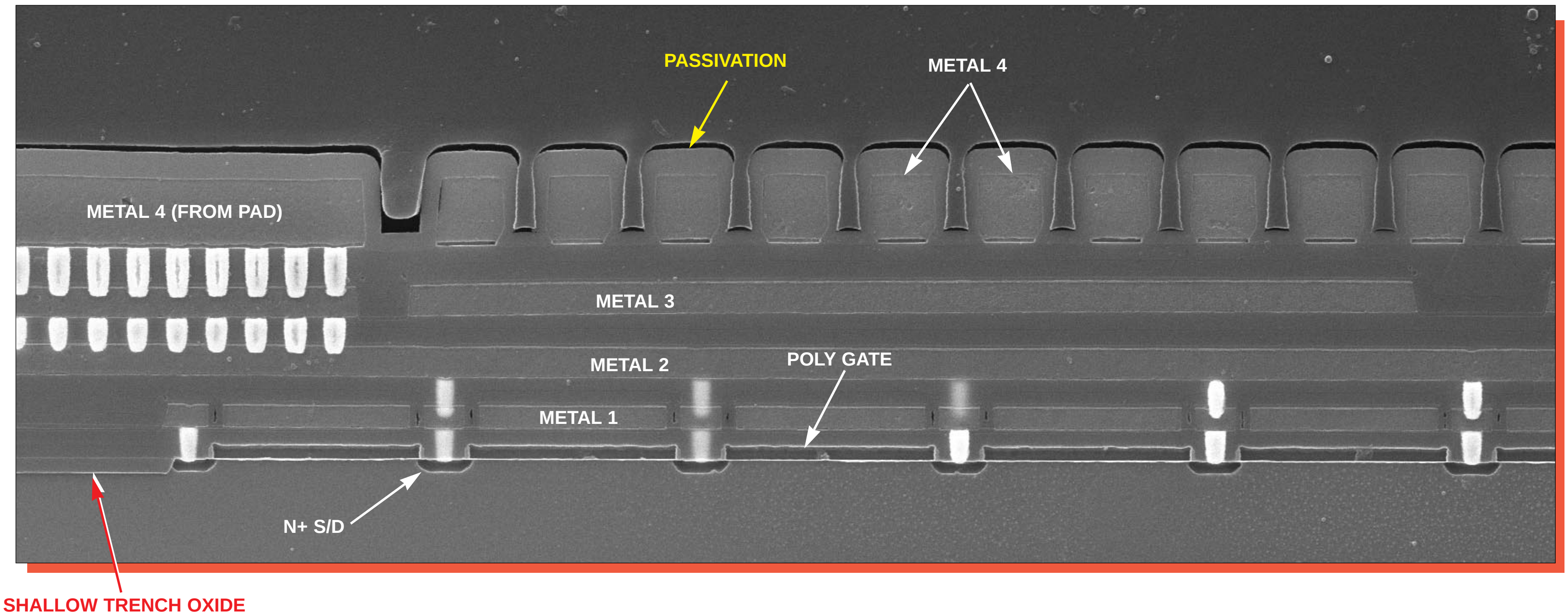
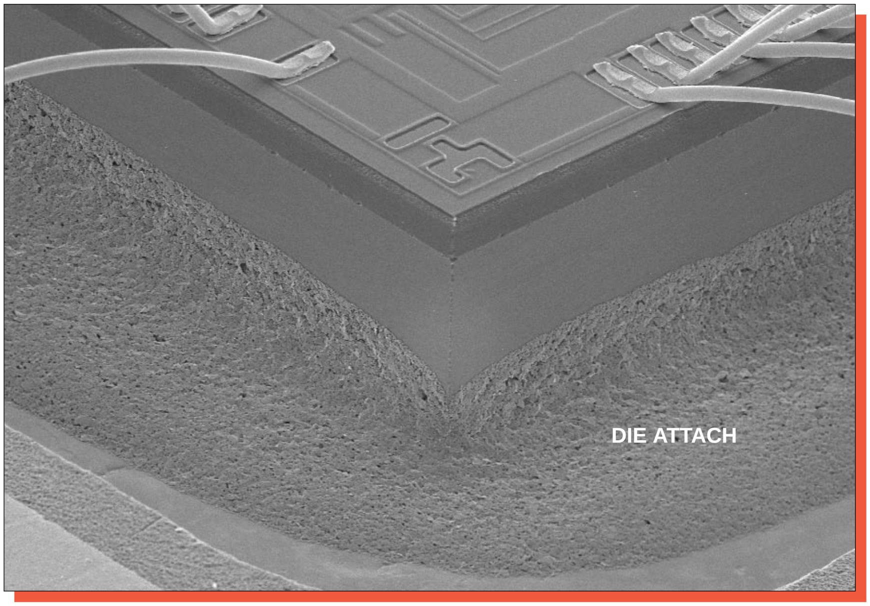
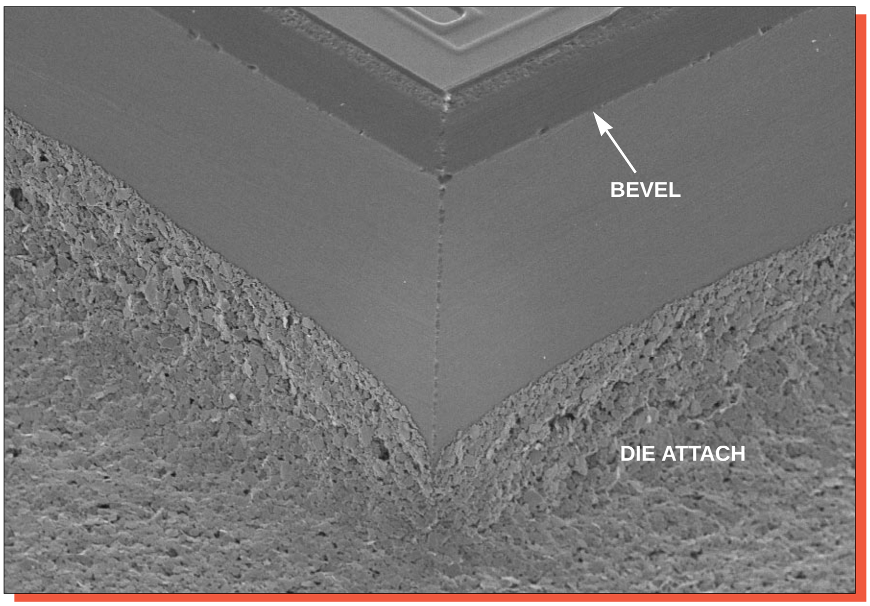


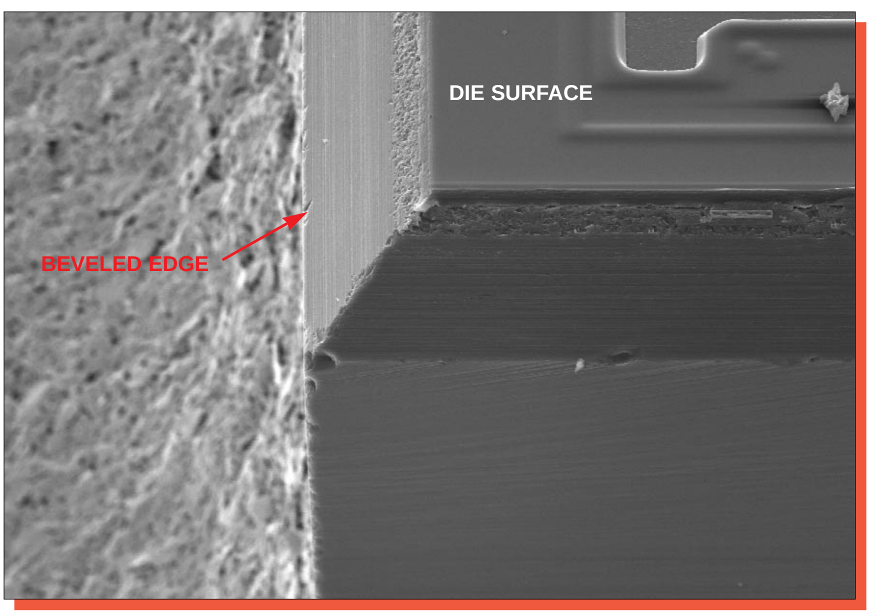
Figure 6. SEM section views of an I/O structure. Mag. 6000x.



Mag. 80x

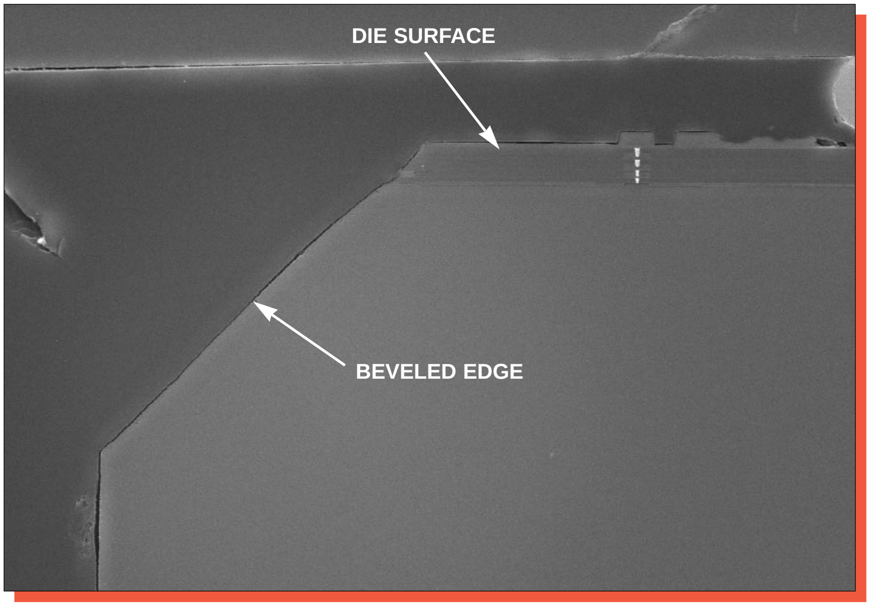


Mag. 160x

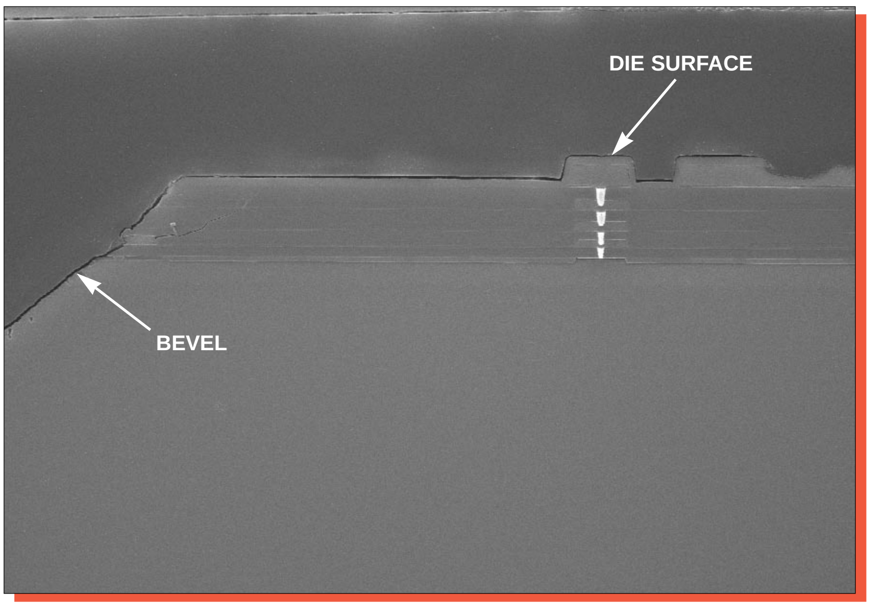


Mag. 350x

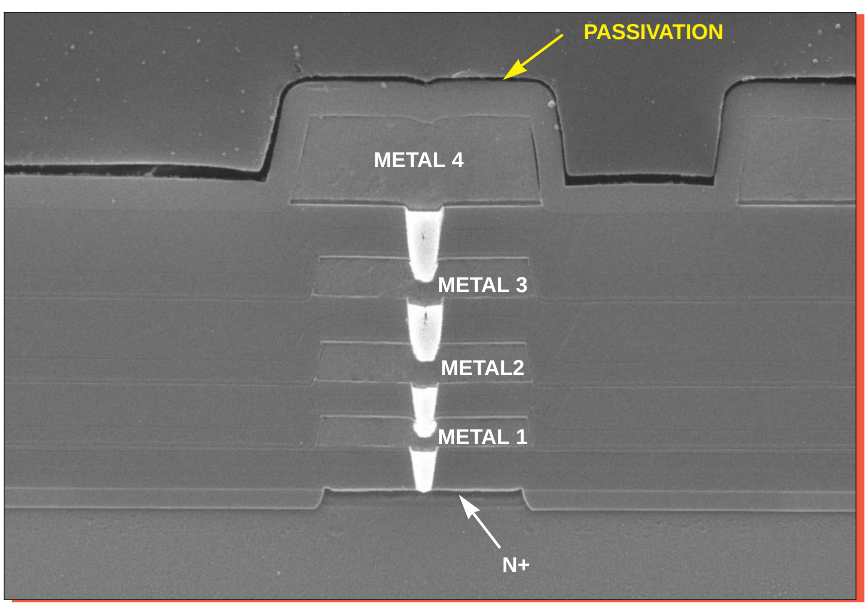
Figure 7. SEM views of a die corner illustrating dicing and die attach. 60°.



Mag. 800x



Mag. 1600x



Mag. 6500x

Figure 8. SEM section views of the edge seal structure.

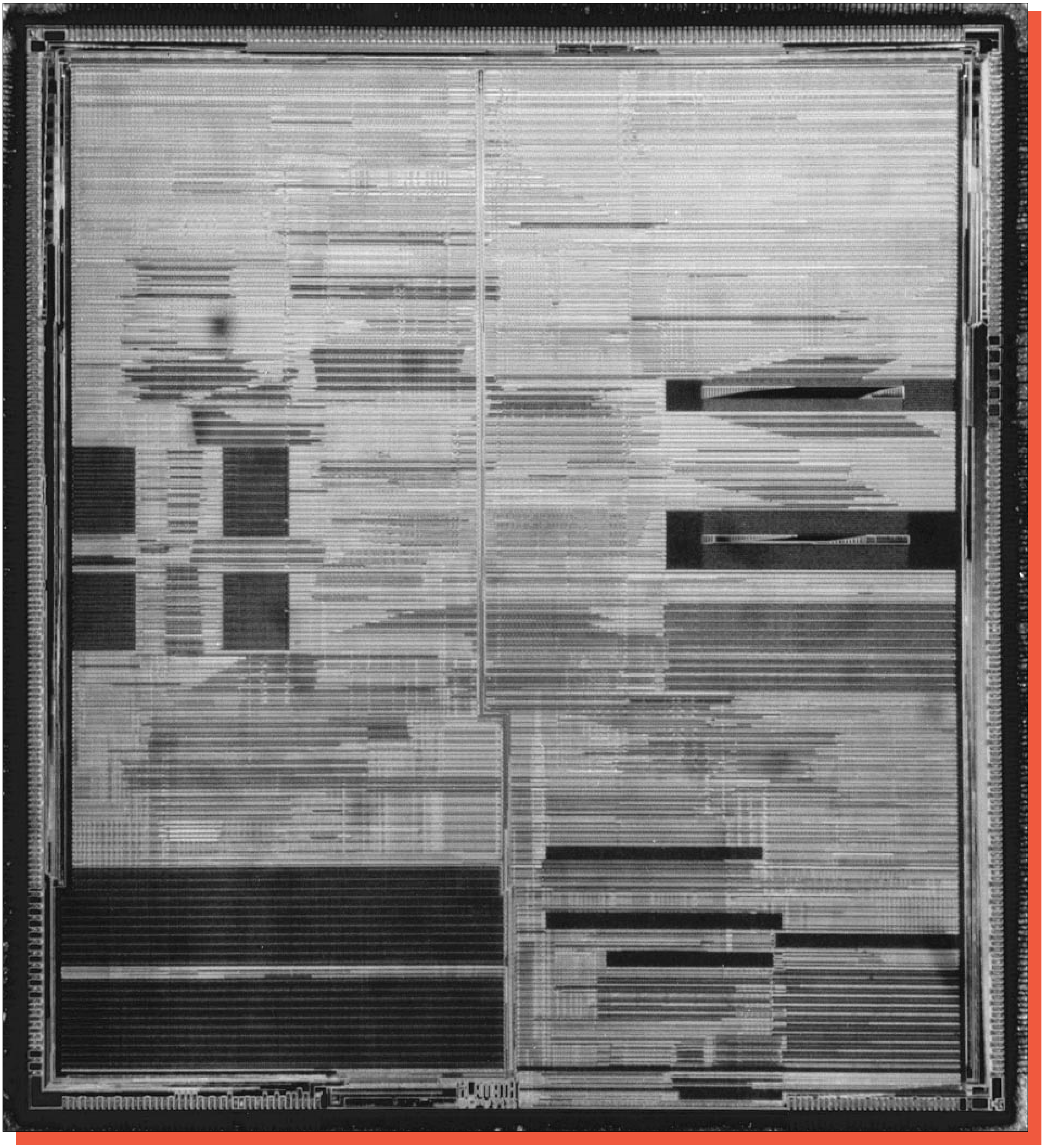


Figure 9. Whole die photograph of the Intel Pentium II Processor. Mag 14x.

Figure 10. Die identification markings. Mag. 100x.

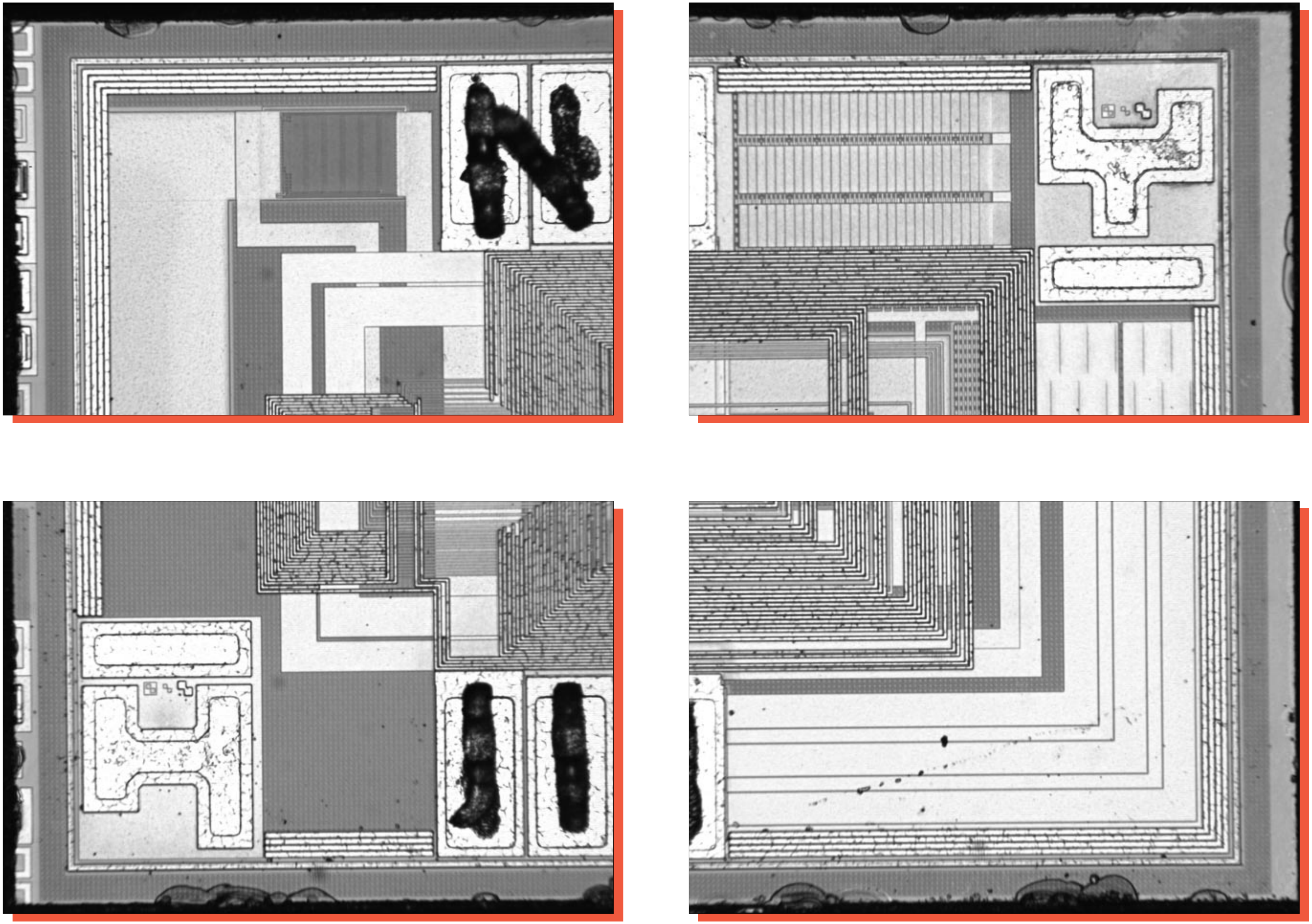


Figure 11. Optical views of die corners. Mag. 225x.

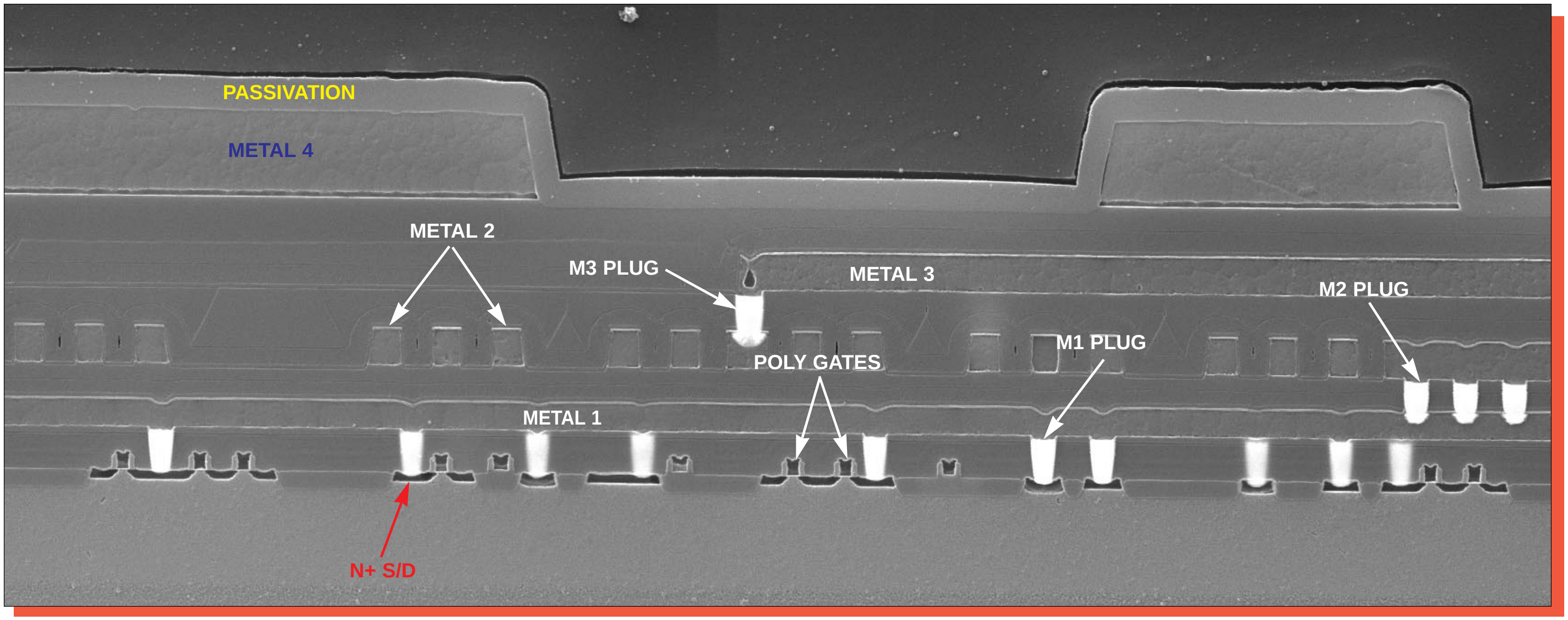
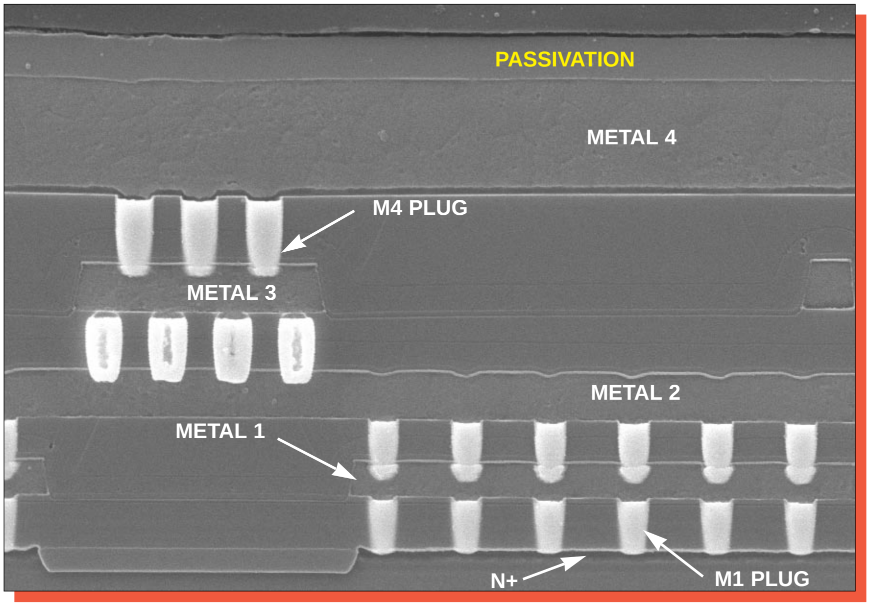
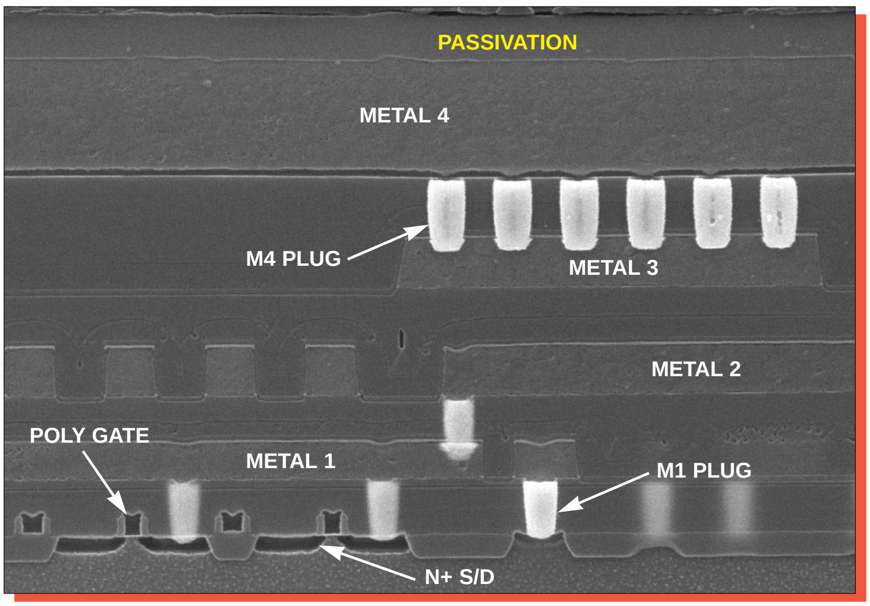


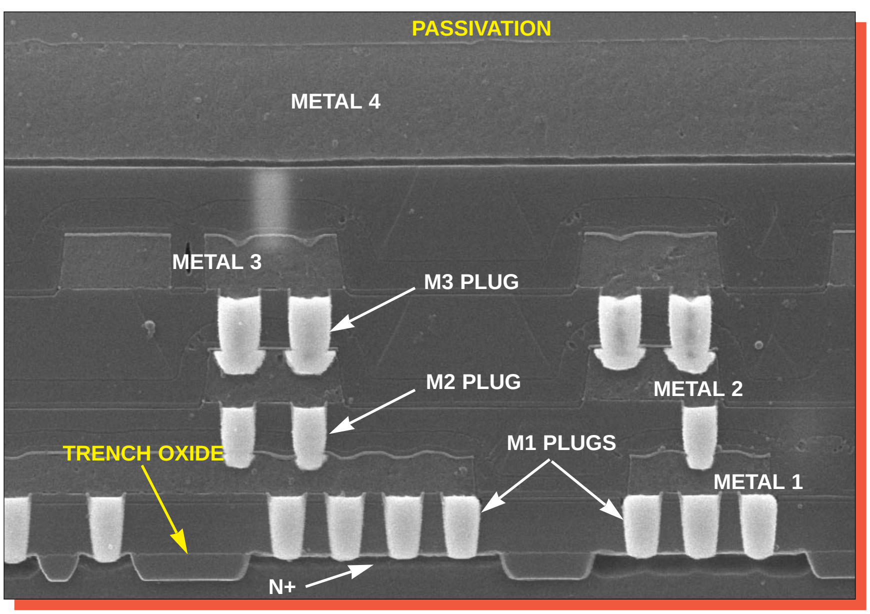
Figure 12. SEM section view illustrating general device structure. Mag. 6500x.



Mag. 8000x



Mag. 8400x



Mag. 9000x

Figure 12a. SEM section views illustrating general device structure.

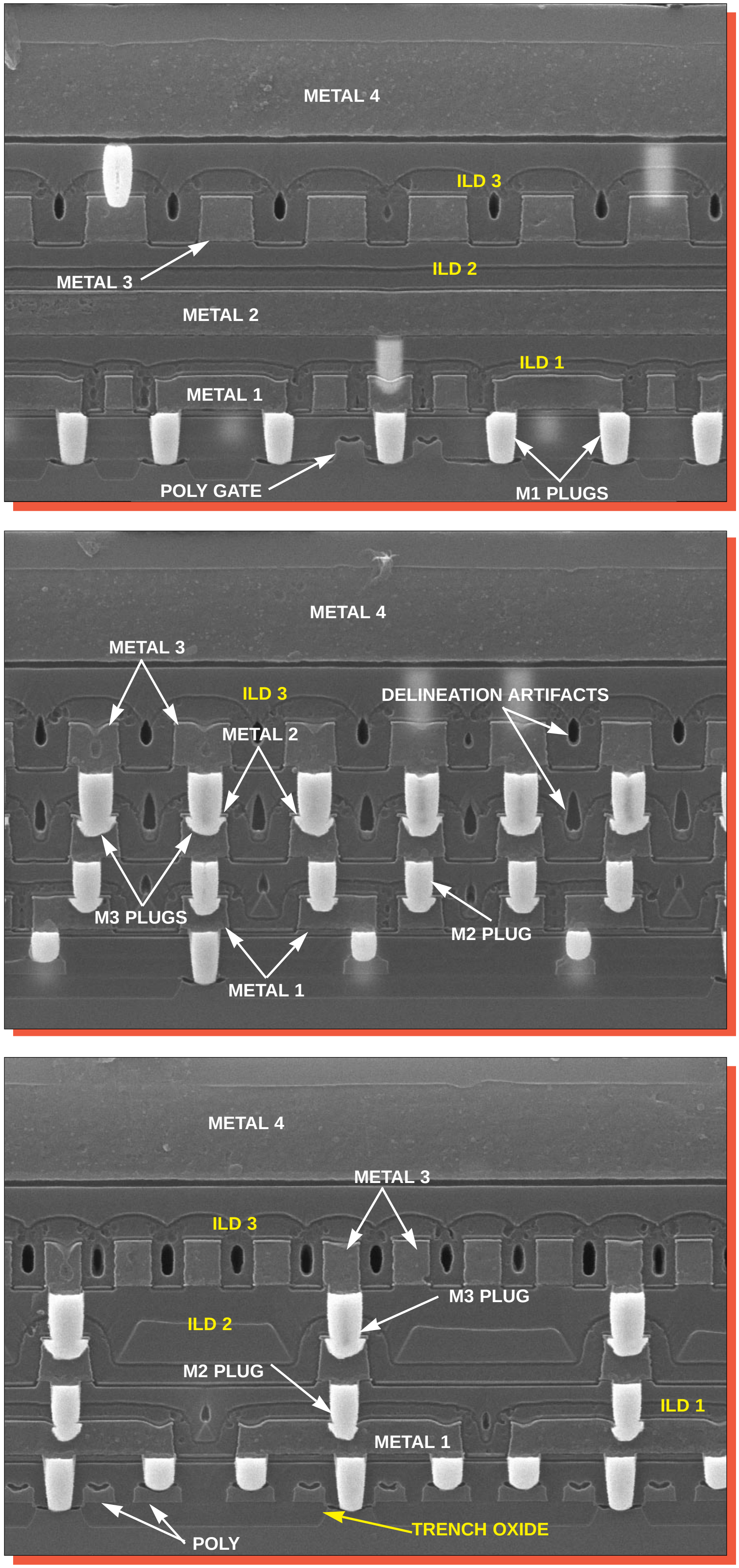
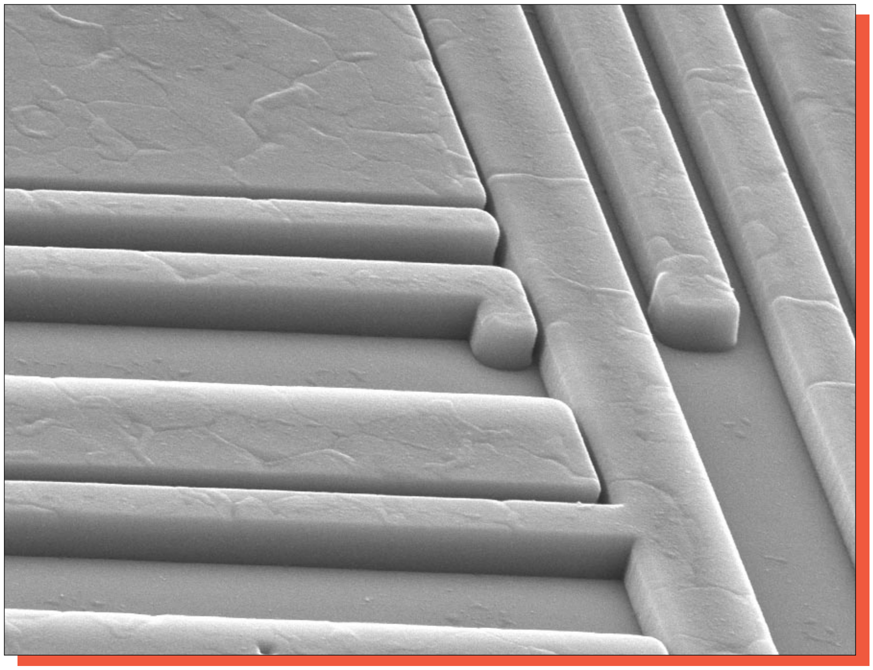
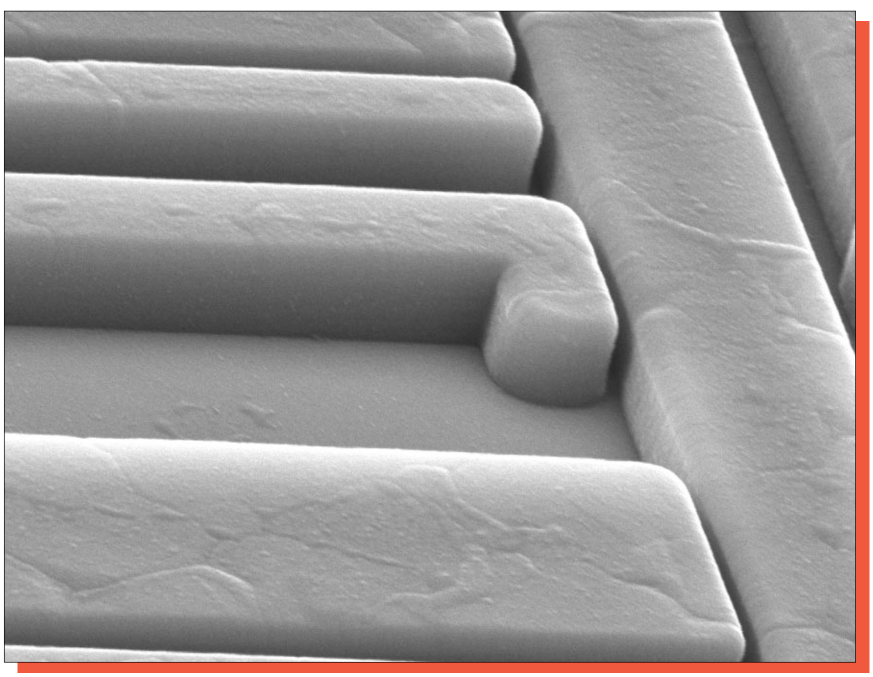


Figure 13. Glass etch section views illustrating general structure. Mag. 9000x.

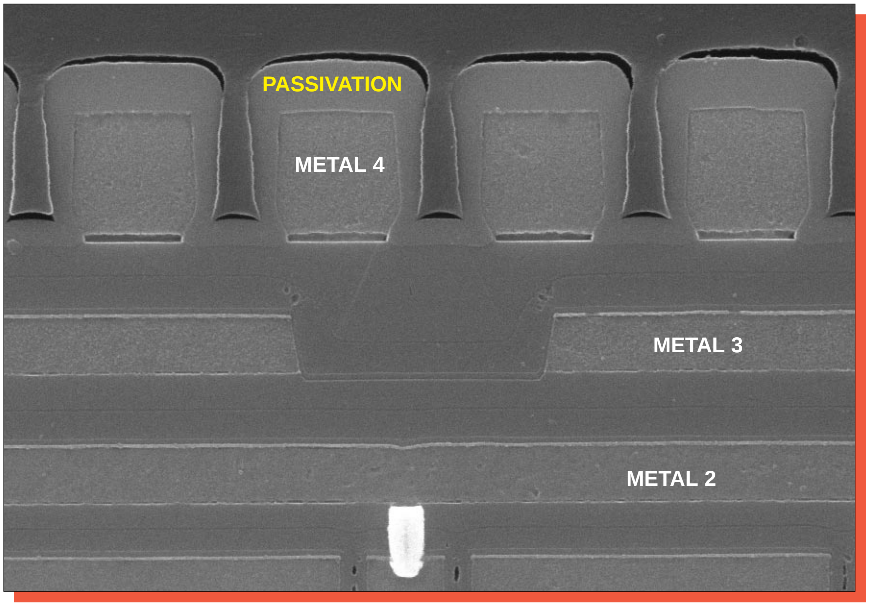


Mag. 2800x

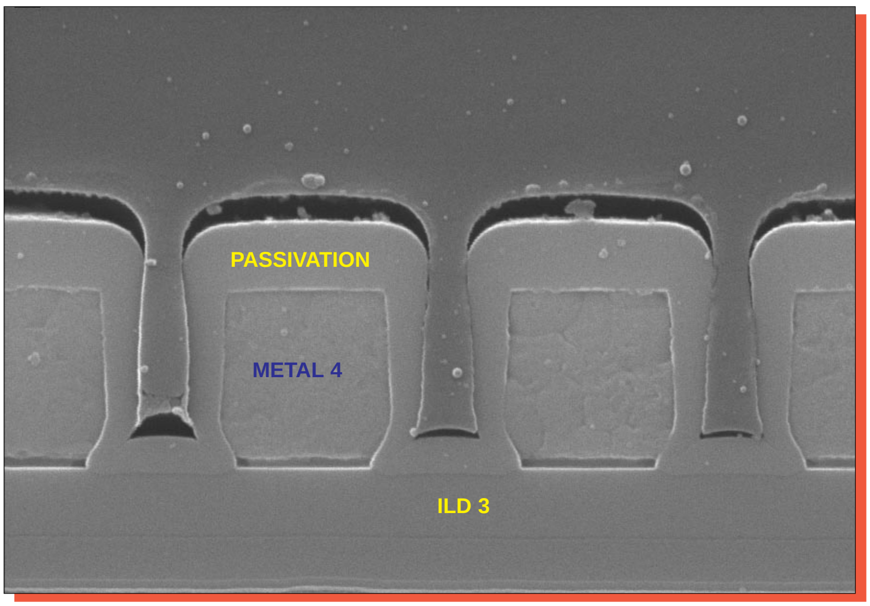


Mag. 5700x

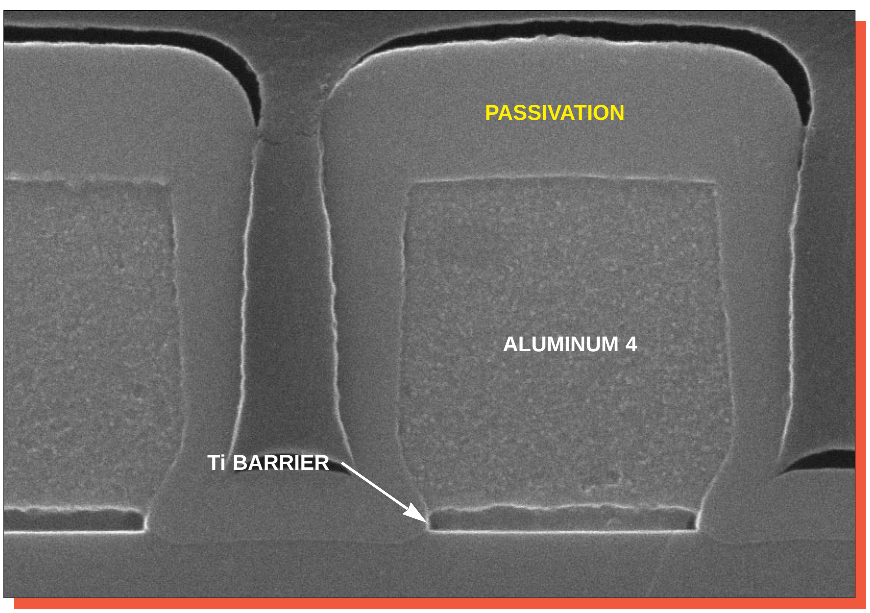
Figure 14. SEM views of general passivation coverage. 60°.



Mag. 10,000x



Mag. 13,000x



Mag. 26,000x

Figure 15. SEM section views of metal 4 line profiles.

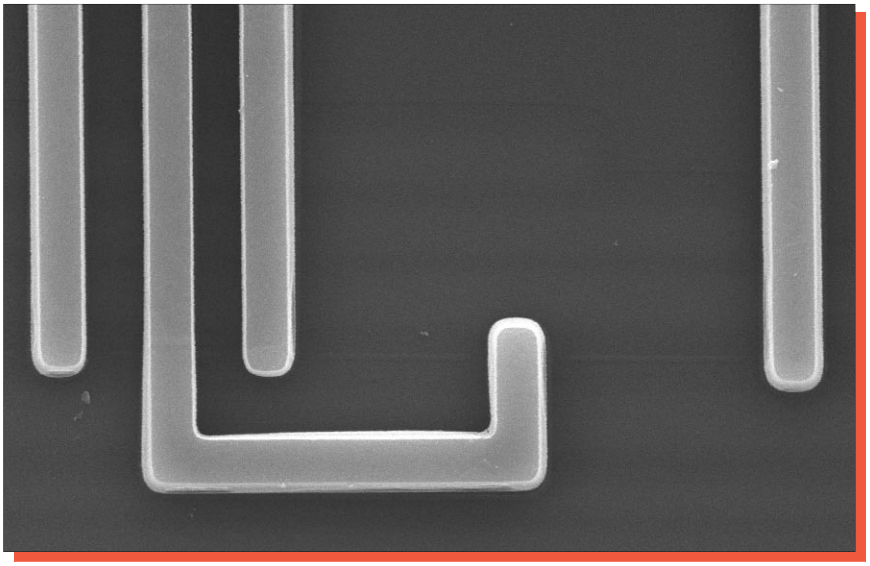
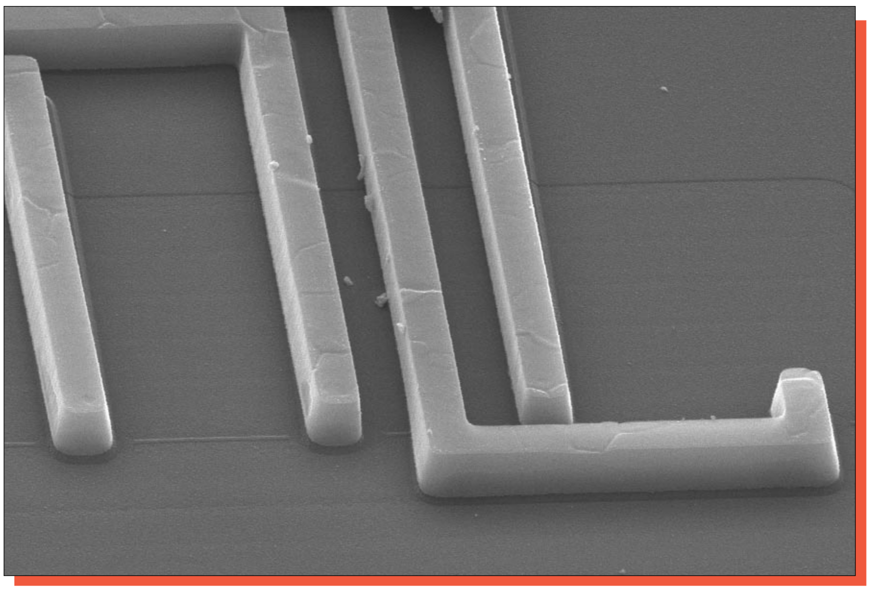
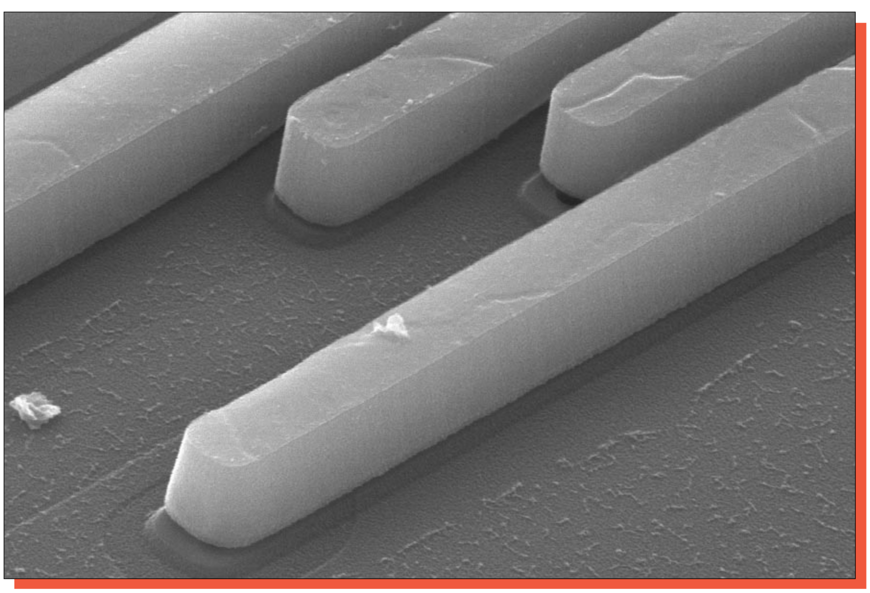


Figure 16. Topological SEM view of metal 4 patterning. Mag. 3700x, 0°.

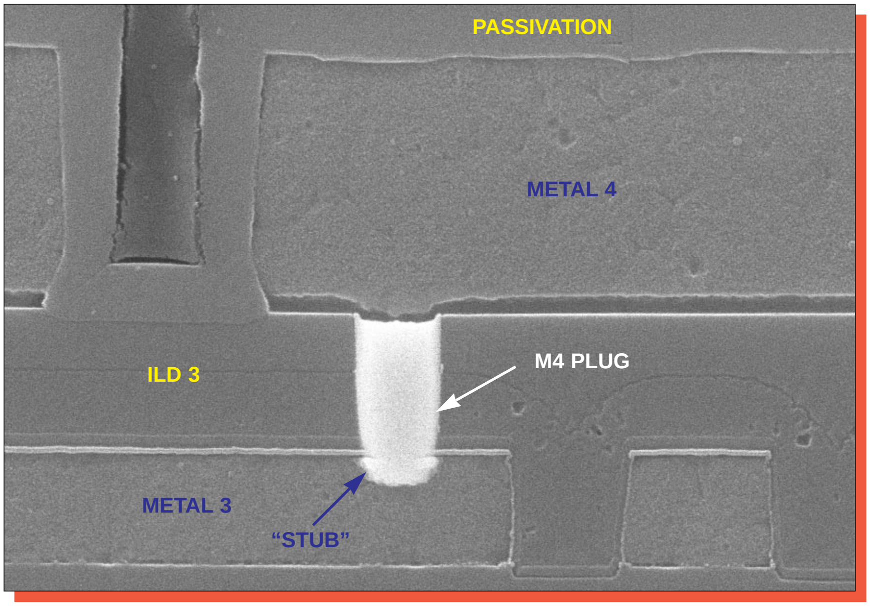


Mag. 3700x

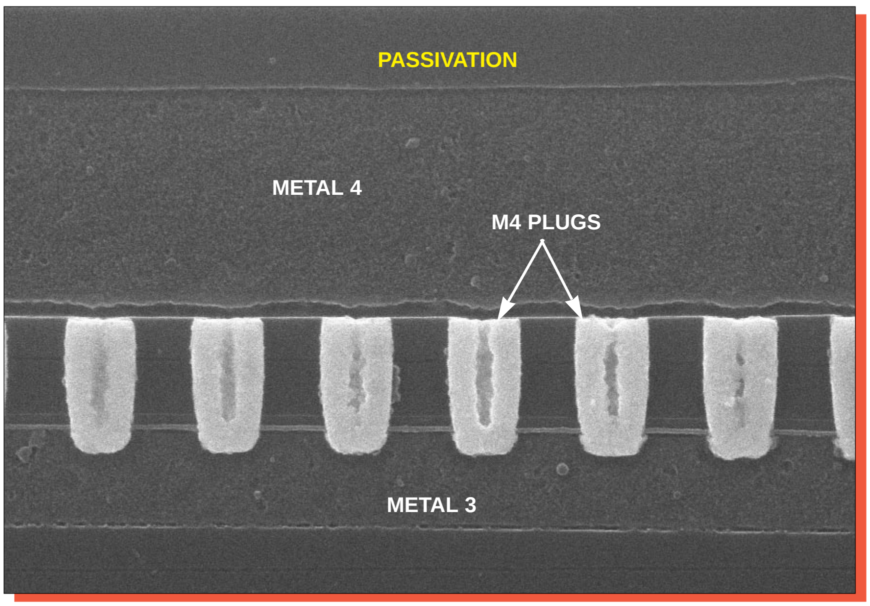


Mag. 7400x

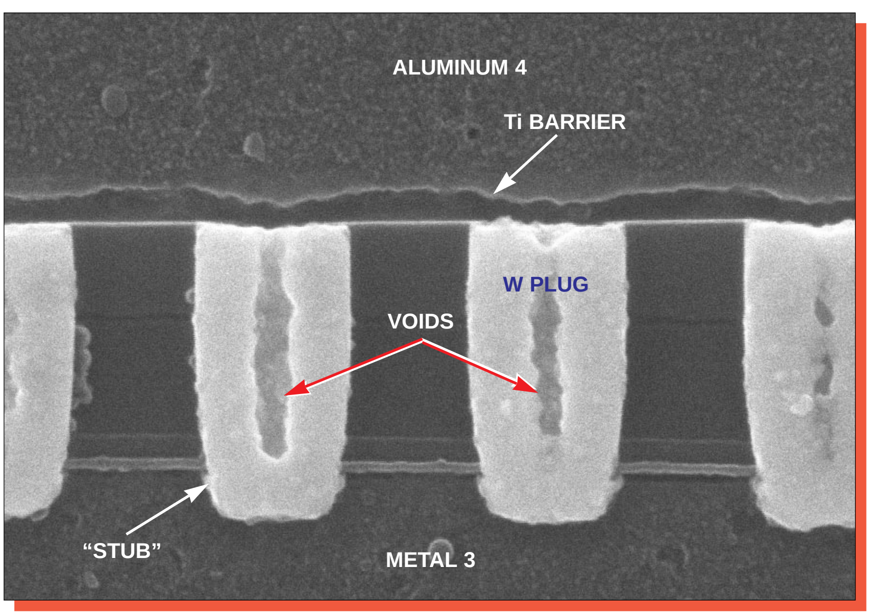
Figure 17. SEM views of general metal 4 coverage. 50°.



Mag. 20,000x

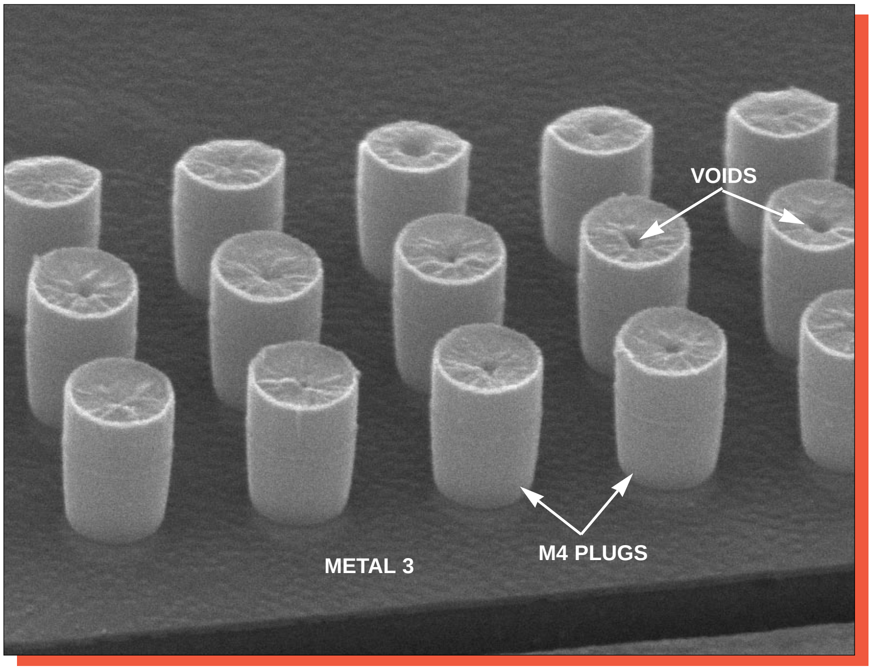


Mag. 15,000x

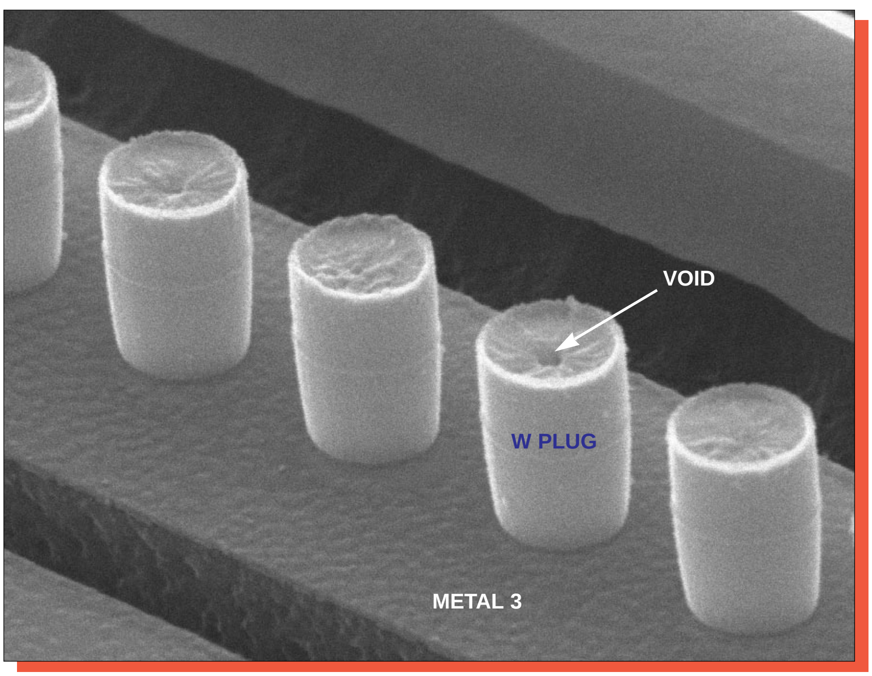


Mag. 35,000x

Figure 18. SEM section views of metal 4-to-metal 3 vias.

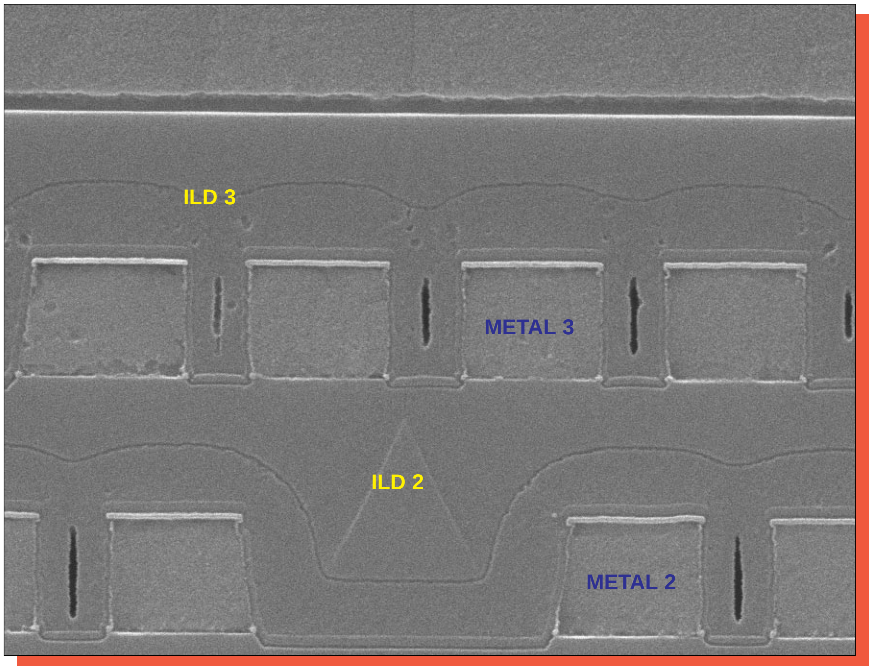


Mag. 25,000x

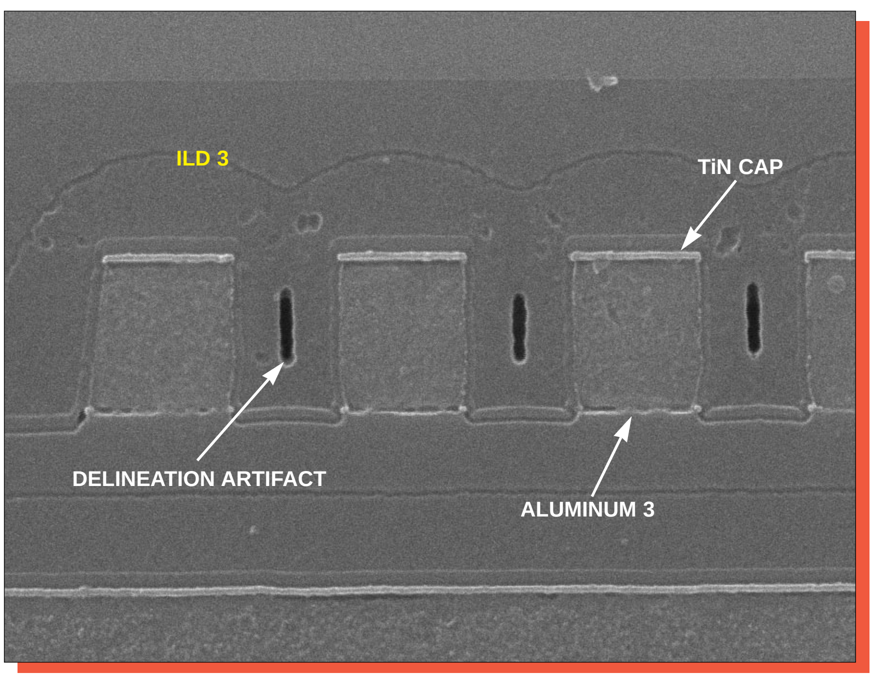


Mag. 35,000x

Figure 19. SEM section views of metal 4 plugs. 55°.

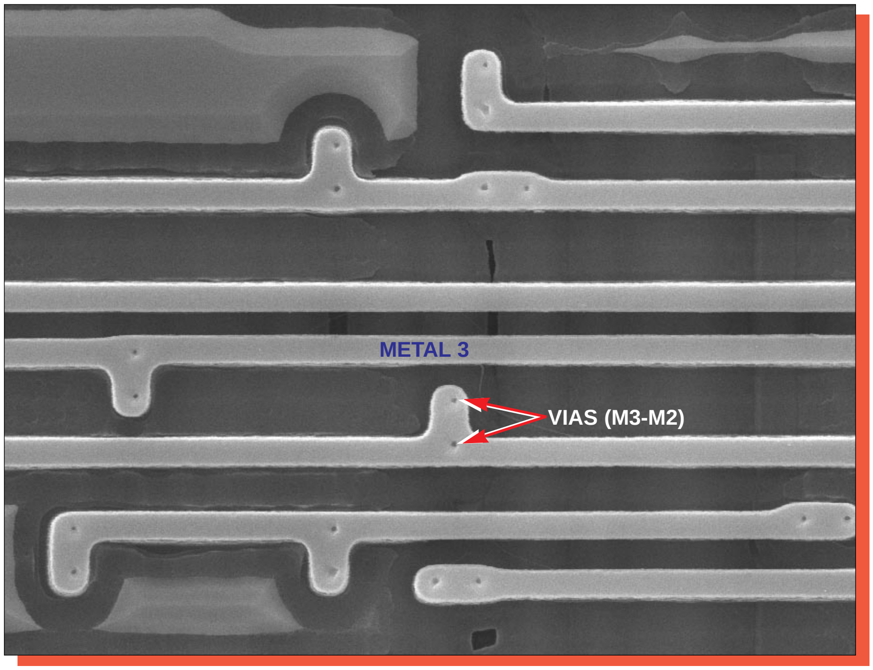


Mag. 20,000x

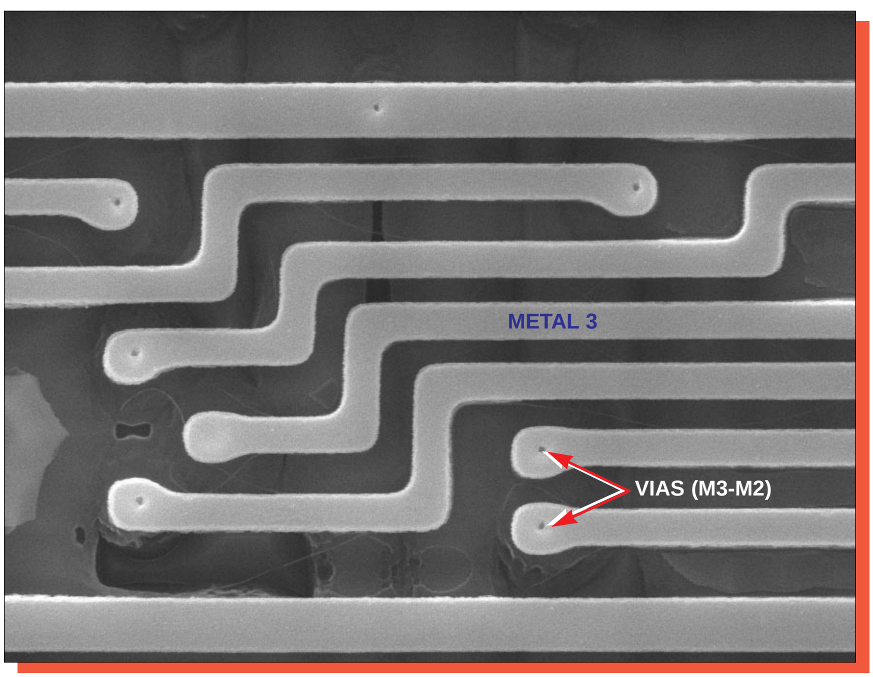


Mag. 26,000x

Figure 20. SEM section views of metal 3 line profiles.

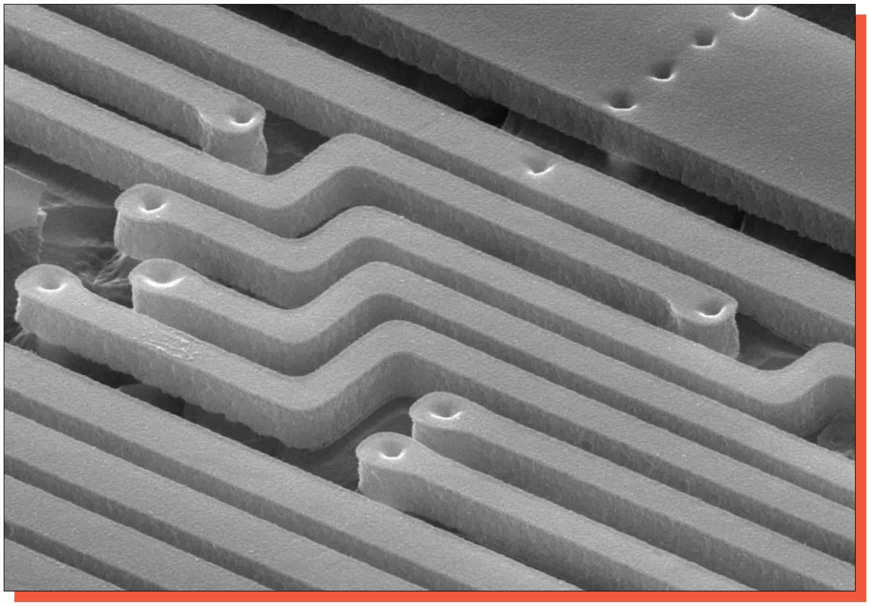


Mag. 6000x

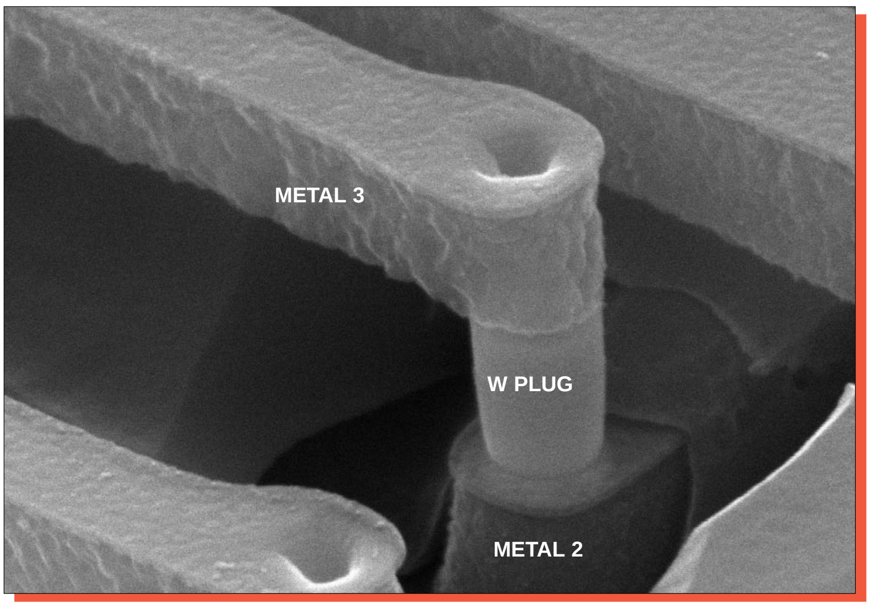


Mag. 8000x

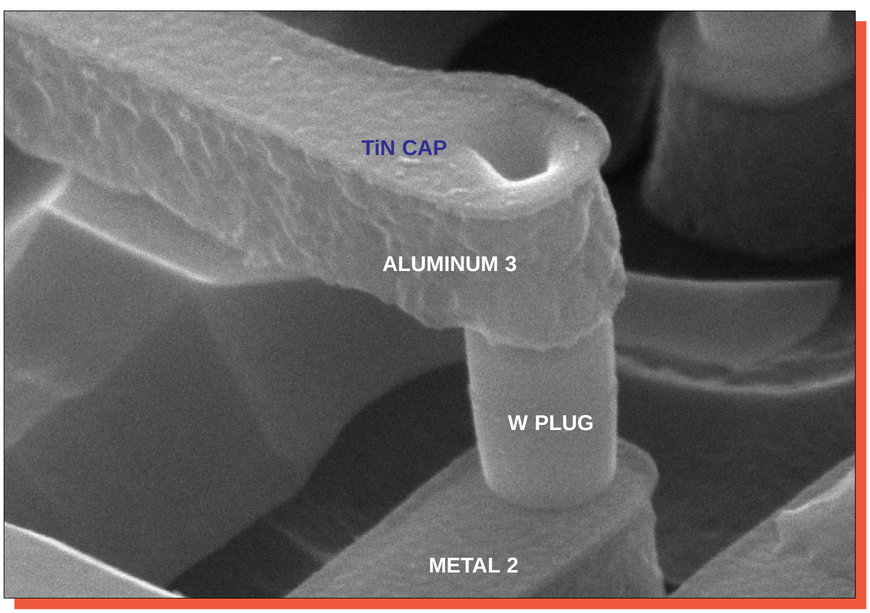
Figure 21. Topological SEM views of metal 3 patterning. 0°.



Mag. 9000x

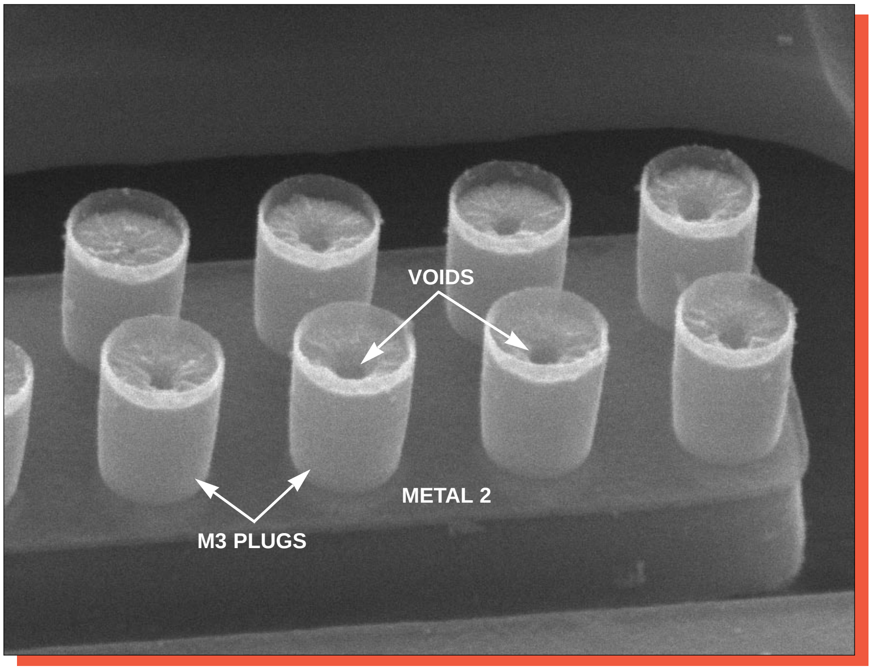


Mag. 30,000x

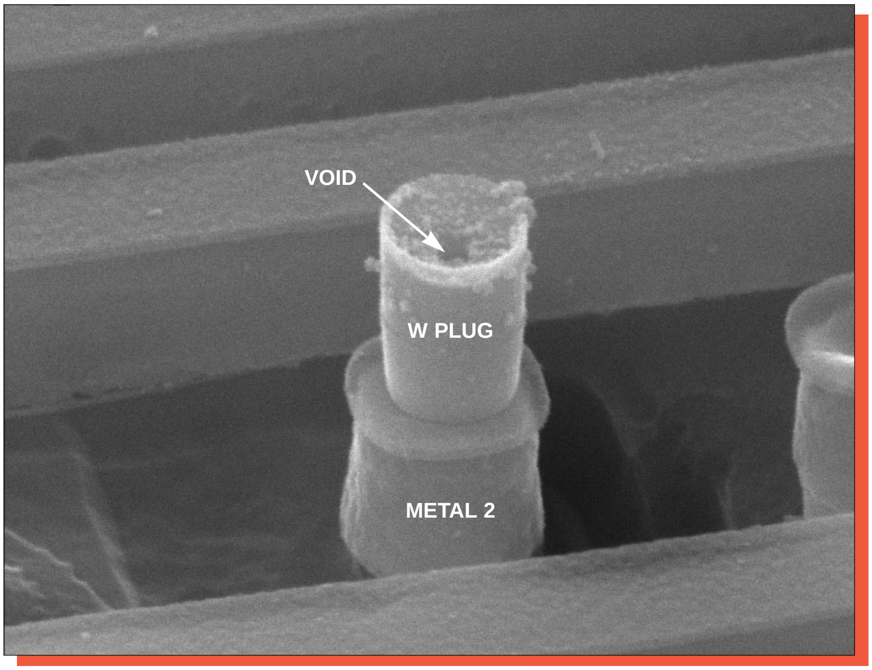


Mag. 34,000x

Figure 22. SEM views of metal 3 coverage. 55°.

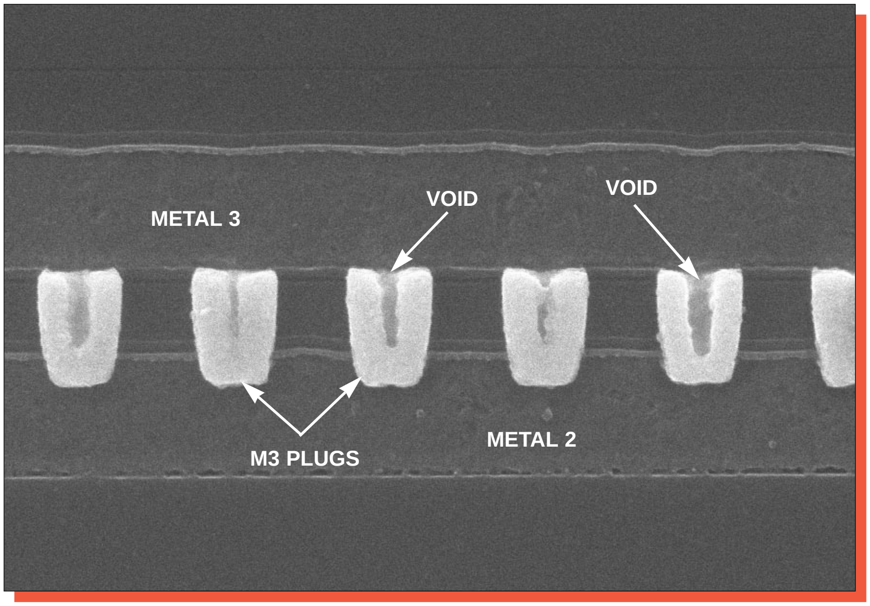


Mag. 27,000x

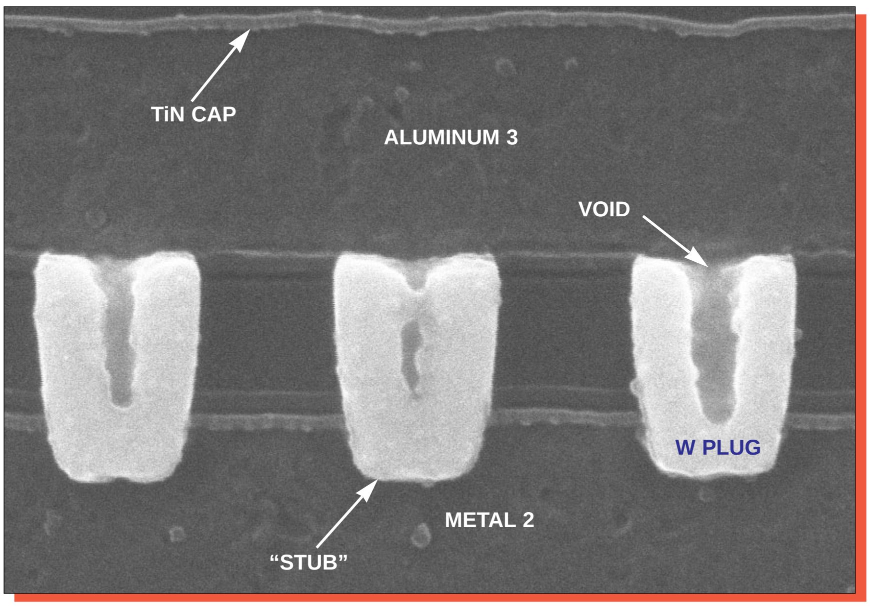


Mag. 35,000x

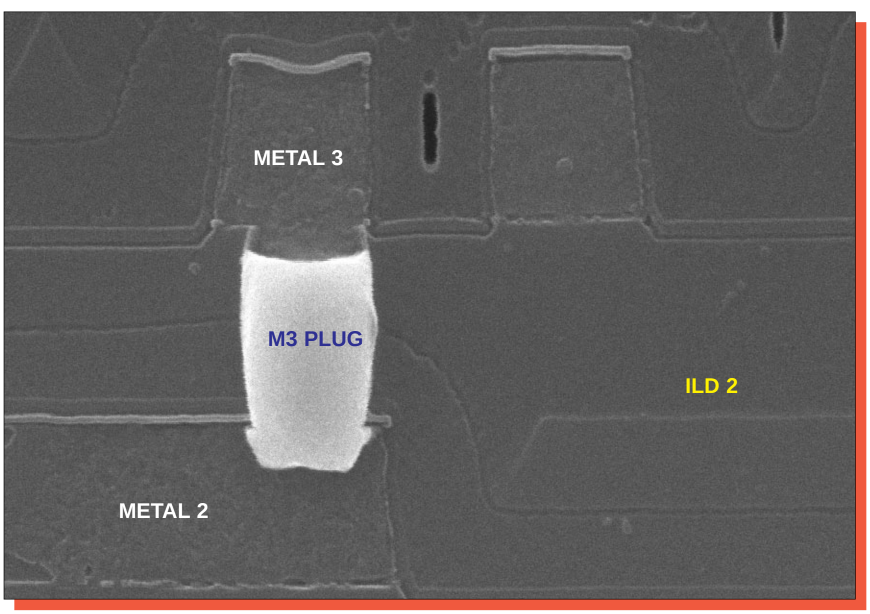
Figure 23. SEM views of metal 3 plugs. 50°.



Mag. 20,000x

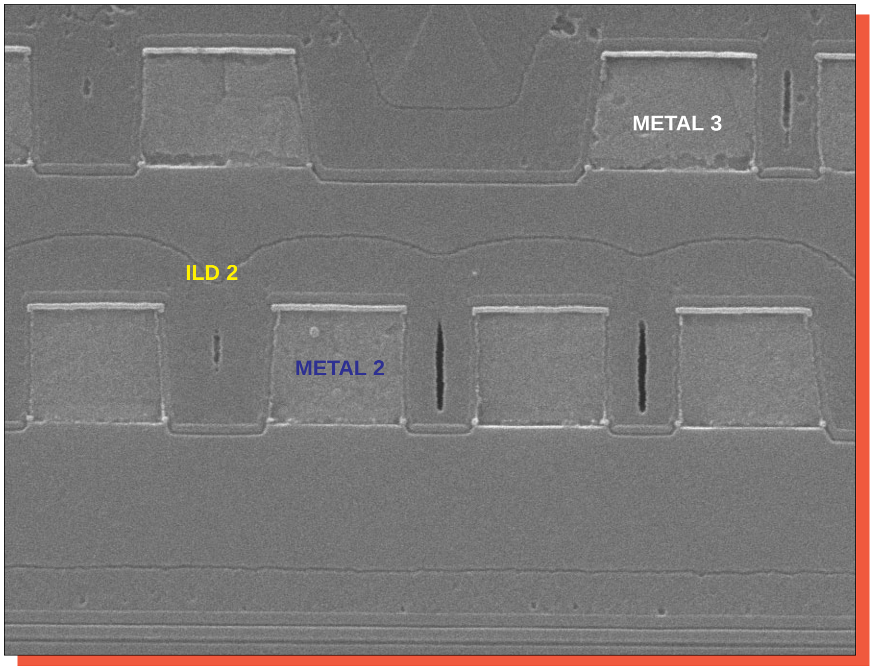


Mag. 40,000x

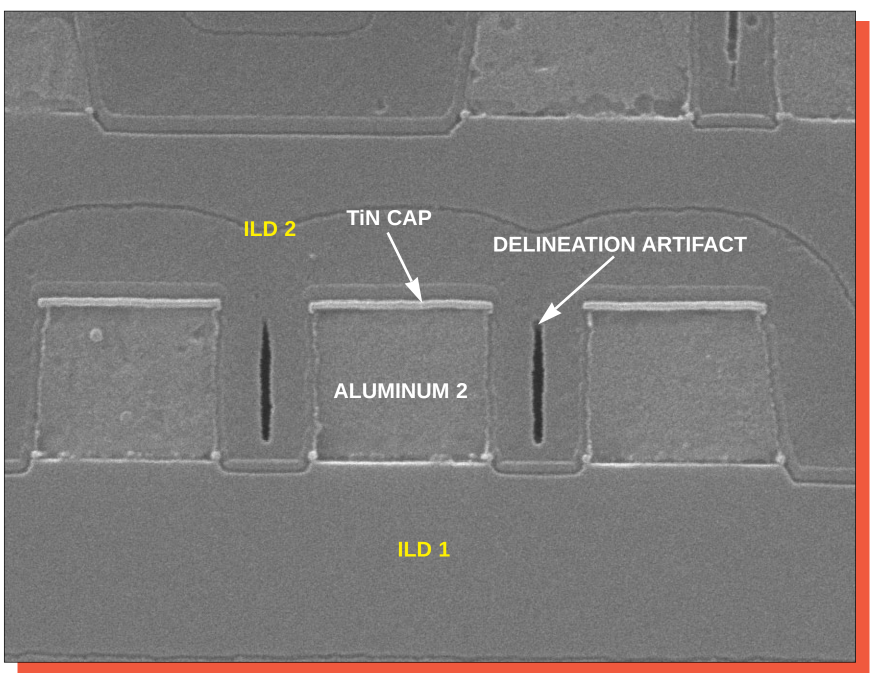


Mag 30,000x

Figure 24. SEM section views of metal 3-to-metal 2 vias.

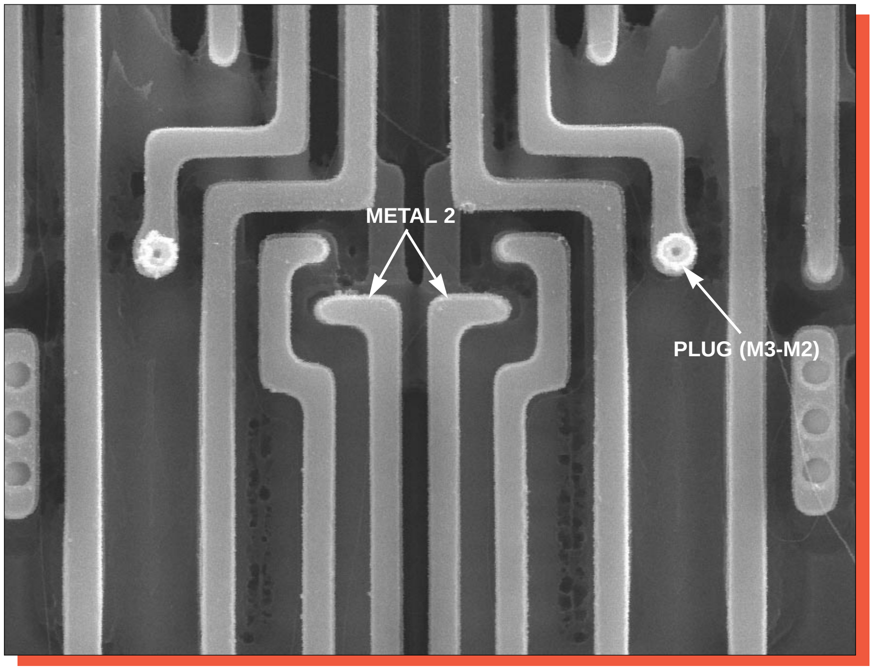


Mag. 20,000x

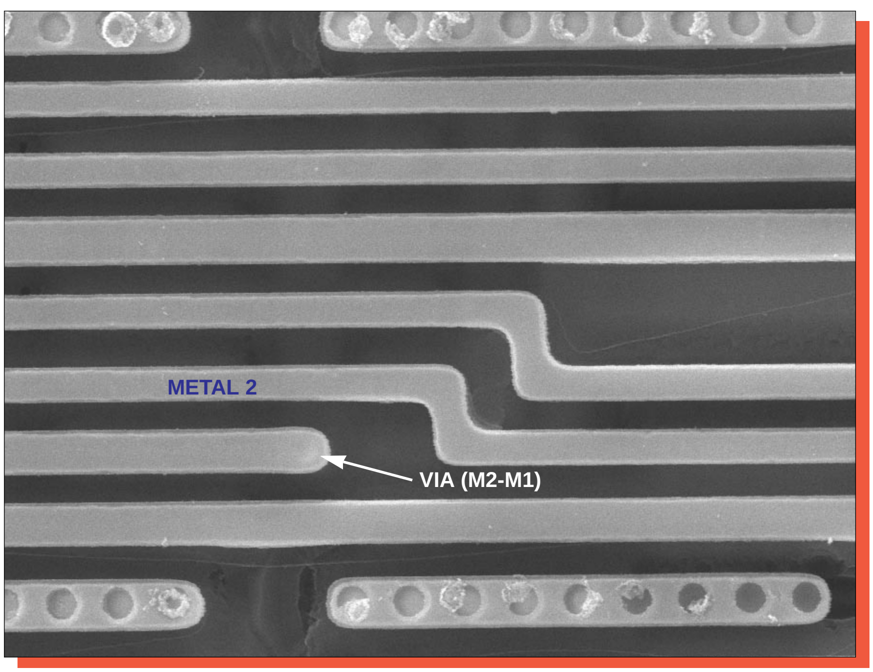


Mag. 26,000x

Figure 25. SEM section views of metal 2 line profiles.

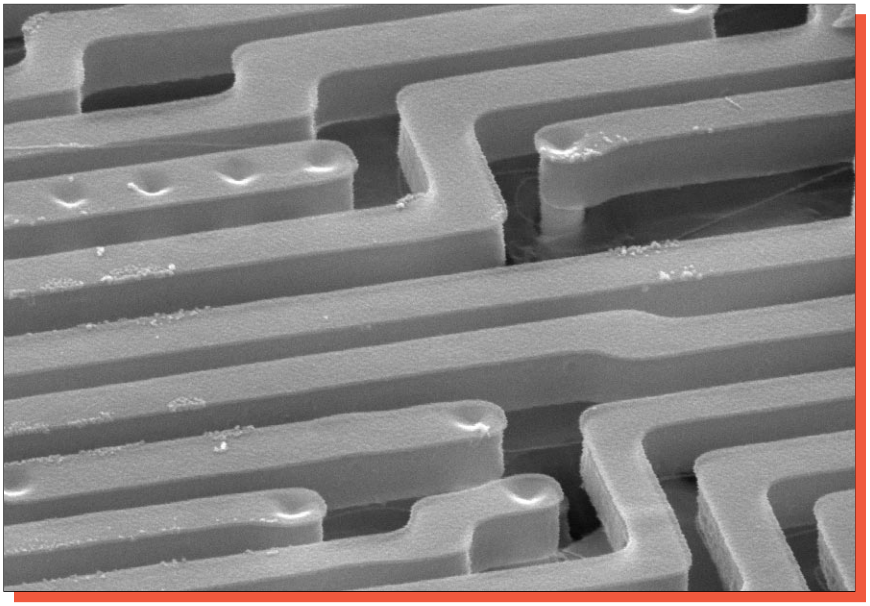


Mag. 7000x

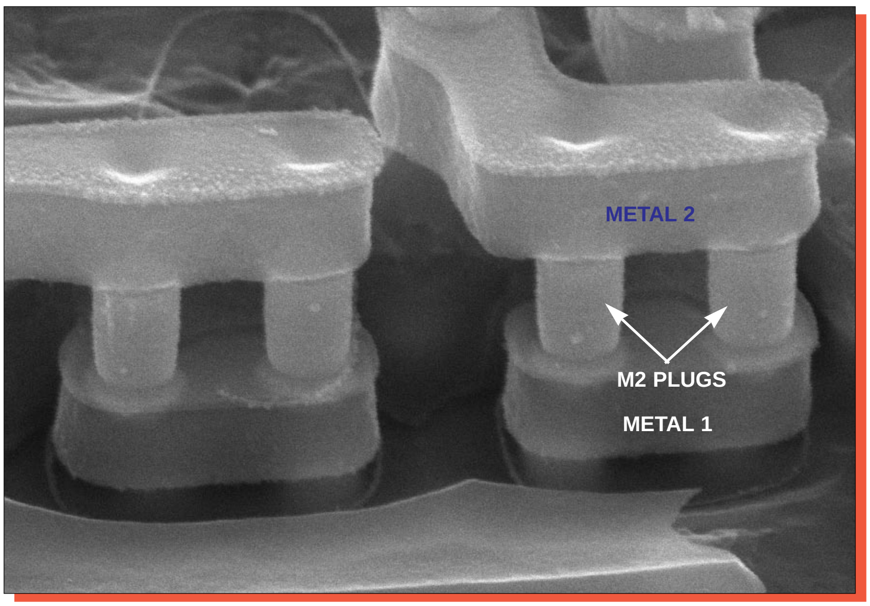


Mag. 8000x

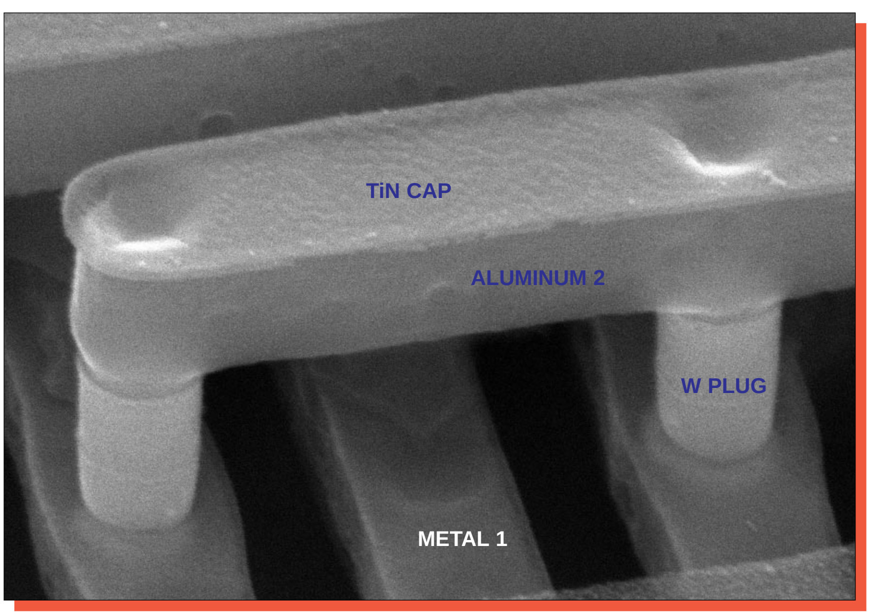
Figure 26. Topological SEM views of metal 2 patterning. 0°.



Mag. 12,500x

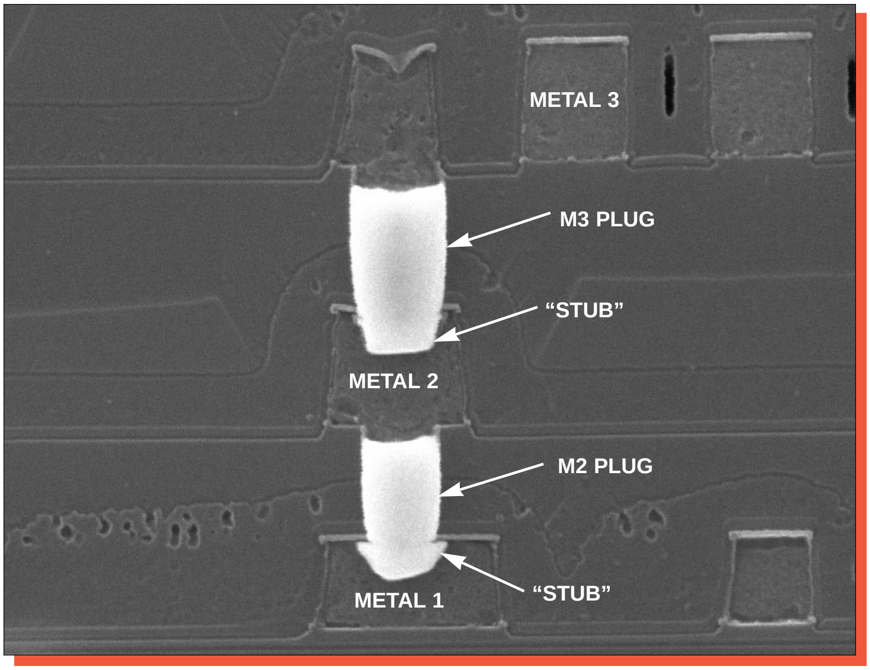


Mag. 26,000x

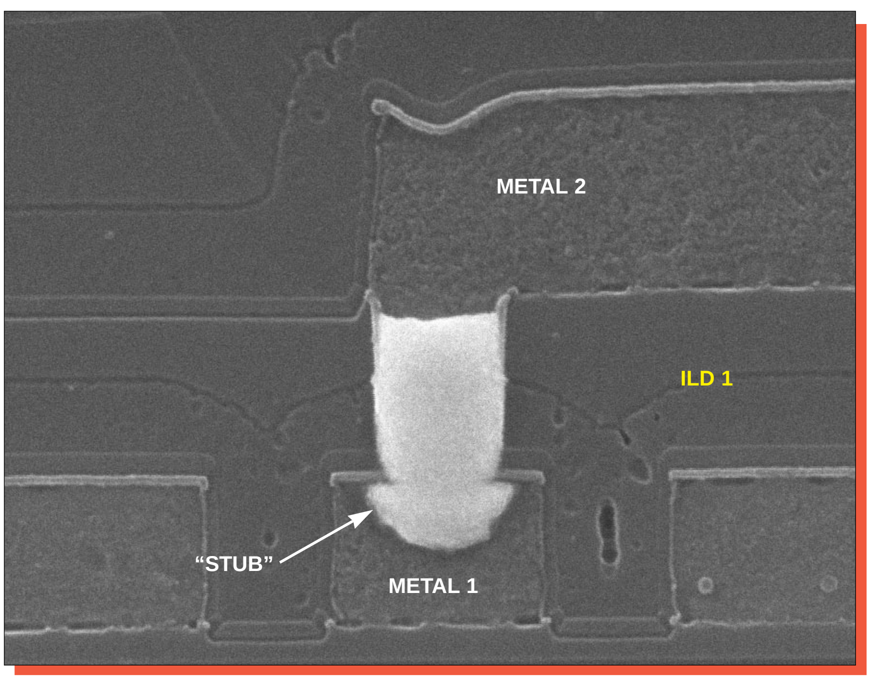


Mag. 35,000x

Figure 27. SEM views of general metal 2 coverage. 55°.

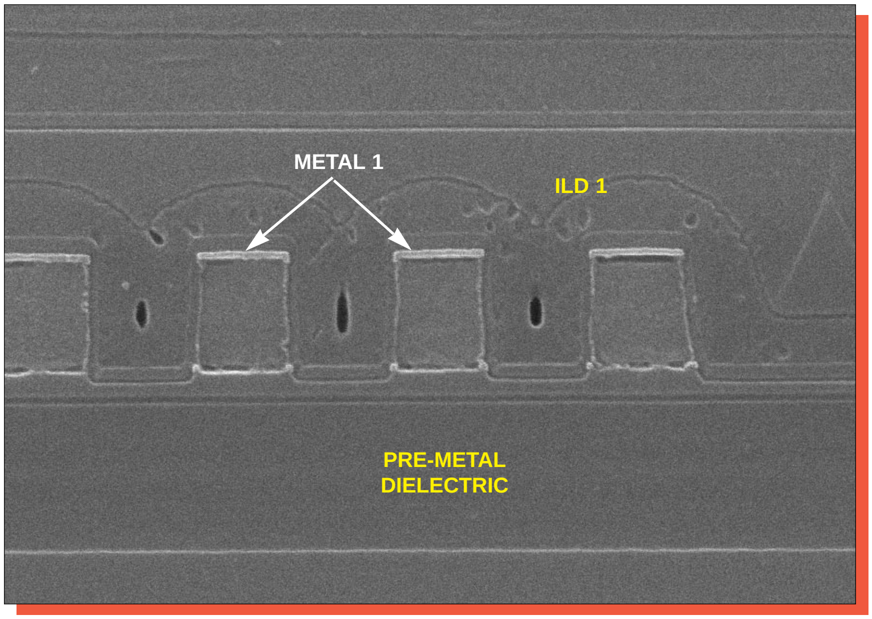


Mag. 22,000x

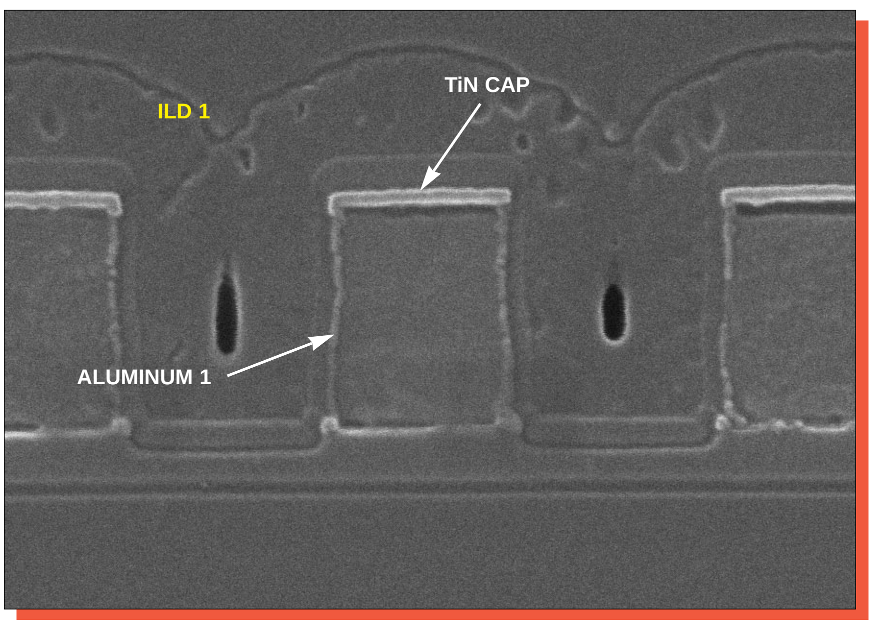


Mag. 35,000x

Figure 28. SEM section views of metal 2-to-metal 1 vias.



Mag. 26,000x



Mag. 52,000x

Figure 29. SEM section views of metal 1 line profiles.

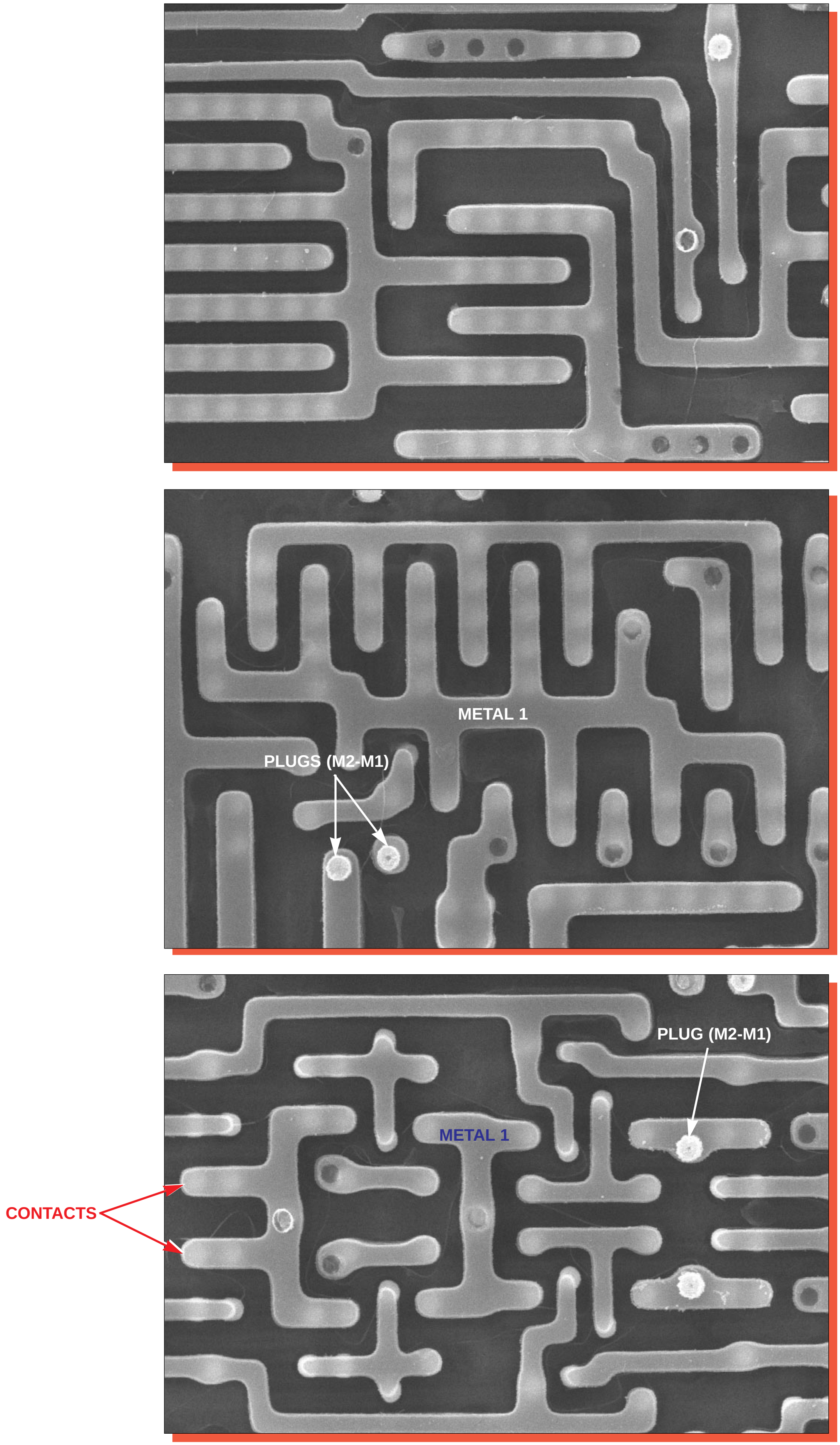
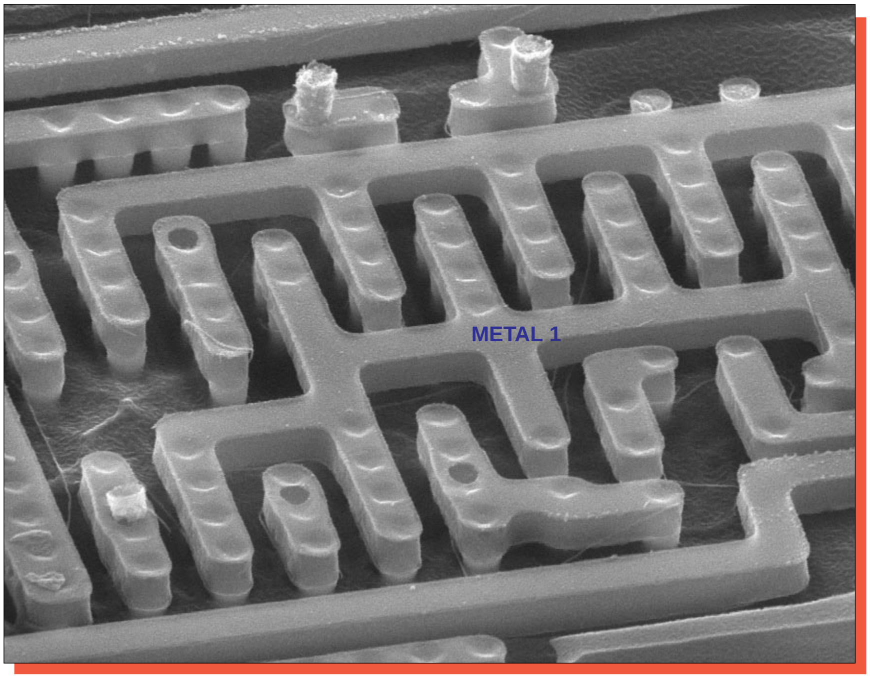
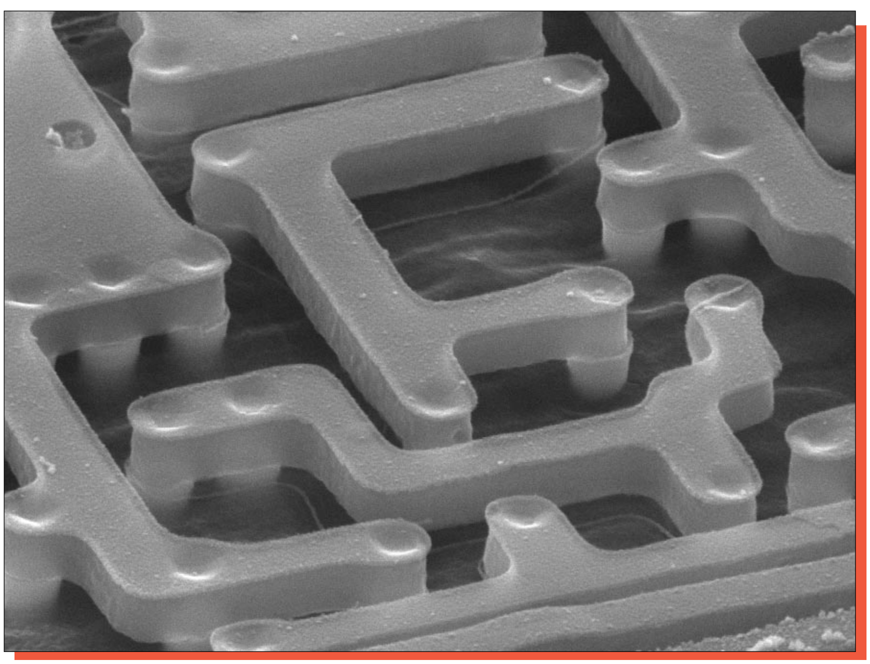


Figure 30. Topological SEM views of metal 1 patterning. Mag. 7000x, 0°.

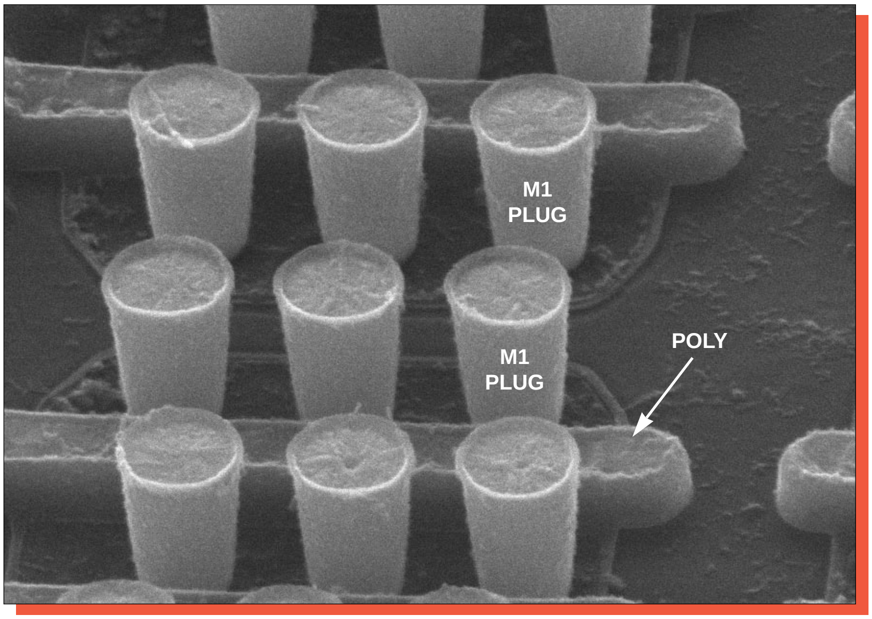


Mag. 9000x

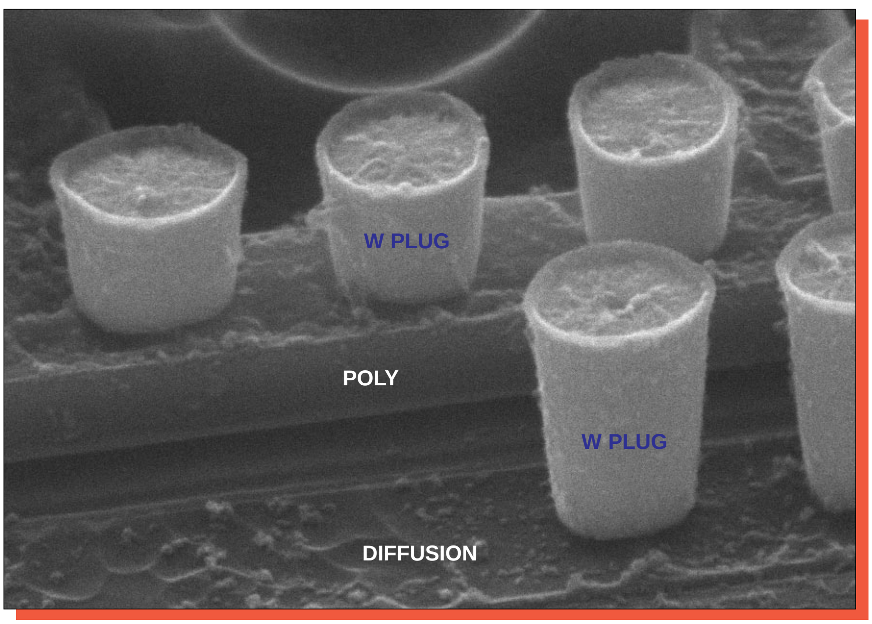


Mag. 13,500x

Figure 31. SEM views of general metal 1 coverage. 55°.

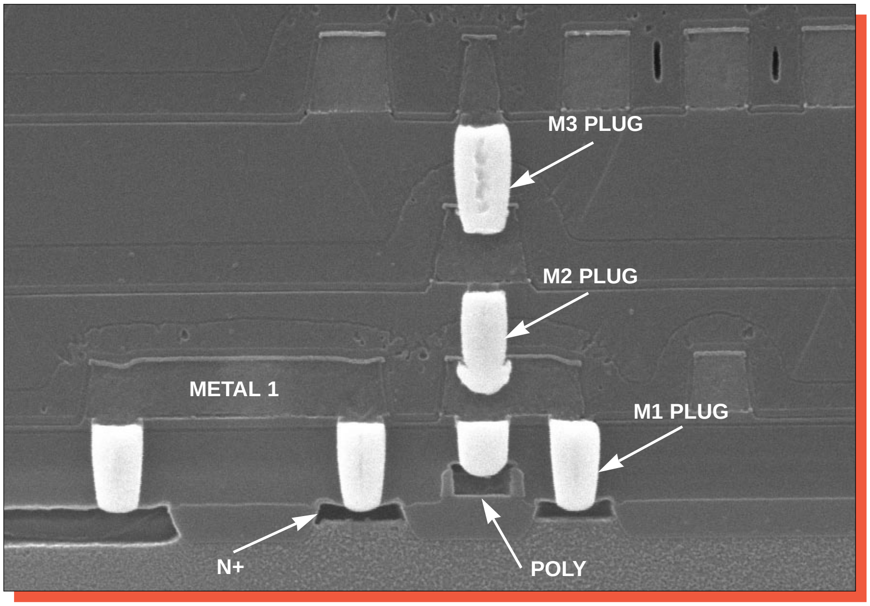


Mag. 25,000x

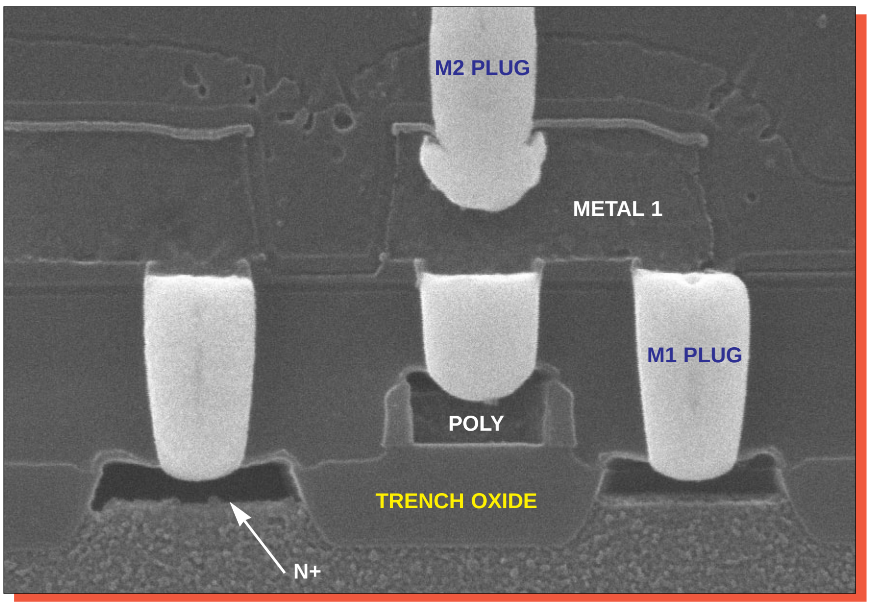


Mag. 40,000x

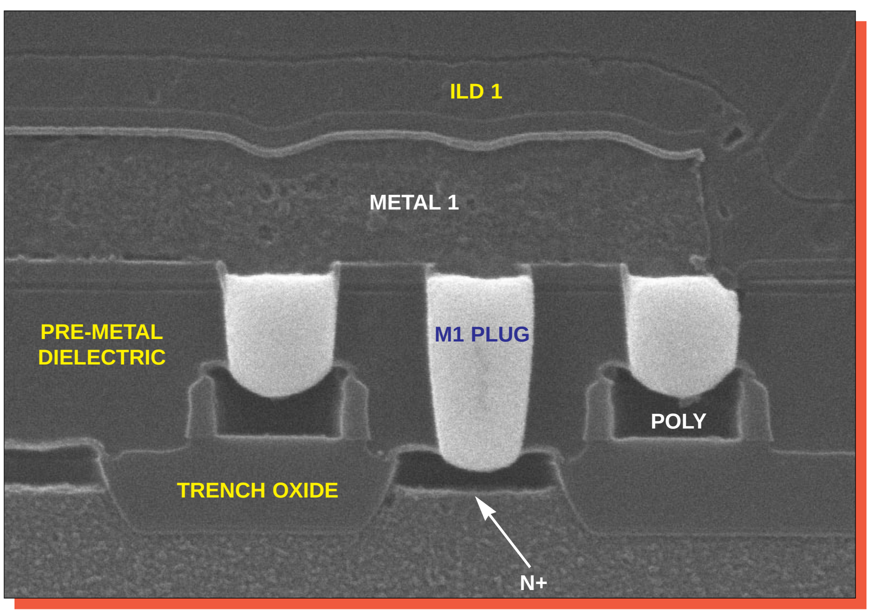
Figure 32. SEM views of metal 1 plugs. 50°.



Mag. 13,000x

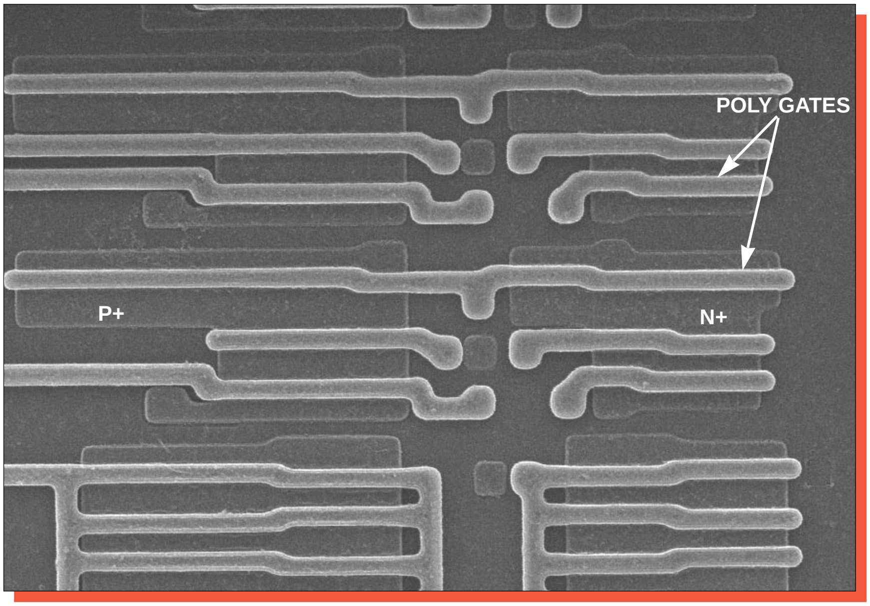


Mag. 30,000x

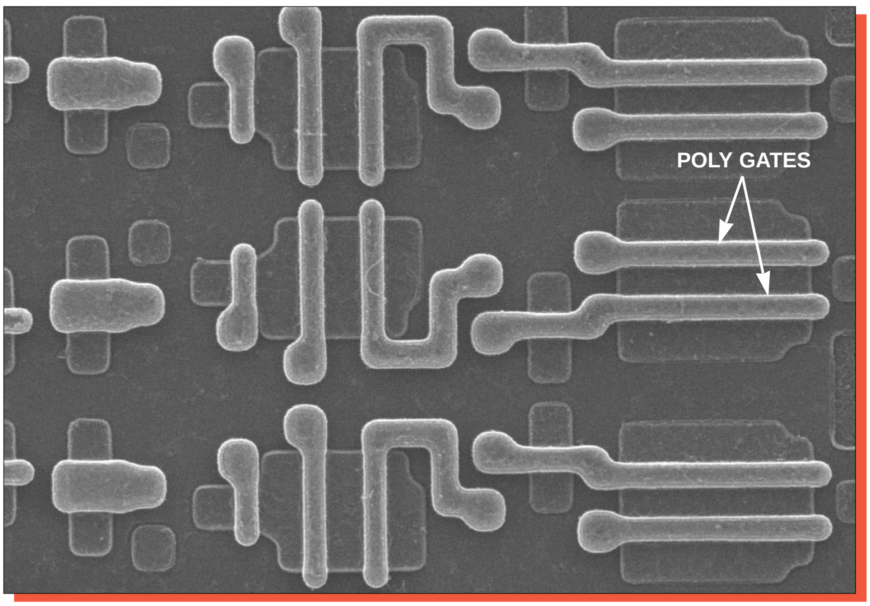


Mag. 30,000x

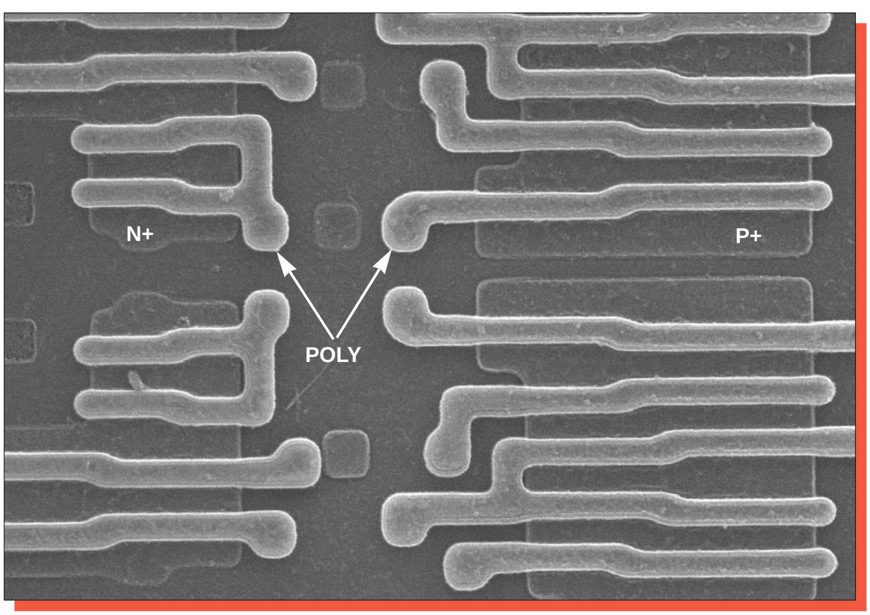
Figure 33. SEM section views of metal 1 contacts.



Mag. 5000x

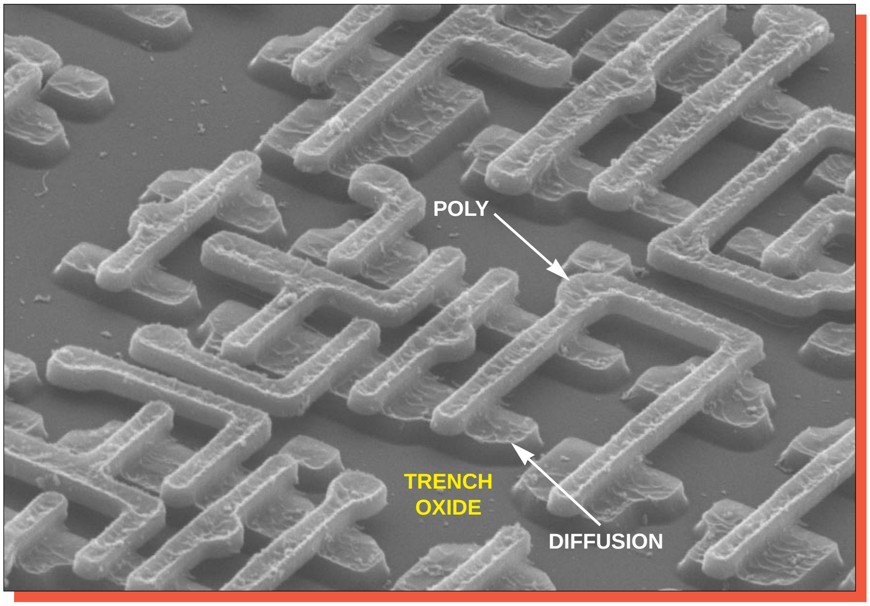


Mag. 6500x

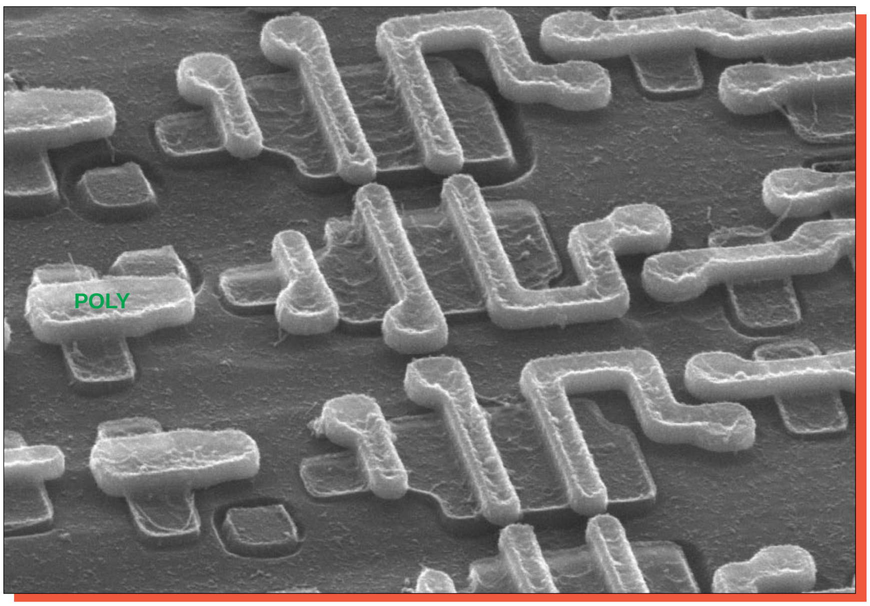


Mag. 7000x

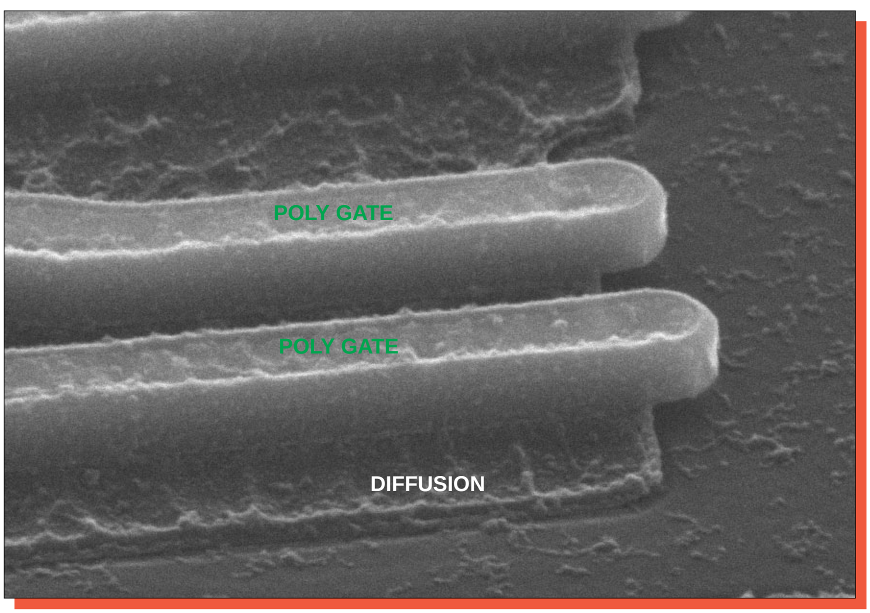
Figure 34. Topological SEM view of poly patterning. 0°.



Mag. 8400x

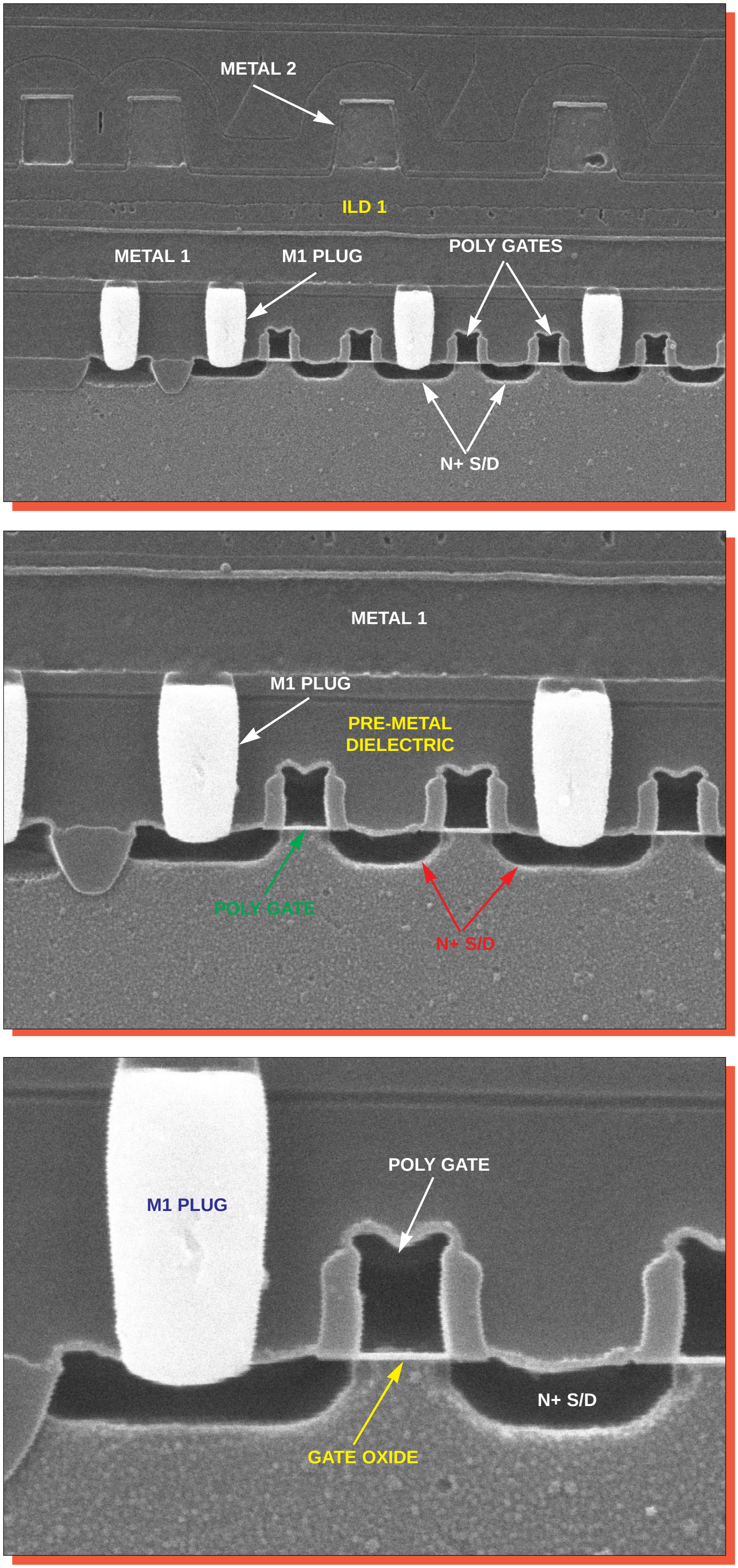


Mag. 10,000x



Mag. 32,000x

Figure 35. Perspective SEM views of poly coverage. 55°.

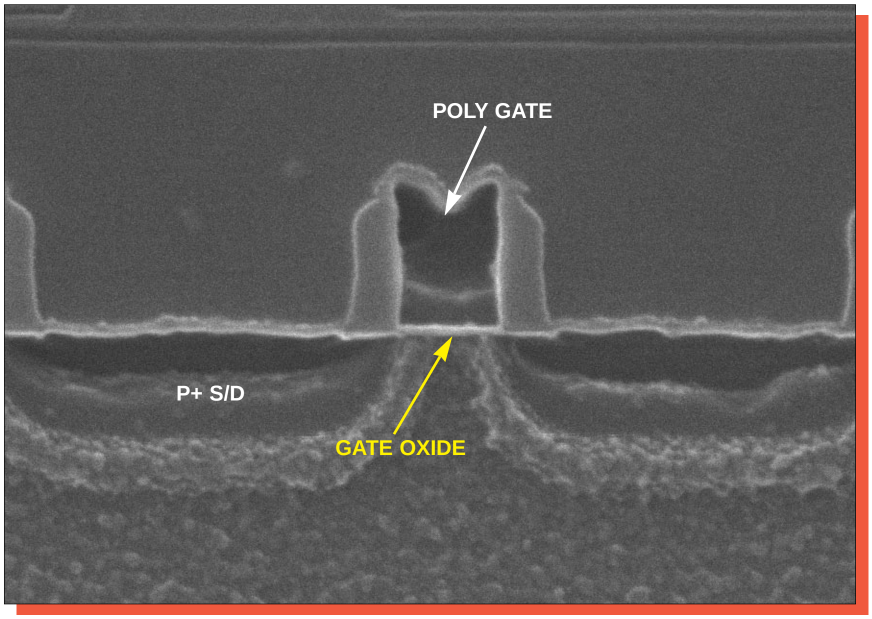


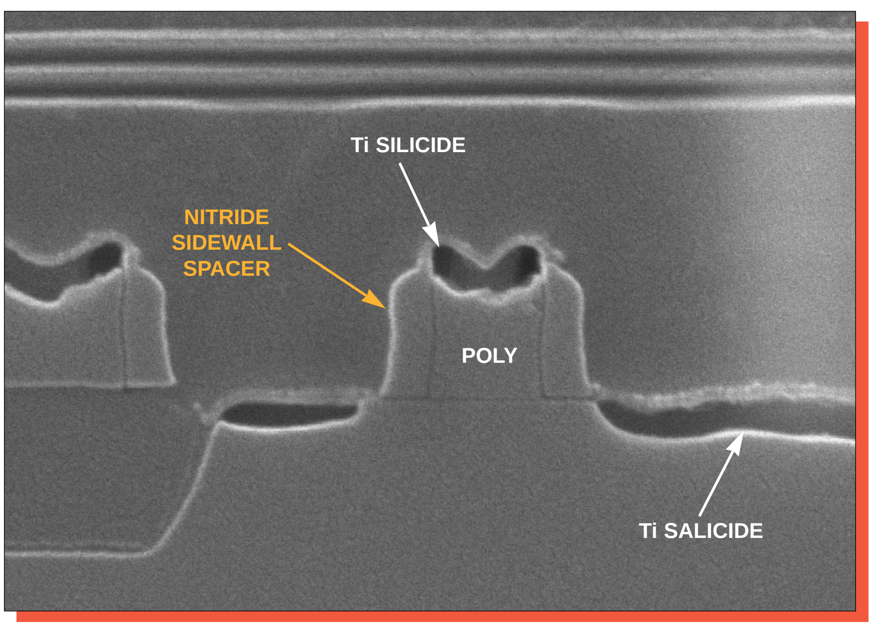
Mag. 13,000x

Mag. 26,000x

Mag. 52,000x

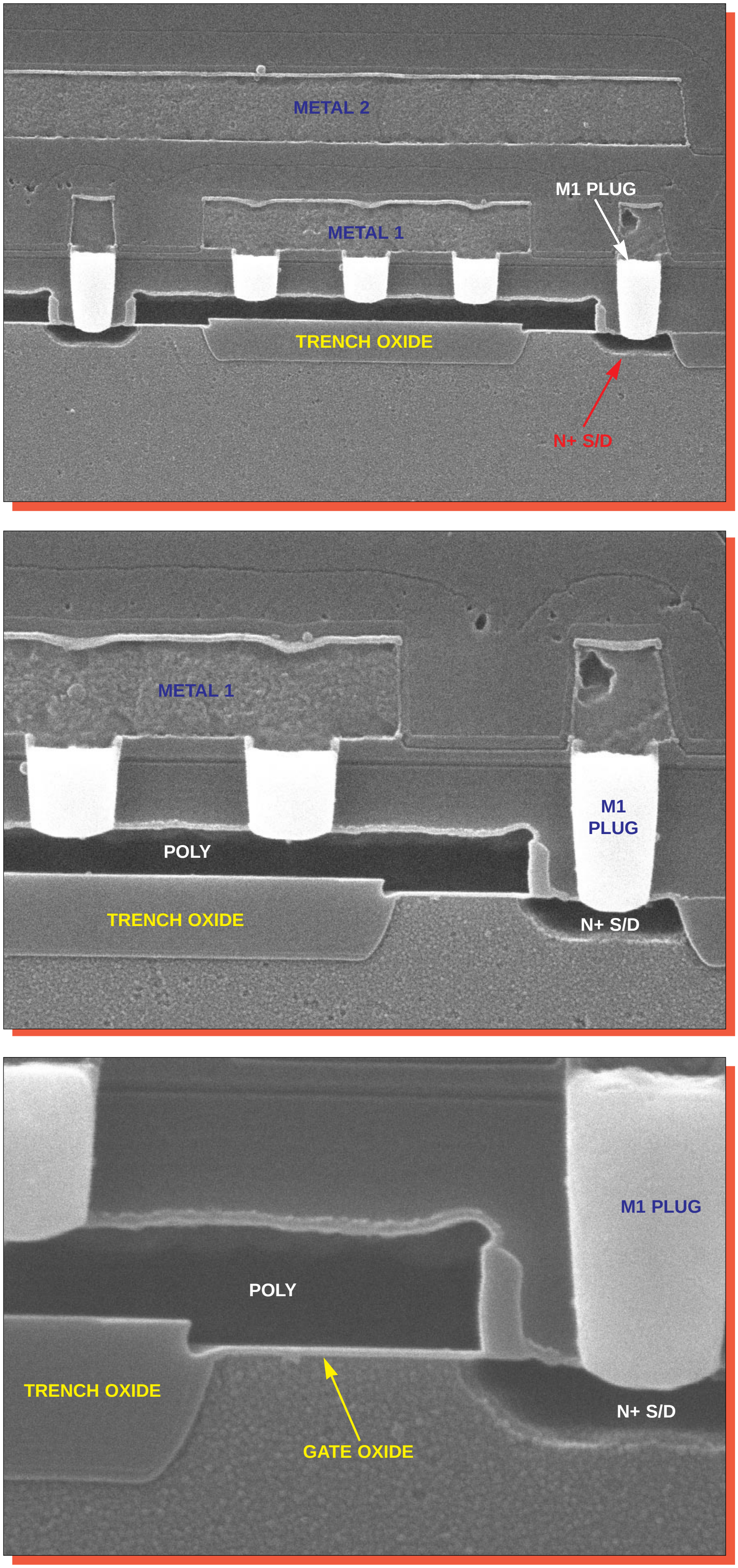
Figure 36. SEM section views of N-channel transistors.





glass etch

Figure 37. SEM section views of P-channel transistors. Mag. 52,000x.

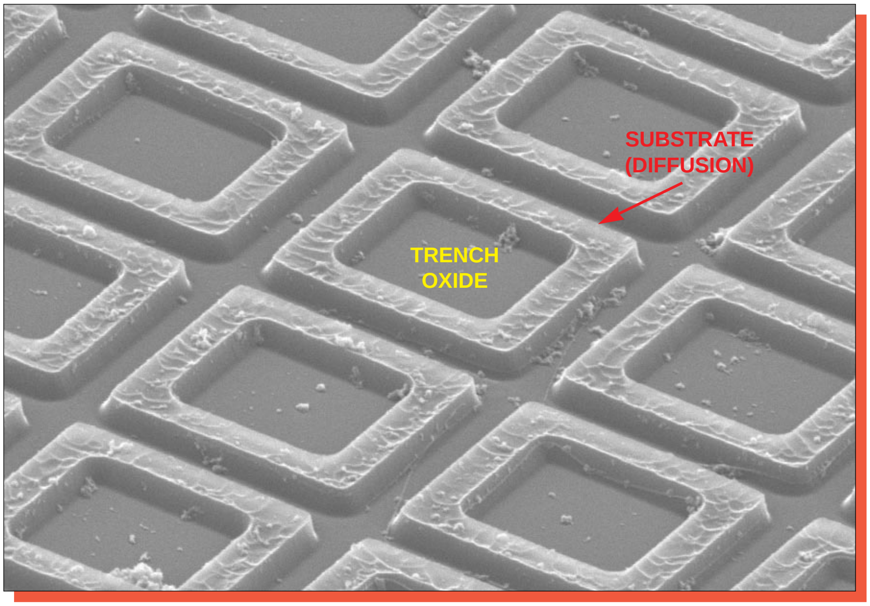


Mag. 13,000x

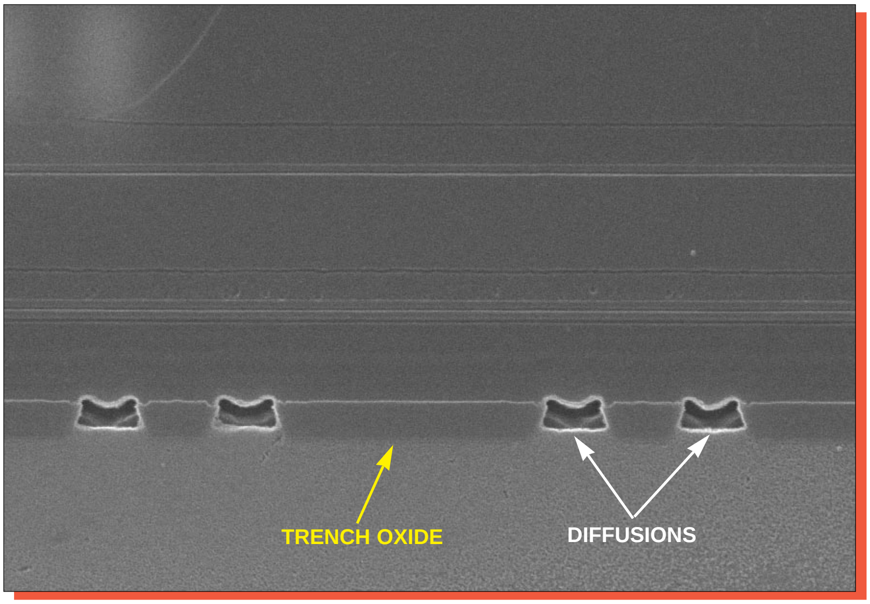
Mag. 26,000x

Mag. 52,000x

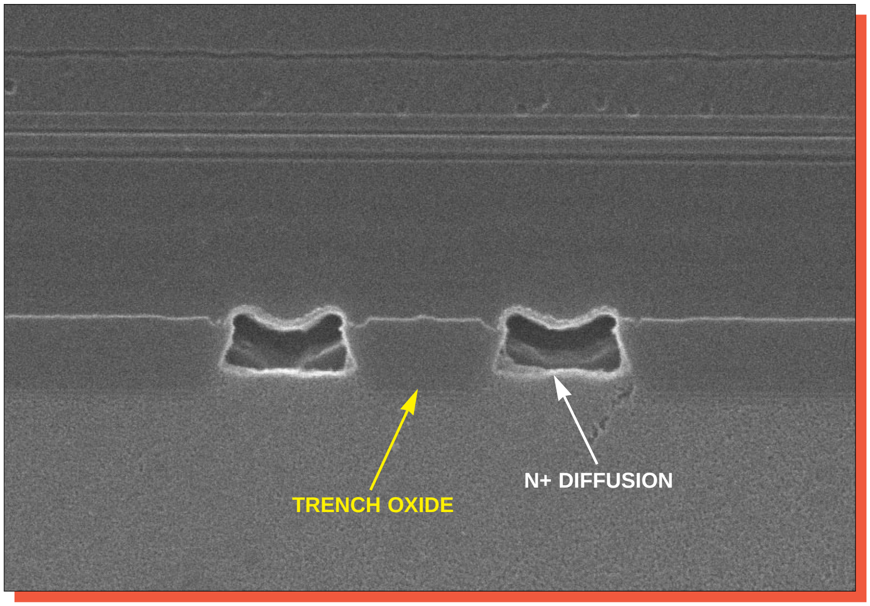
Figure 38. SEM section view of unique transistor structure.



Mag. 10,000x, 55°

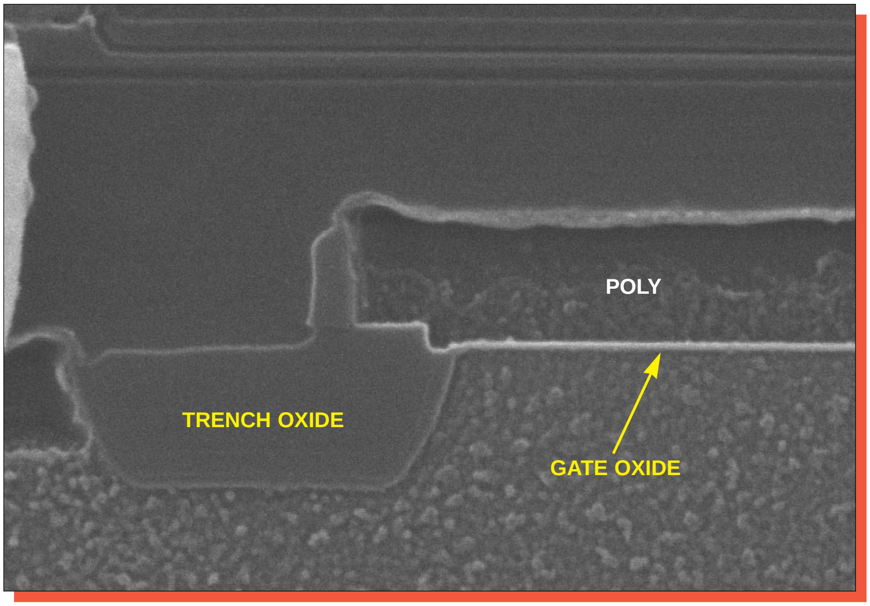


Mag. 15,000x

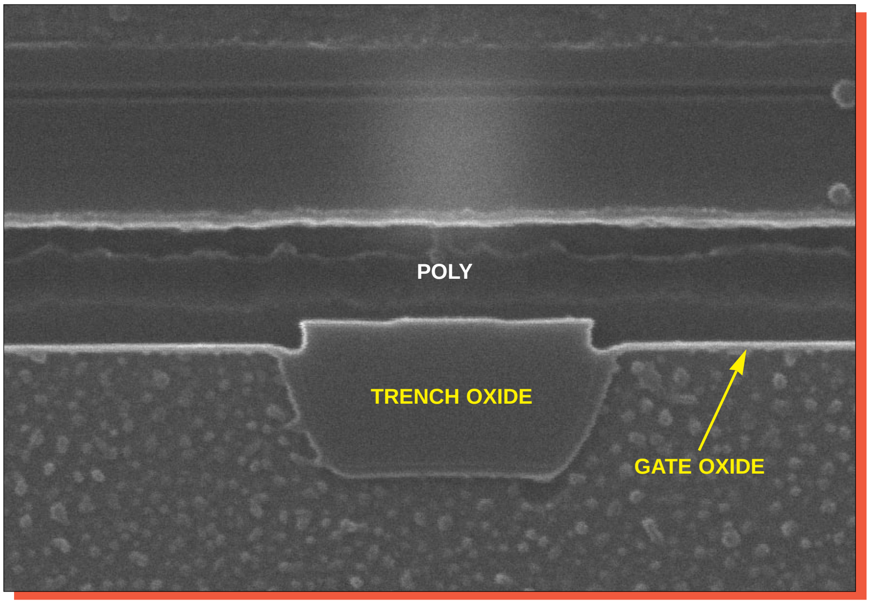


Mag. 30,000x

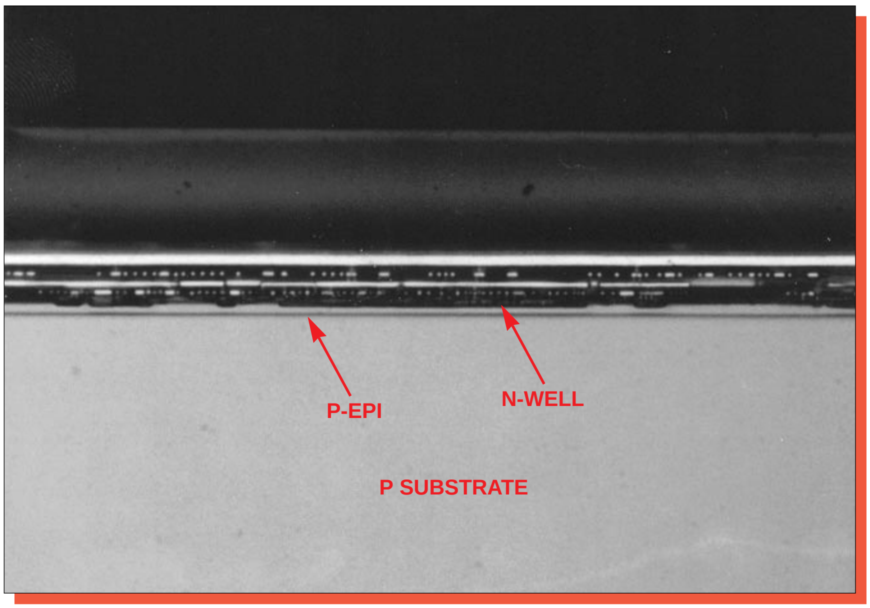
Figure 39. SEM views illustrating anti-dishing patterns.



Mag. 50,000x

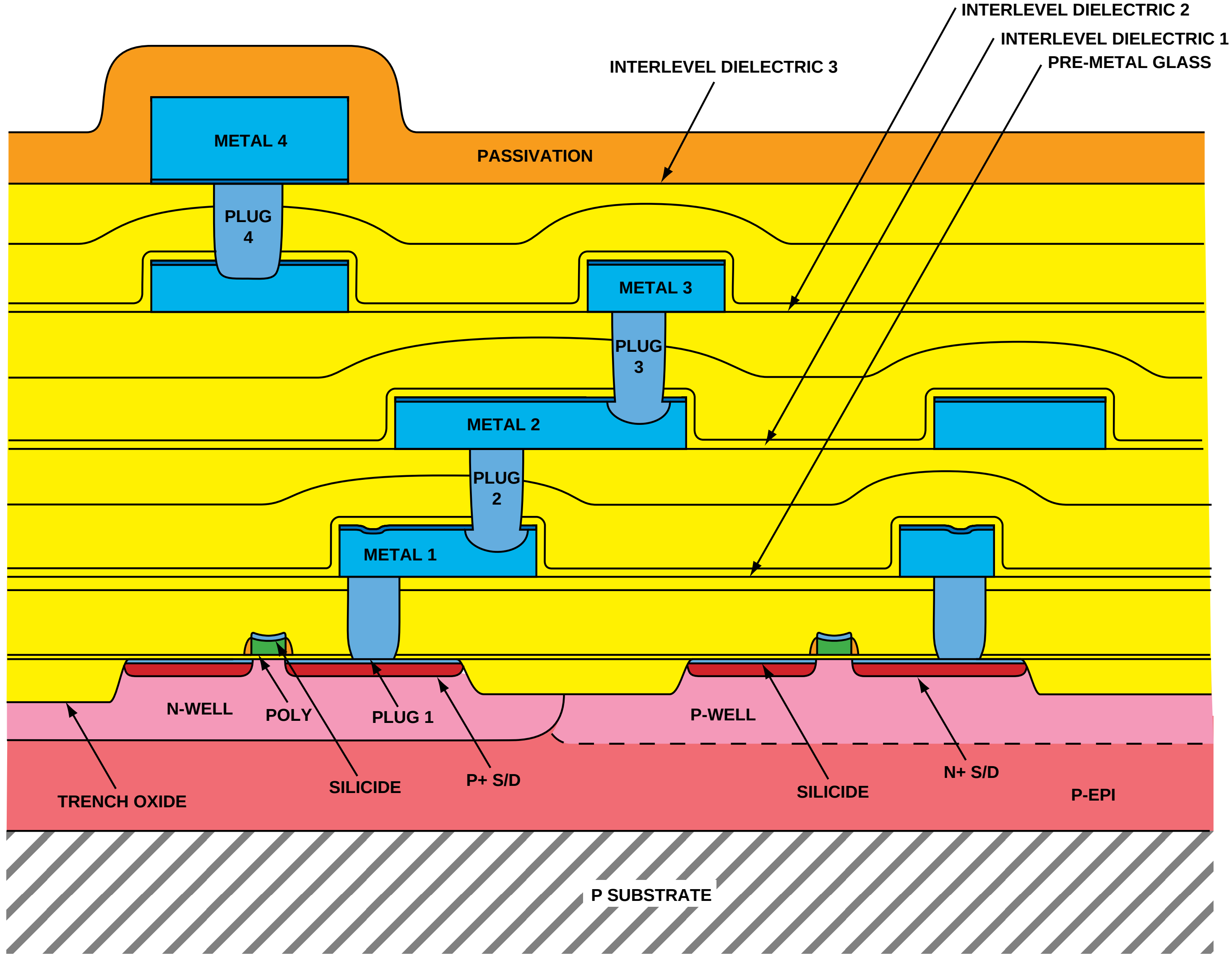


Mag. 50,000x



Mag. 800x

Figure 40. Section views illustrating trench oxide and well structure.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 41. Color cross section drawing illustrating device structure.

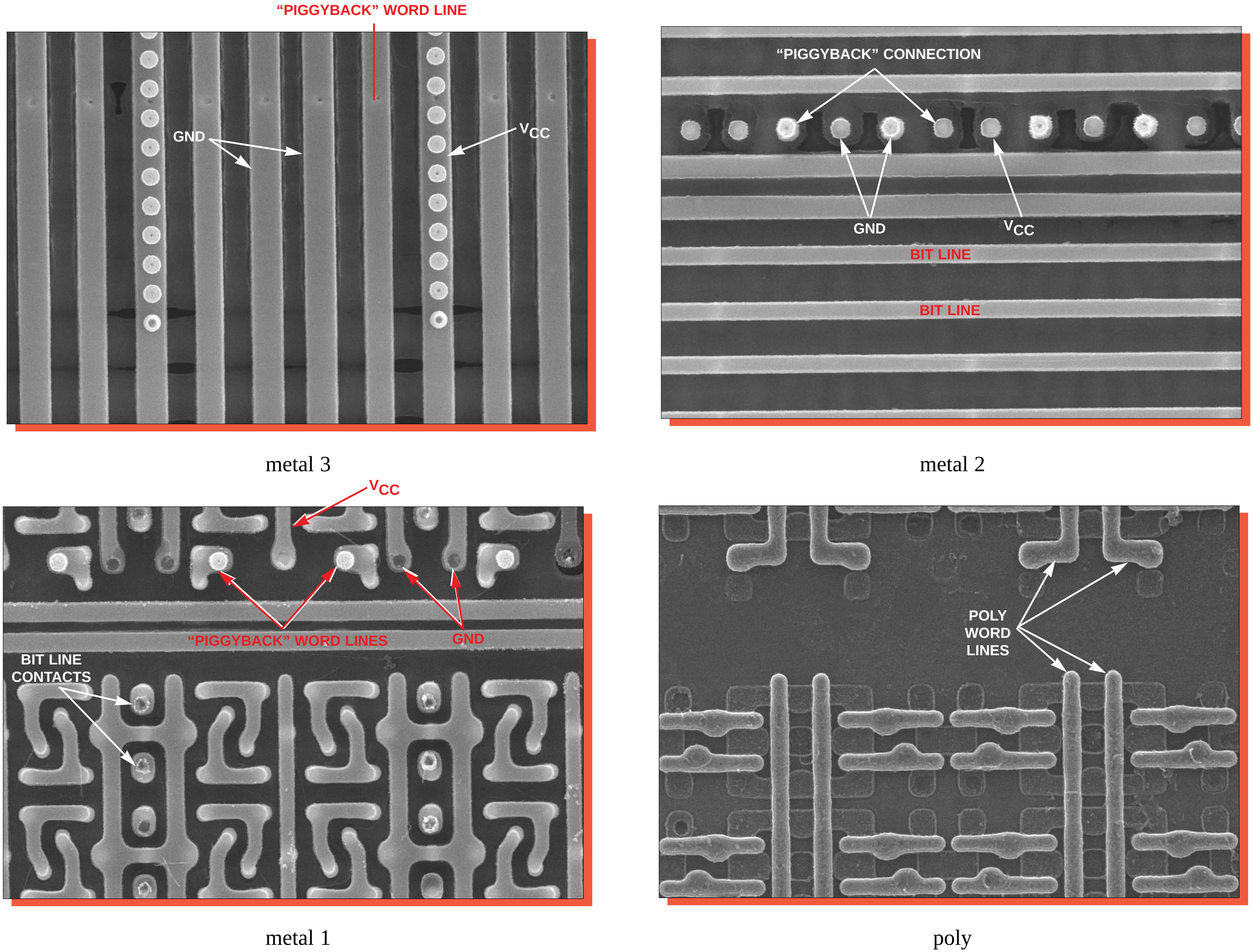
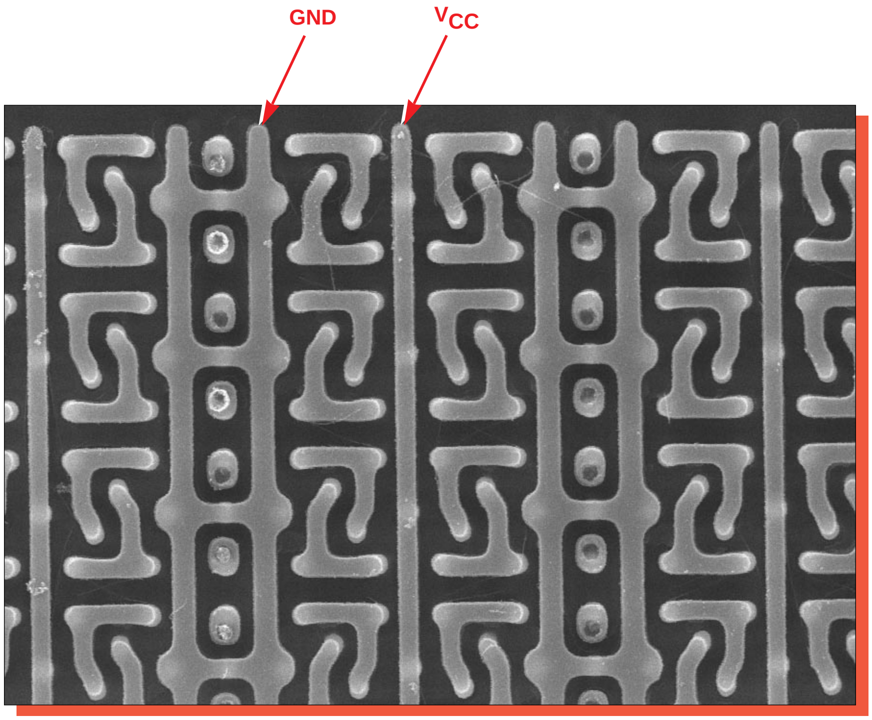
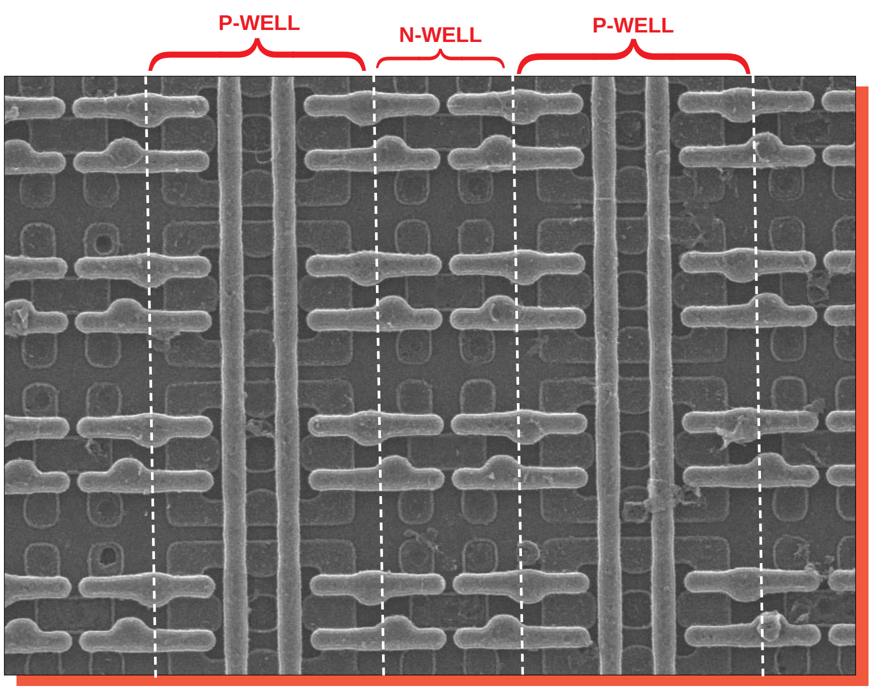


Figure 42. Topological SEM views of Cache SRAM cells illustrating "piggyback" word line connections. Mag. 6000x, 0°.

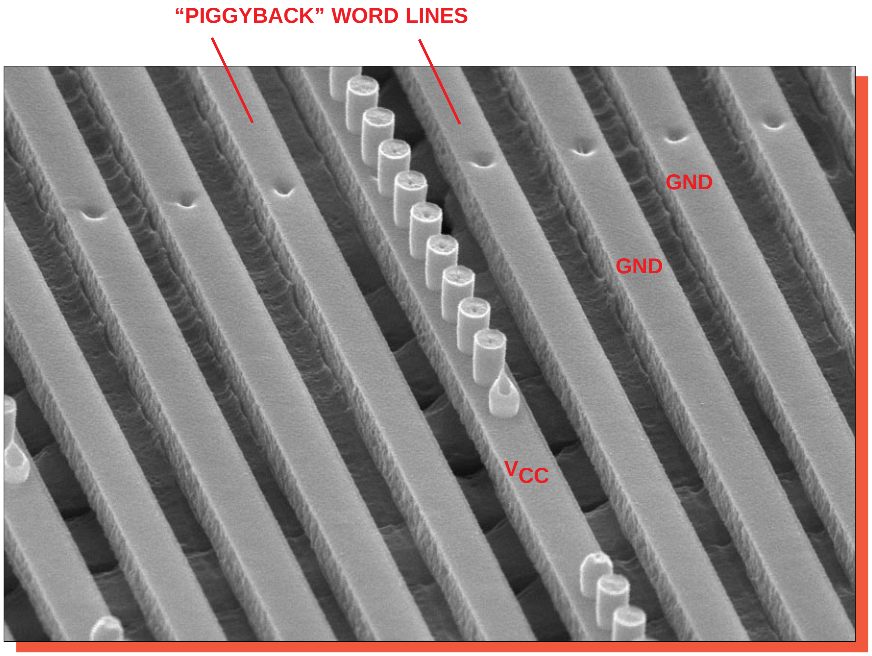


metal 1

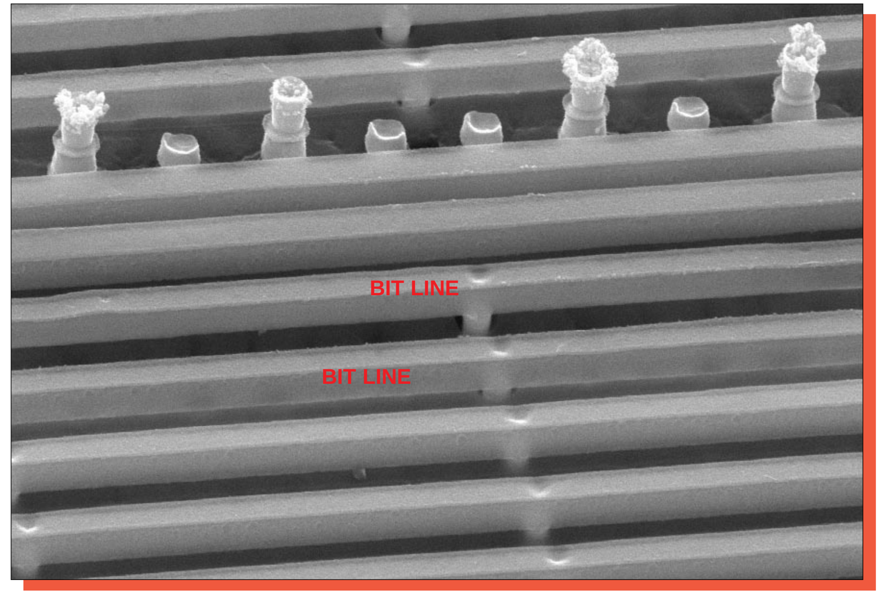


poly

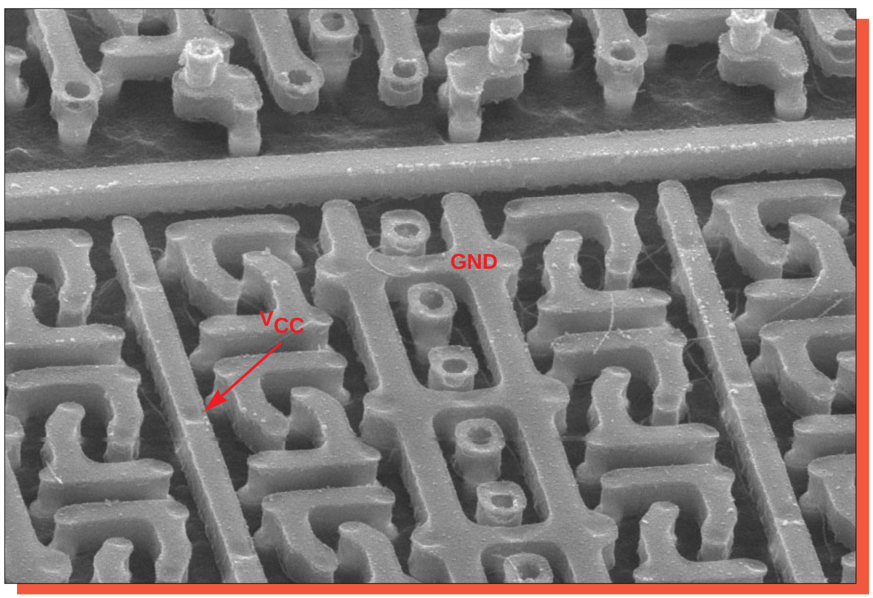
Figure 43. Topological SEM views of the Cache SRAM array. Mag. 5000x, 0°.



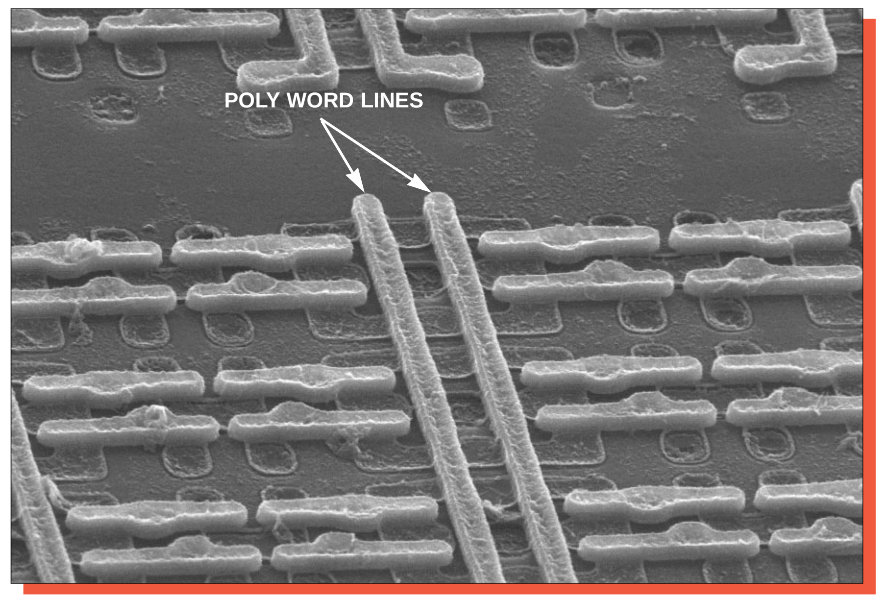
metal 3



metal 2

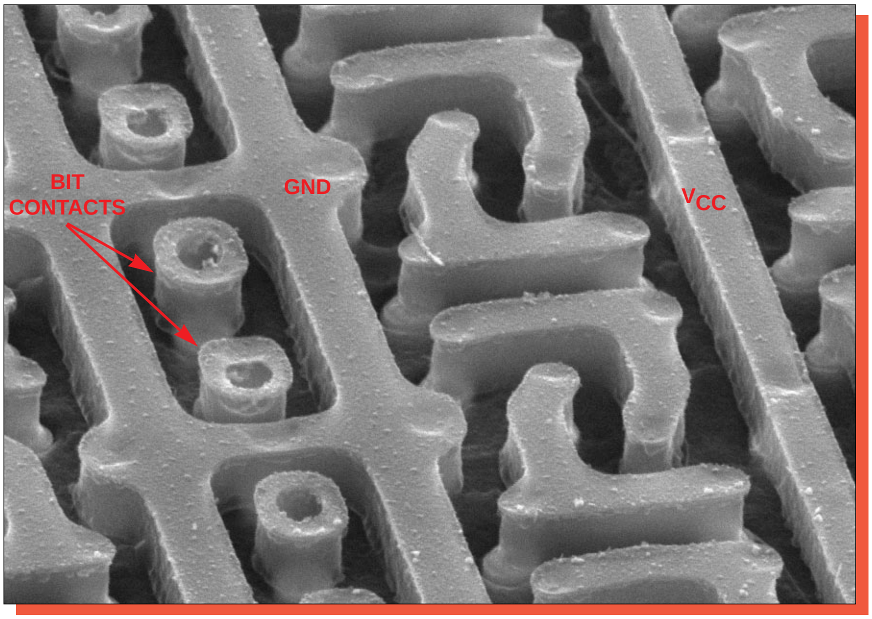


metal 1

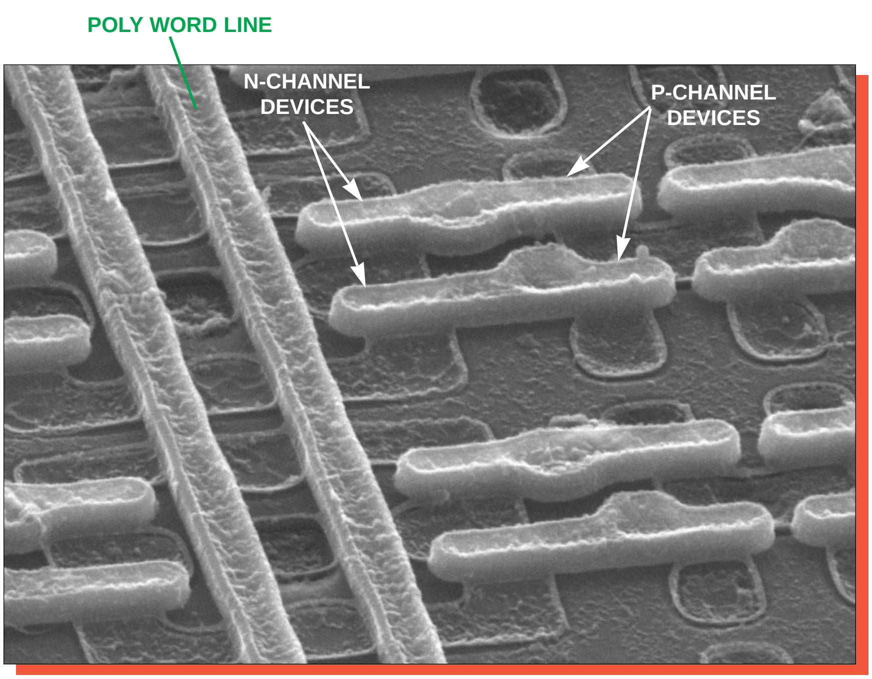


poly

Figure 44. Perspective SEM views of the Cache SRAM array. Mag. 7400x, 55°.

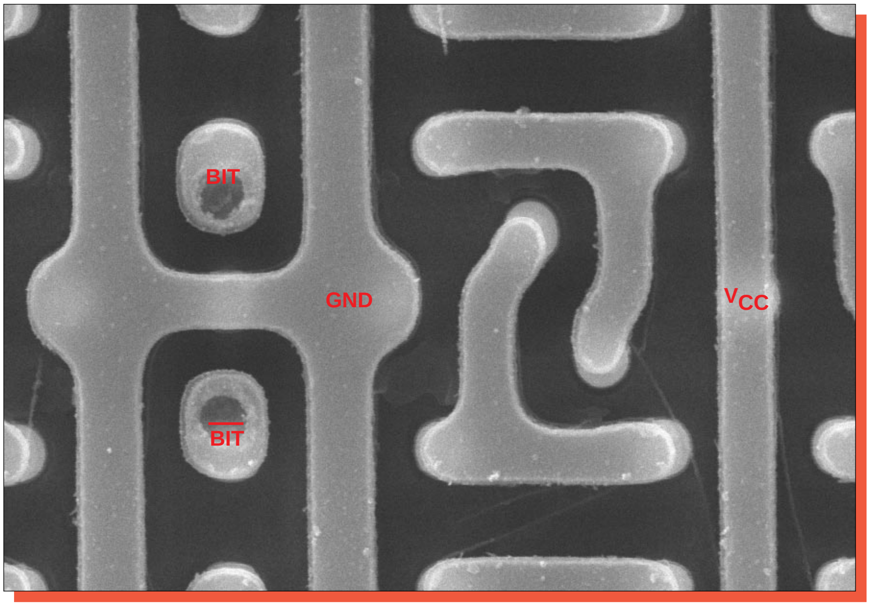


metal 1

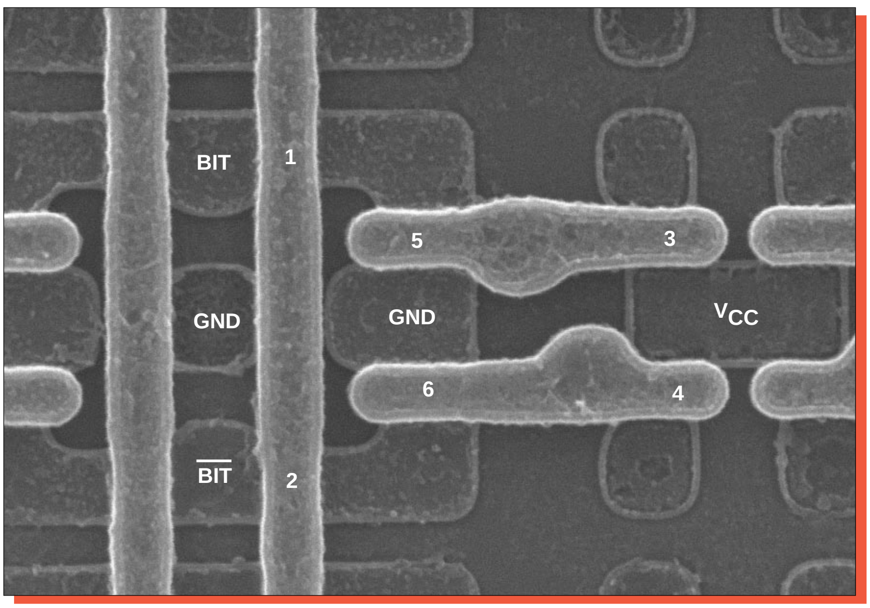


delayered

Figure 45. Detail SEM views of Cache SRAM cells. Mag. 14,000x, 55°.



metal 1



delayered

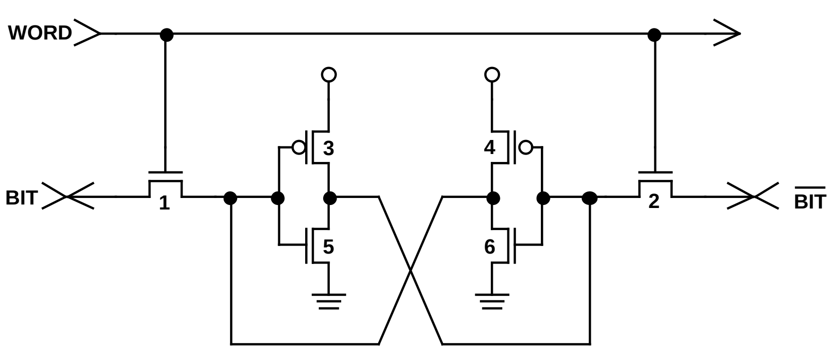
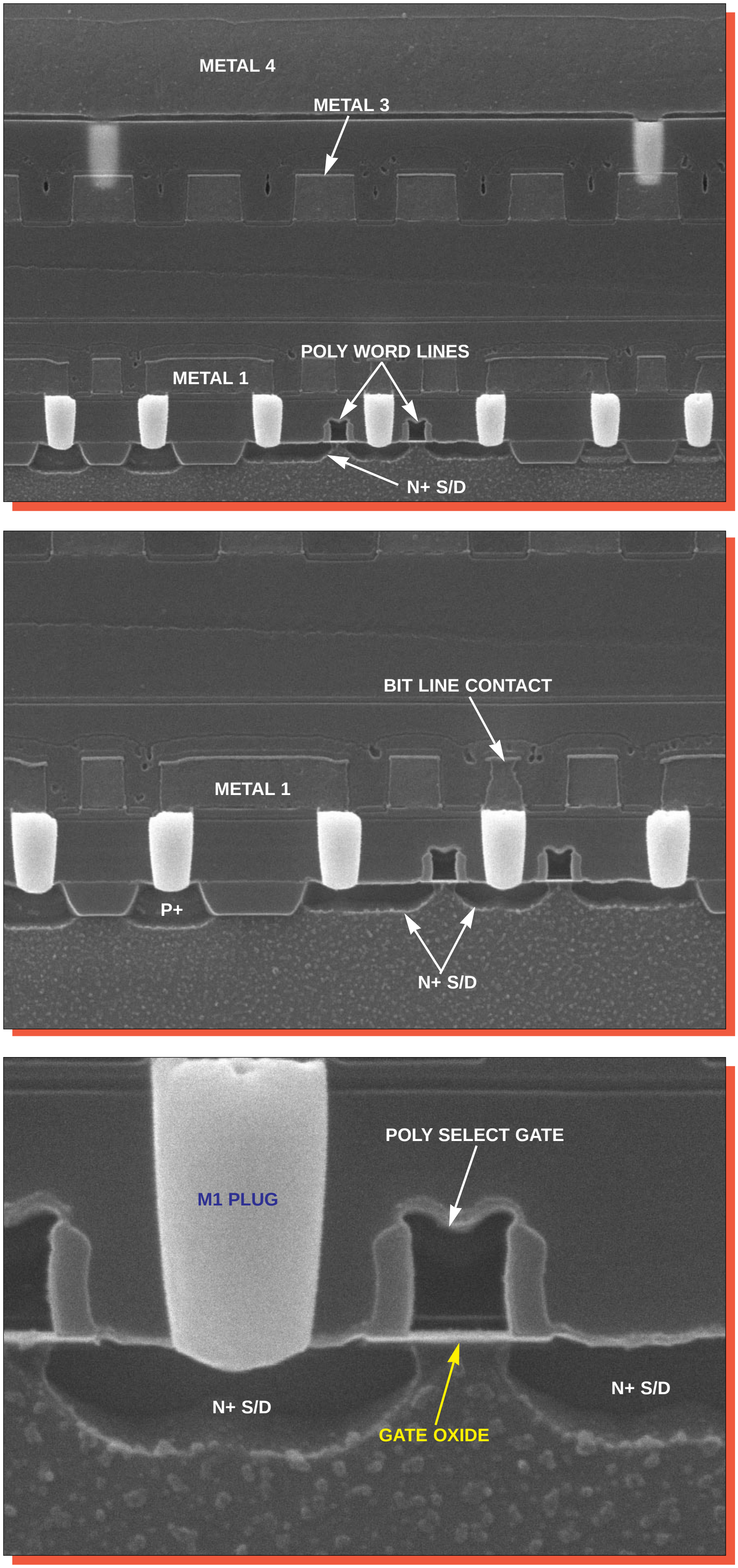


Figure 46. Topological SEM views and schematic of a Cache SRAM cell. Mag. 15,000x, 0°.

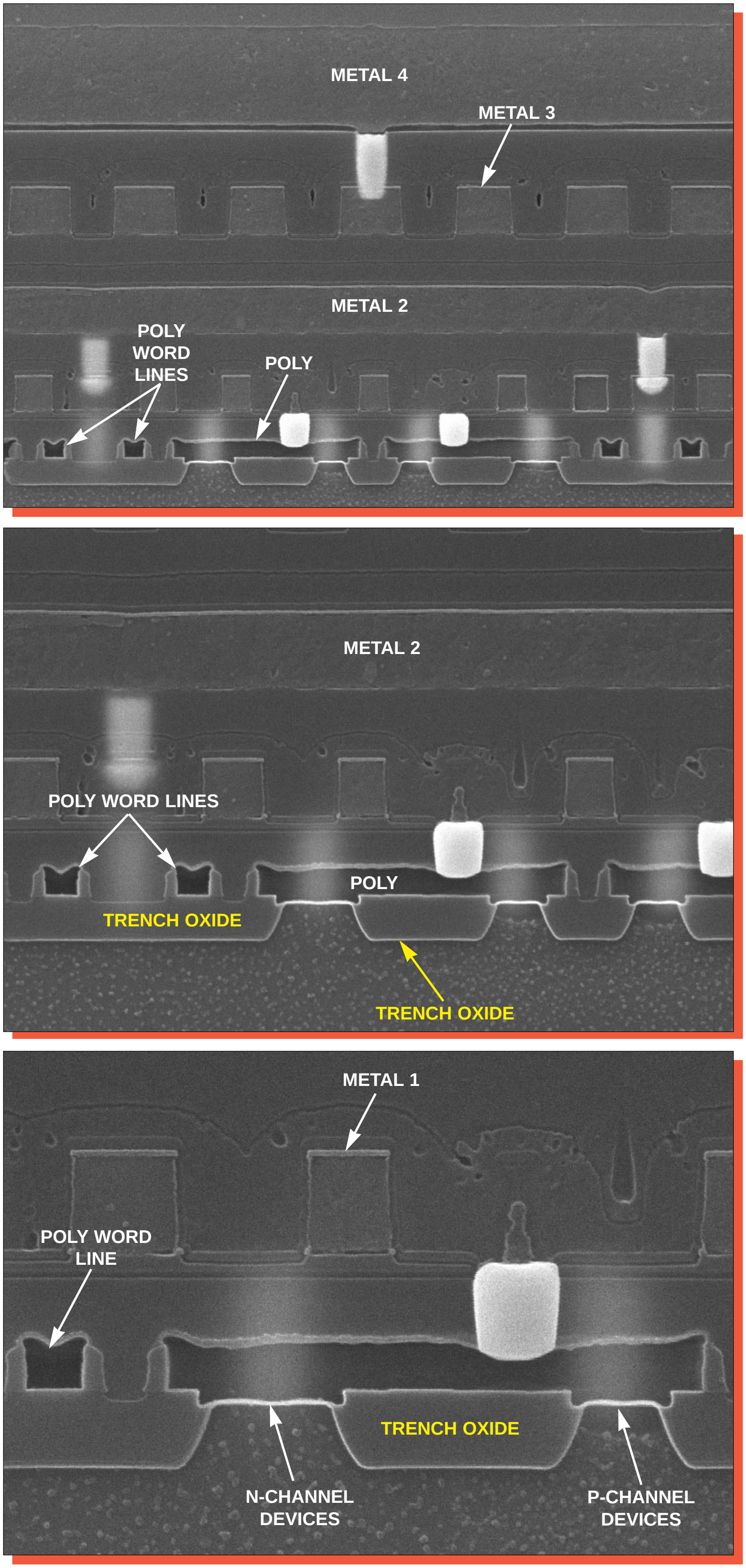


Mag. 9000x

Mag. 13,000x

Mag. 52,000x

Figure 47. SEM section views of a Cache SRAM cell (perpendicular to word lines).

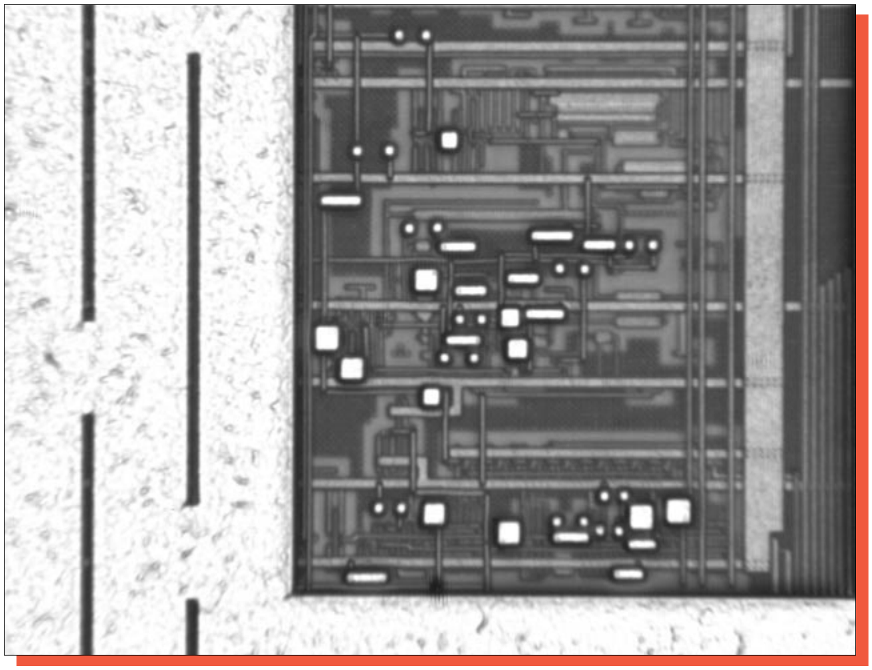


Mag. 9000x

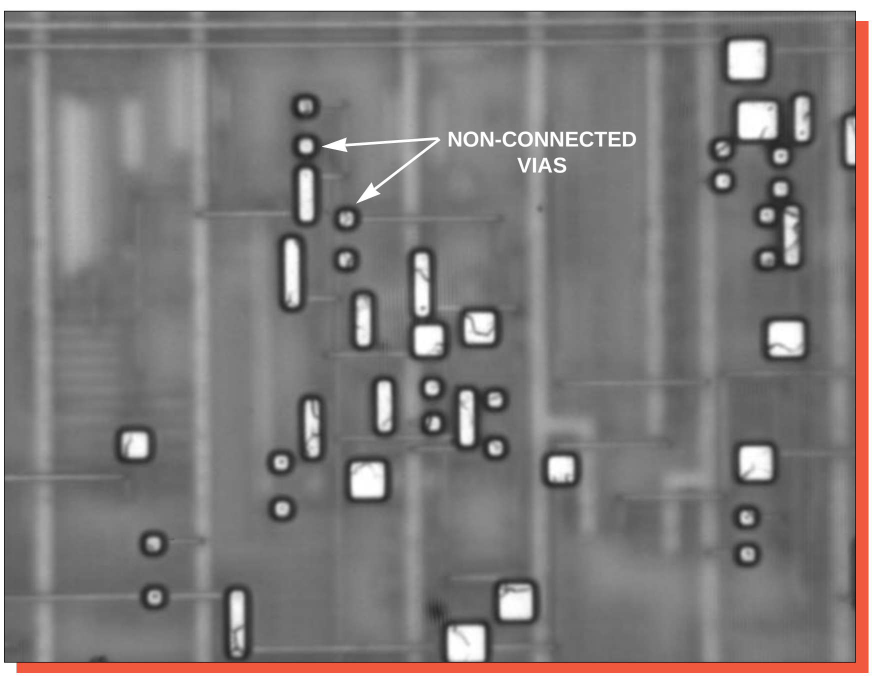
Mag. 15,000x

Mag. 26,000x

Figure 48. SEM section views of a Cache SRAM cell (parallel to storage and pull-up transistors).



Mag. 410x



Mag. 1015x

Figure 49. Optical views of general circuit layout.