Construction Analysis

Lattice GAL22LV10D-4LJ
EEPLD

Report Number: SCA 9704-536

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a competitive analysis of the Lattice GAL22LV10D-4LJ CMOS EEPLD. Four devices packaged in 28-pin Plastic Leaded Chip Carriers (PLCCs) were received for the analysis. Devices were date coded 9606.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Sub-micron gate lengths (0.4 micron N-channel and 0.45 micron P-channel).

Design Features:

- Slotted and beveled metal 2 bus lines.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in 28-pin Plastic Leaded Chip Carriers (PLCCs) with J-leads.
- Copper (Cu) leadframe appeared to be internally plated with silver (Ag).
- External pins (J-lead) were apparently tinned with tin-lead (SnPb) solder.
- Lead-locking provisions (anchors) at all pins.
- Thermosonic ball bonding using 1.2 mil O.D. gold wire.
- Pins 14 and 28 were double wirebonded (Vcc and GND). Pins 1, 8, 15 and 22 were not used.
- Sawn dicing (full-depth).
- Silver-filled epoxy die attach.

Die Process and Design:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P-substrate. No epi was used.
- Passivation consisted of a layer of nitride over a layer of glass.
- Metallization interconnect employed two layers of metal. Both consisted of aluminum with a titanium-nitride cap and barrier. Standard vias and contacts were used (no plugs).
- Pre-metal glass consisted of a layer of reflow glass over various densified oxides. Glass was reflowed prior to contact cuts only.

TECHNOLOGY DESCRIPTION (continued)

- A single layer of polycide (tungsten silicide) was used to form all gates on the die and the top plates of all capacitors. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A step was present at the edge of the well which indicates a twin-well process was used. No problems were noted.

- The EEPROM memory cell consisted of metal 2 program and output lines (via metal 1). Metal 1 was used to form select, output select, and to distribute ground. Polycide was used to form the top plates of all capacitors and gates. Programming is achieved through an ultra-thin (tunnel) oxide window.

- Redundancy fuses were not used.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 5**

Questionable Items: None.

General items:

- Devices were encapsulated in 28-pin Plastic Leaded Chip Carriers (PLCCs) with J-leads.
- Overall package quality: Good. Internal plating of the copper leadframe was silver. External pins were tinned with tin-lead (SnPb). No cracks or voids present. No gaps were noted at lead exits.
- Lead-locking provisions (anchors) were present at all pins.
- Wirebonding: Thermosonic ball method using 1.2 mil O.D. gold wire. No bond lifts occurred during wire pull tests and bond pull strengths were good (see page 10). No problems are foreseen.
- Vcc and GND pins were double wire bonded. Pins 1, 8, 15 and 22 were not connected.
- Die attach: Silver-filled epoxy of good quality. No voids were noted in the die attach and no problems are foreseen.
- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.
- Rolled aluminum was present in the scribe lane. It is possible that this aluminum could break free and cause a short if the die were assembled in a package containing a cavity, but no danger exists in plastic packages.

ANALYSIS RESULTS II

Die Process: **Figures 5 - 37**

Questionable Items:[1] None.

Special Features:

- Sub-micron gate lengths (0.4 micron N-channel and 0.45 micron P-channel).

Design features:

- Slotted and beveled metal 2 bus lines.

General items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P-substrate. No epi was used.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage of contamination was found.

- Die coat: No die coat was present.

- Overlay passivation: A layer of nitride over a layer of glass. Overlay integrity test indicated defect-free passivation. Edge seal was good.

- Metallization: Two layers of metal. Both metal layers consisted of aluminum with titanium-nitride caps and barriers. Standard vias and contacts were used (no plugs).

- Metal patterning: Both metal layers were patterned by a dry etch of normal quality.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal defects: No voiding, notching, or neckdown was noted in either of the metal layers. Contacts and vias were completely surrounded by metal. No silicon nodules were noted following removal of either metal layer.

- Metal step coverage: Metal 2 aluminum thinned up to 75 percent at some vias. Barrier metal maintained continuity and reduced thinning to 70 percent. Metal 1 aluminum thinned up to 80 percent at some contacts. Total metal 1 thinning was reduced by the cap and barrier metals to 70 percent.

- Interlevel glass: Two layers of silicon-dioxide were present under metal 2 (interlevel dielectric). The first layer had been subjected to an etchback process. A layer of spin-on-glass (SOG) was present between the two layers for planarization purposes.

- Pre-metal glass: A layer of reflow glass over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts only. No problems were found.

- Contact defects: Contact and via cuts were defined by a two-step process. No over-etching of the contacts or vias was noted.

- A single layer of polycide (tungsten silicide) was used to form all gates on the die and the top plates of all capacitors. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry-etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

- Local oxide (LOCOS) isolation was used with a step present at the well boundary indicating that a twin-well process was employed.

ANALYSIS RESULTS II (continued)

- The EEPROM memory cell consisted of metal 2 program and output lines (via metal 1). Metal 1 formed select, output select, and distributed GND. Polycide formed all gates and the top plates of capacitors. Programming is achieved through a ultra-thin (tunnel) oxide. Cell pitch was 11.3 x 13.5 microns (152 microns^2)

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	N
Die attach quality	G
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	G
Wirebond method	Thermosonic ball bond method using 1.2 mil O.D. gold wire.
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Metal registration	N
Contact coverage	N
Contact registration	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP	BOTTOM
GAL22LV10D LATTICE (LOGO) 4LJ A623A23	9606 KOREA 60 263-07

WIREBOND STRENGTH

Wire material:	1.2 mil O.D. gold
Die pad material:	aluminum
Material at package lands:	silver

Sample #	**1**
# of wires tested:	15
Bond lifts:	0
Force to break - high:	16.0g
- low:	12.0g
- avg.:	13.9g
- std. dev.:	1.0

DIE MATERIAL ANALYSIS

Overlay passivation:	A layer of silicon-nitride over a layer of glass.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Silicide (poly):	Tungsten (W).

HORIZONTAL DIMENSIONS

Die size:	2.2 x 2.7 mm (87 x 107 mils)
Die area:	6.0 mm^2 (9309 $mils^2$)
Min pad size:	0.12 x 0.12 mm (4.8 x 4.8 mils)
Min pad window:	0.1 x 0.1 mm (4.0 x 4.0 mils)
Min pad space:	44 microns
Min metal 2 width:	1.0 micron
Min metal 2 space:	2.1 microns
Min metal 2 pitch:	3.3 microns
Min metal 1 width:	0.9 micron
Min metal 1 space:	1.1 micron
Min metal 1 pitch:	2.1 microns
Min via:	1.0 micron
Min contact:	1.0 micron
Min polycide width:	0.4 micron
Min polycide space:	1.1 micron
Min gate length* - (N-channel):	0.4 micron
- (P-channel):	0.45 micron
Cell pitch:	11.3 x 13.5 microns
Cell size:	152.5 $microns^2$

**Physical gate length*

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (20 mils)

Layers:

Passivation 2:	0.5 micron
Passivation 1:	0.25 micron
Metal 2 - cap:	0.05 micron (approximate)
- aluminum:	0.8 micron
- barrier:	0.1 micron
Interlevel dielectric - glass 2:	0.5 micron
- glass 1:	0.4 micron (average)
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.5 micron
- barrier:	0.12 micron
Intermediate glass:	0.5 micron (average)
Oxide on polycide:	0.15 micron
Polycide - silicide:	0.12 micron
- poly:	0.12 micron
Local oxide:	0.35 micron
N+ S/D:	0.17 micron
P+ S/D:	0.2 micron
N-well:	3 microns
P-well:	3 microns

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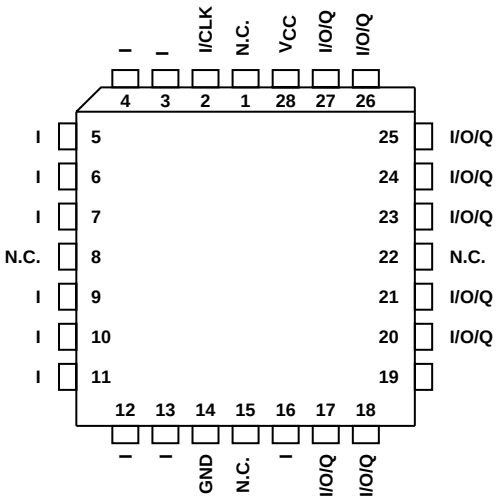


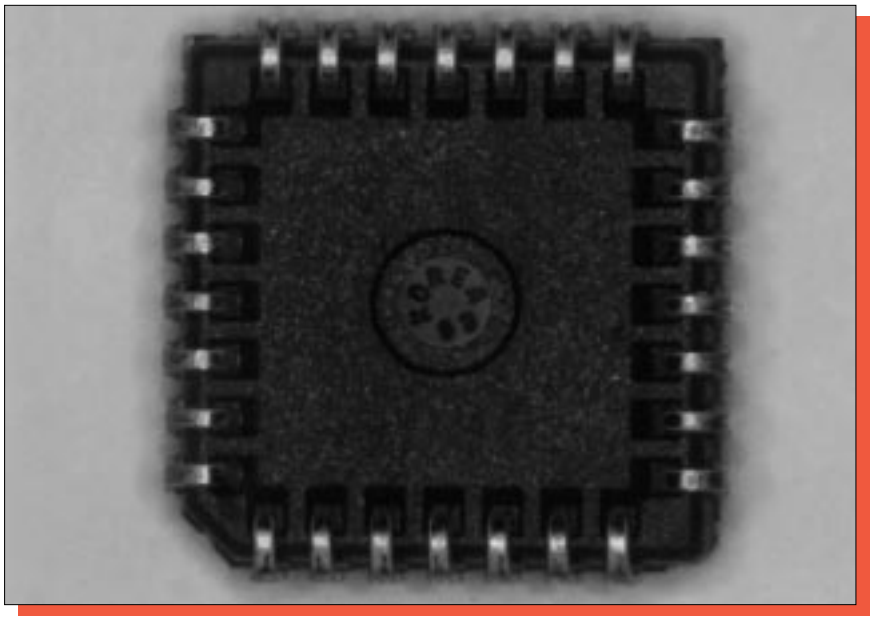
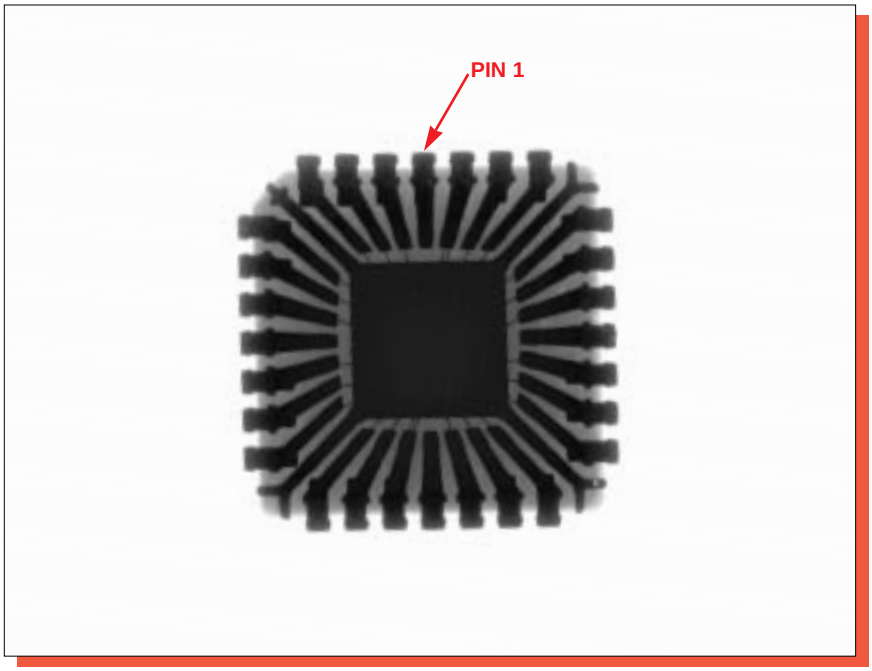
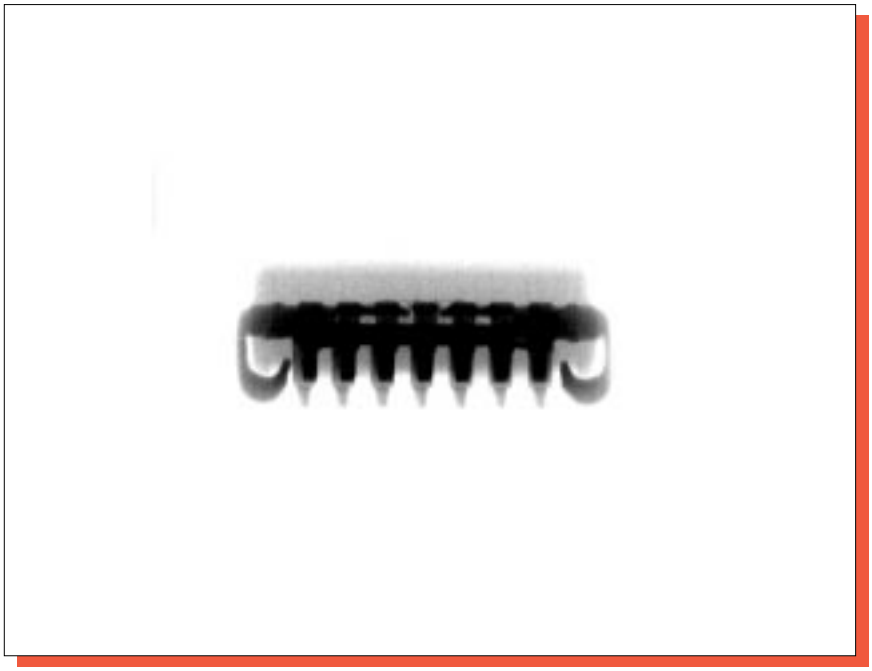


Figure 1. Package photographs and pinout of the Lattice GAL22LV10D PLD.
Mag. 5.7x.

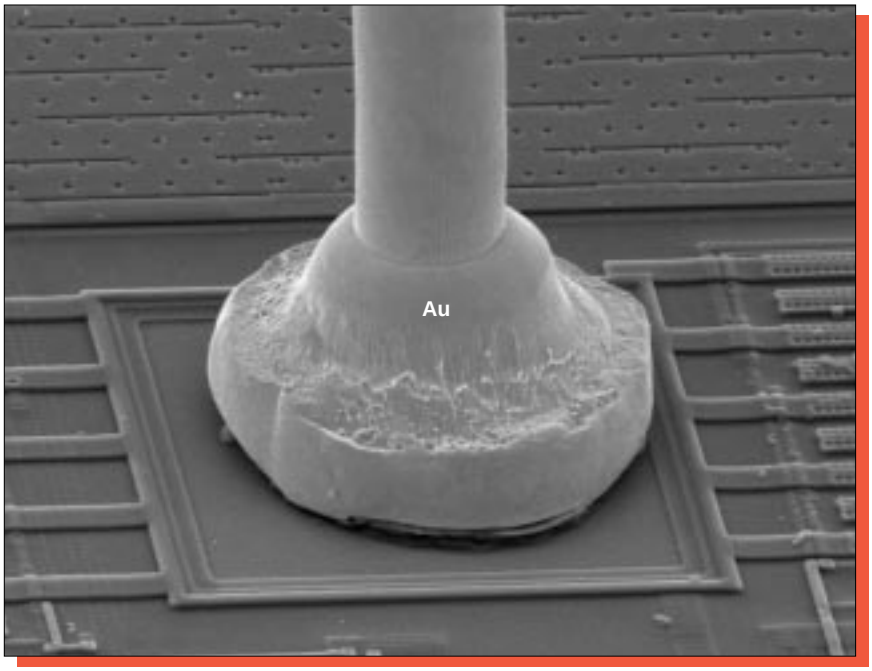


top



side

Figure 2. X-ray views of the package. Mag. 4x.



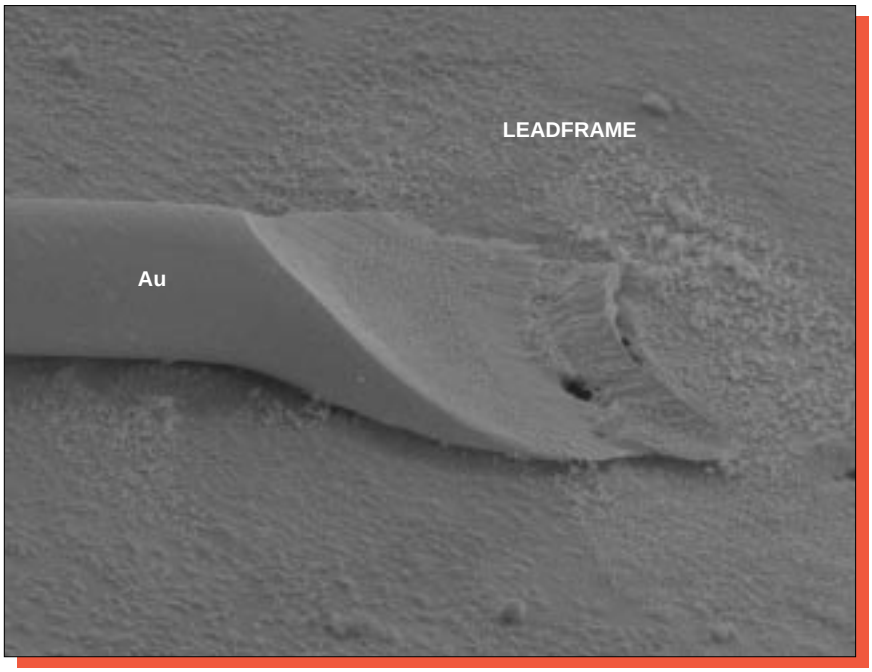
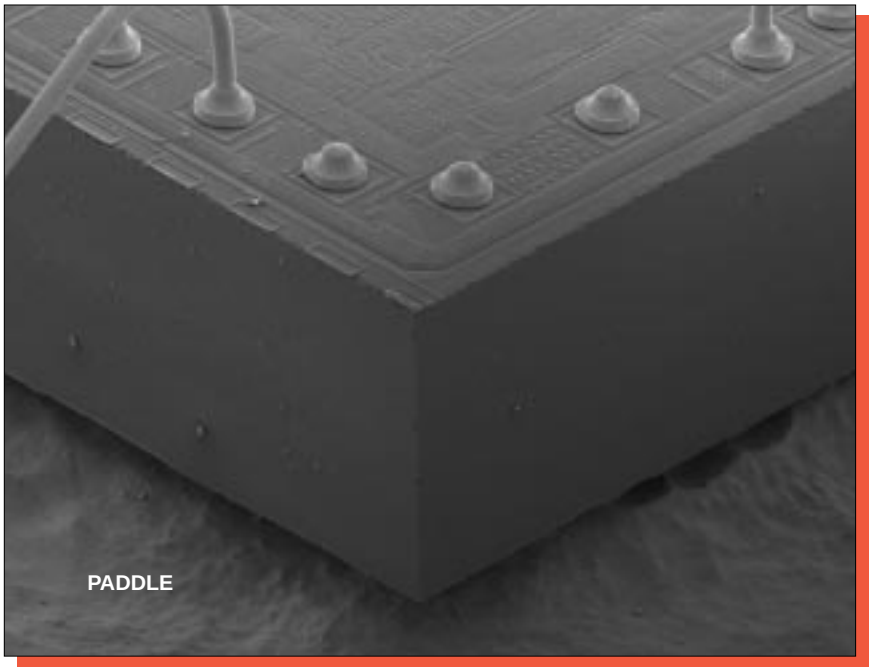
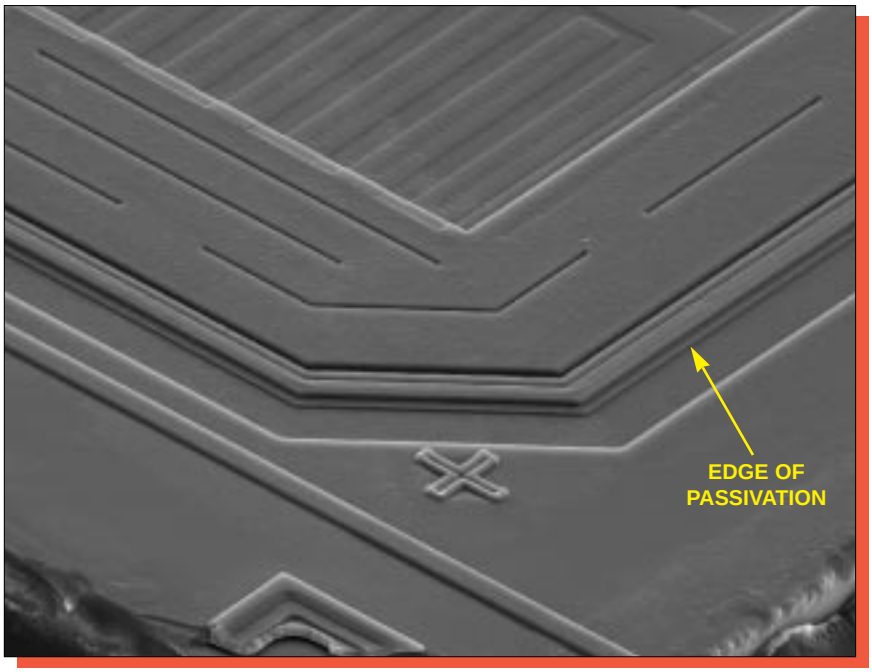


Figure 3. SEM views of typical wire bonding. Mag. 620x, 60°.

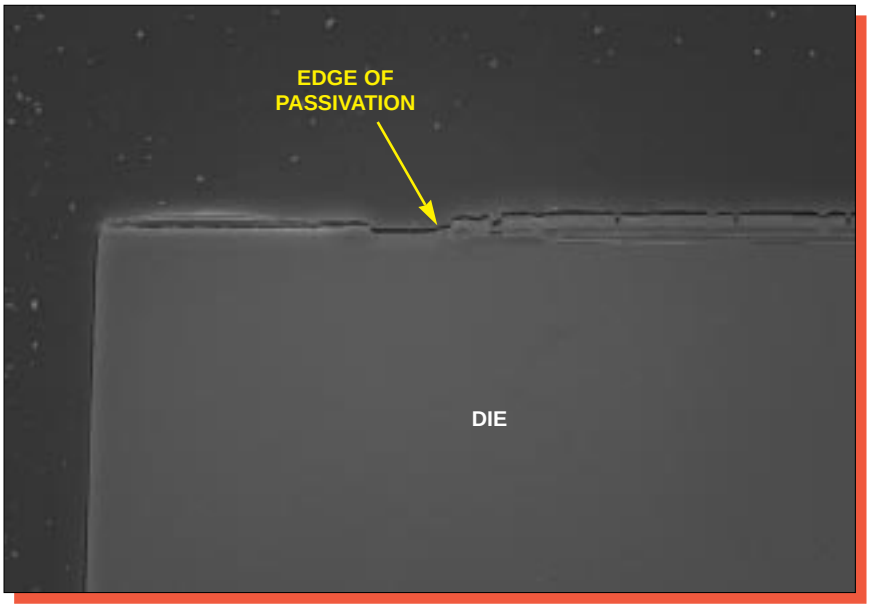


Mag. 90x

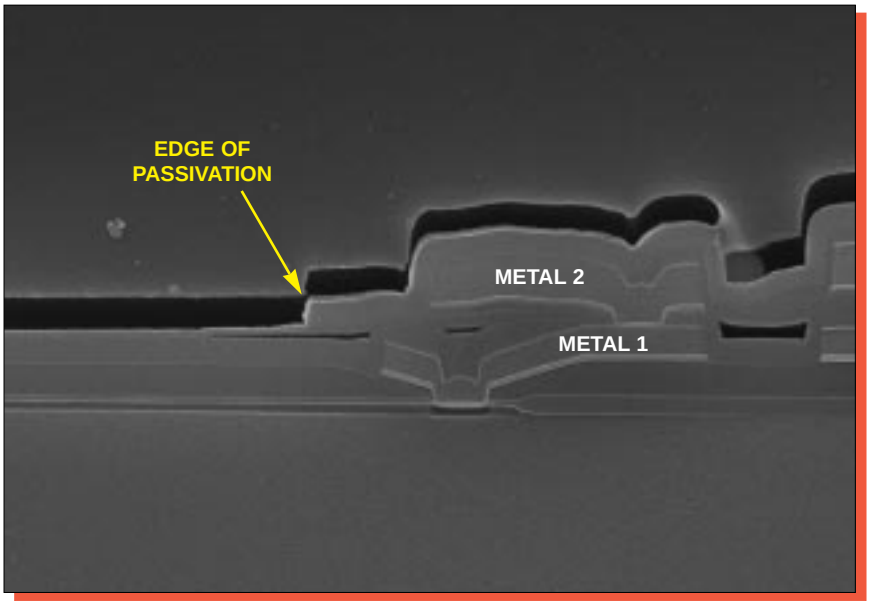


Mag. 740x

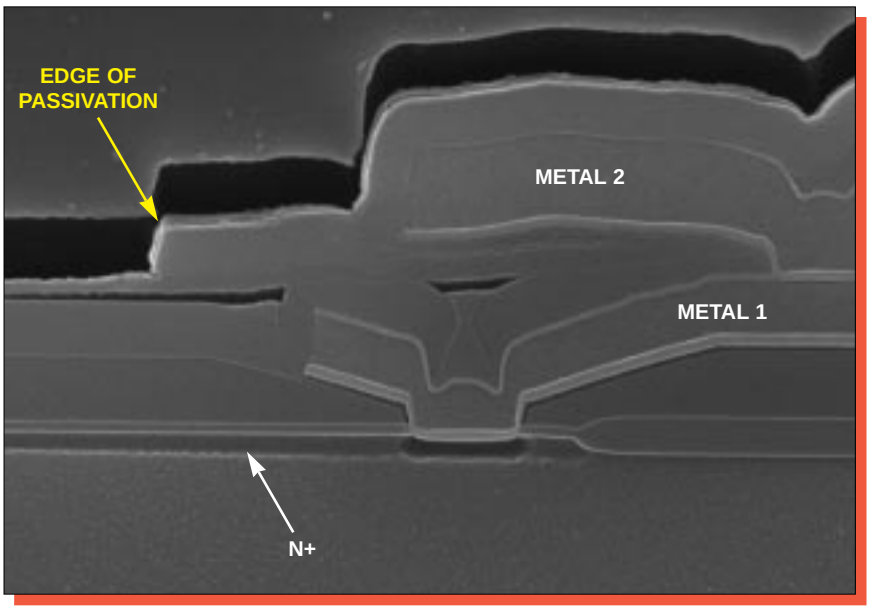
Figure 4. SEM views of dicing and edge seal. 60°.



Mag. 800x



Mag. 6500x



Mag. 13,000x

Figure 5. SEM section views of the edge seal.

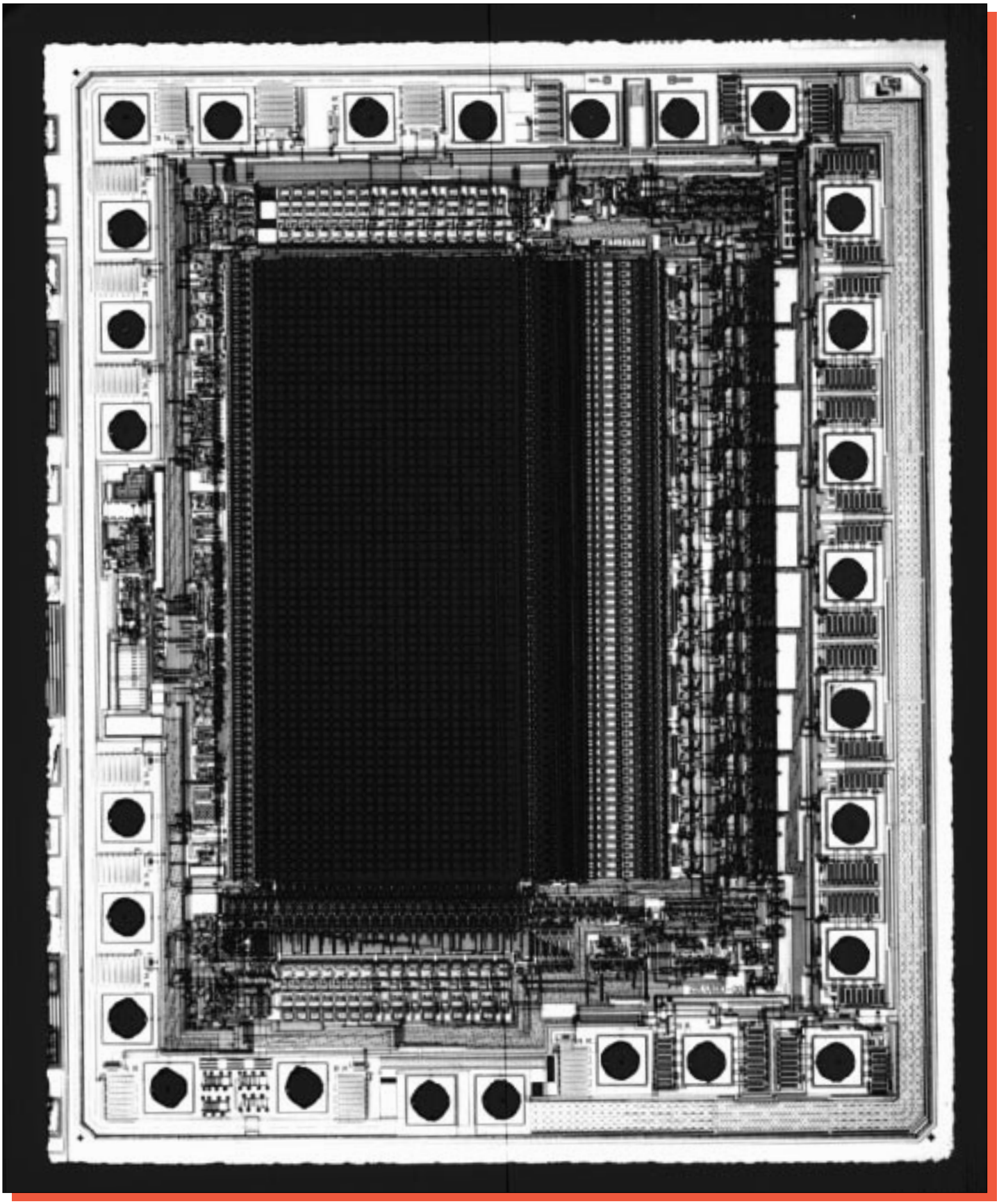
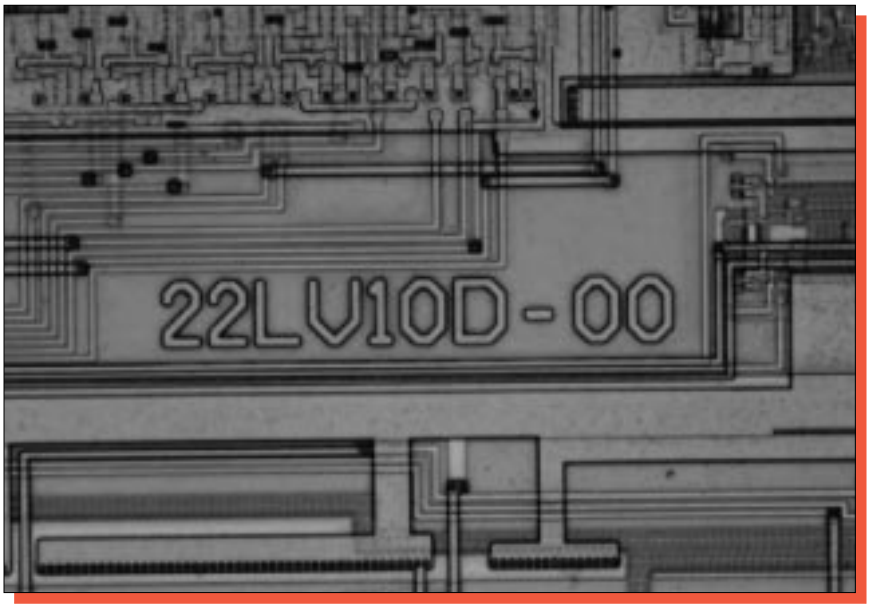


Figure 6. Whole die photograph of the Lattice GAL22LV10D. Mag. 75x.



Mag. 500x

Mag. 800x

Mag. 800x

Figure 7. Optical views of die markings.

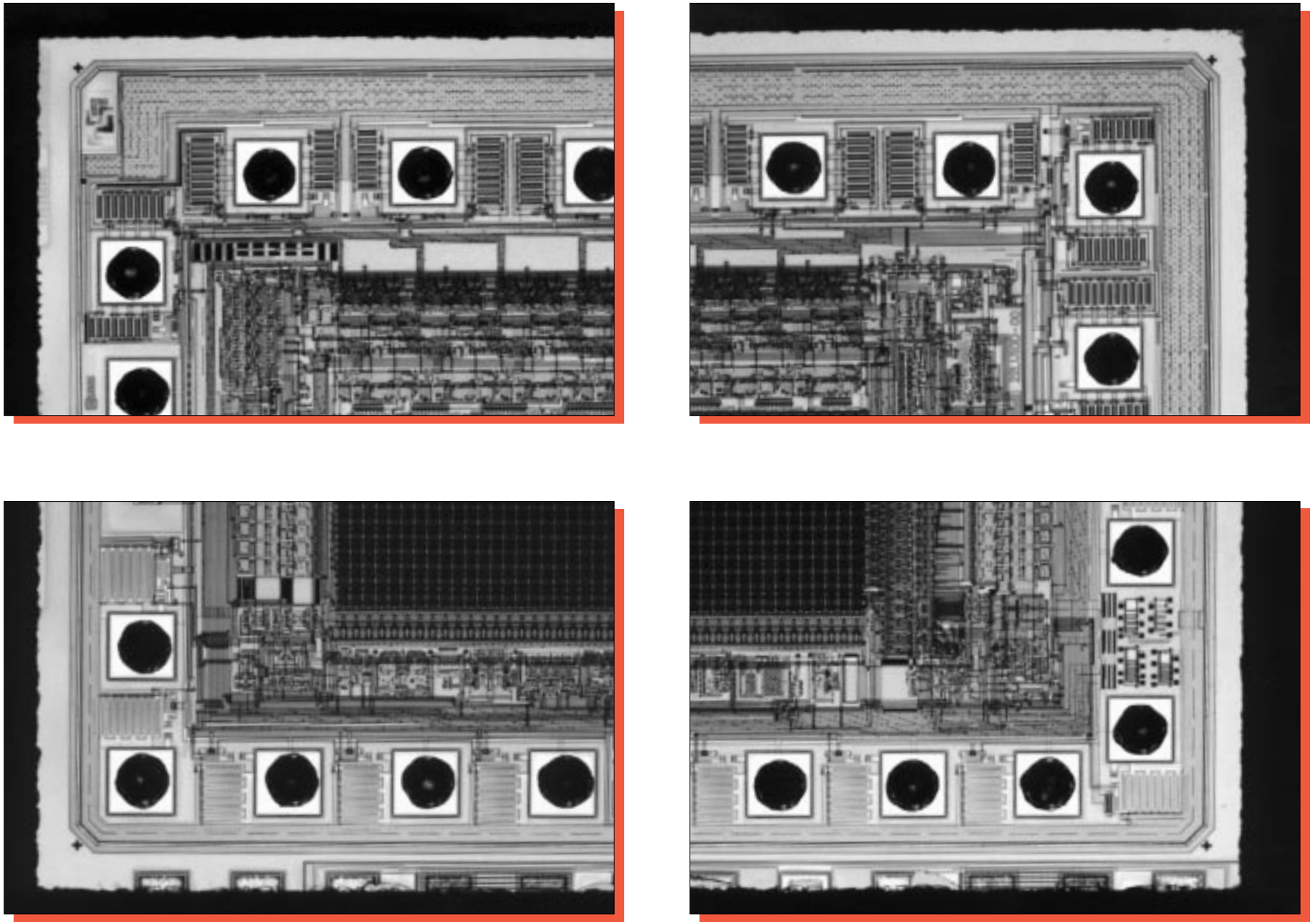
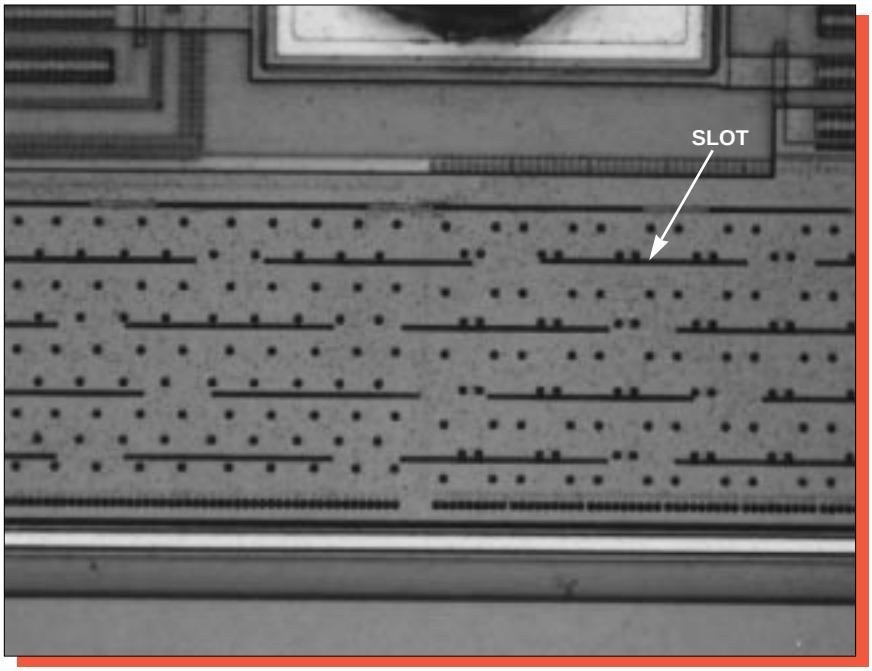
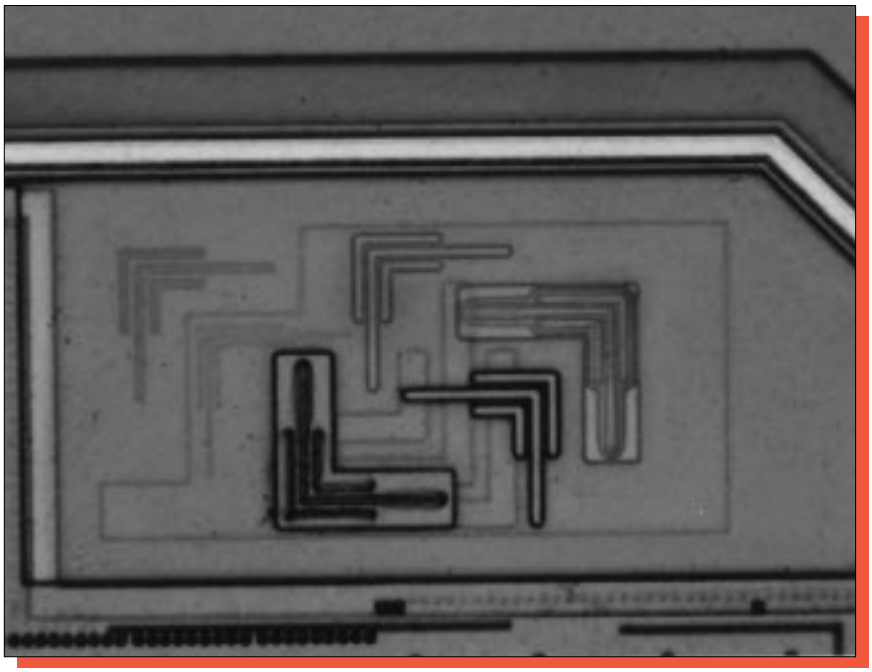


Figure 8. Optical views of die corners. Mag. 100x.

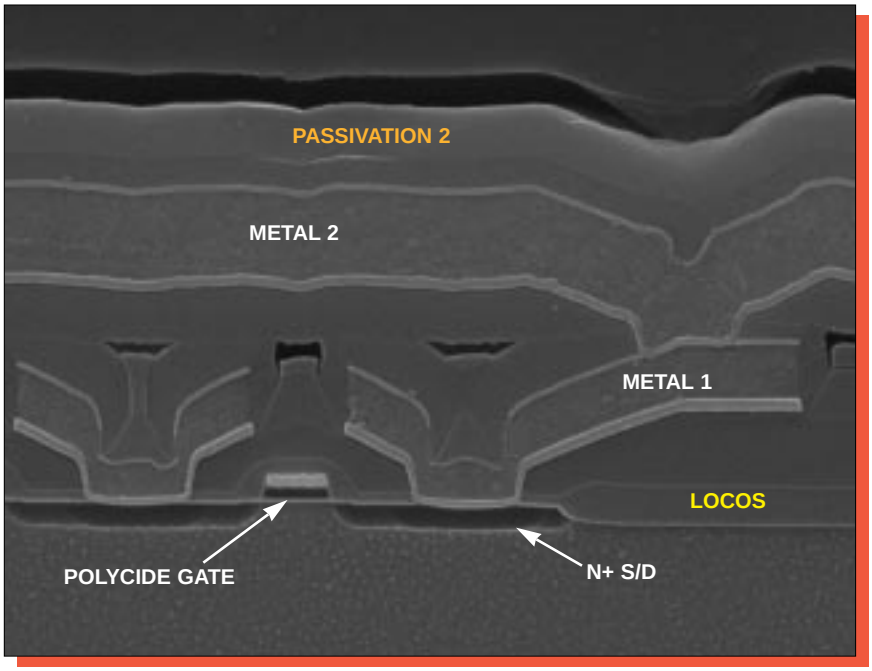


Mag. 500x



Mag. 800x

Figure 9. Optical views of a slotted bus line and a resolution pattern.



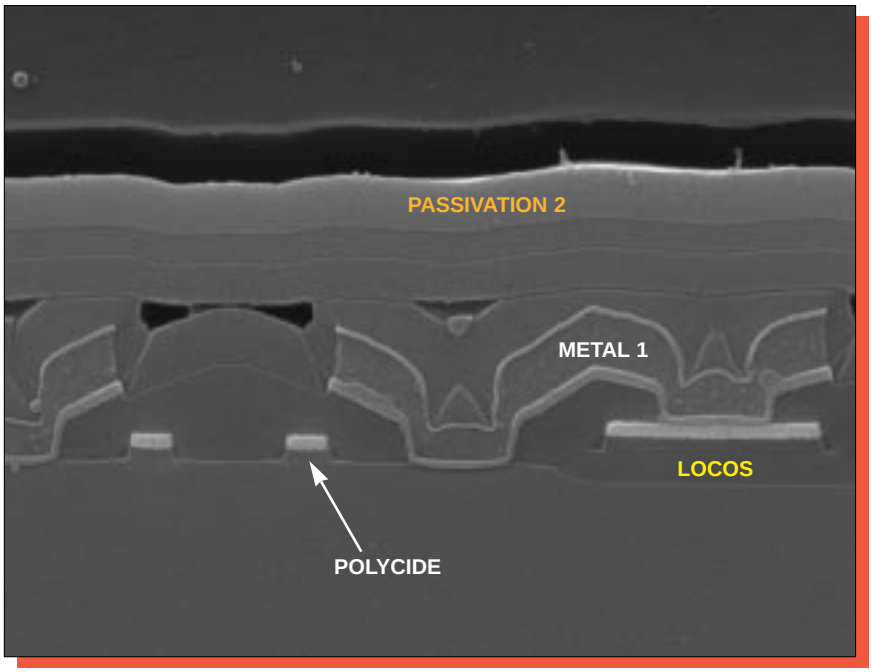
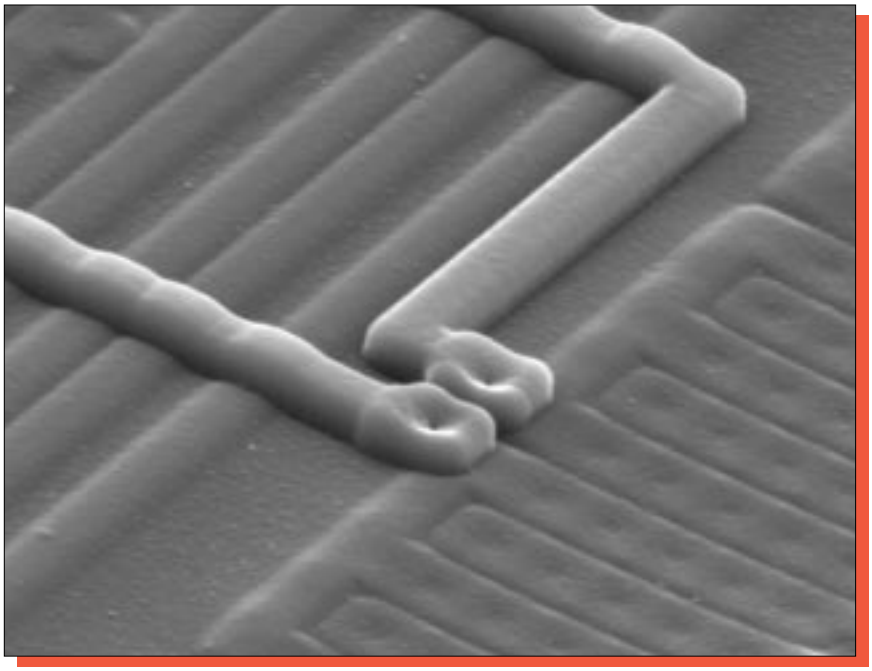
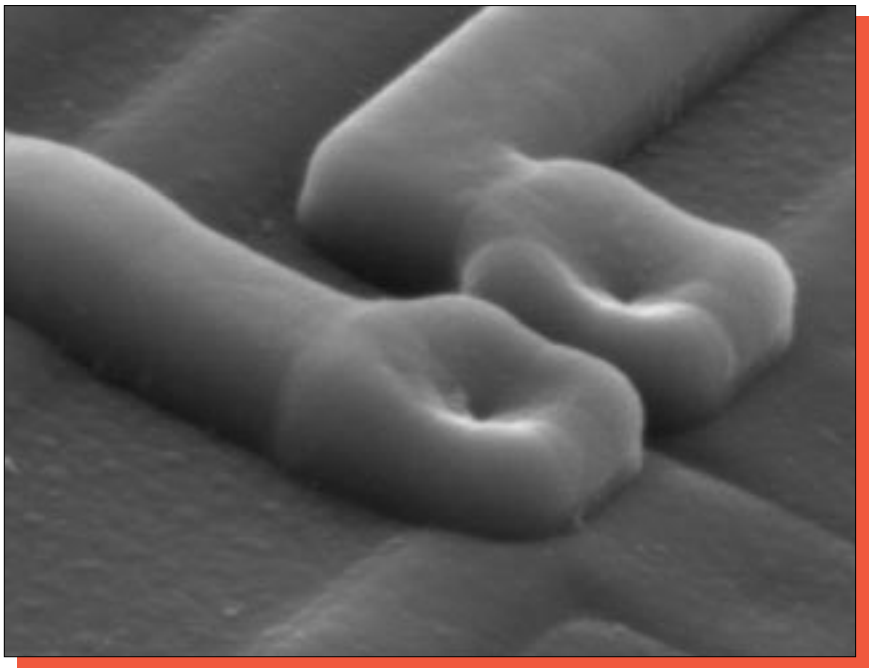


Figure 10. SEM section views illustrating general structure. Mag. 13,000x.

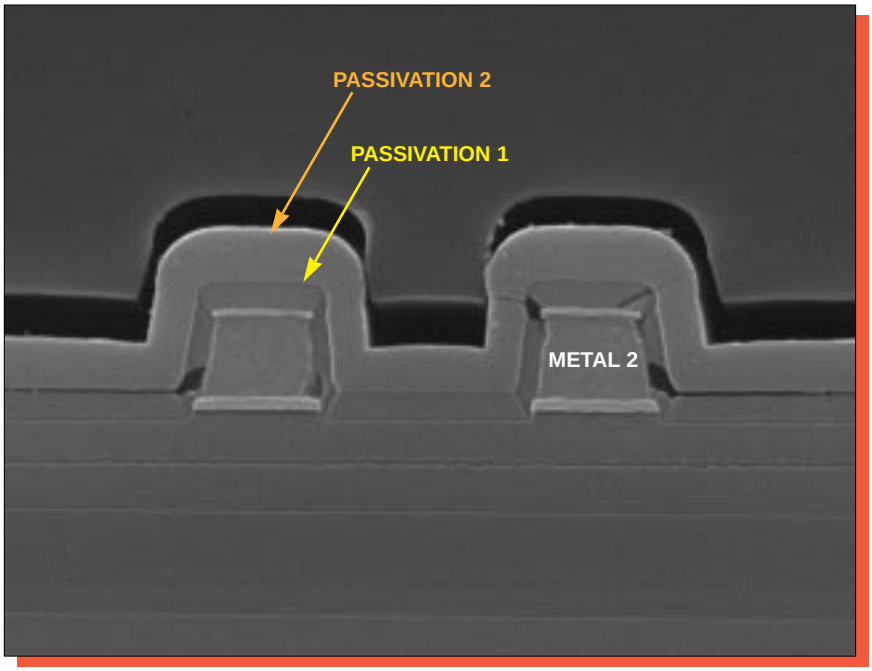


Mag. 4600x

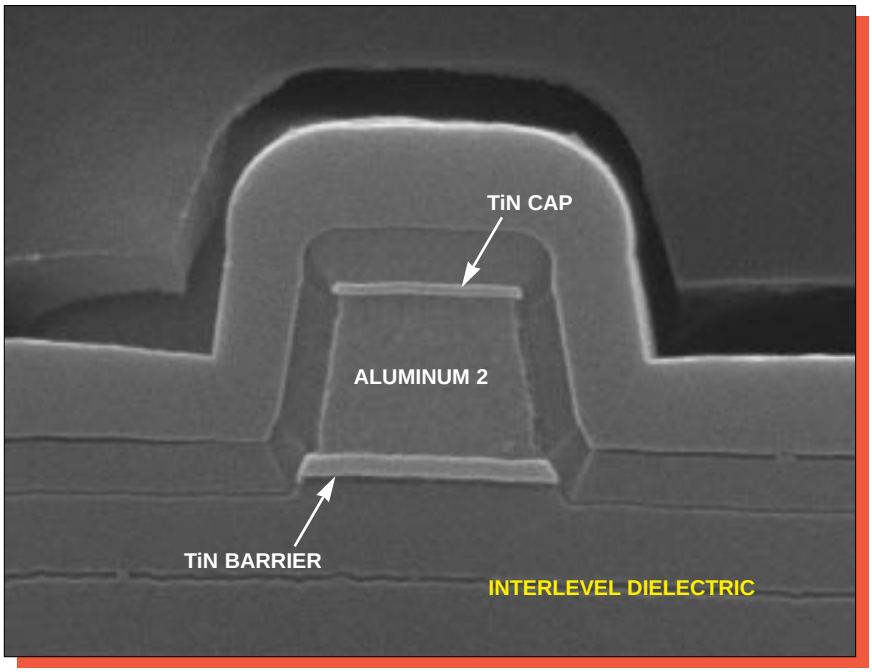


Mag. 12,000x

Figure 11. SEM views illustrating passivation overlay. 60°.



Mag. 13,000x



Mag. 26,000x

Figure 12. SEM section views illustrating metal 2 line profiles.

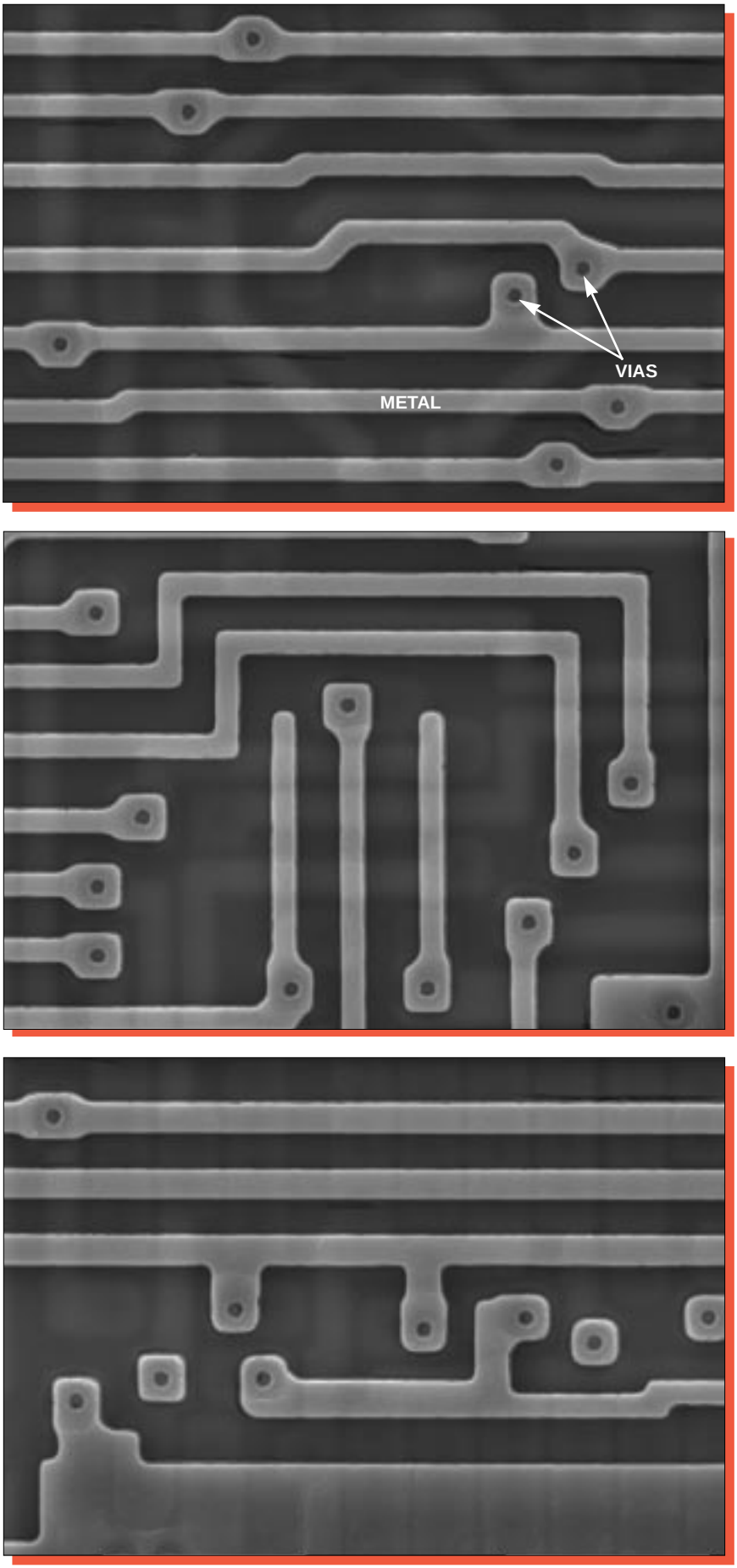
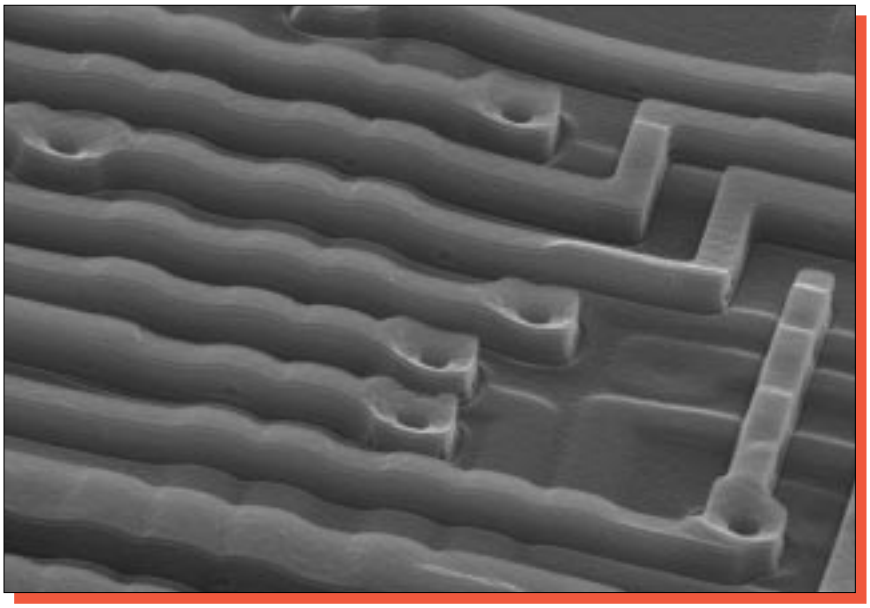
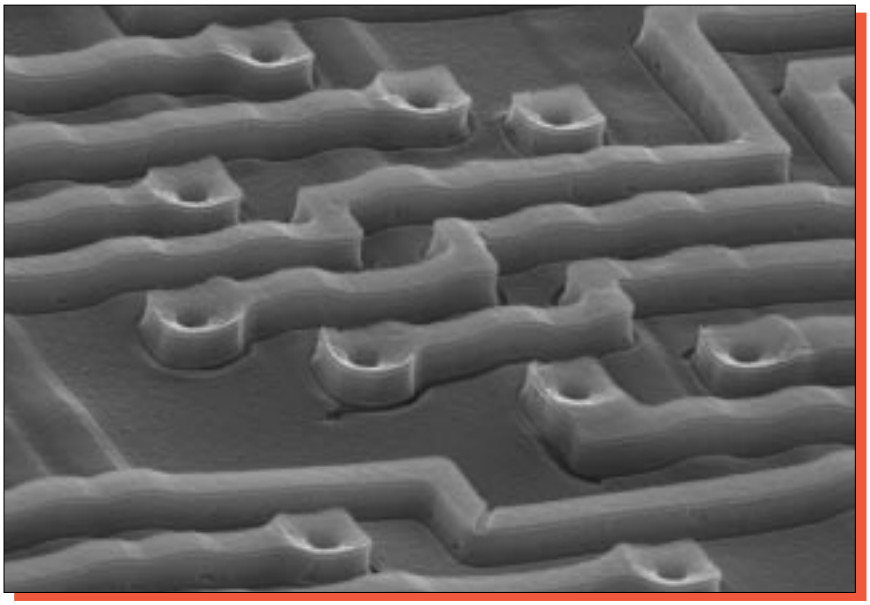


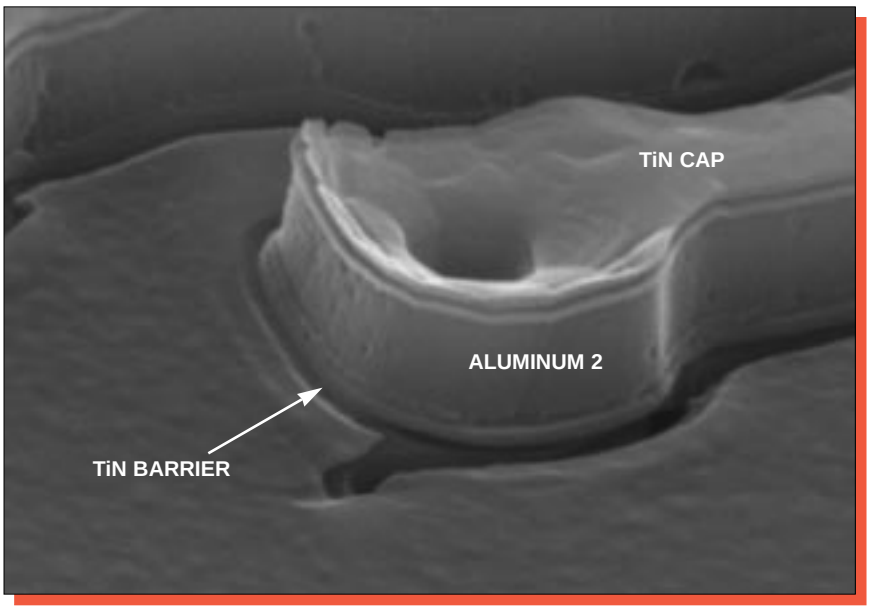
Figure 13. Topological SEM views of metal 2 patterning. Mag. 3200x, 0°.



Mag. 5000x

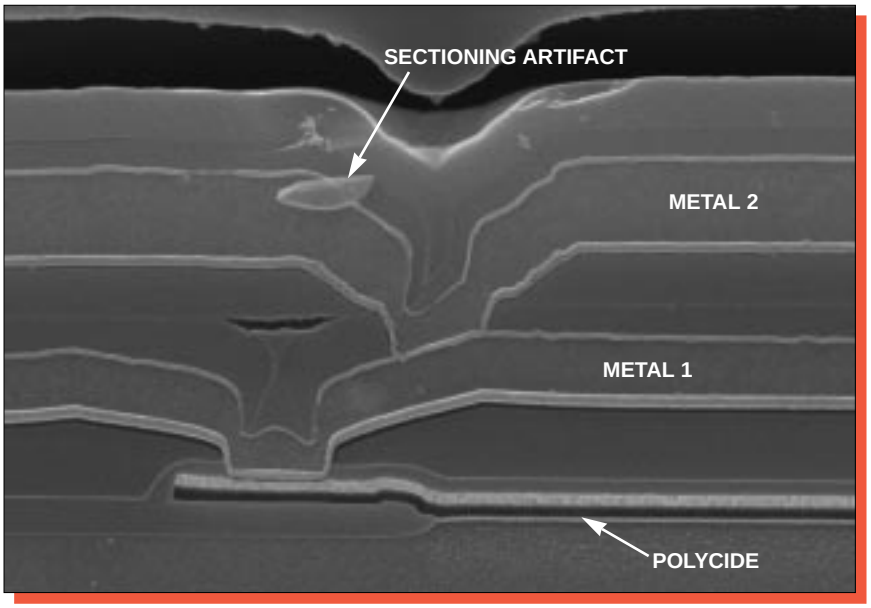


Mag. 5000x

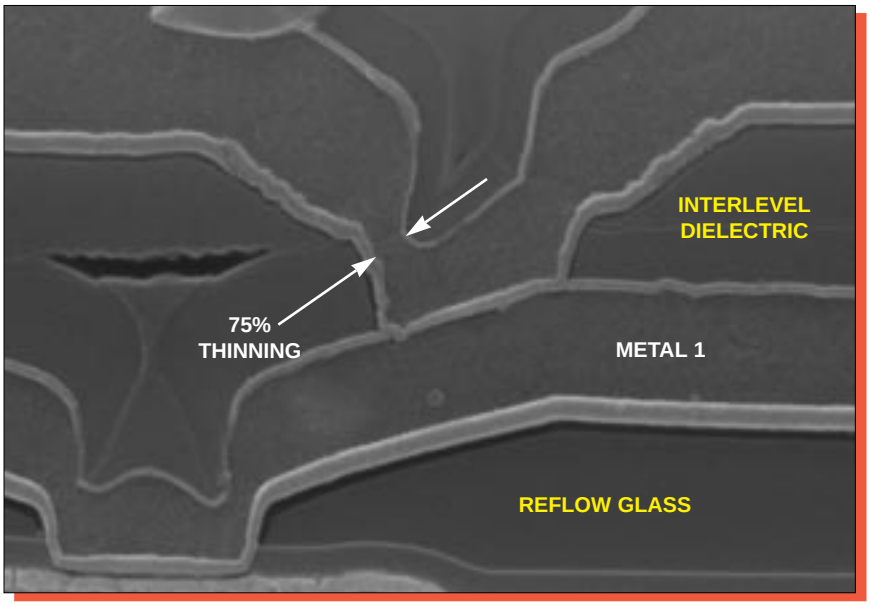


Mag. 20,000x

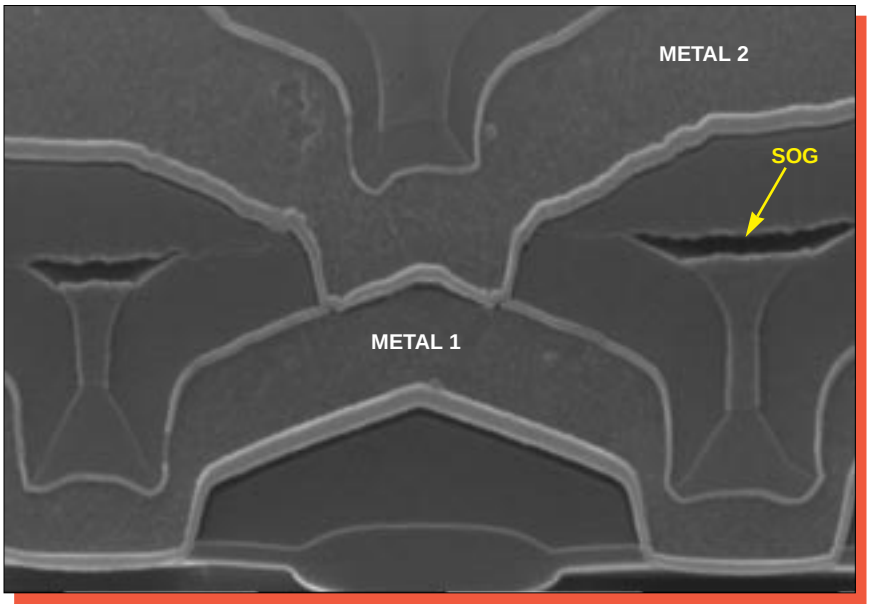
Figure 14. Perspective SEM views of metal 2 step coverage. 60°.



Mag. 13,000x

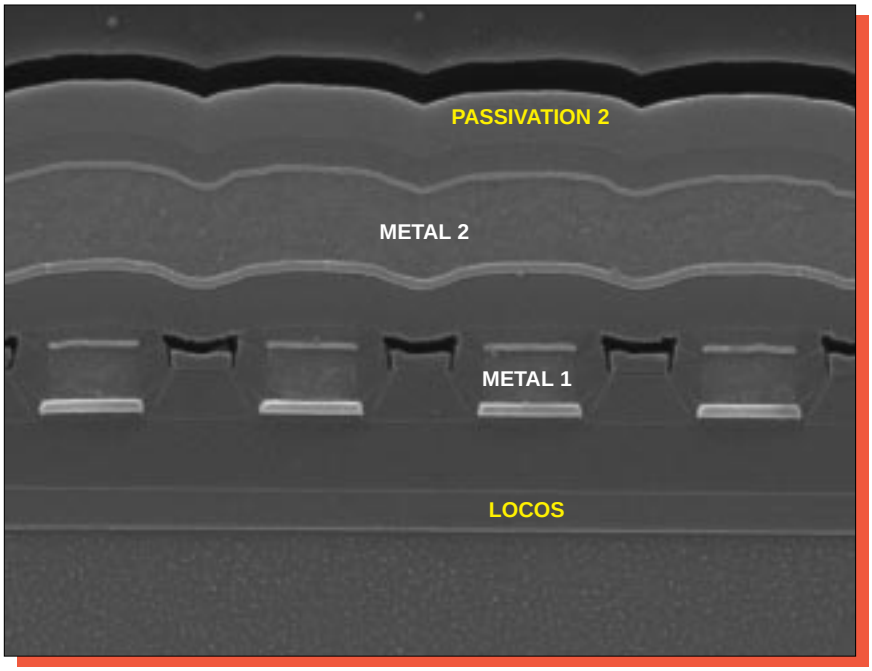


Mag. 26,000x

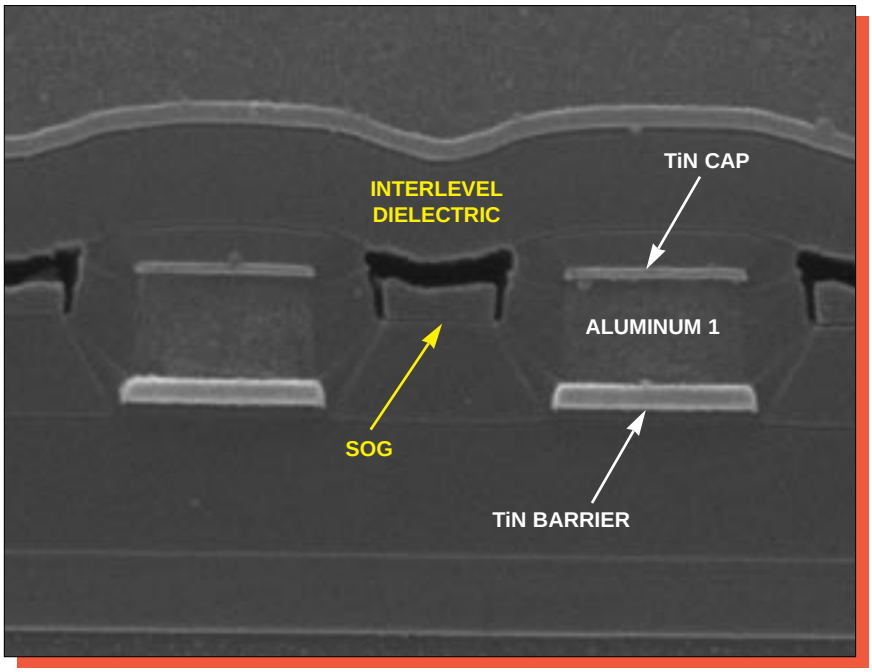


Mag. 26,000x

Figure 15. SEM section views illustrating metal vias and interlevel dielectric composition.

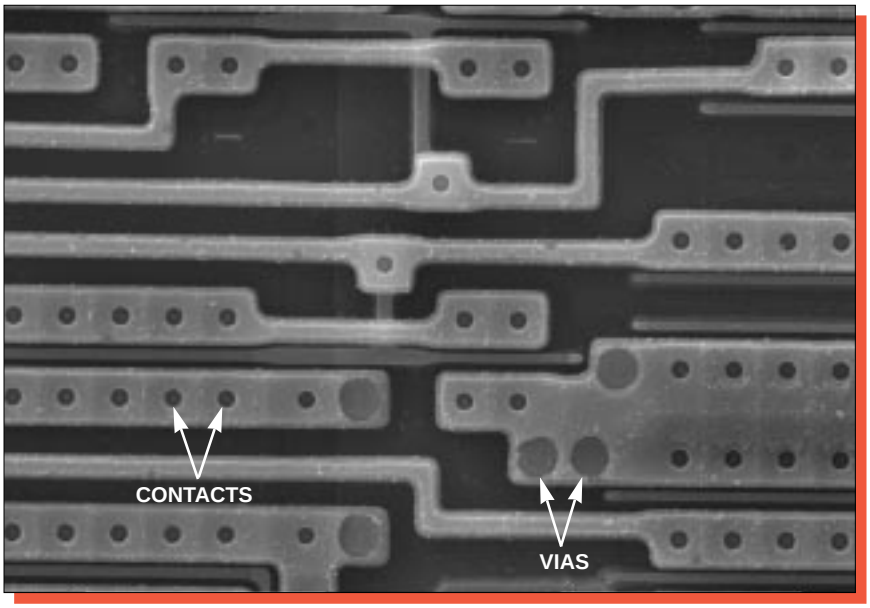


Mag. 13,000x

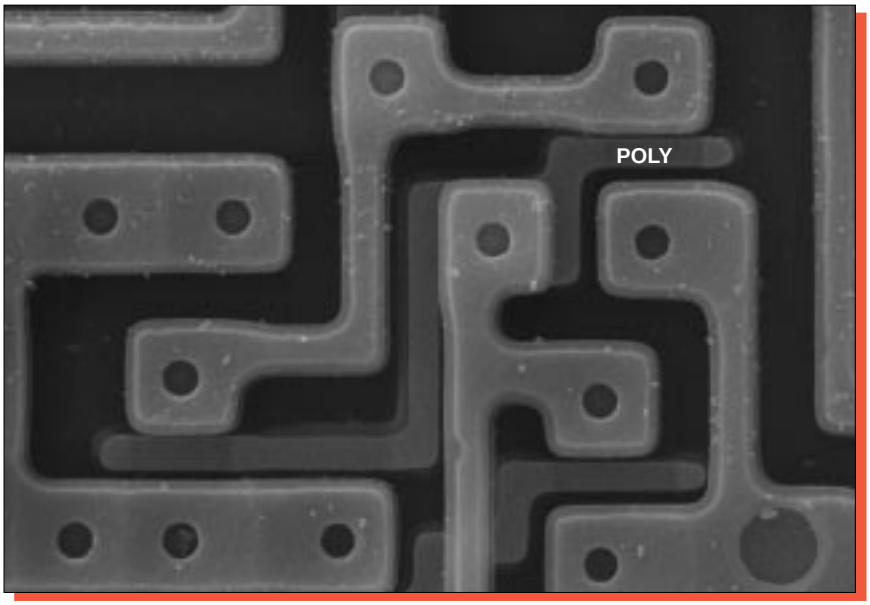


Mag. 26,000x

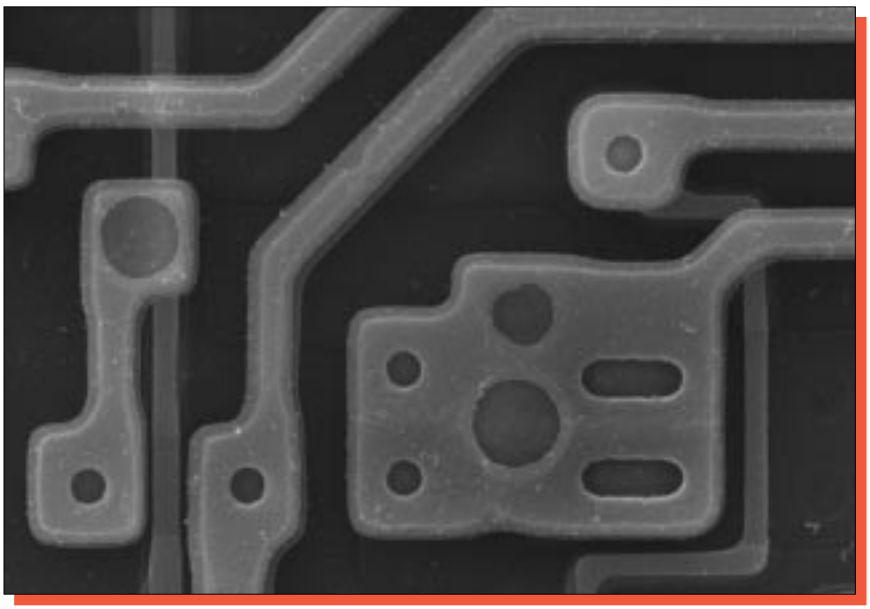
Figure 16. SEM section views of metal 1 line profiles.



Mag. 3200x

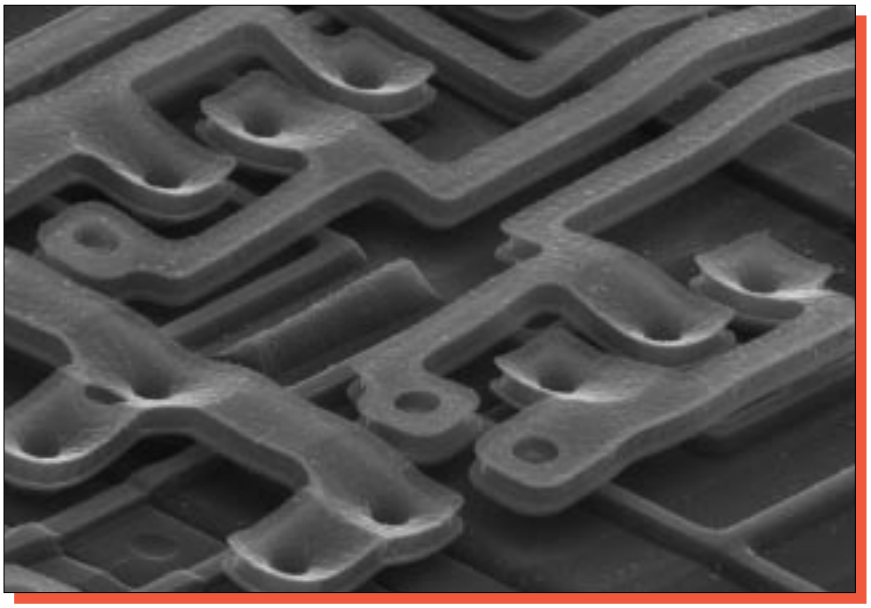


Mag. 6500x

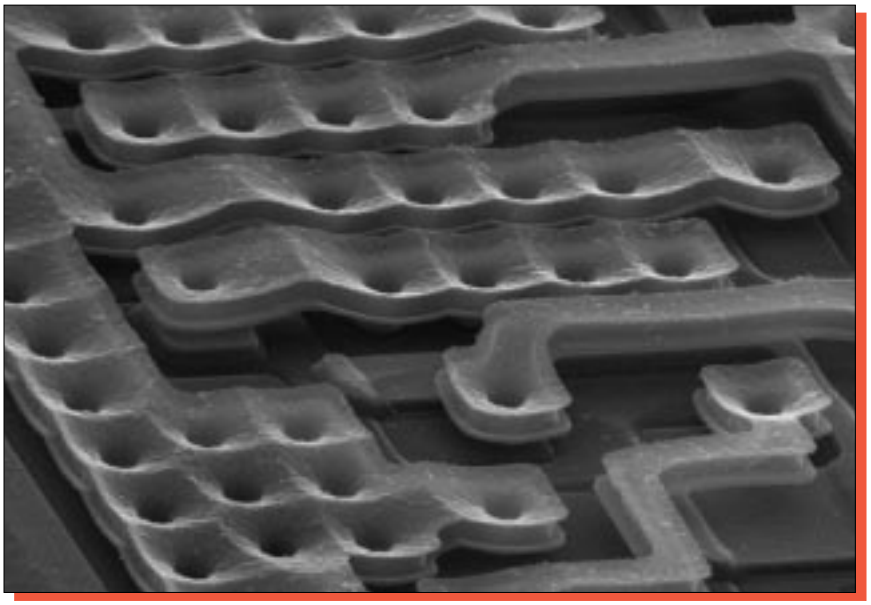


Mag. 6500x

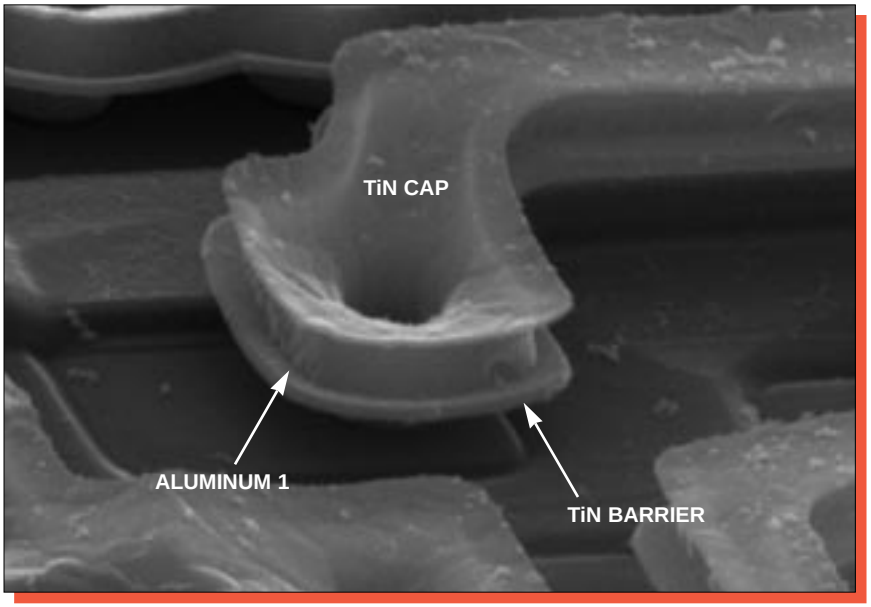
Figure 17. Topological SEM views of metal 1 patterning. 0°.



Mag. 6500x



Mag. 6500x



Mag. 18,000x

Figure 18. Perspective SEM views of metal 1 step coverage. 60°.

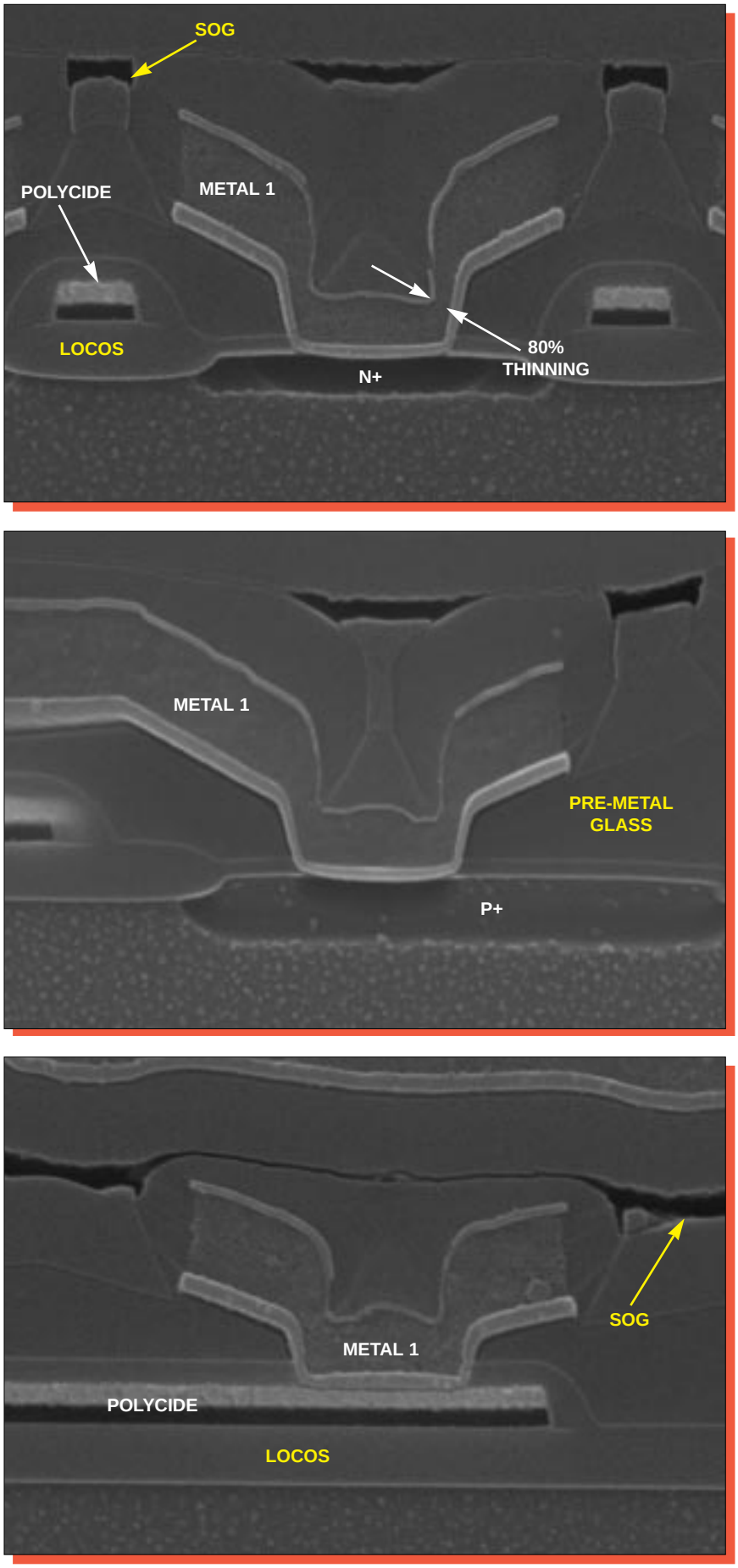
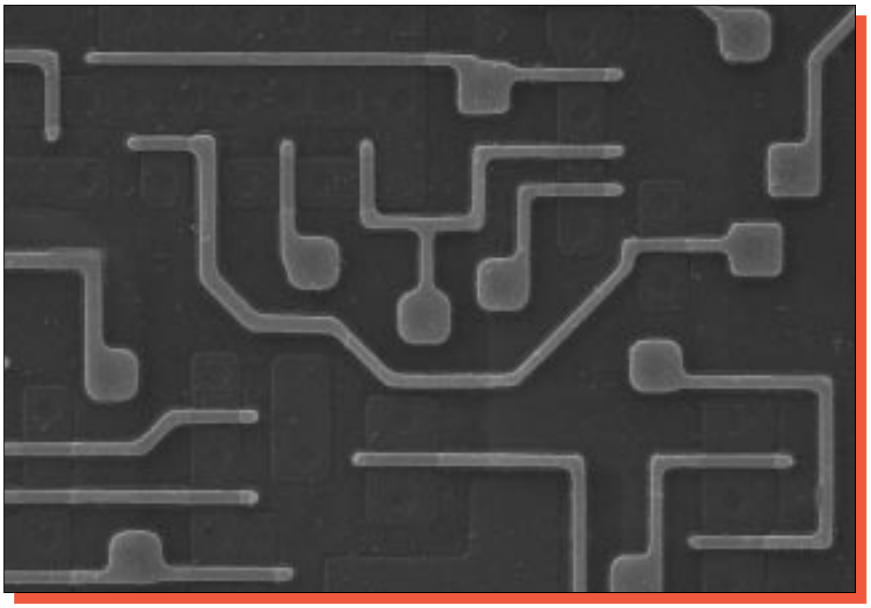
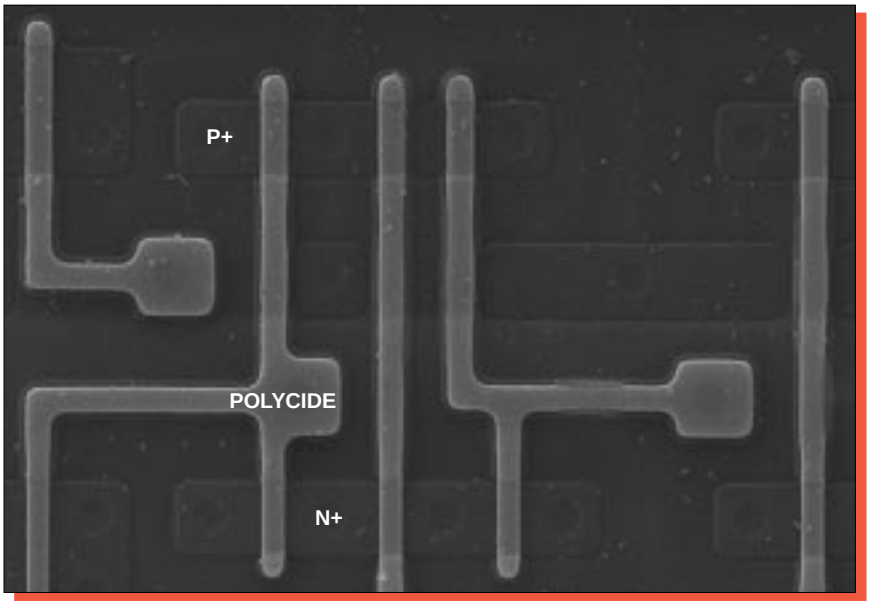


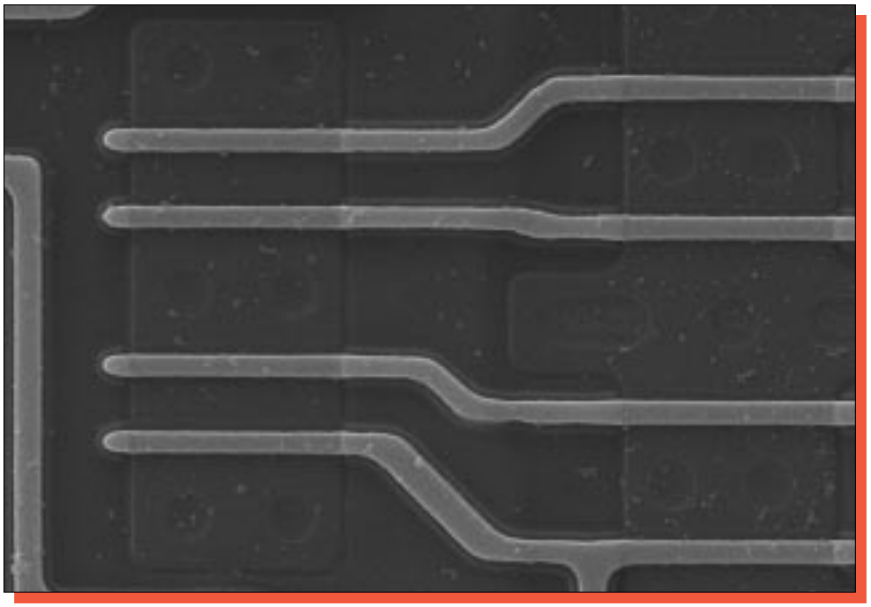
Figure 19. SEM section views of typical metal 1 contacts. Mag. 26,000x.



Mag. 3200x

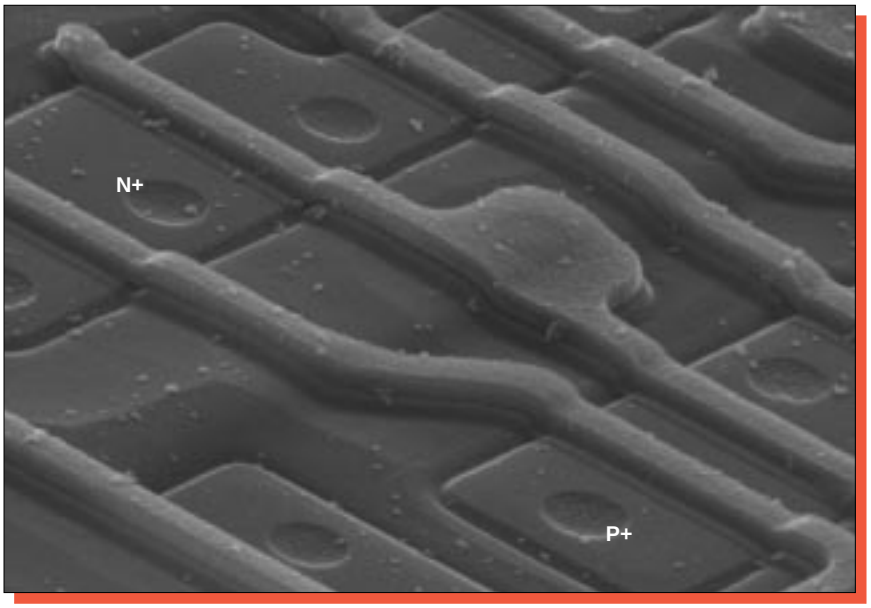


Mag. 5000x

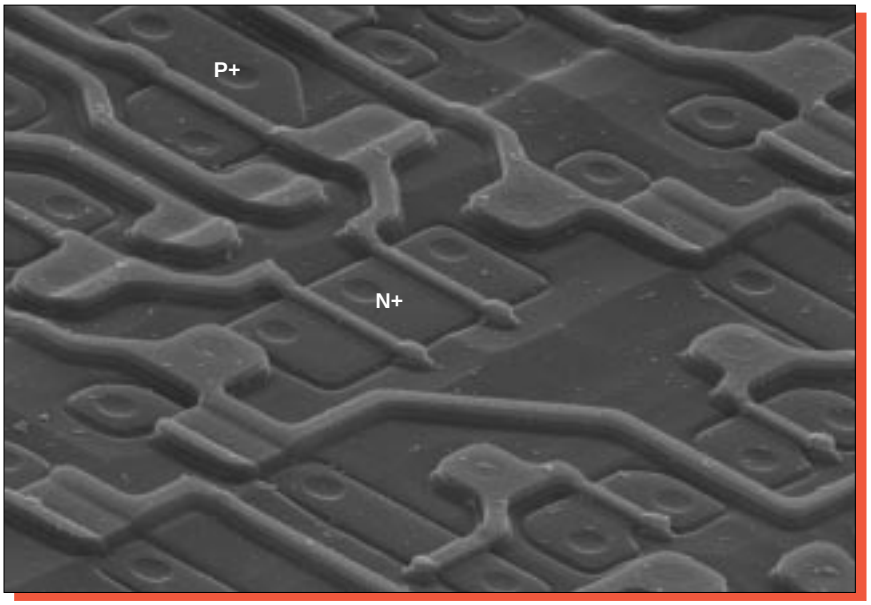


Mag. 6500x

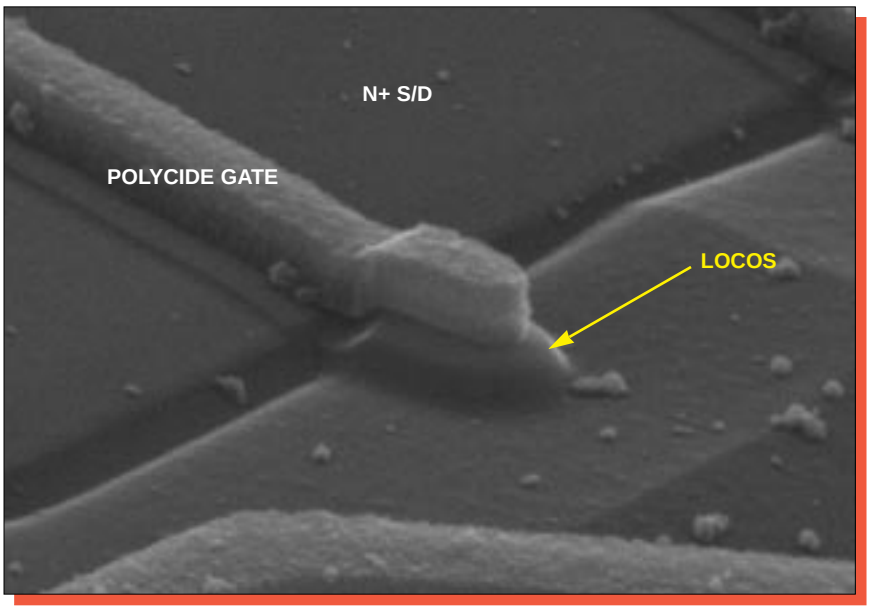
Figure 20. Topological SEM views illustrating polycide patterning. 0°.



Mag. 12,000x

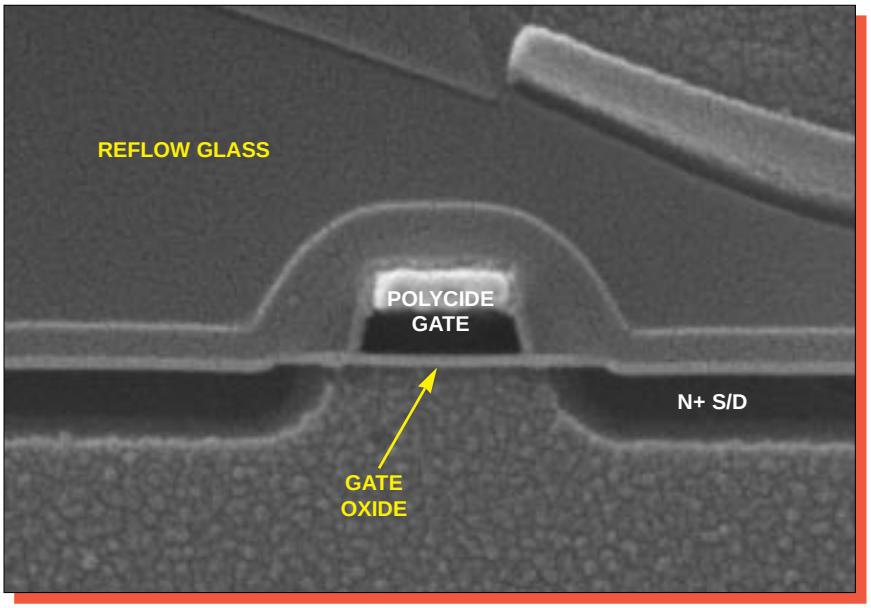


Mag. 6000x

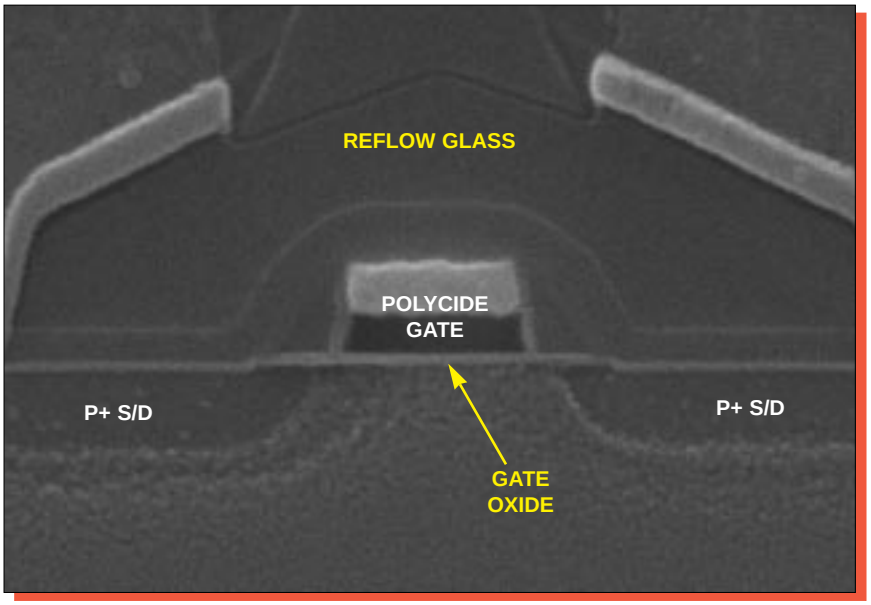


Mag. 34,000x

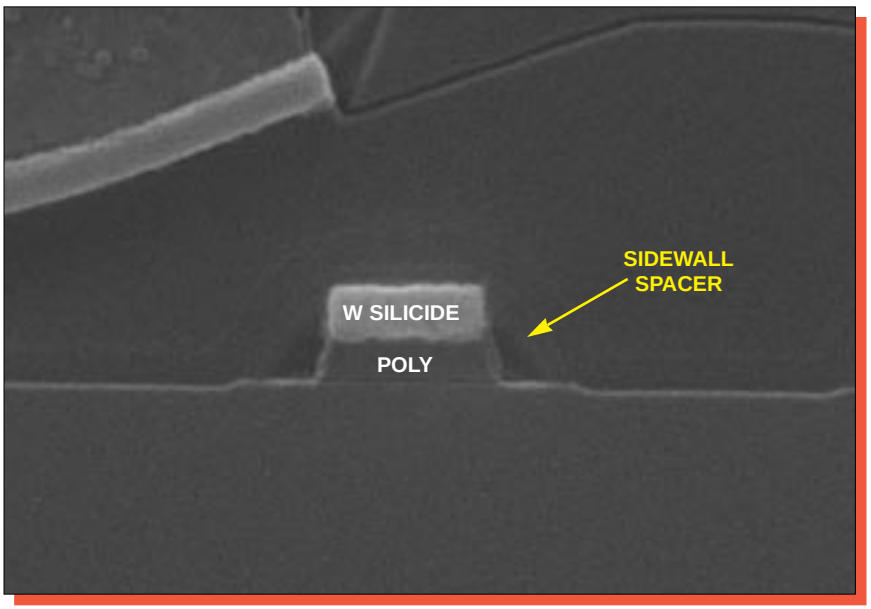
Figure 21. Perspective SEM views illustrating polycide coverage. 60°.



N-channel

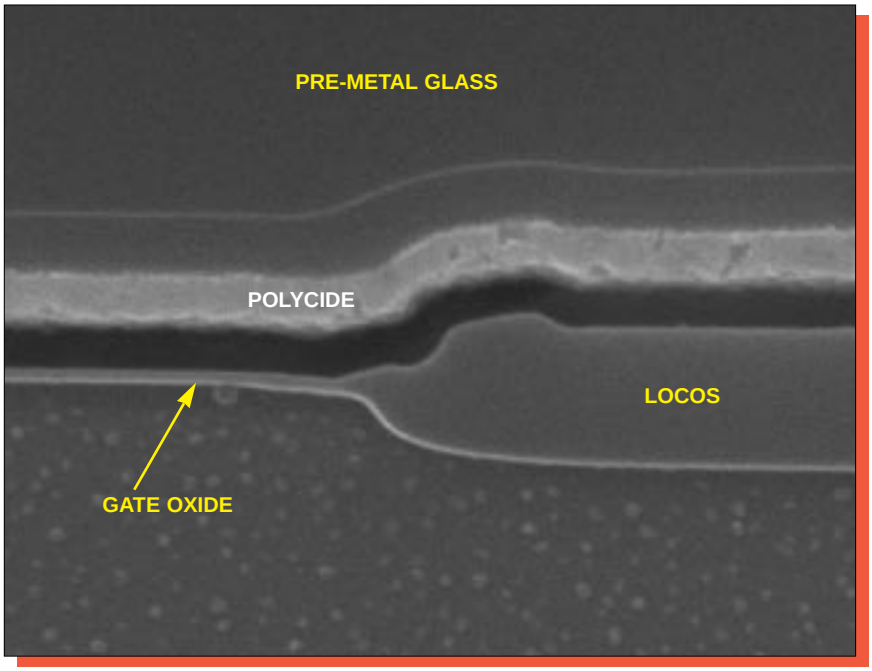


P-channel

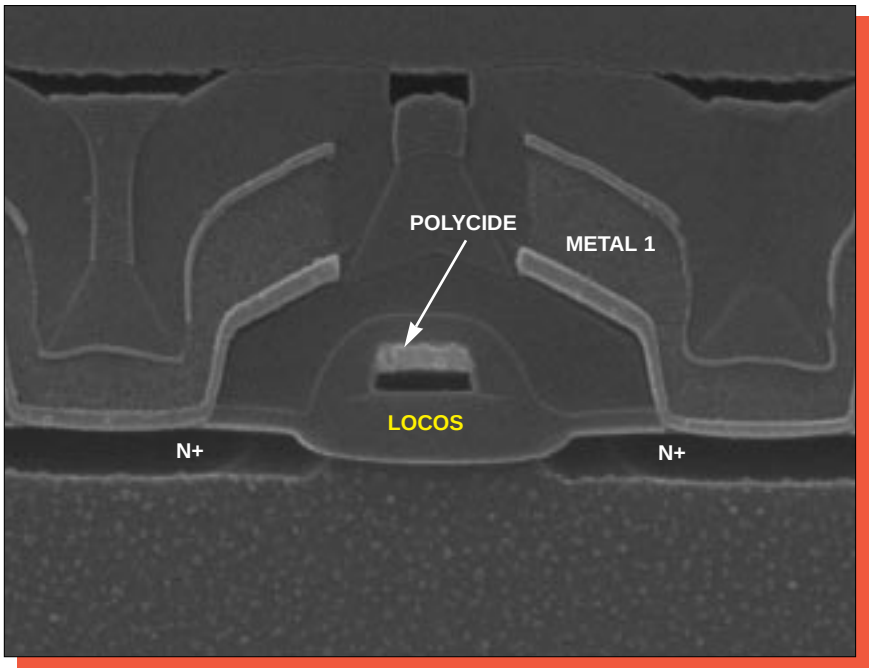


glass etch

Figure 22. SEM section views of typical transistors. Mag. 52,000x.

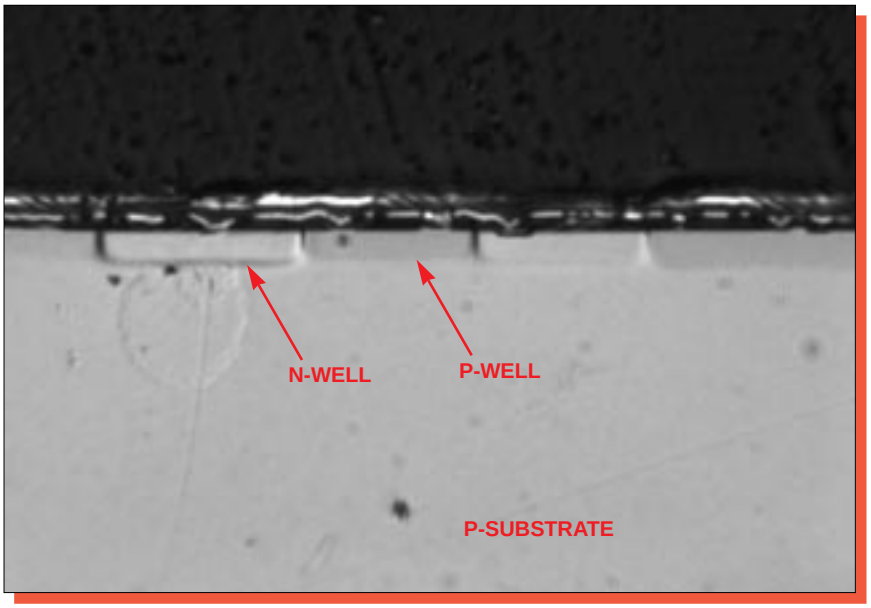


Mag. 52,000x

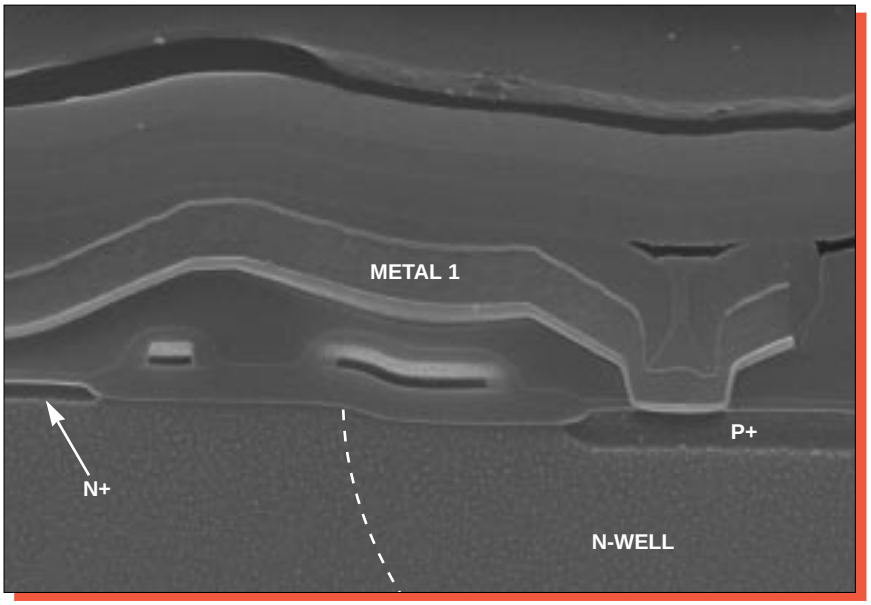


Mag. 26,000x

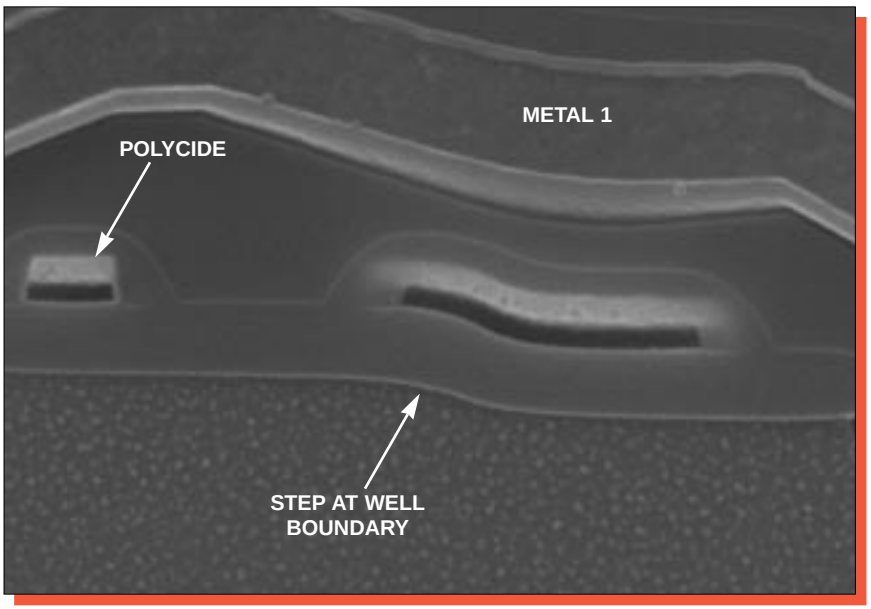
Figure 23. SEM section views of a typical birdsbeak and field oxide isolation.



Mag. 1200x

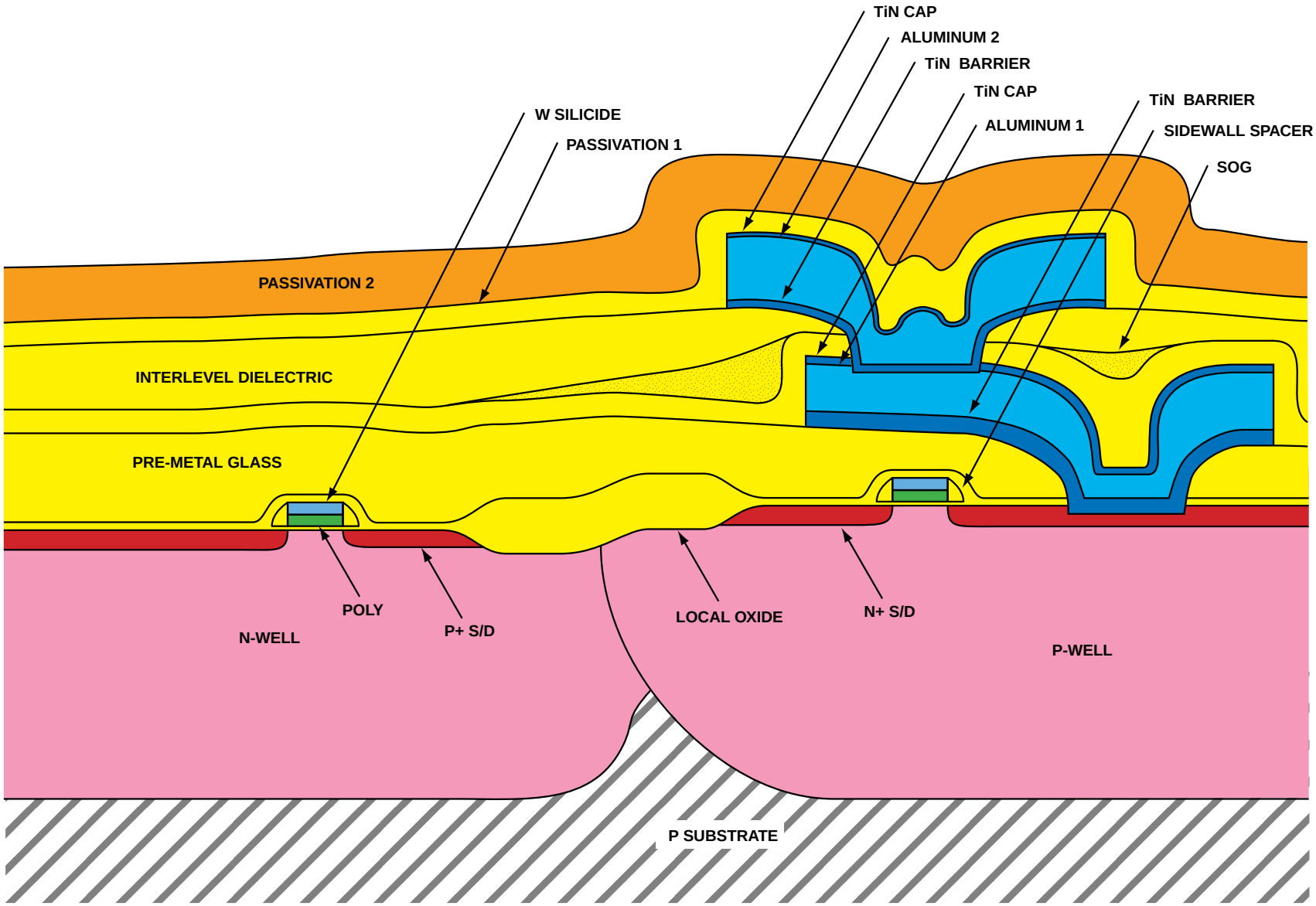


Mag. 13,000x



Mag. 26,000x

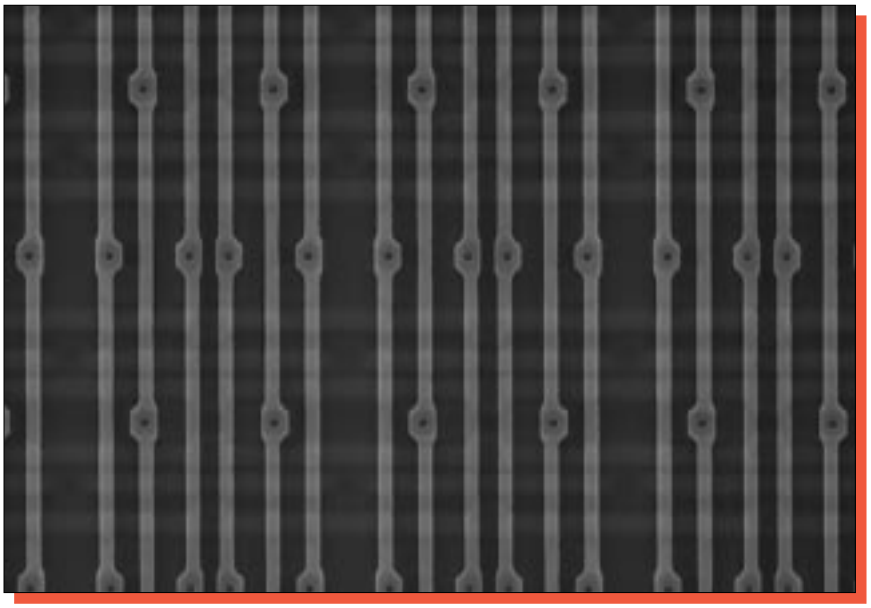
Figure 24. Section views illustrating well structure.



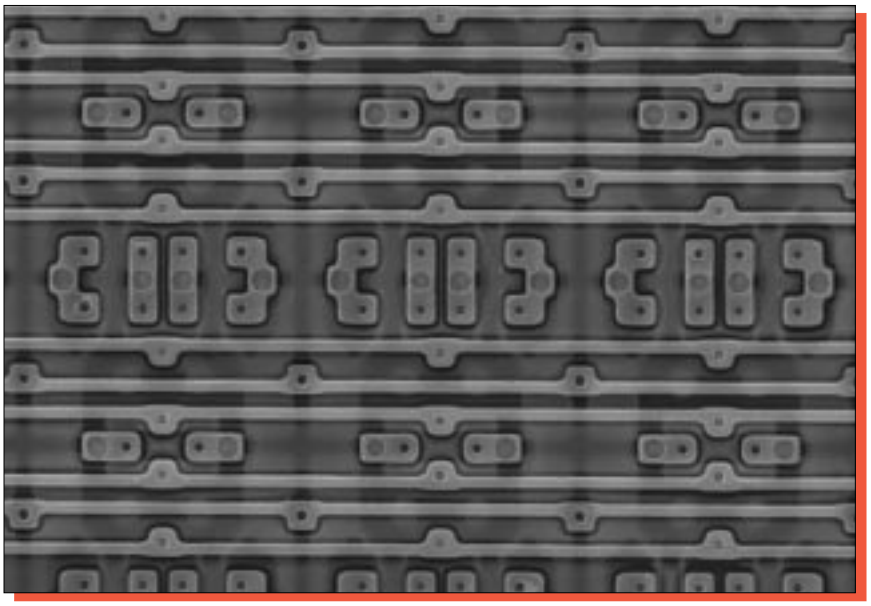
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

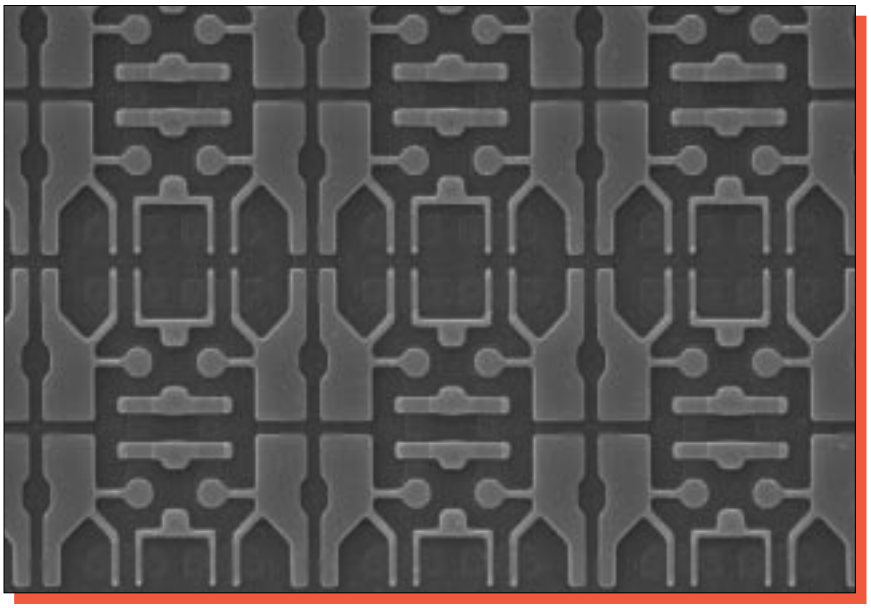
Figure 25. Color cross section drawing illustrating device structure.



metal 2



metal 1



unlayered

Figure 26. Topological SEM views illustrating the EEPROM cell array.
Mag. 1600x, 0°.

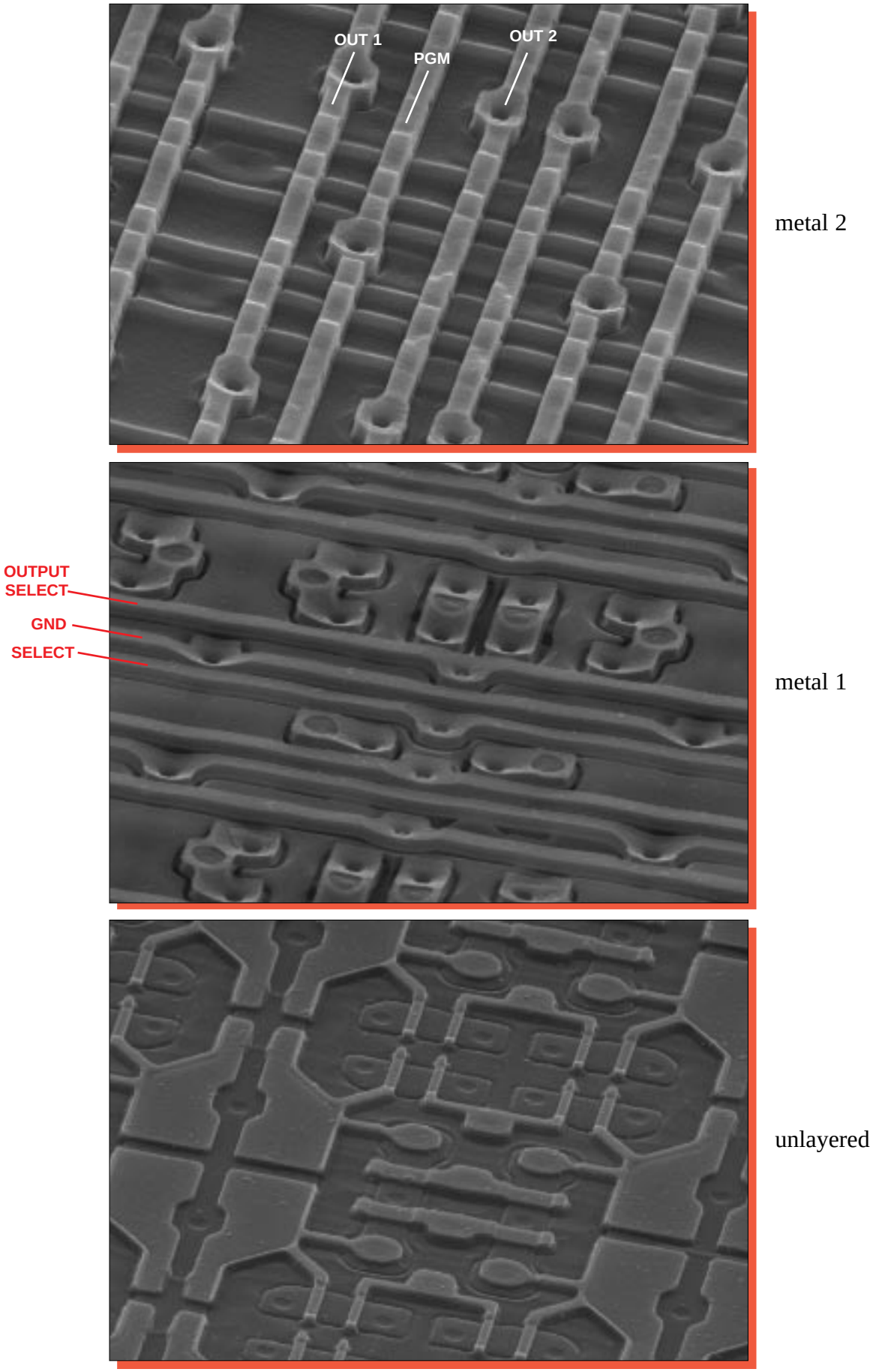
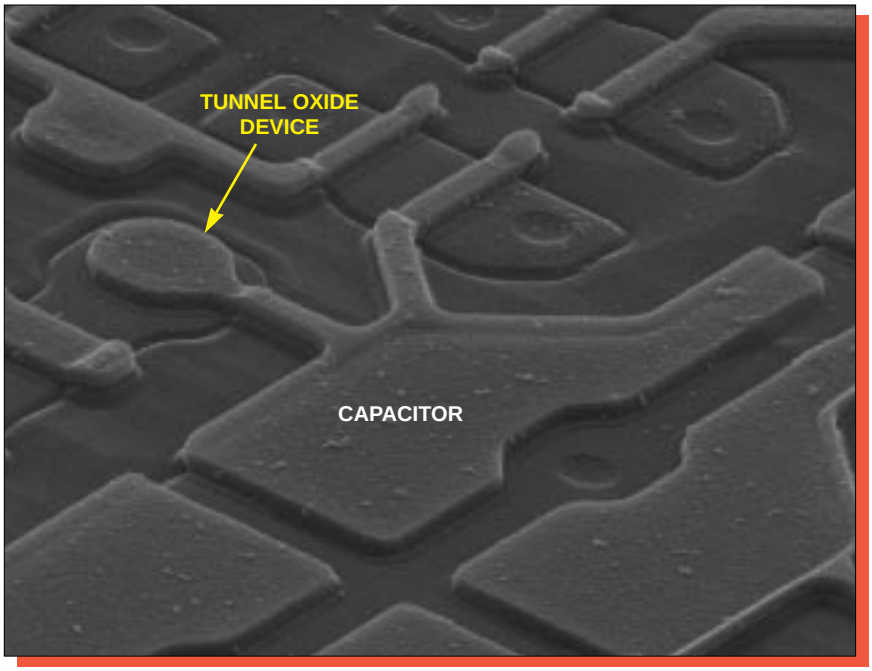
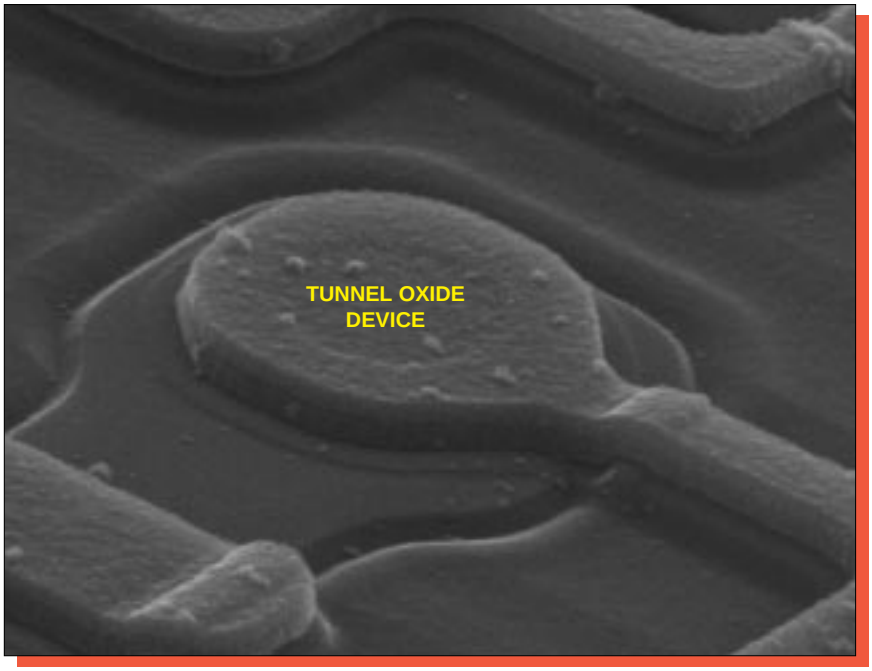


Figure 27. Perspective SEM views illustrating the EEPROM cell array.
Mag. 4000x, 60°.

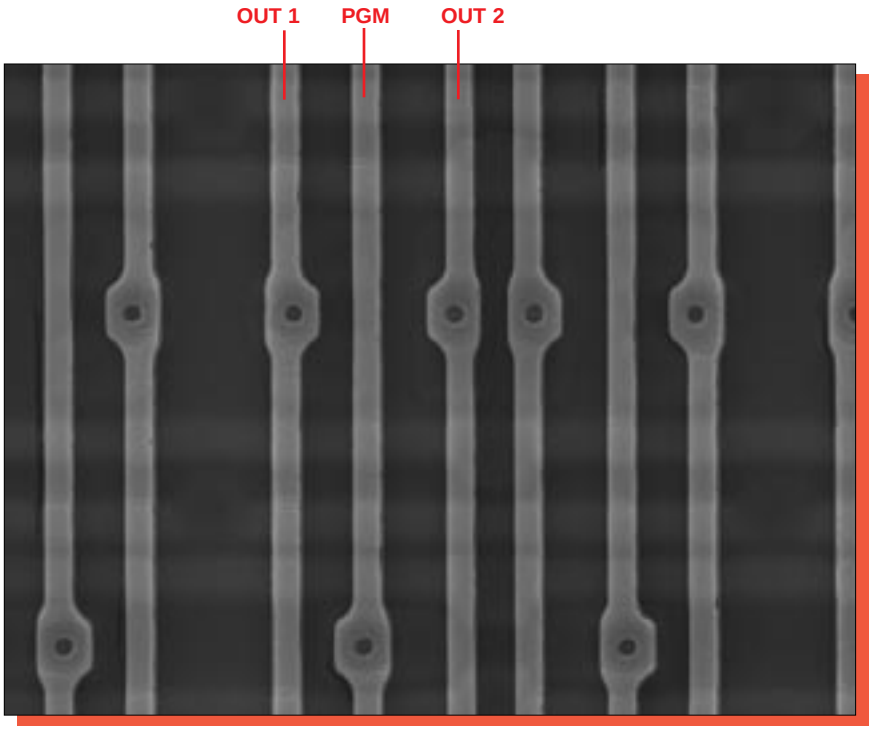


Mag. 8400x



Mag. 25,000x

Figure 28. Detailed SEM views of the EEPROM cell. Unlayered, 60°.



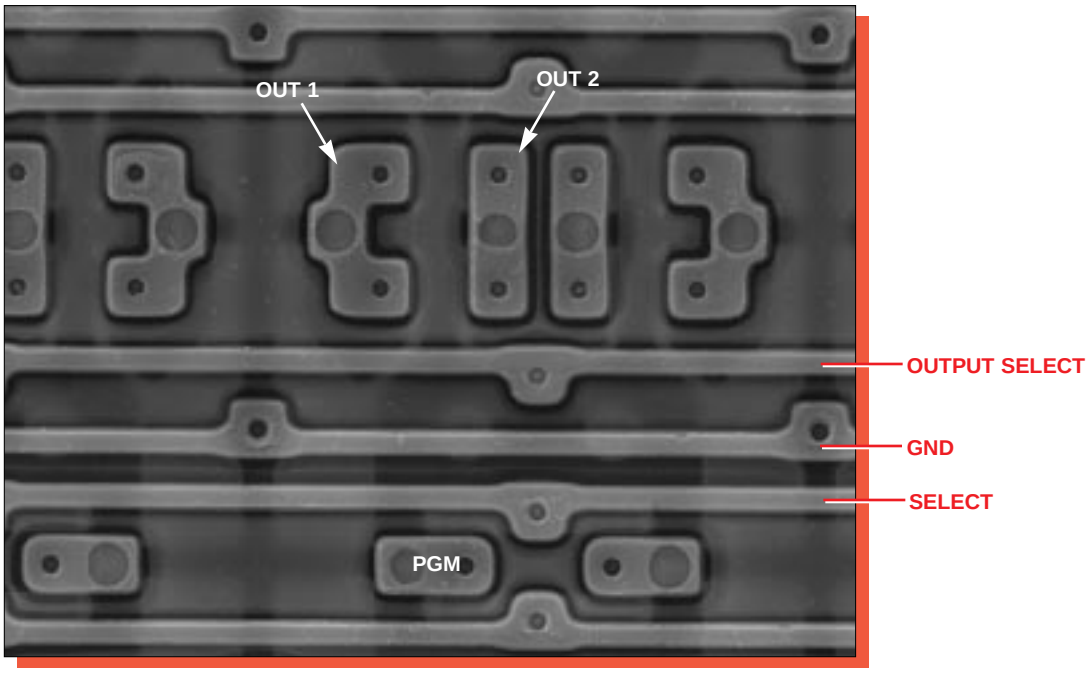
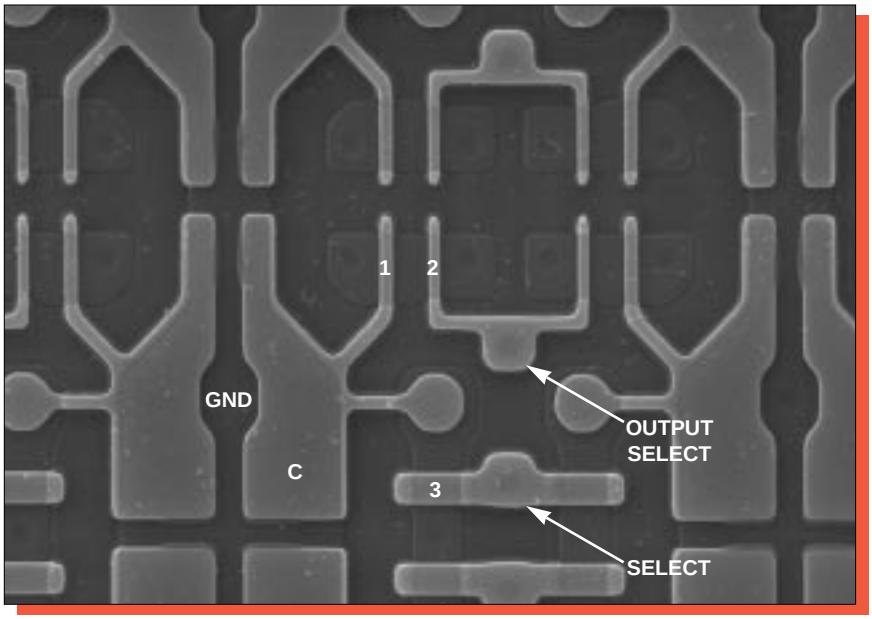


Figure 29. Topological SEM views of an EEPROM cell. Mag. 3200x, 0°.



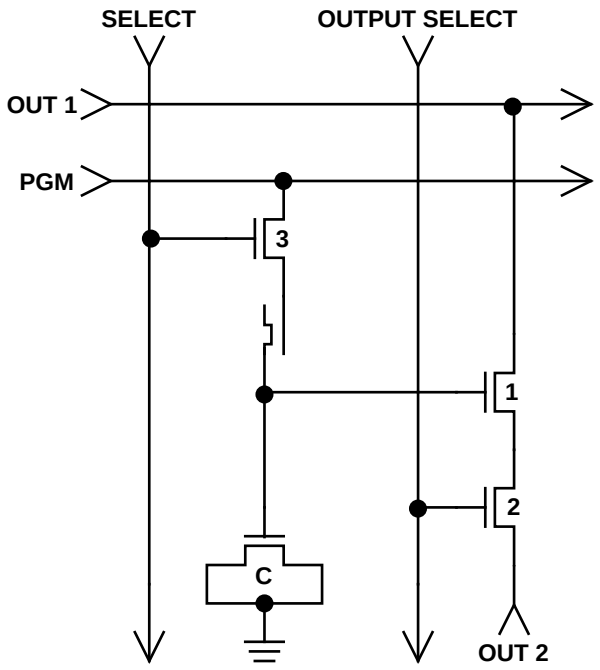
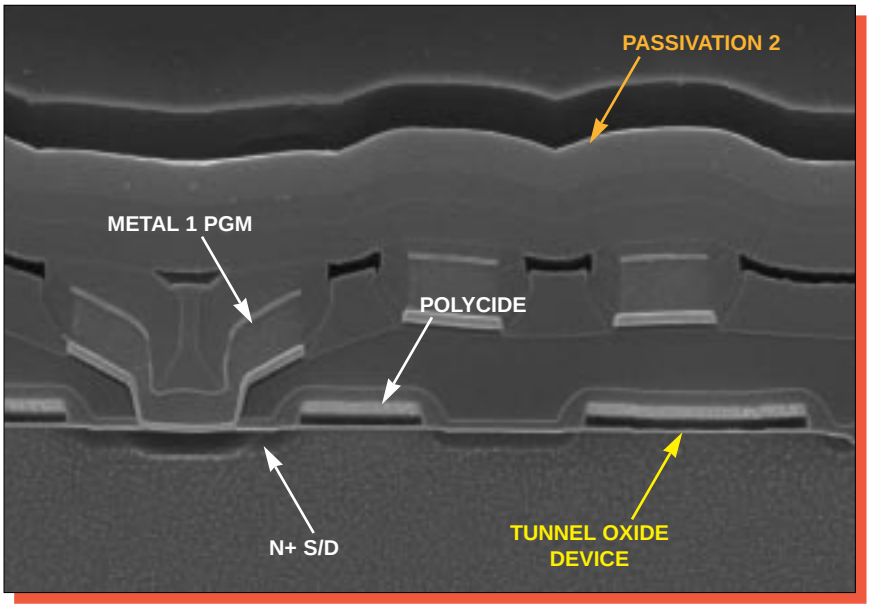
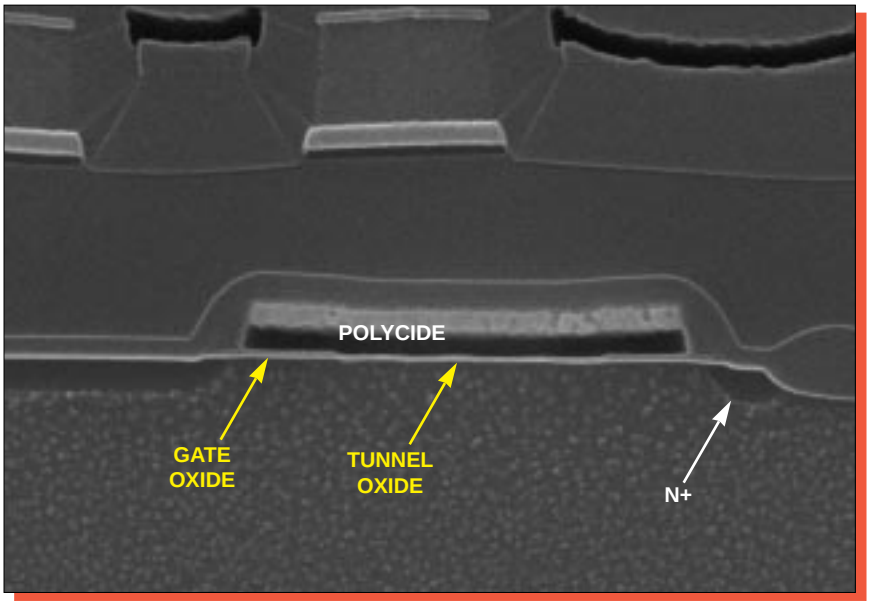


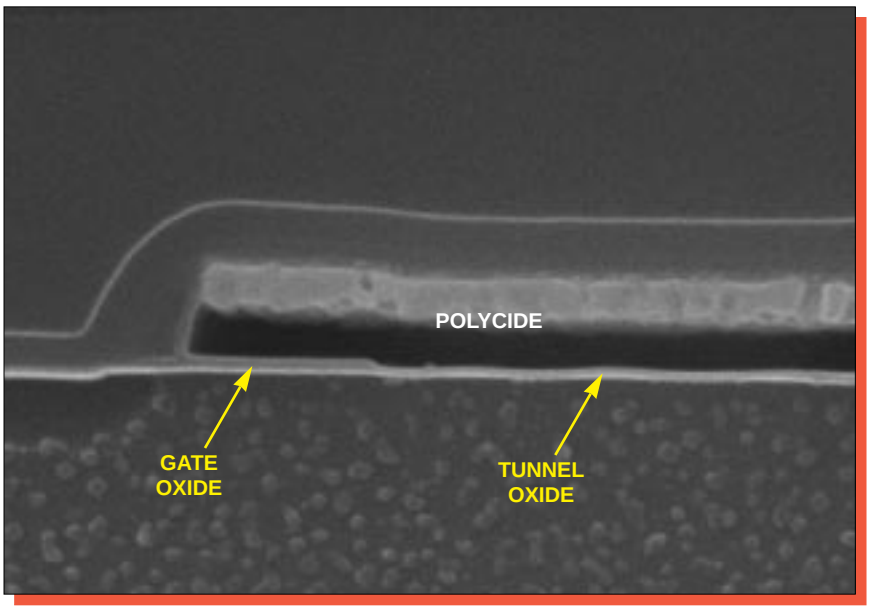
Figure 30. Topological SEM view and schematic of the EEPROM cell.
Mag. 3200x, 0°.



Mag. 13,000x

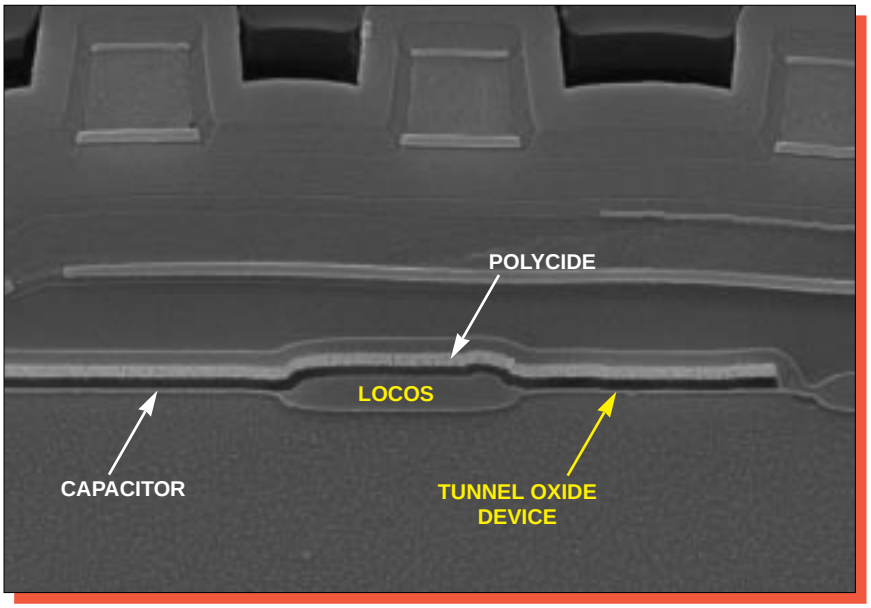


Mag. 26,000x

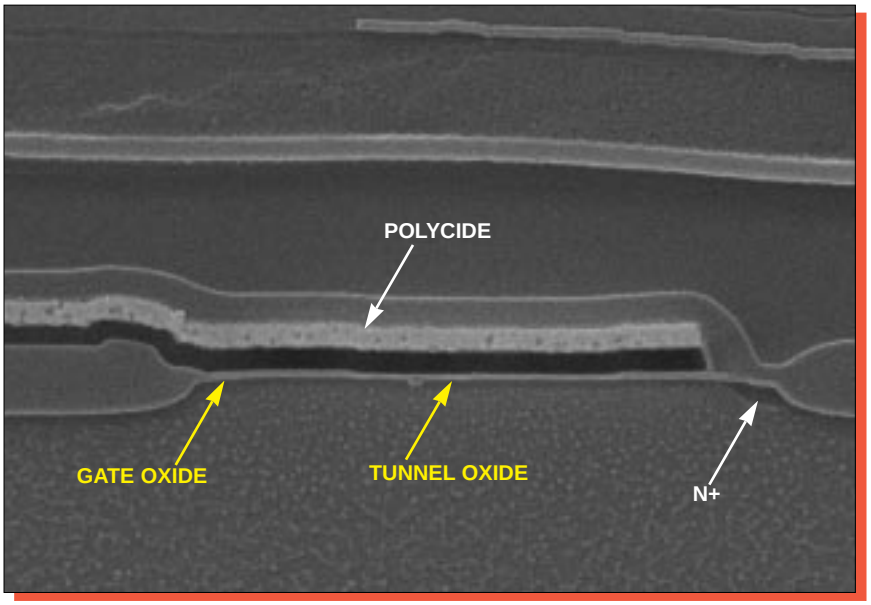


Mag. 52,000x

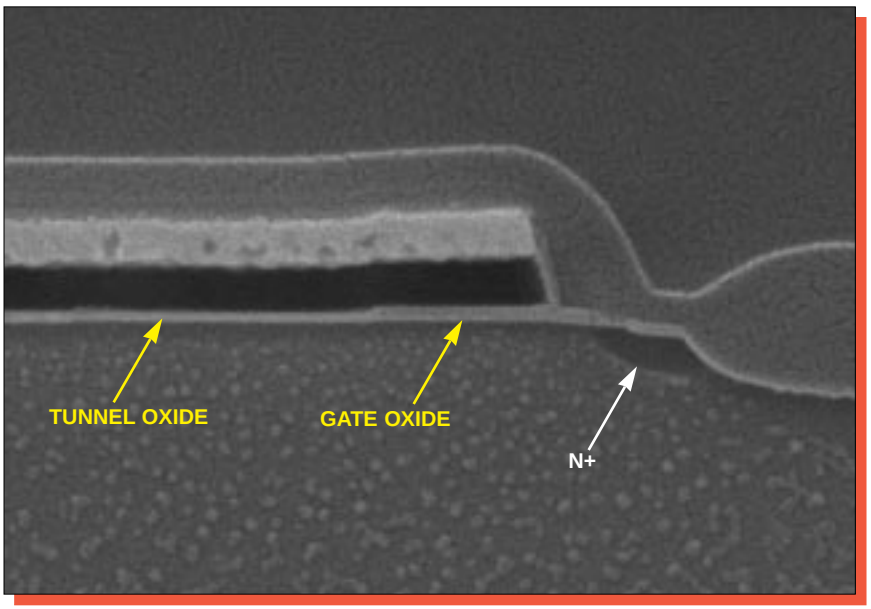
Figure 31. SEM section views of the EEPROM cell.



Mag. 13,000x

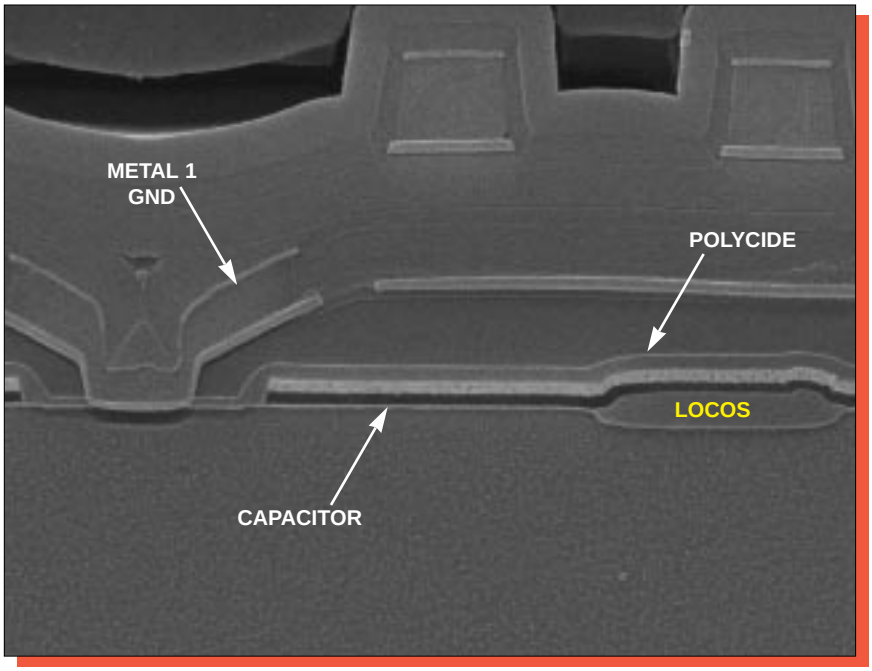


Mag. 26,000x

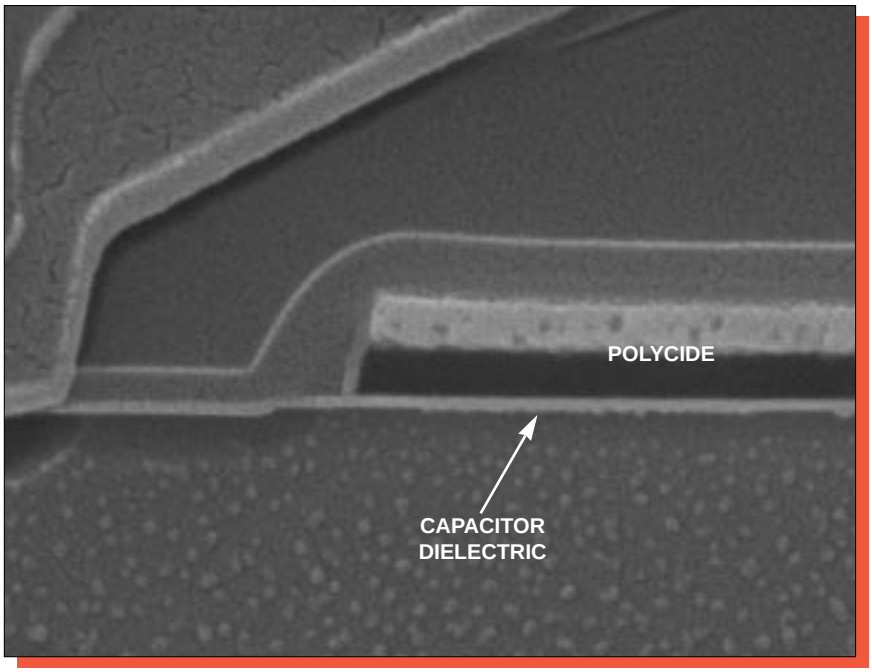


Mag. 52,000x

Figure 32. Additional SEM section views of the EEPROM cell.

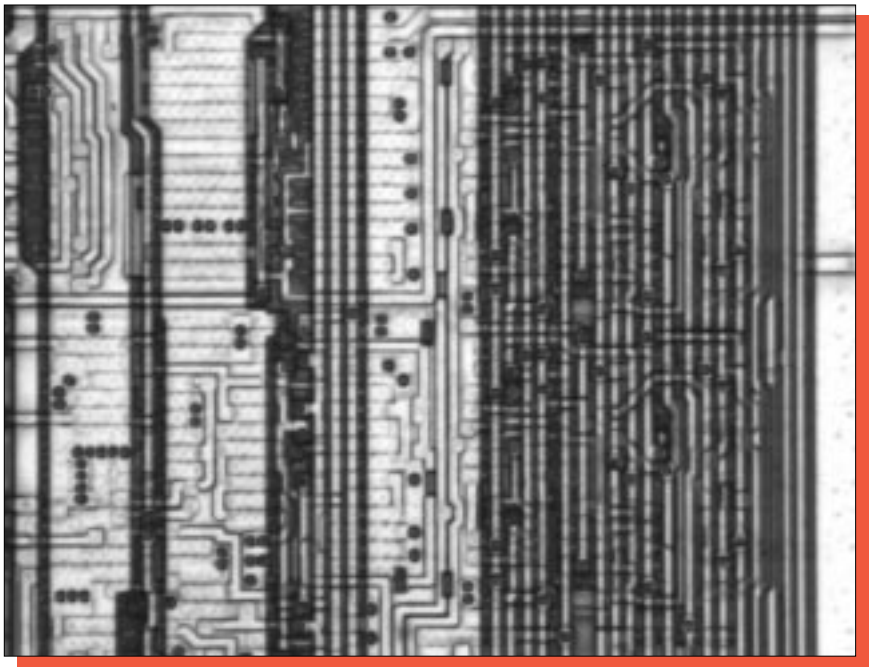


Mag. 13,000x



Mag. 52,000x

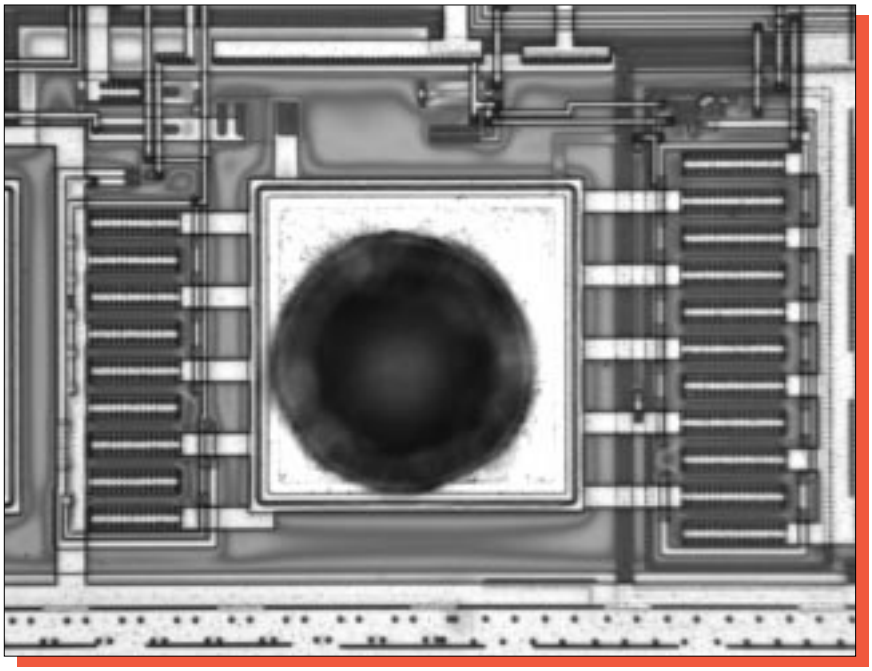
Figure 33. Additional SEM section views of the EEPROM cell.



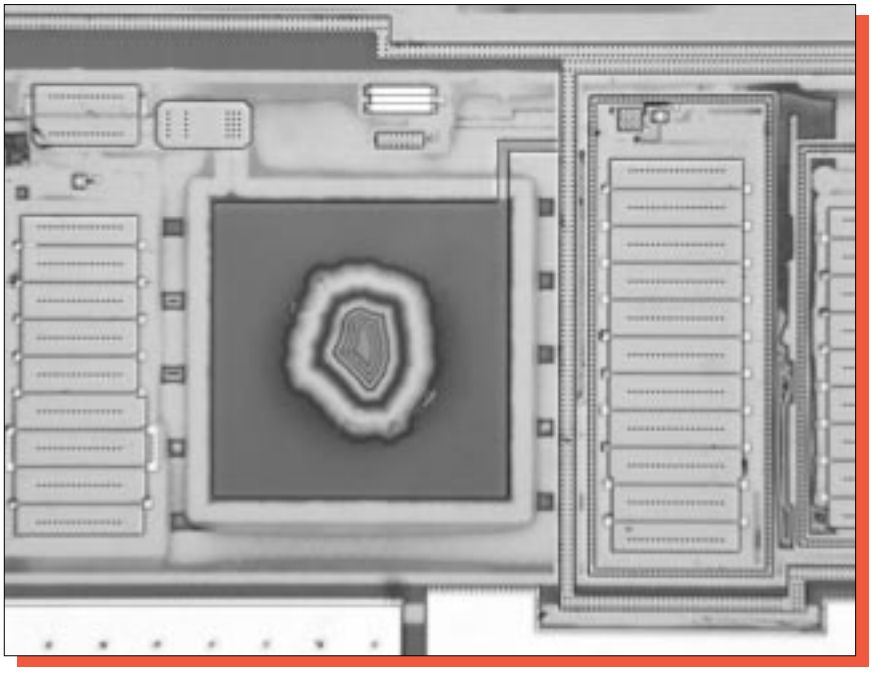
intact

unlayered

Figure 34. Optical views of typical device circuitry. Mag. 700x.

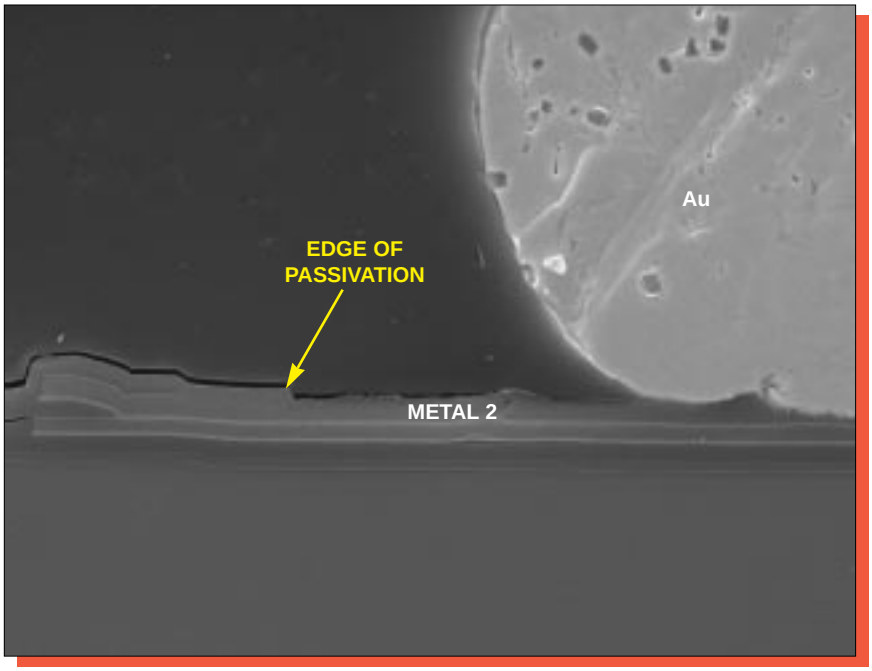


intact

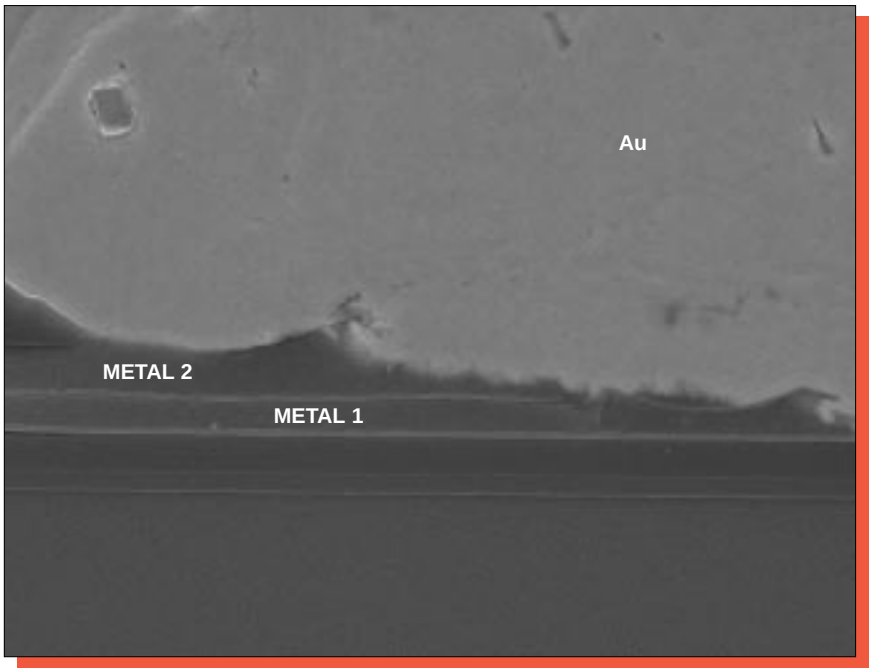


unlayered

Figure 35. Optical views of a typical I/O structure. Mag. 350x.

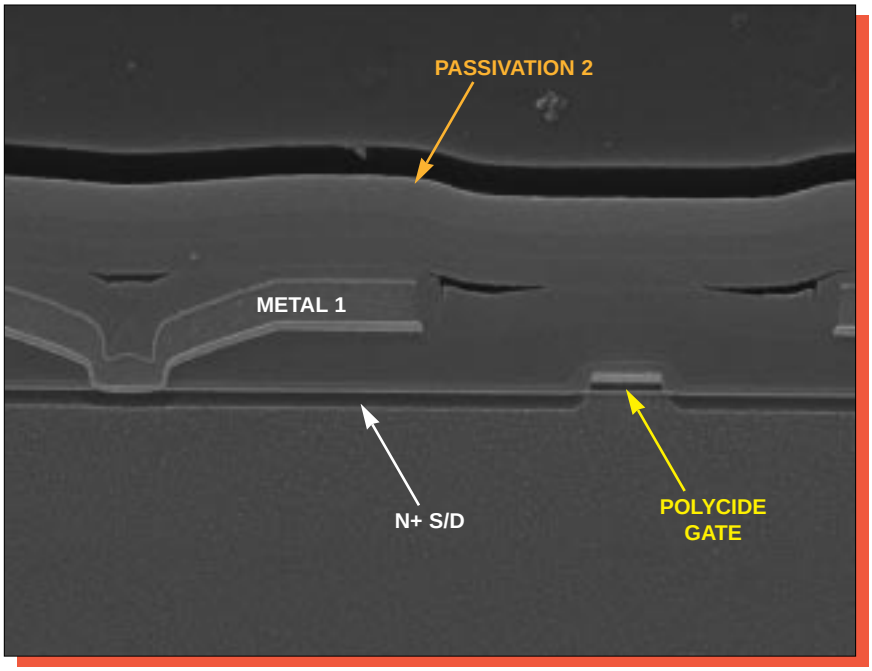


Mag. 3200x

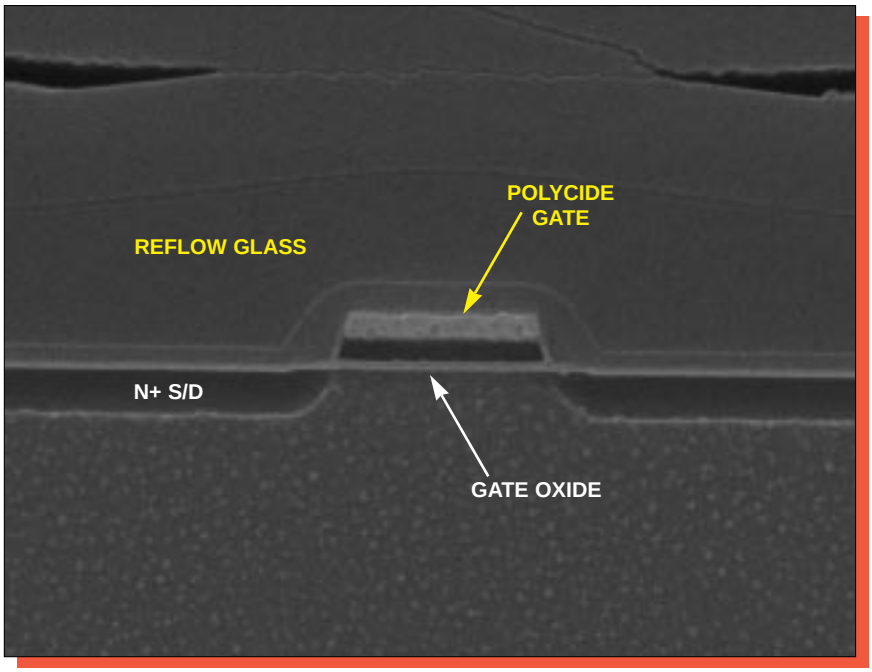


Mag. 6500x

Figure 36. SEM section views illustrating intermetallic formation.



Mag. 10,000x



Mag. 26,000x

Figure 37. SEM section views of I/O circuitry.