Construction Analysis

NEC Serial-Parallel 32Mbit MROM

Report Number: SCA 9703-534

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the NEC 32 Mbit serial-parallel NAND MROM. Two devices encapsulated in 44-pin Small Outline Integrated Circuit (SOICs) packages, and two devices encapsulated in 42-pin Plastic Dual In-Line Packages (PDIPs) were supplied for the analysis. The SOICs were date coded 9643, and the PDIPs were date coded 9644. Both package types were photographed, x-rayed and decapsulated. The devices were then analyzed for differences in process. Since both processes were found to be the same, an SOIC packaged die was used for the rest of the analysis.

MAJOR FINDINGS

Questionable Items:[1]

- Maximum aluminum thinning of up to 90 percent[2] at some contacts (Figure 18). Barrier metal maintained continuity and reduced overall thinning to 80 percent.

Special Features:

- Sub-micron gate lengths (0.6 micron N- and P-channel, 0.2 micron gates in ROM array).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in 44-pin SOICs (2) and 42 pin PDIPs (2).
- Lead-locking provisions (anchors) were present at all pins.
- Copper (Cu) leadframe internally plated with silver (Ag), externally plated with tin lead solder (SnPb).
- Thermosonic ball bond method employing 1.2 mil O.D. gold wire.
- Pin 44 was connected on the SOIC parts while the same bonding site on PDIP devices was disconnected (Figure 9).
- Pin 13 of SOIC devices and Pin 12 of the PDIPs were connected directly to the packaged header/paddle to bias the substrate.
- Saw and break dicing (60 percent sawn).
- Die was mounted to the copper header/paddle using an adequate amount of silver-filled epoxy.

Die Process and Design

- Fabrication process: Selective oxidation CMOS process.
- Overlay passivation: Single layer of silicon-dioxide.
- Metallization: Metal consisted of a single layer of aluminum doped with silicon. A titanium nitride (TiN) cap and barrier metal was used. A thin adhesion layer of titanium (Ti) was present beneath the barrier. The metallization layer was defined by a dry-etch technique of normal quality.

TECHNOLOGY DESCRIPTION (continued)

- Pre-metal glass: A single layer of reflow glass (BPSG) over various densified oxides. This layer was reflowed prior to contact cuts.

- Polysilicon: One layer of dry-etched polysilicon with a tungsten silicide was used to form word lines/select gates in the array and all gates in the periphery.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Sidewalls spacers were present on the gates indicating an LDD process was used.

- Wells: N- and P-wells in a P substrate. No epi was present.

- Memory cells: The memory cell design consisted of polycide word lines/select gates. Metal formed the bit lines. Programming is achieved by implanted diffusions.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 10**

Questionable Items: None.

General Items:

- Devices were encapsulated in 44-pin SOICs and 42-pin PDIPS.

- Overall package quality: Normal. No defects were found on the external or internal portions of the packages.

- The leadframe consisted of copper (Cu) and was externally plated with tin-lead (SnPb) solder, and internally plated with silver.

- Lead-locking provisions (anchors) were present at all leads.

- Wirebonding: Thermosonic ball bond method using 1.2 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good. Some incomplete intermetallic formation was noted during sectioning of the ball bonds, but it did not seem to affect the quality of the bond (Figure 8). Wire spacing was normal.

- Die attach: Silver epoxy of normal quantity and quality.

- Die dicing: Die separation was by saw-and-break (60 percent sawn). No problems were noted.

ANALYSIS RESULTS II

Die Process and Design: **Figures 11 - 32**

Questionable Items:[1]

- Maximum aluminum thinning of up to 90 percent[2] at some contacts (Figure 18).

Special Features:

- Sub-micron gate lengths (0.6 micron N- and P-channel, 0.2 micron N-channel gates in ROM array).

General Items:

- Fabrication process: Selective oxidation CMOS process employing N- and P-wells in a P-substrate.

- Design and layout: Die layout was clean and efficient. Customization by metal mask changes appears to be used. Alignment was good.

- Die surface defects: None. No contamination, toolmarks or processing defects were noted.

- Overlay passivation: One layer of silicon-dioxide. Overlay integrity tests indicated defect-free passivation. Edge seal was good.

- Metallization: One level of metallization. Metal consisted of aluminum doped with silicon. A titanium nitride (TiN) cap and barrier metal was used on a thin layer of titanium (Ti).

- Metal patterning: The metal layer was defined by a dry etch of good quality.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metal defects: Silicon nodules were found at metal contact steps (Figures 18-19) occupying 100 percent of the cross-sectional area. No voiding or notching of the metal layer was present.

- Metal step coverage: Maximum aluminum thinning up to 90 percent at some contacts (Figure 18). Total metal thinning (including cap and barrier) was typically 80 percent.

- Contacts: Metal contact cuts were made in a two-step etch. No significant over-etching of the contacts was present.

- Pre-metal glass: A single layer of reflow glass (BPSG) over densified oxides. This layer was reflowed prior to contact cuts. No problems were found.

- Polysilicon: One layer of dry-etched polycide was used to form word lines and select gates in the array and all gates in the periphery. No problems were found anywhere.

- Isolation: Local oxide (LOCOS). No problems were present at birdsbeaks or elsewhere.

- Diffusions: Standard implanted N+ and P+ diffusions were used for sources and drains. No problems were found. The P+ diffusions used in the I/O structure (Figure 10) were twice as deep (0.4 micron) as in the normal circuitry. Sidewalls spacers were present on the gates indicating an LDD process was probably used.

- Wells: N- and P-wells in a P-substrate. No epi was present.

- Memory cells: The memory cell design consisted of polycide word lines/select gates. Metal formed the bit lines. Programming is achieved through implanted diffusions.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

SEM inspection of assembly features and passivation

Passivation integrity tests

Wirepull tests

Passivation removal

Delayer to metal and inspect

Metal removal and inspect barrier

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Die attach quality	G
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	N
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die attach method	Silver-epoxy
Dicing method	Sawn (60 percent sawn)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP[1]
Contact coverage	N
Contact registration	N
Contact defects	N

[1] *Aluminum thinning up to 90 percent.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS (SOIC)

Top	Bottom
MPR - 188553 JO2 964312901	A6 2

PACKAGE MARKINGS (PDIP)

Top	Bottom
MPR - 19193 WO2 964412901	A3 19

WIREBOND STRENGTH

Wire material:	1.2 mil diameter gold
Die pad material:	aluminum
Material at package post:	silver
# of wires tested:	30
Bond lifts:	0
Force to break - high:	10g
- low:	7g
- avg.:	8.9g
- std. dev.:	0.7

DIE MATERIAL ANALYSIS

Passivation:	A single layer of glass.
Metallization:	Silicon doped aluminum (Al) with a titanium-nitride (TiN) cap and barrier on a titanium (Ti) adhesion layer.
Polycide:	Tungsten-silicide on polysilicon.

HORIZONTAL DIMENSIONS

Die size:	5.6 x 8.8 mm (219 x 347 mils)
Die area:	49 mm^2 (75,993 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.4 x 4.4 mils)
Min pad window:	0.1 x 0.1 mm (3.9 x 3.9 mils)
Min pad space:	71 microns (2.8 mils)
Min pad-to-metal:	25 microns (1.0 mil)
Min metal width:	0.6 micron
Min metal space:	1.0 micron
Min metal pitch:	1.6 micron
Min contact:	1.7 micron
Min polycide width (array):	0.2 micron
Min polycide space:	0.5 micron
Min gate length - periphery:	0.6 micron (N and P-channel)
Min gate length - ROM array:	0.2 micron

VERTICAL DIMENSIONS

Die thickness:	0.4 mm (15.6 mils)
Layers	
Passivation:	0.4 micron
Metallization - cap:	0.05 micron (approximate)
- aluminum:	0.75 micron
- barrier:	0.1 micron
- adhesion layer	0.05 micron (approximate)
Pre-metal glass:	0.3 micron (average)
Polycide - tungsten:	0.15 micron
- poly:	0.13 micron
Local oxide:	0.3 micron
Peripheral diffusion - N+ :	0.2 micron
- P+ :	0.2 micron
I/O diffusion - N+ :	0.2 micron
- P+ :	0.4 micron
N-well:	4.3 microns
P-well:	Could not delineate

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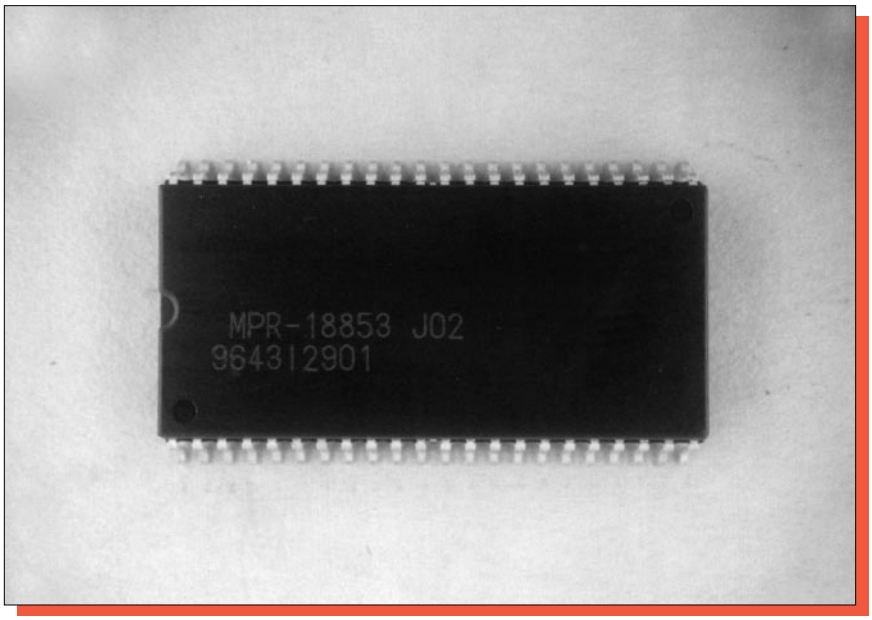


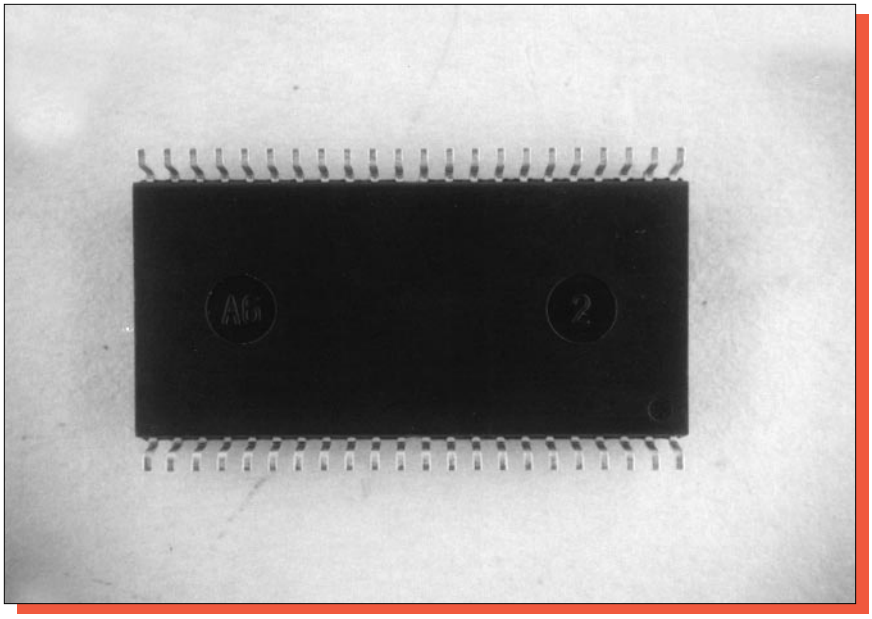
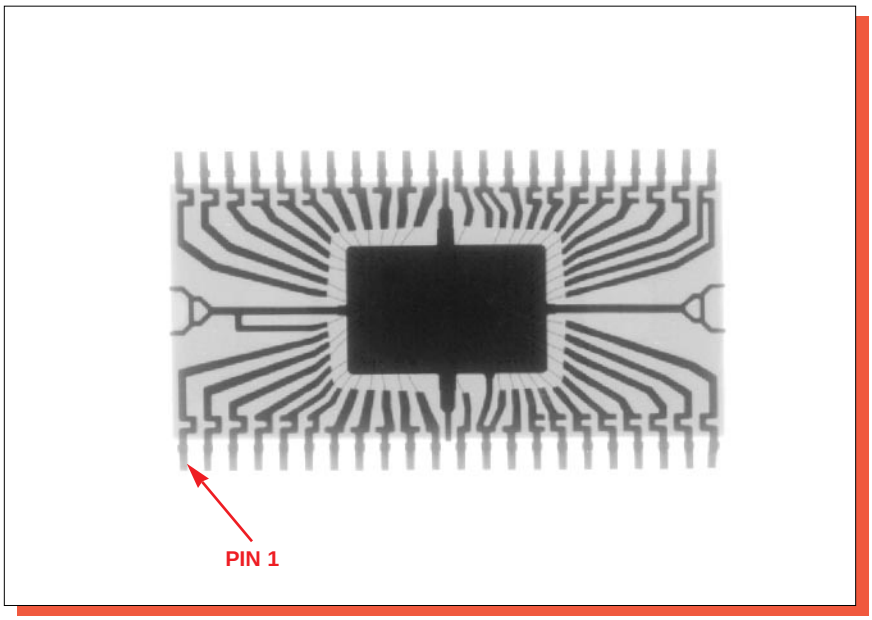


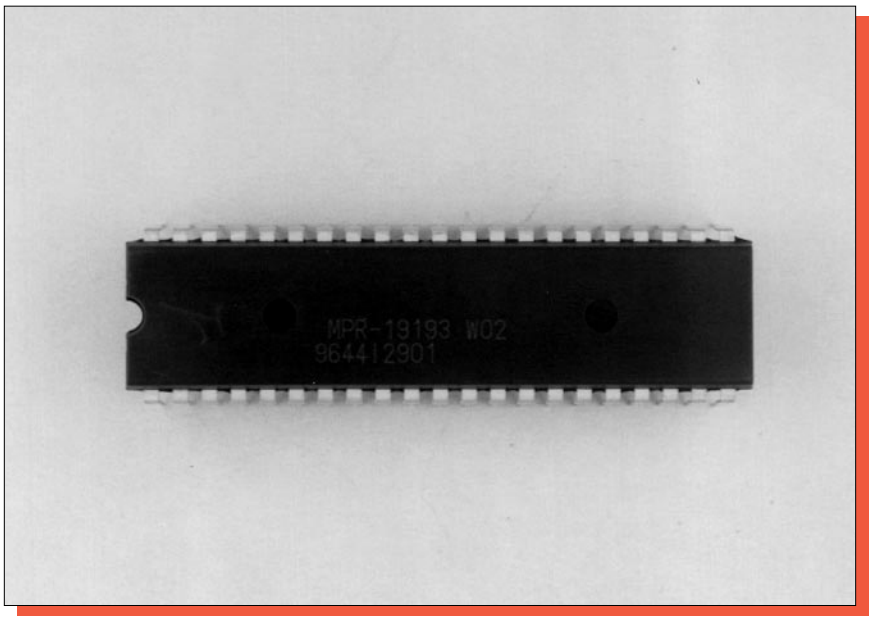
Figure 1. Package photographs of the NEC D23C32000A SOIC packaged device.
Mag. 2.6x.



top

side

Figure 2. X-ray views of the SOIC package. Mag. 2.6x.



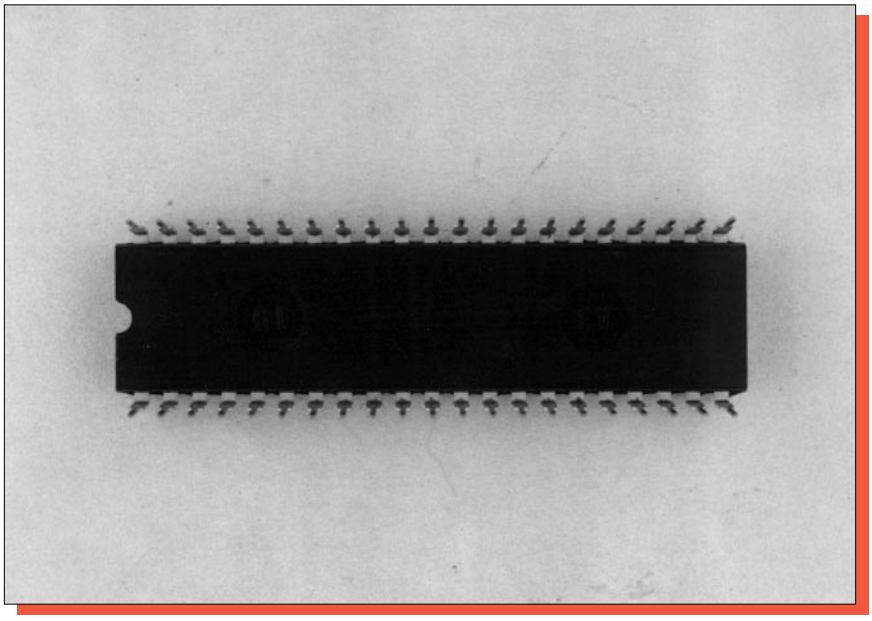
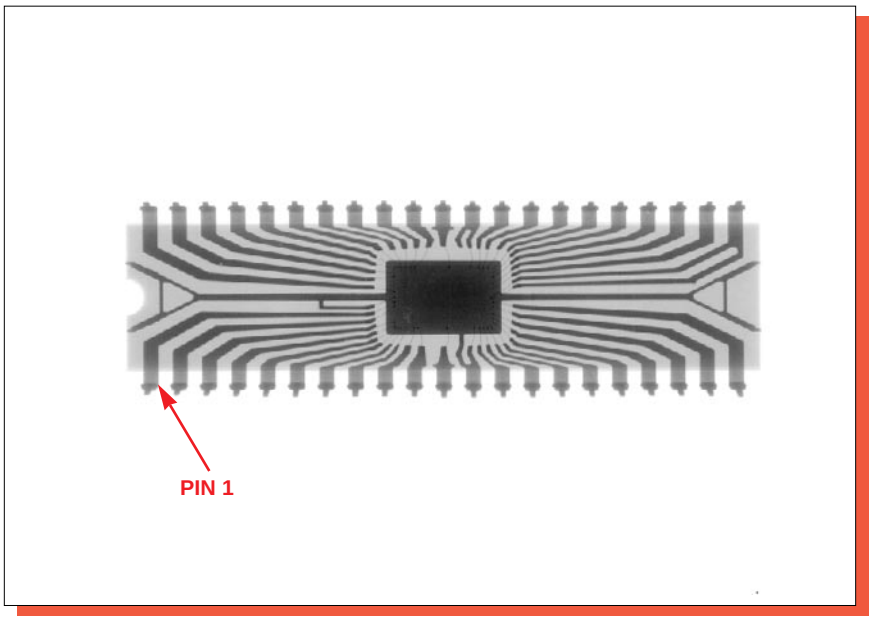


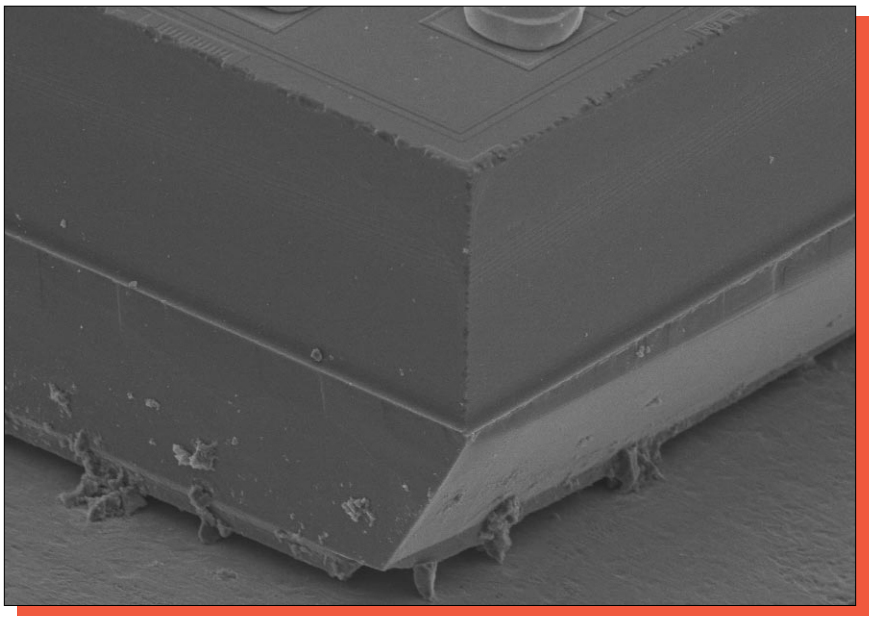
Figure 3. Package photographs of the NEC D23C32020A PDIP device. Mag. 1.5x.



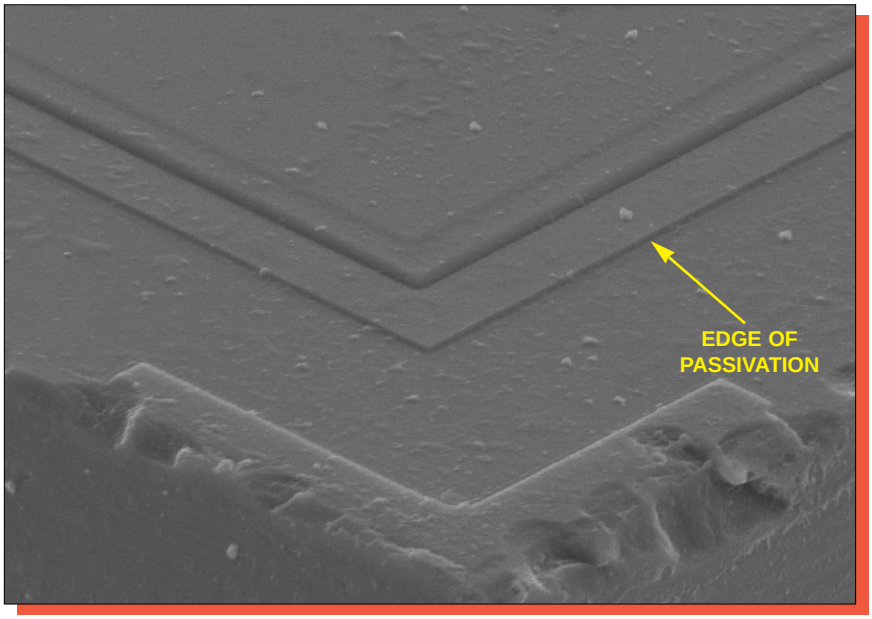
top

side

Figure 4. X-ray views of the PDIP package. Mag. 1.5x.

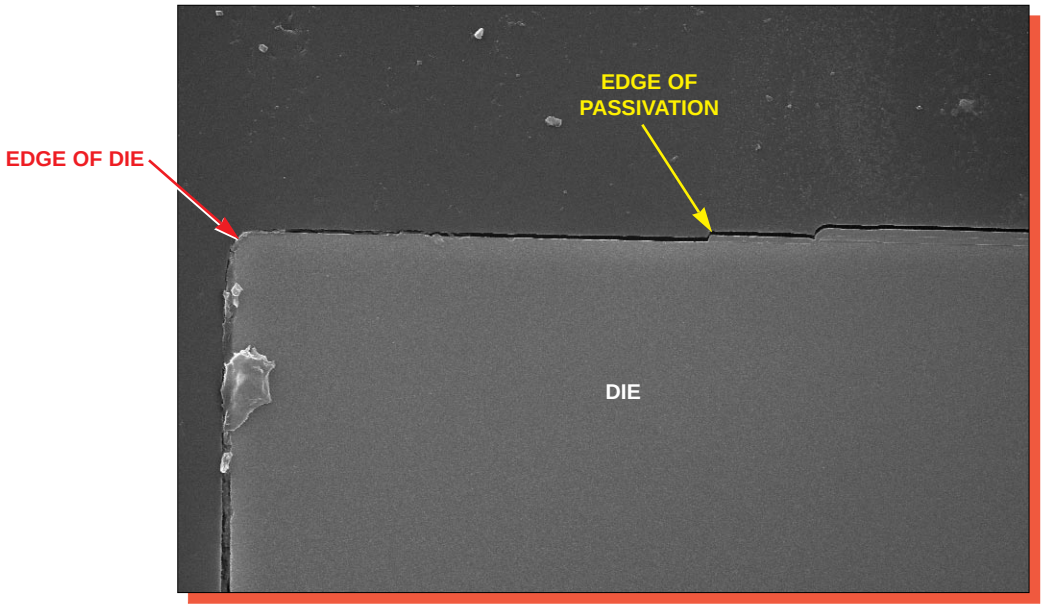


Mag. 180x

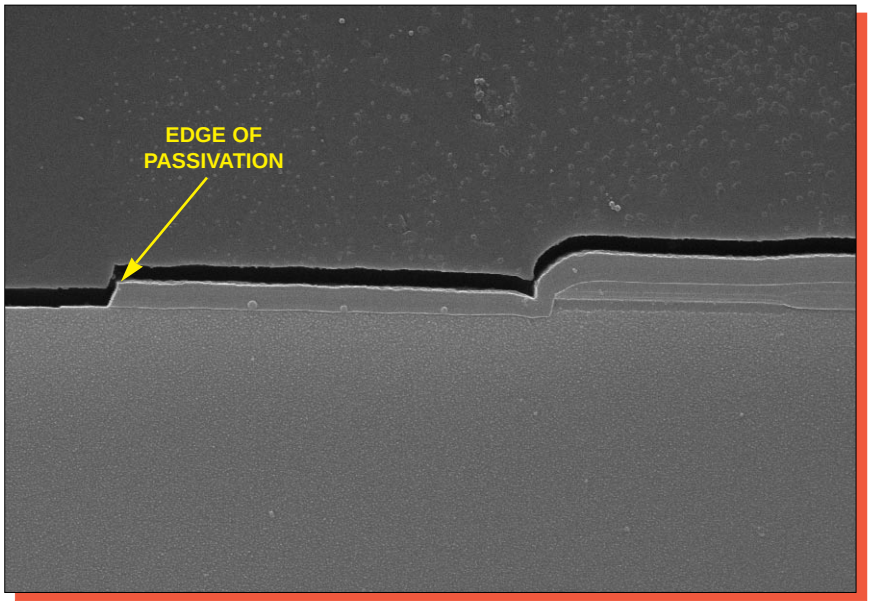


Mag. 1400x

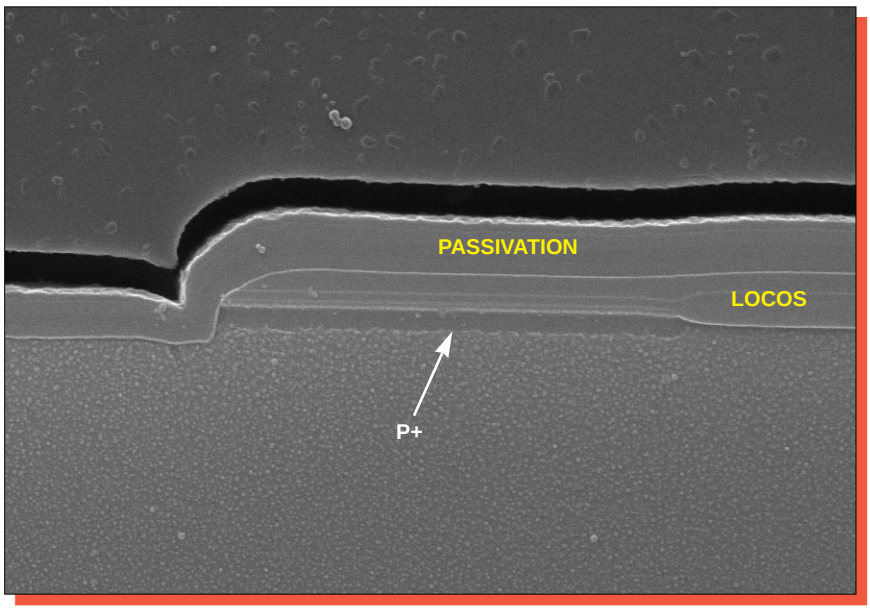
Figure 5. SEM views of a die corner and edge seal. 60°.



Mag. 1600x

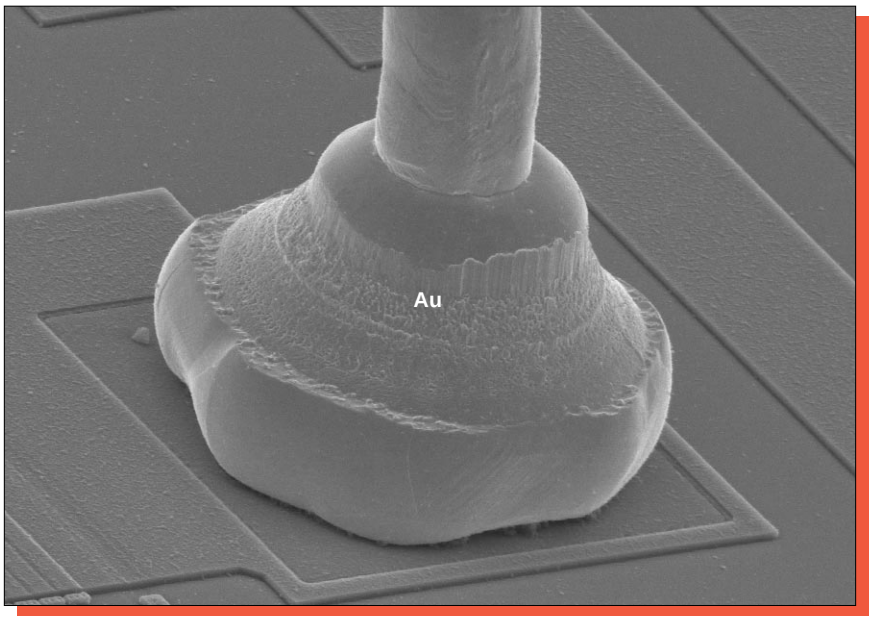


Mag. 6500x

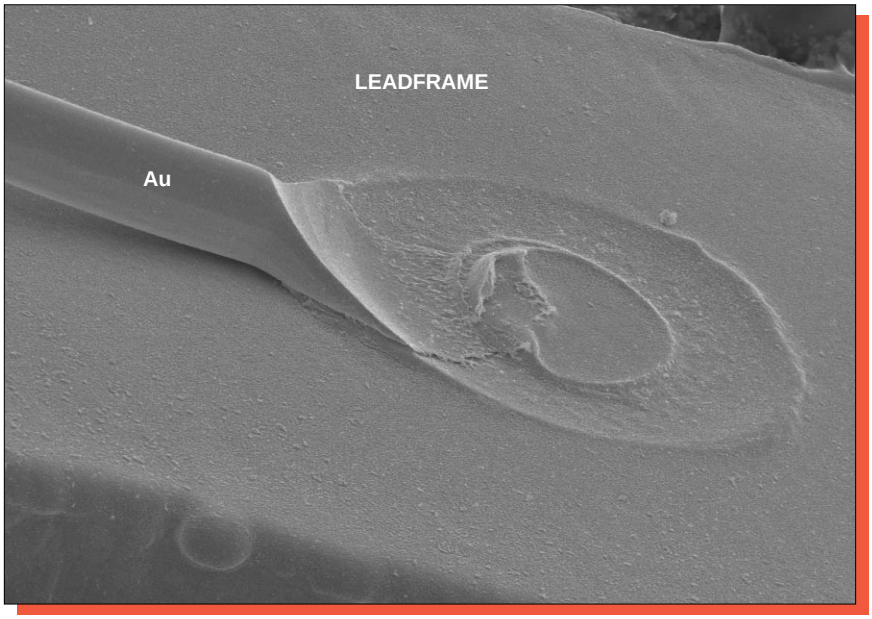


Mag. 13,000x

Figure 6. SEM section views of the edge seal.

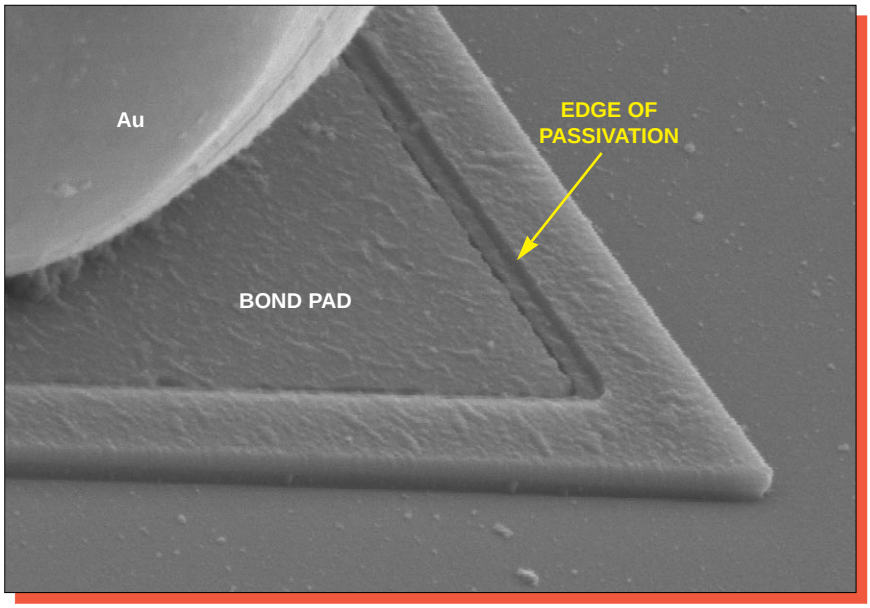


Mag. 700x

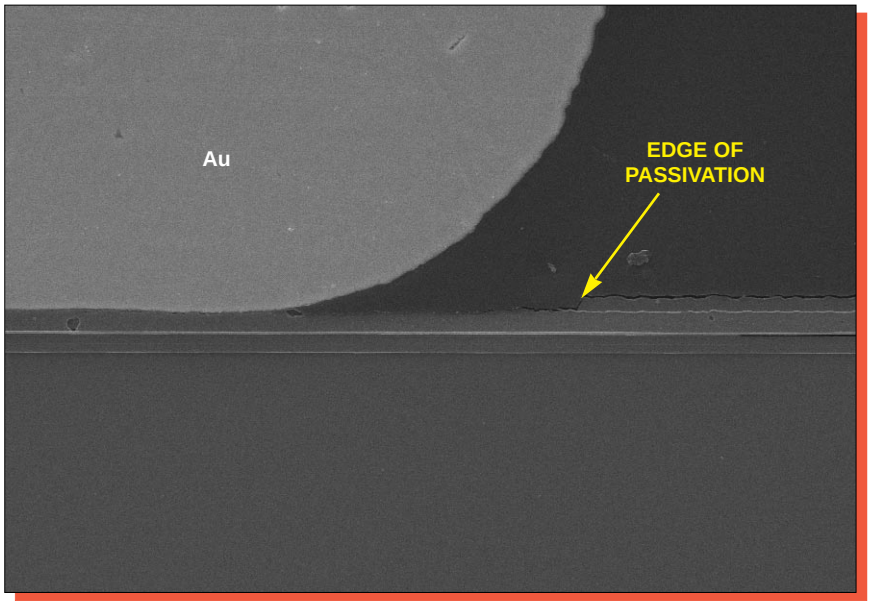


Mag. 420x

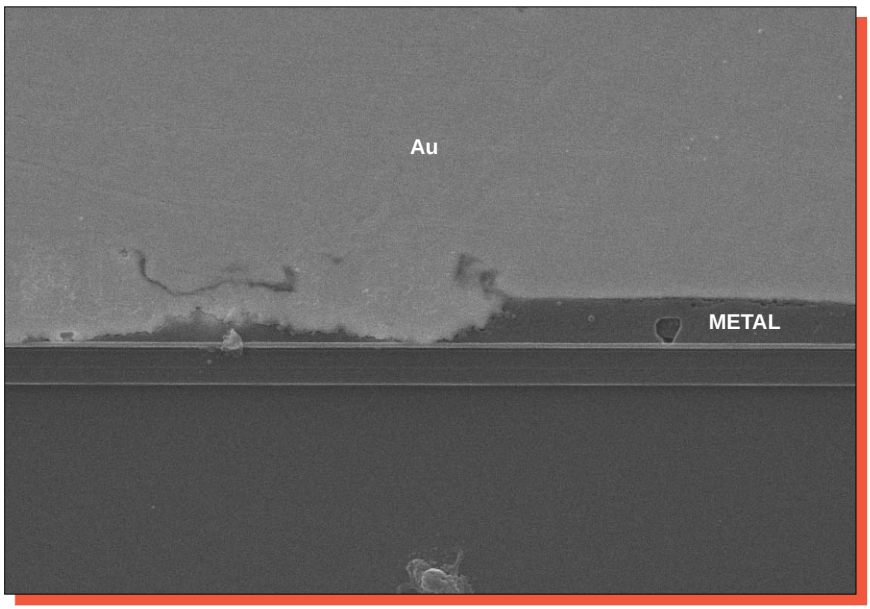
Figure 7. SEM views of typical wirebonds. 60°.



Mag. 2800x, 60°

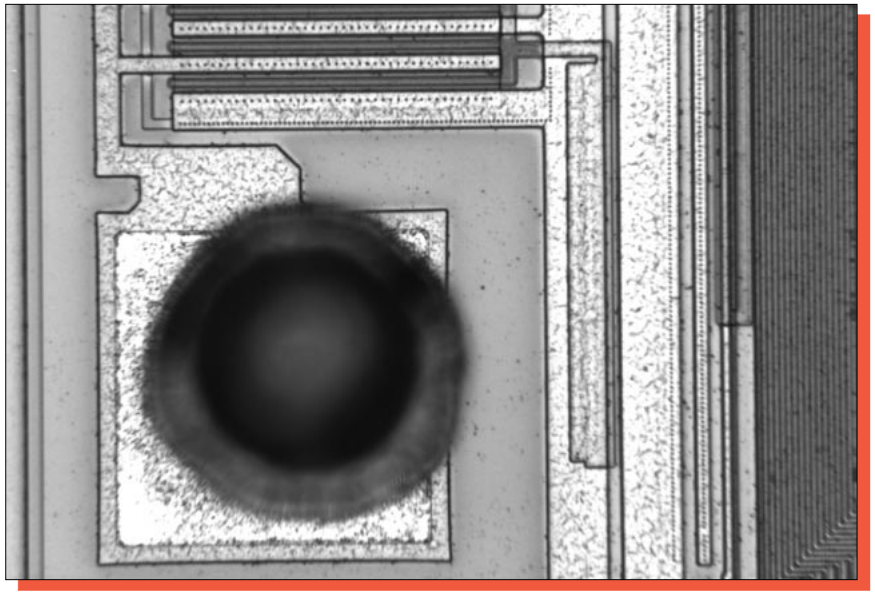


Mag. 3200x

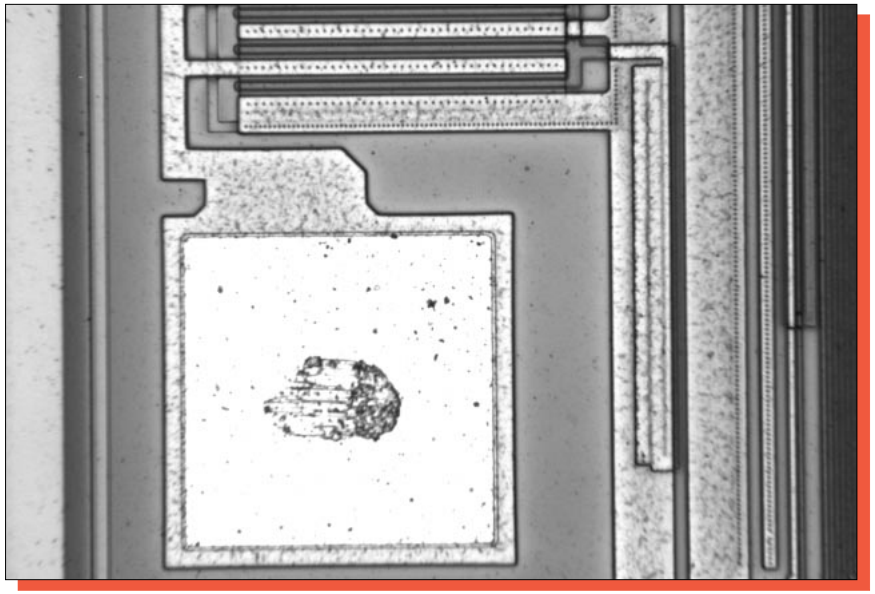


Mag. 6500x

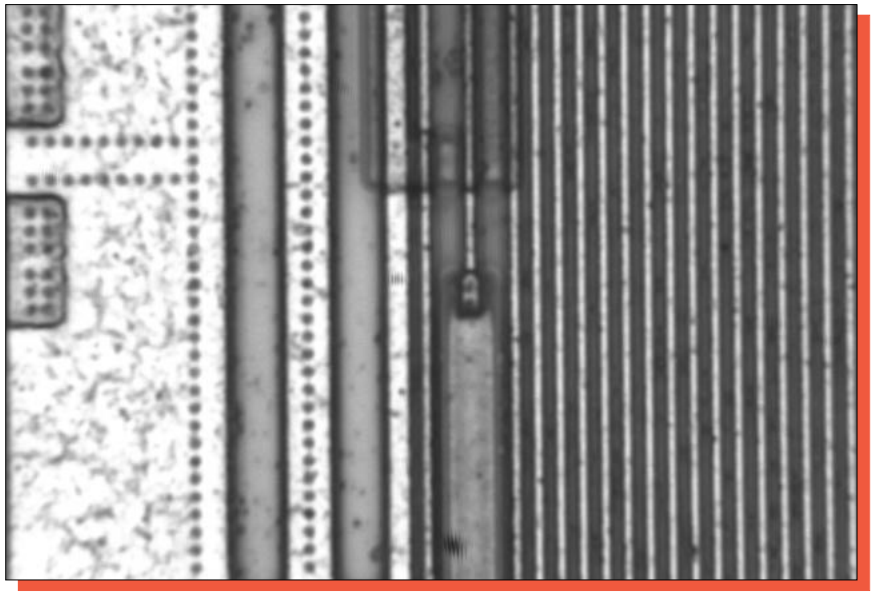
Figure 8. SEM views illustrating pad window and intermetallic formation.



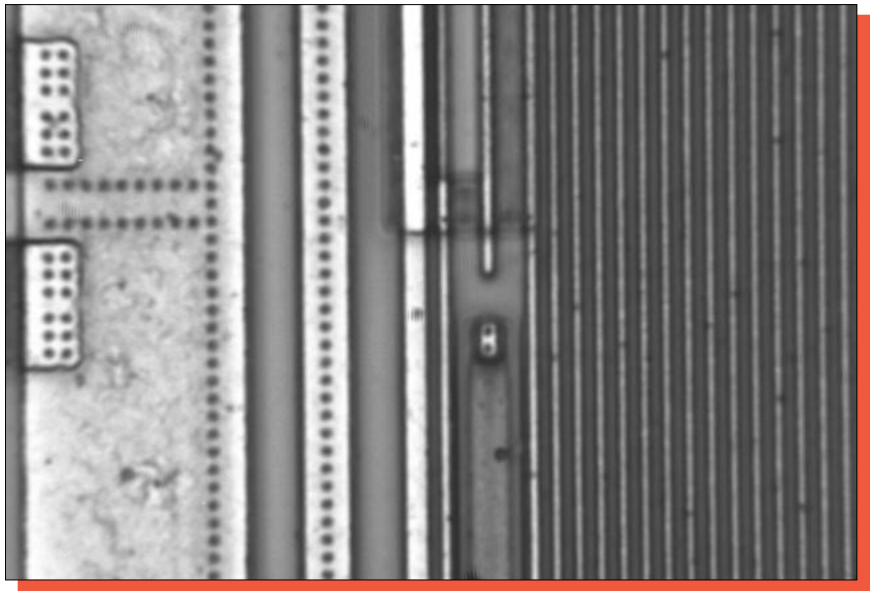
Pin 44, SOIC, Mag. 410x



PDIP, Mag. 410x

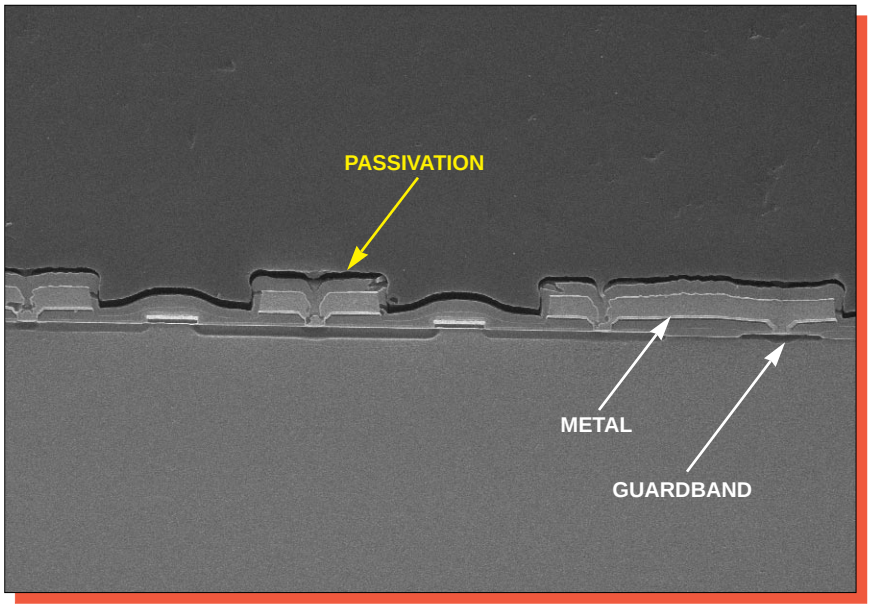


SOIC, Mag. 1500x



PDIP, Mag. 1500x

Figure 9. Optical views illustrating different pad connections on the NEC D23C32020A. SOIC vs. PDIP.



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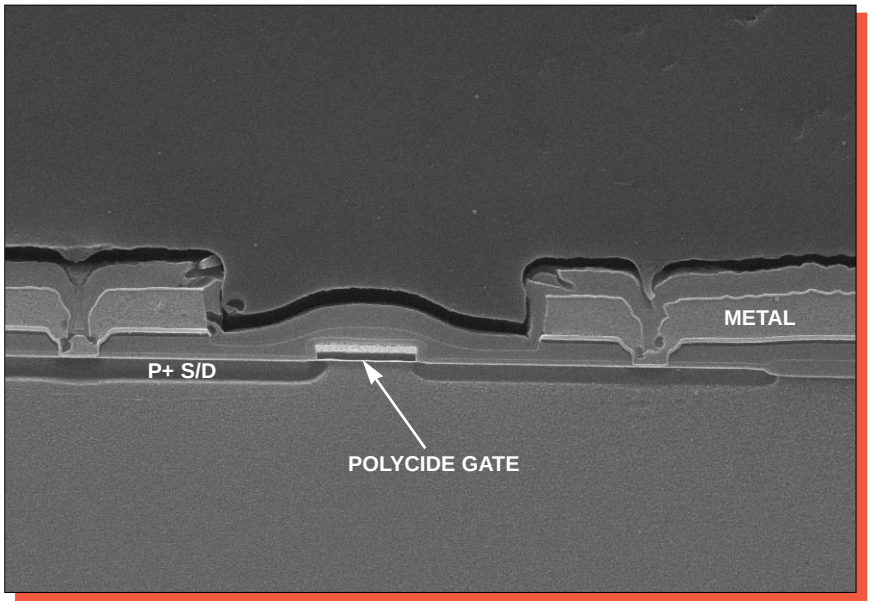
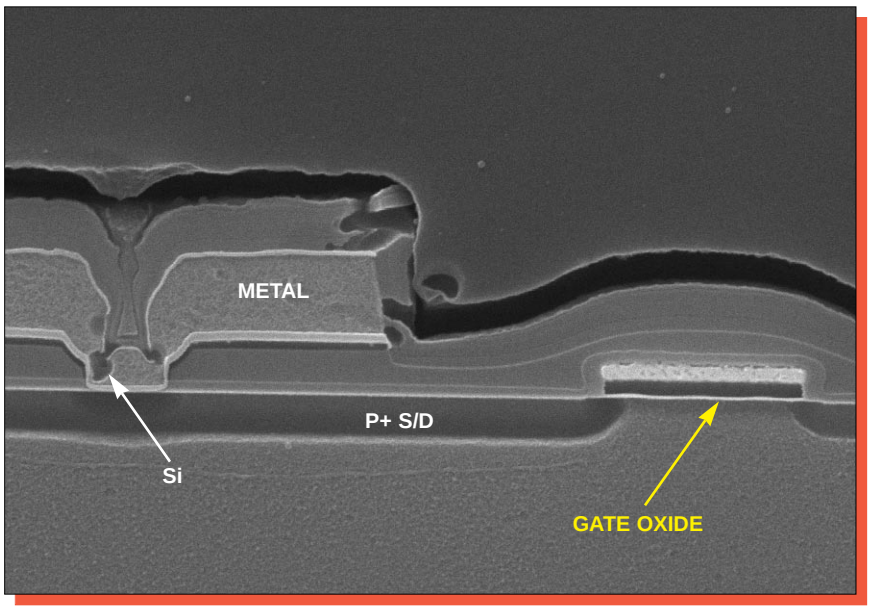


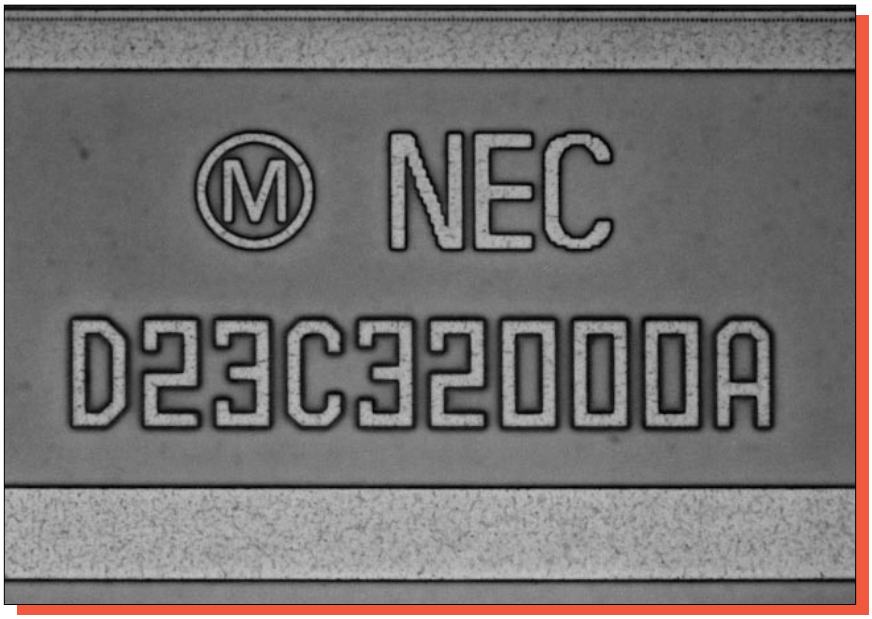
Mag. 6500x



Mag. 13,000x

Figure 10. SEM section views of the I/O structure.

Figure 11. Whole die photograph or the NEC D23C32000A. Mag. 26x.

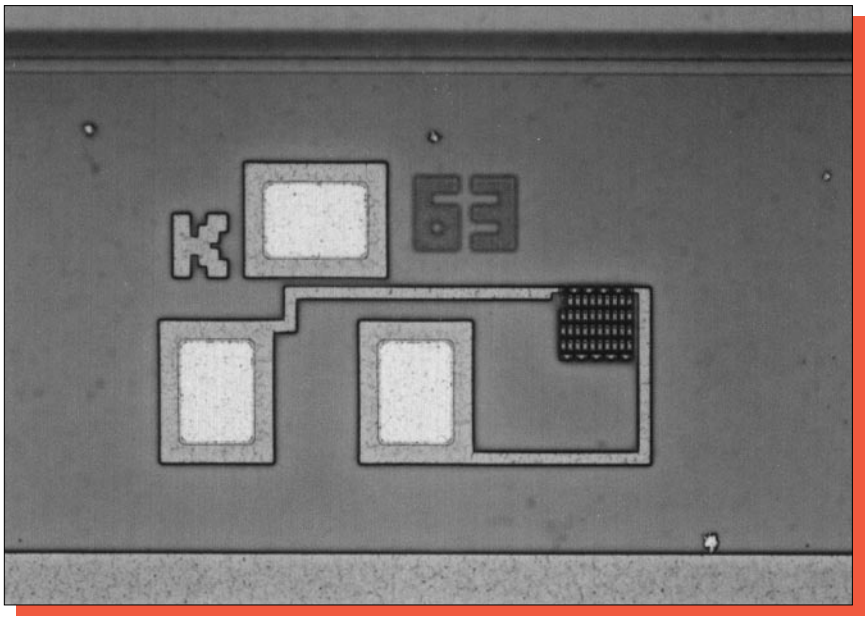


SOIC packaged die

PDIP packaged die

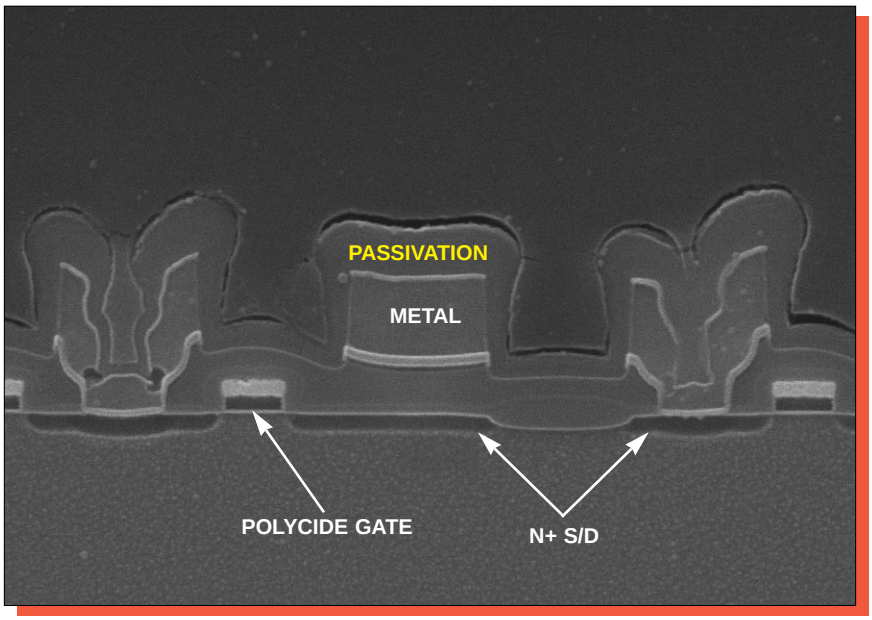
Figure 12. Optical views of die markings from both package types. Mag. 400x.

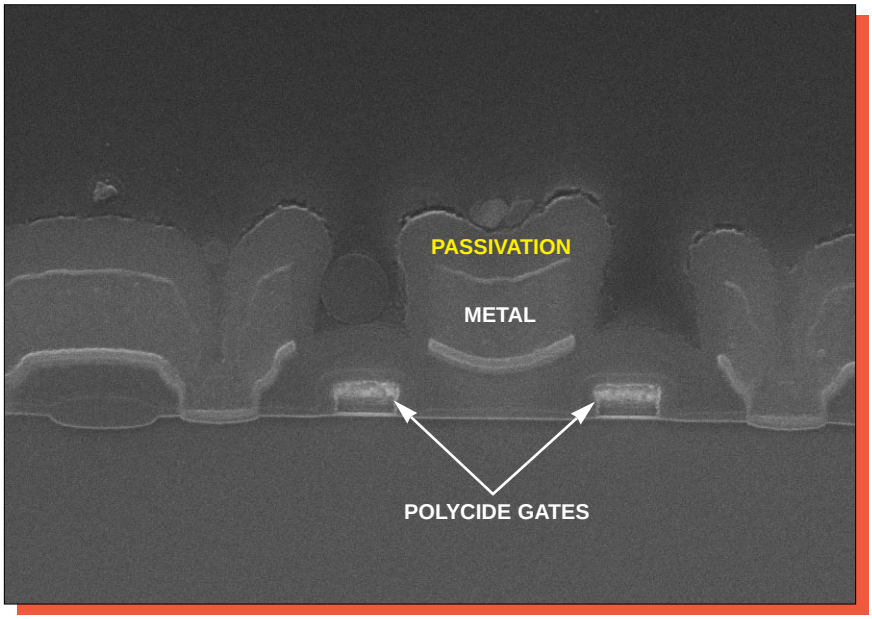
Mag. 200x



Mag. 400x

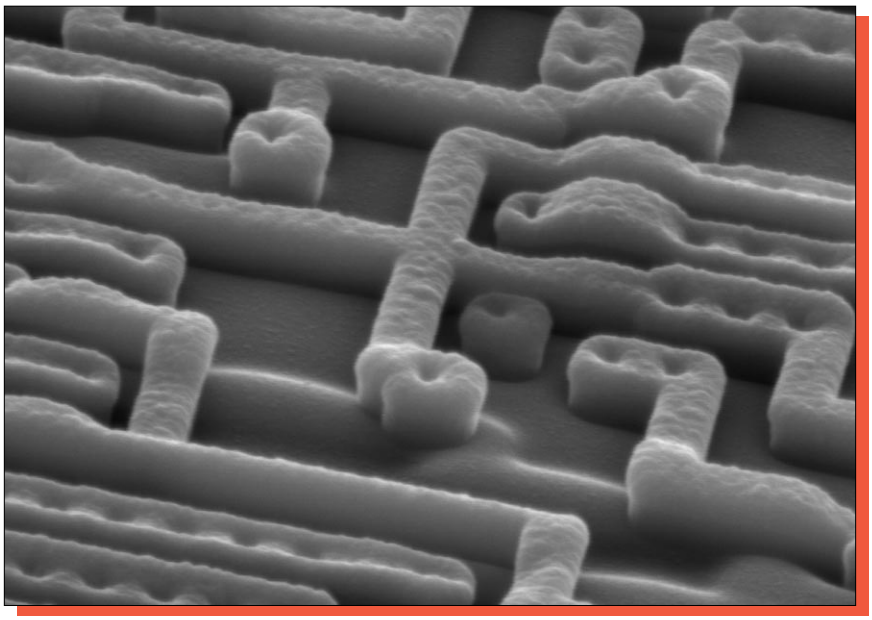
Figure 12a. Optical views illustrating die markings and a test device present on both die types.



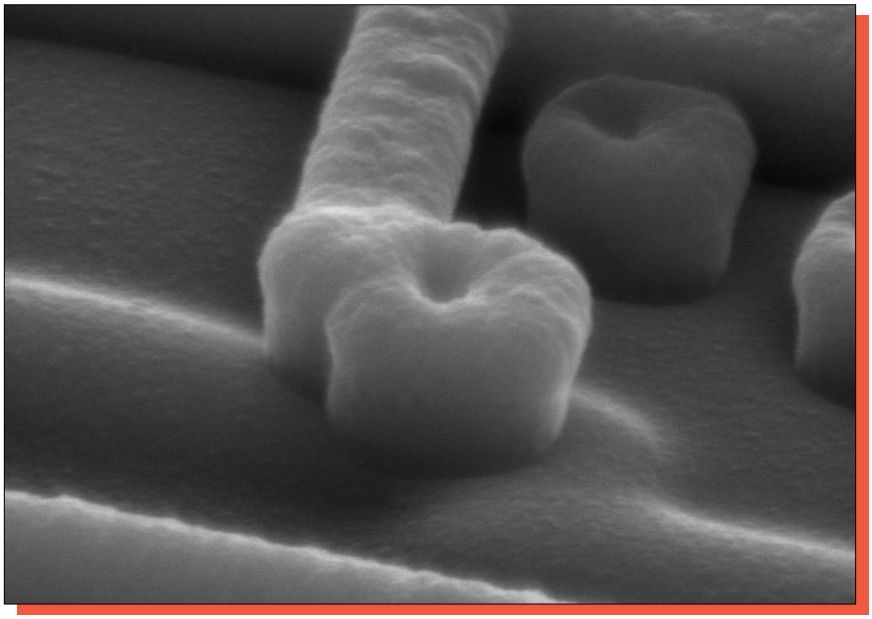


plasma etch

Figure 13. SEM section views illustrating general structure. Mag. 13,000x.

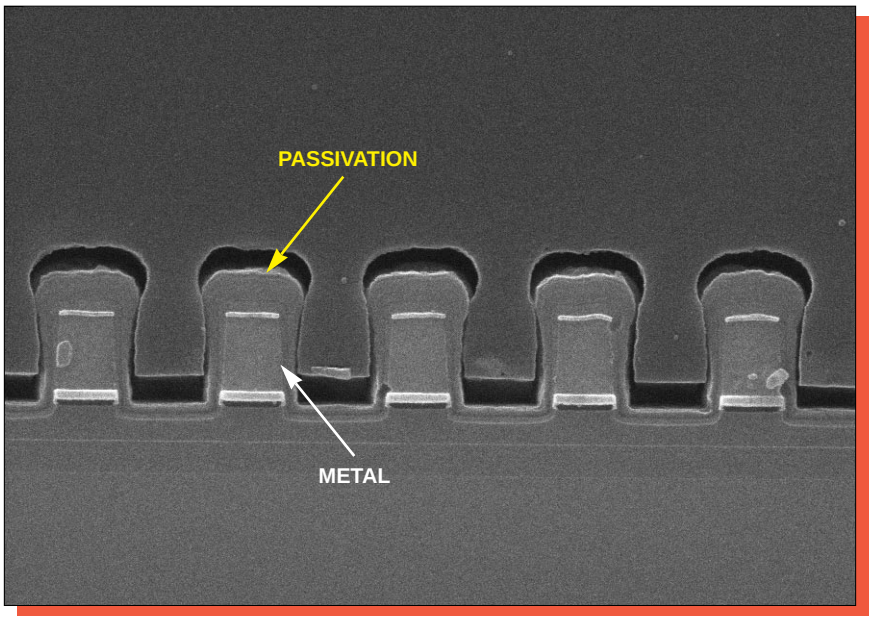


Mag. 6000x

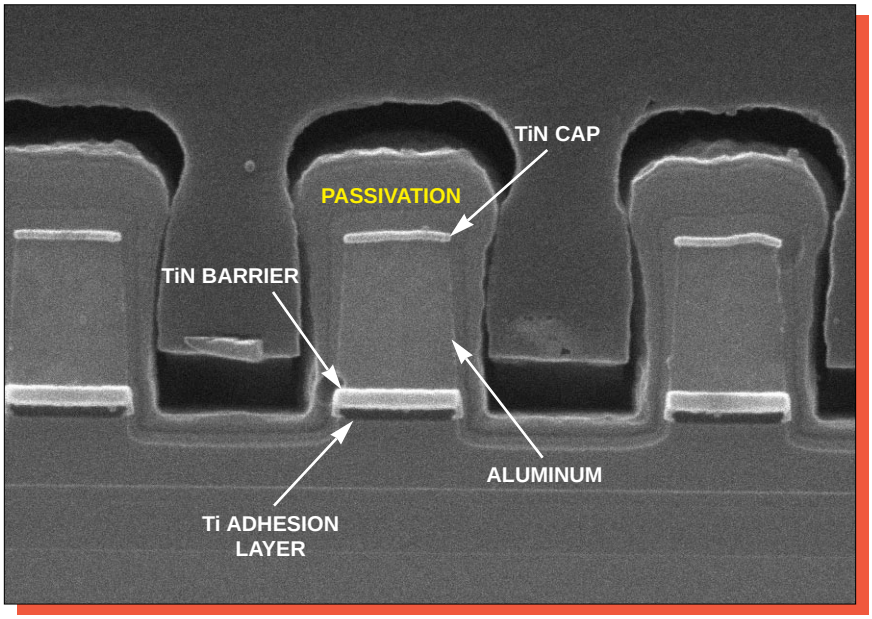


Mag. 15,000x

Figure 14. SEM views of overlay passivation coverage. 60°.



Mag. 13,000x



Mag. 26,000x

Figure 15. SEM section views of metal line profiles. Glass etch.

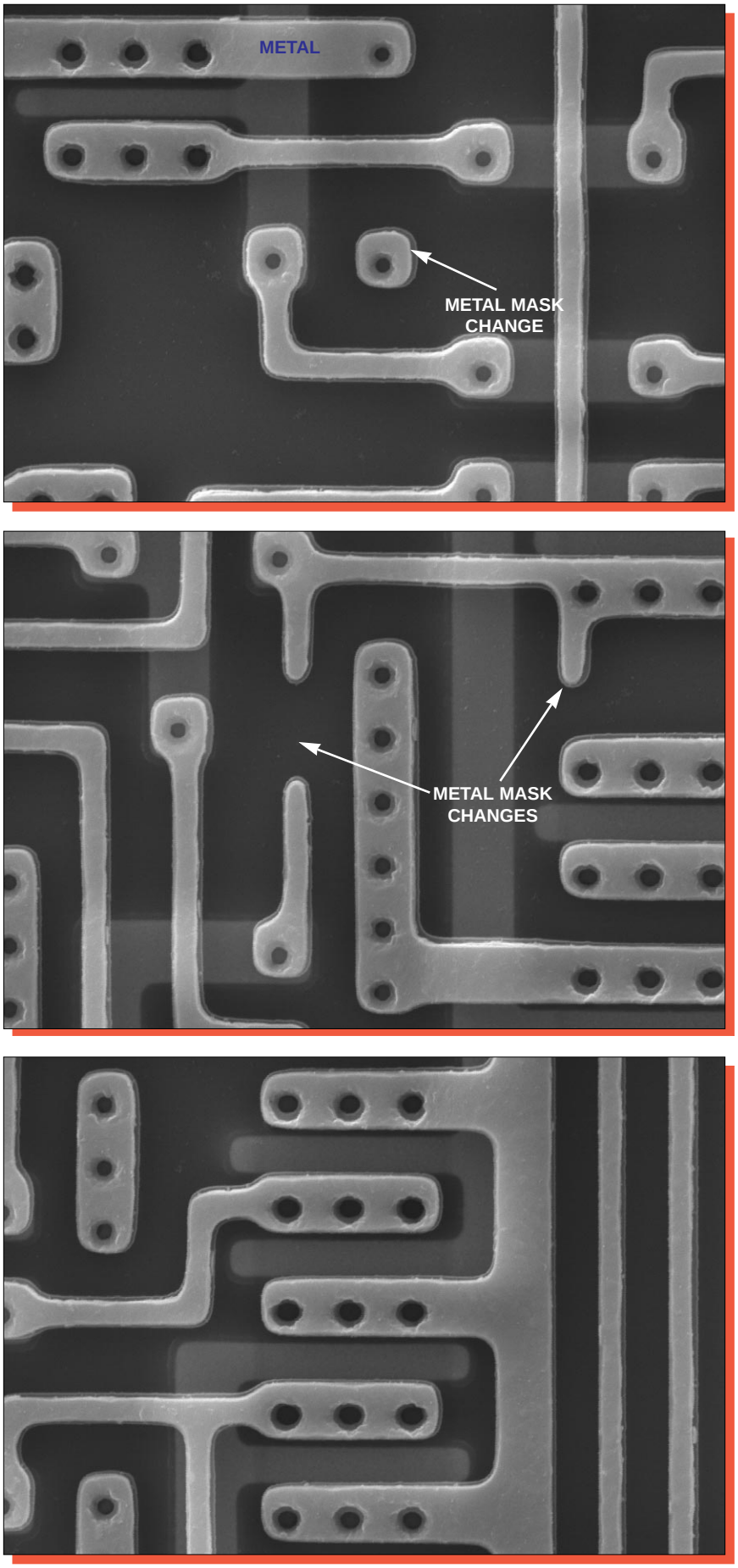
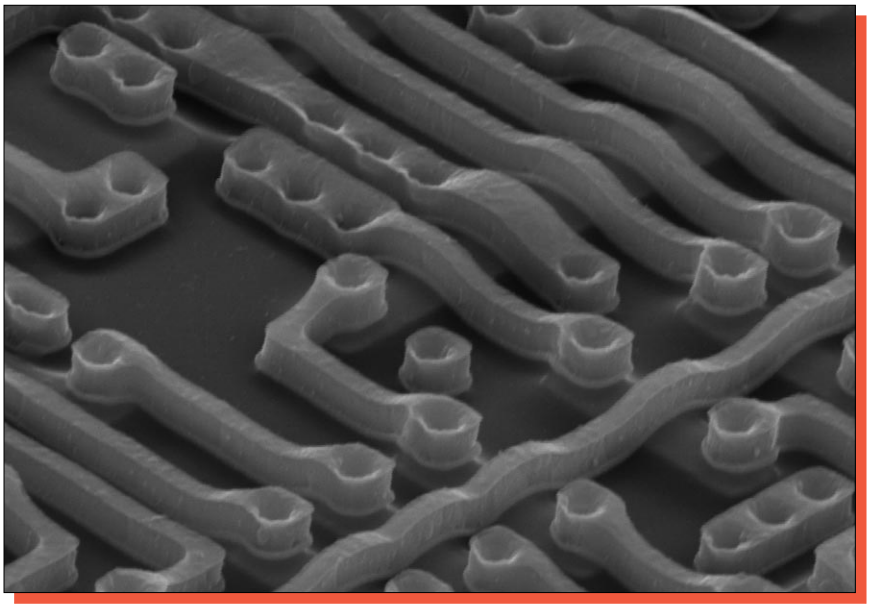
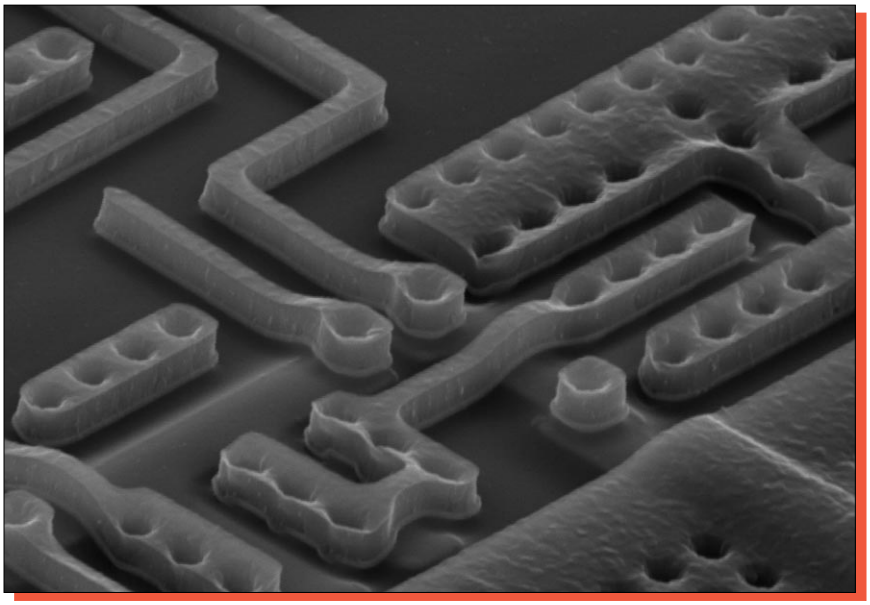


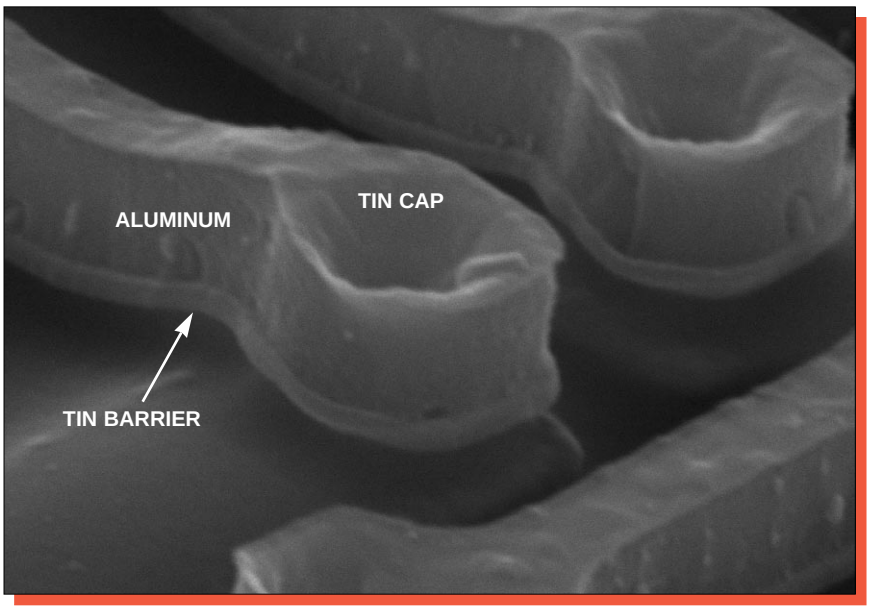
Figure 16. Topological SEM views of metal patterning. Mag. 6500x, 0°.



Mag. 6000x

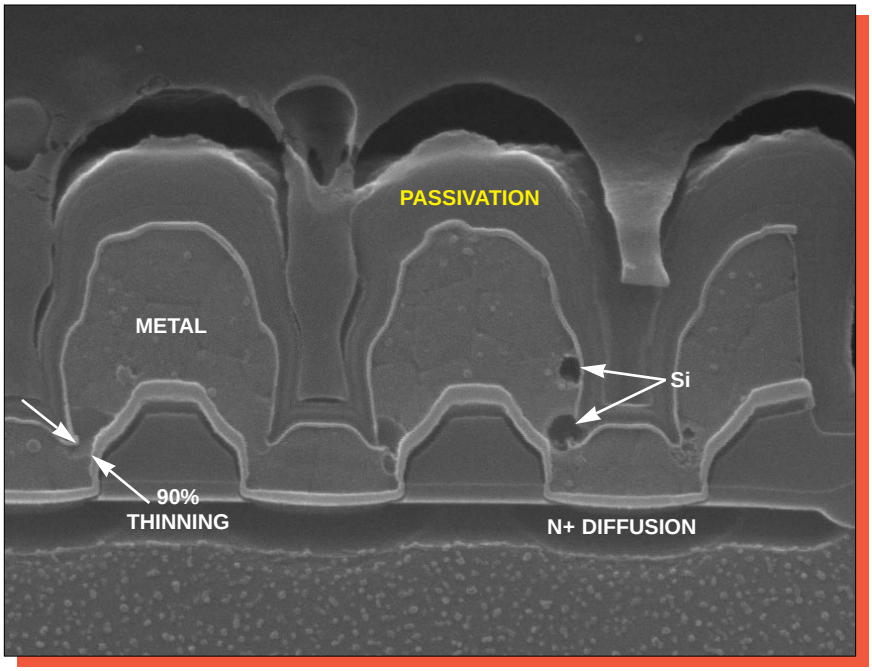


Mag. 6000x



Mag. 24,000x

Figure 17. Perspective SEM views of metal step coverage. 60°.



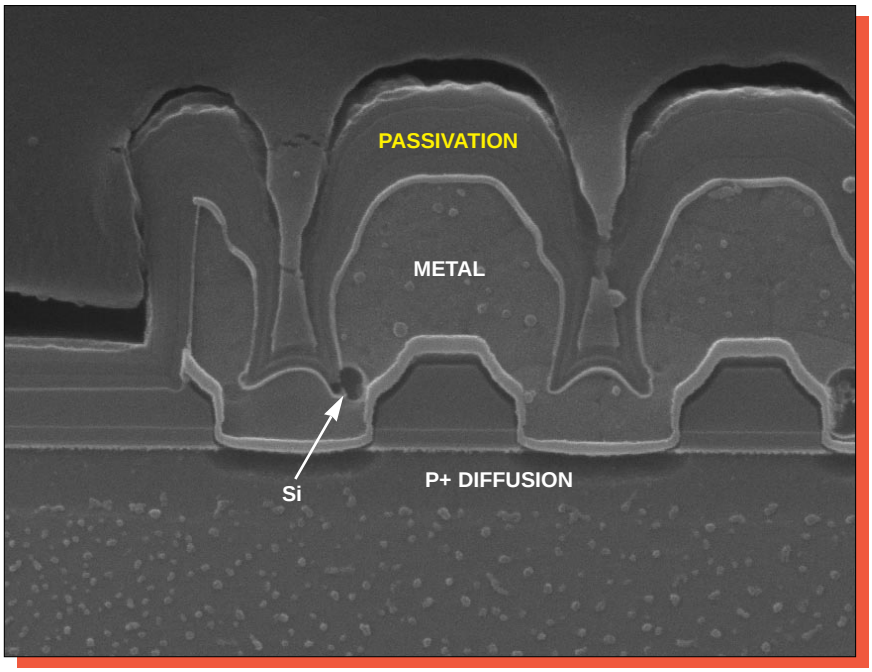
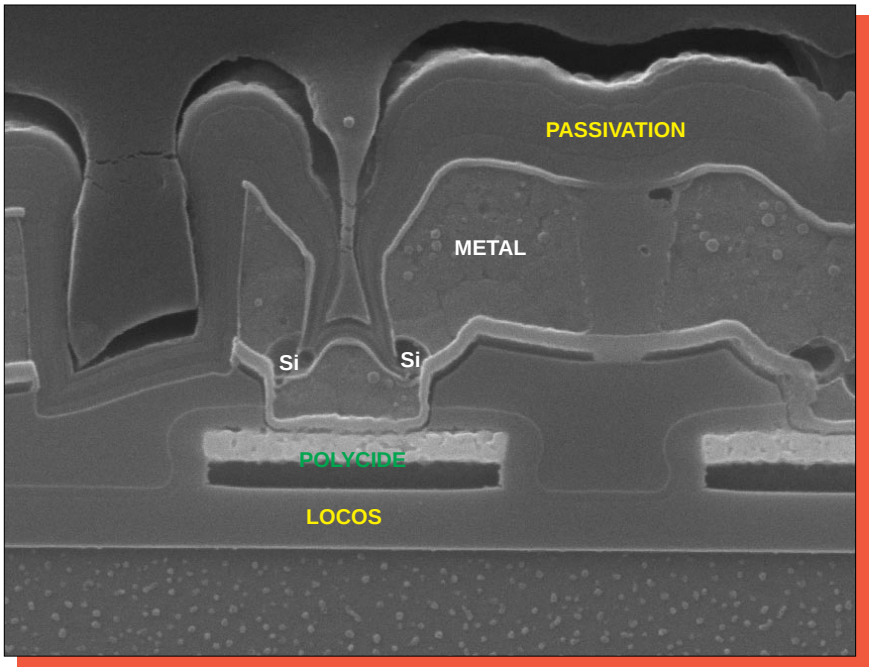
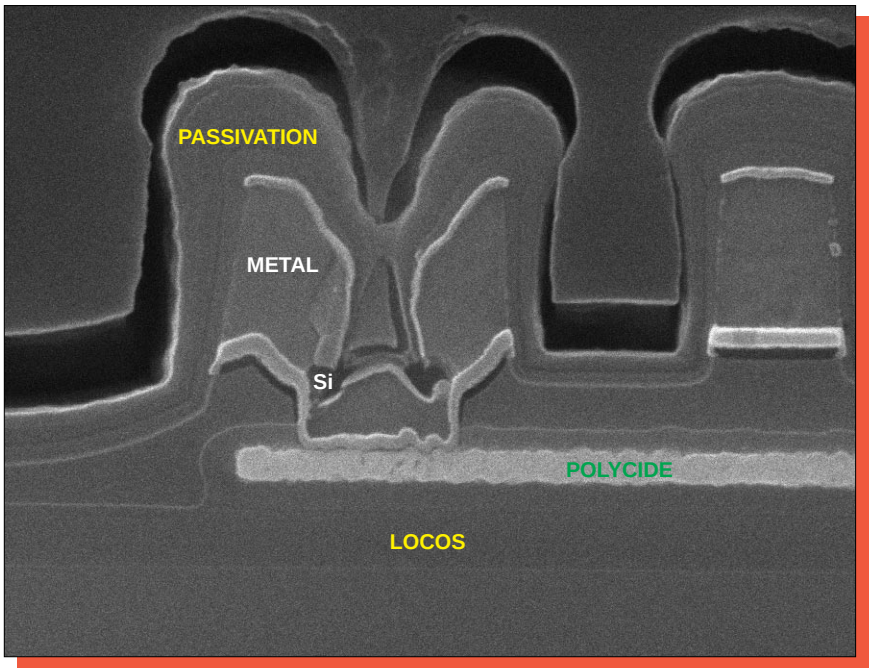


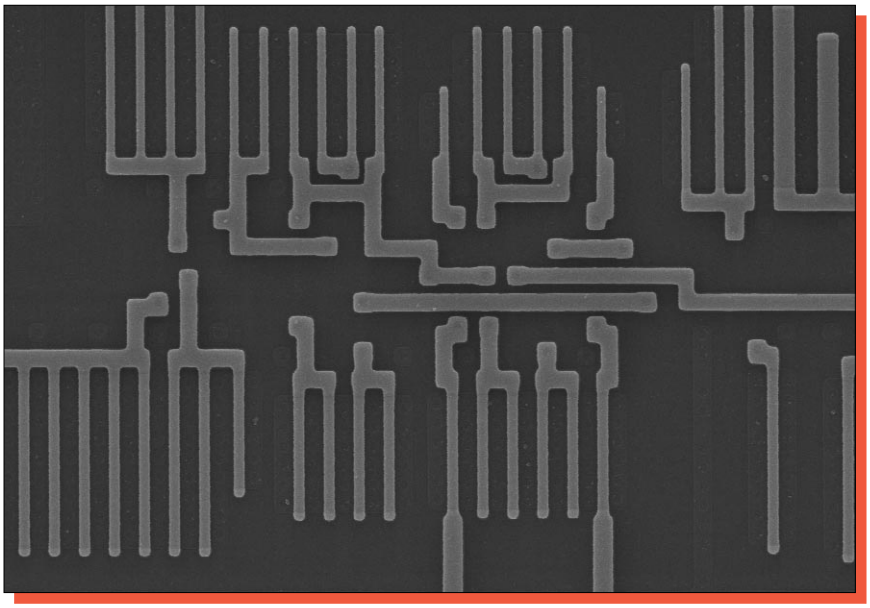
Figure 18. SEM section views of typical metal contacts. Mag. 26,000x.



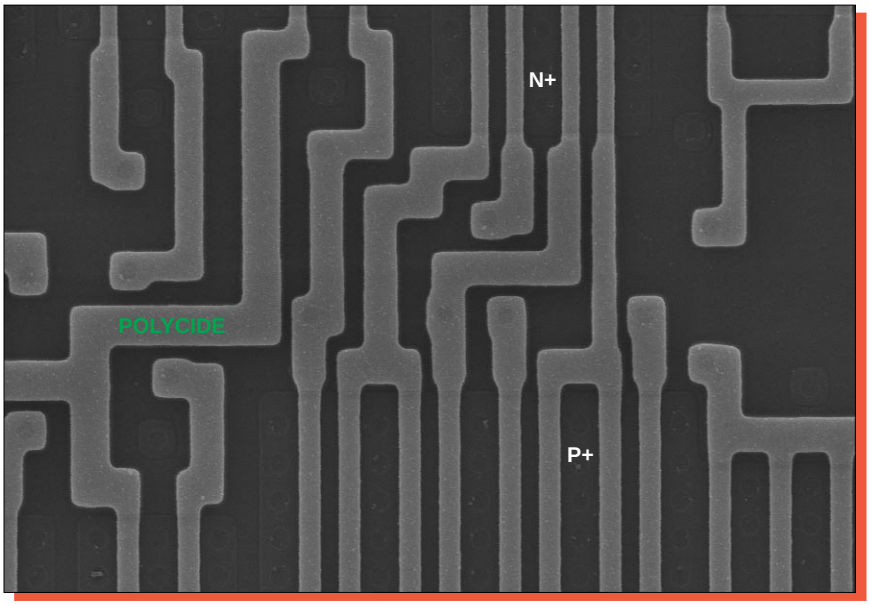


glass etch

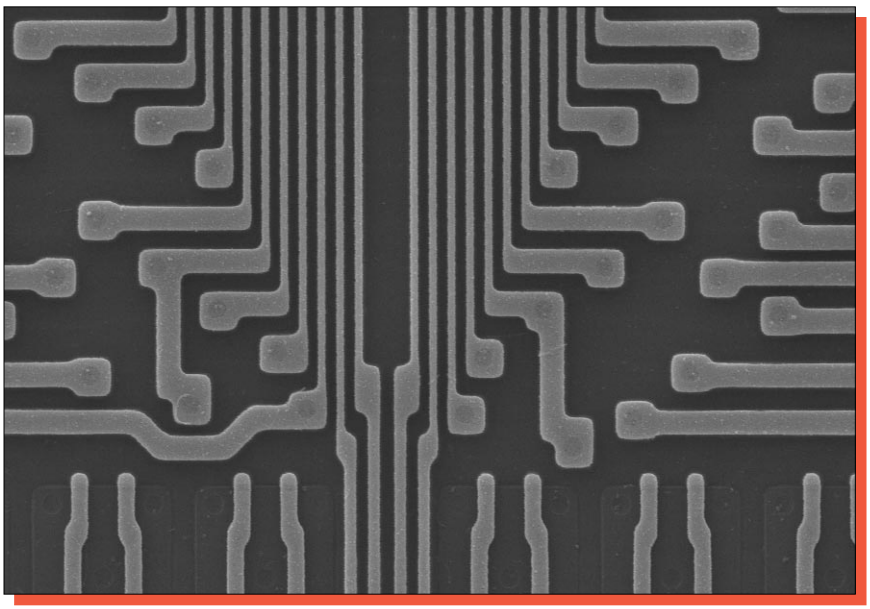
Figure 19. SEM section views of metal-to-polycide contacts. Mag. 26,000x.



Mag. 1600x

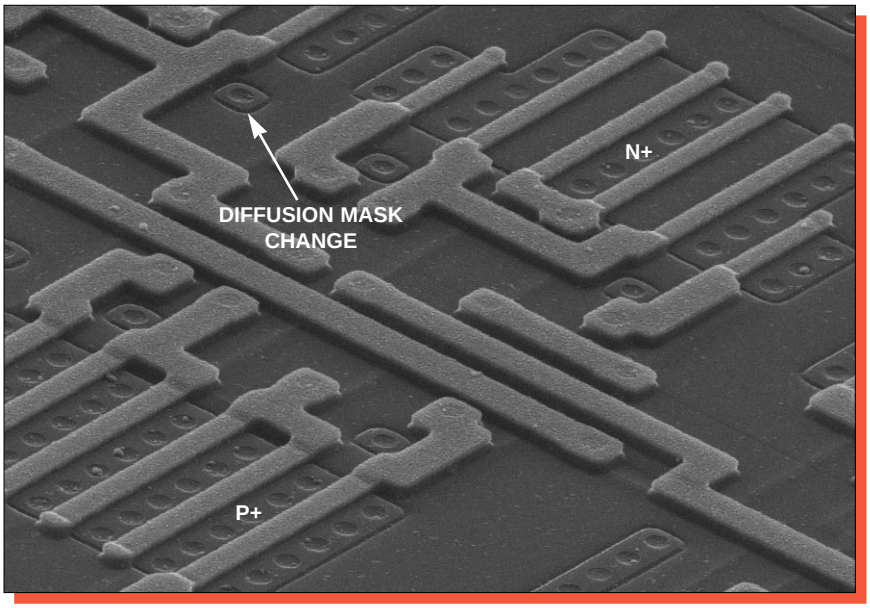


Mag. 3200x

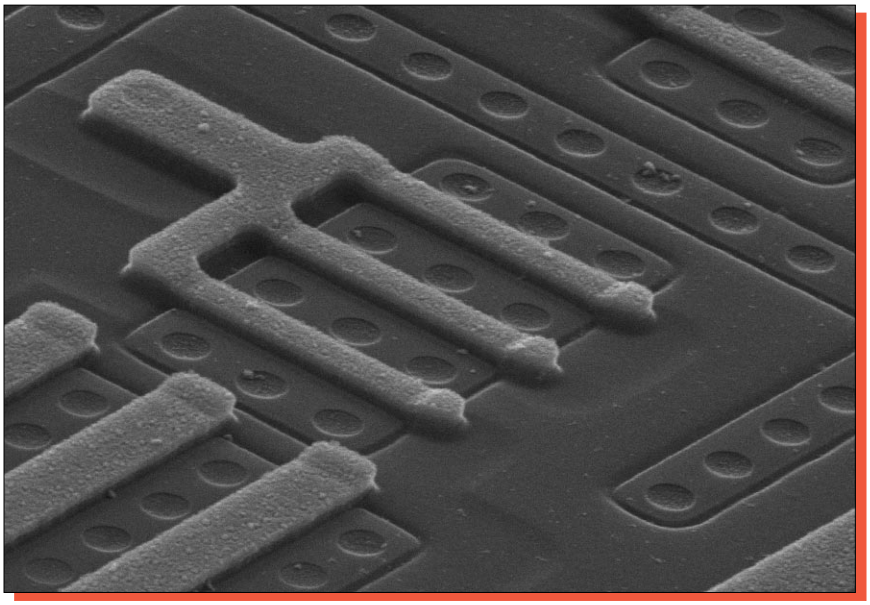


Mag. 3200x

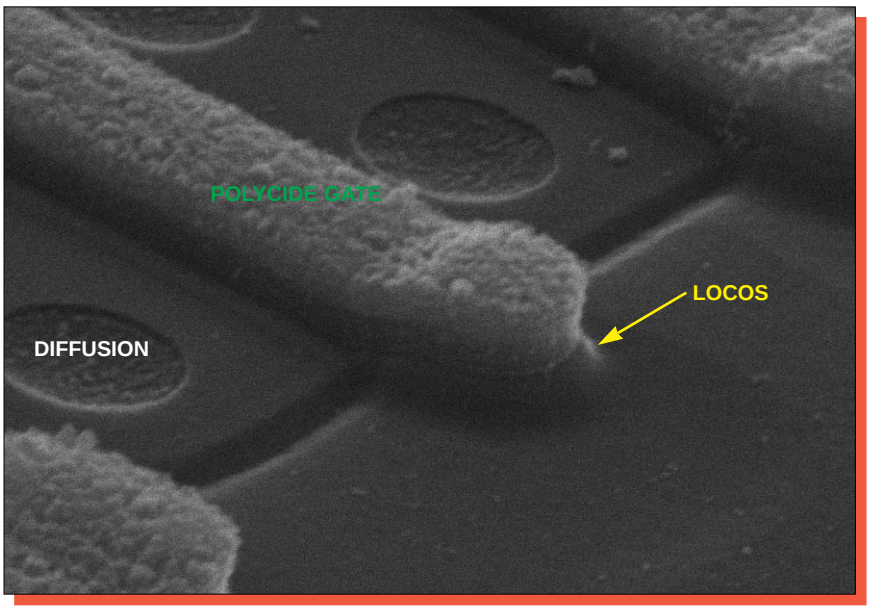
Figure 20. Topological SEM views of polycide patterning. 0°.



Mag. 4200x

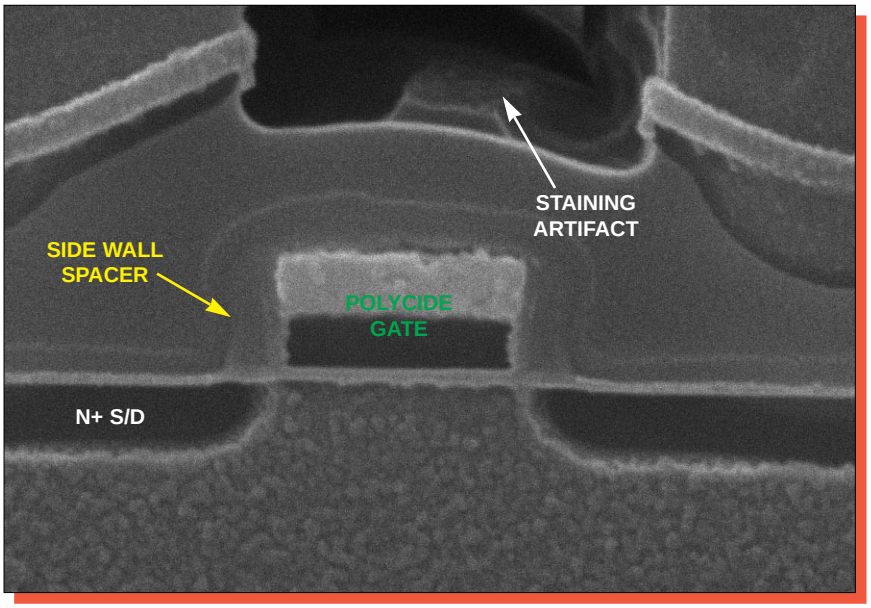


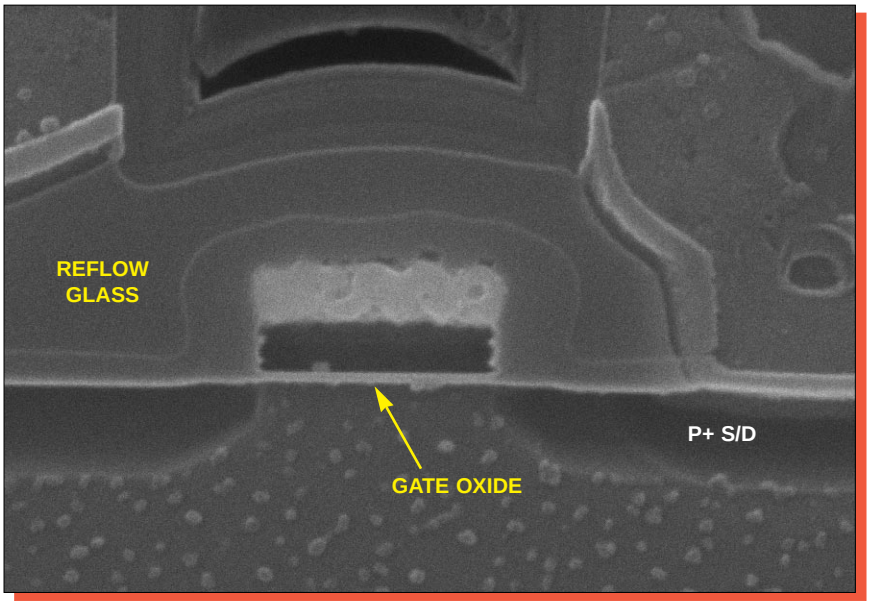
Mag. 8400x

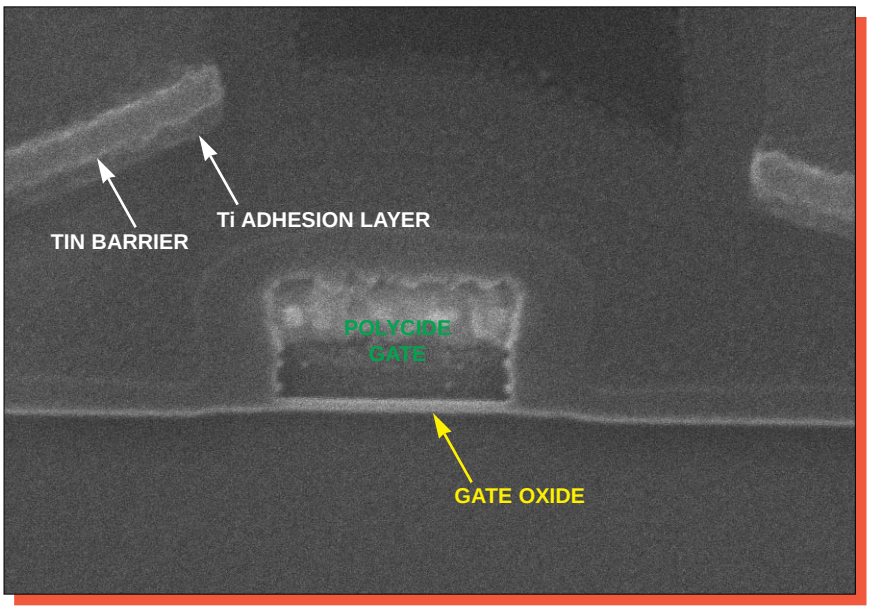


Mag. 33,600x

Figure 21. Perspective SEM views of polycide coverage. 60°.







plasma etch

Figure 22. SEM section views of typical transistors. Mag. 52,000x.

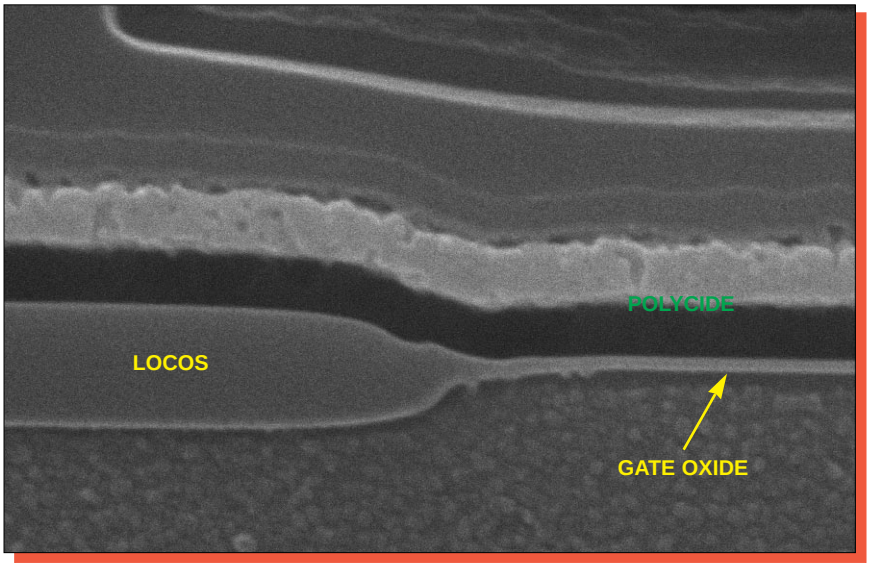
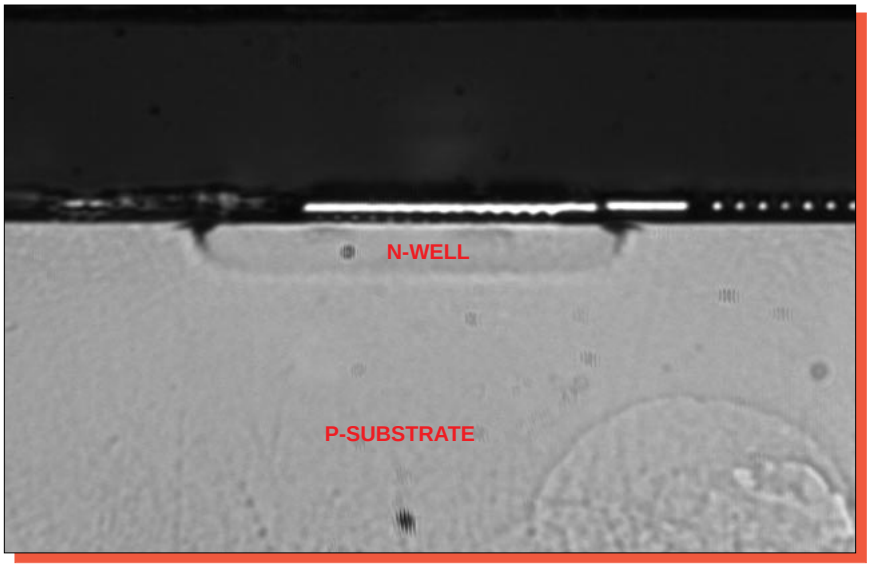
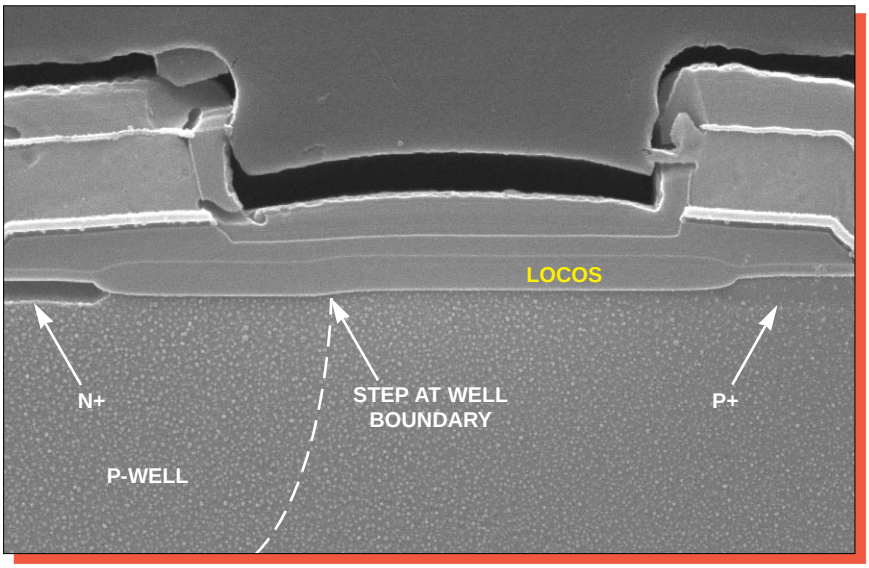


Figure 23. SEM section views of a typical birdsbeak. Mag. 52,000x.

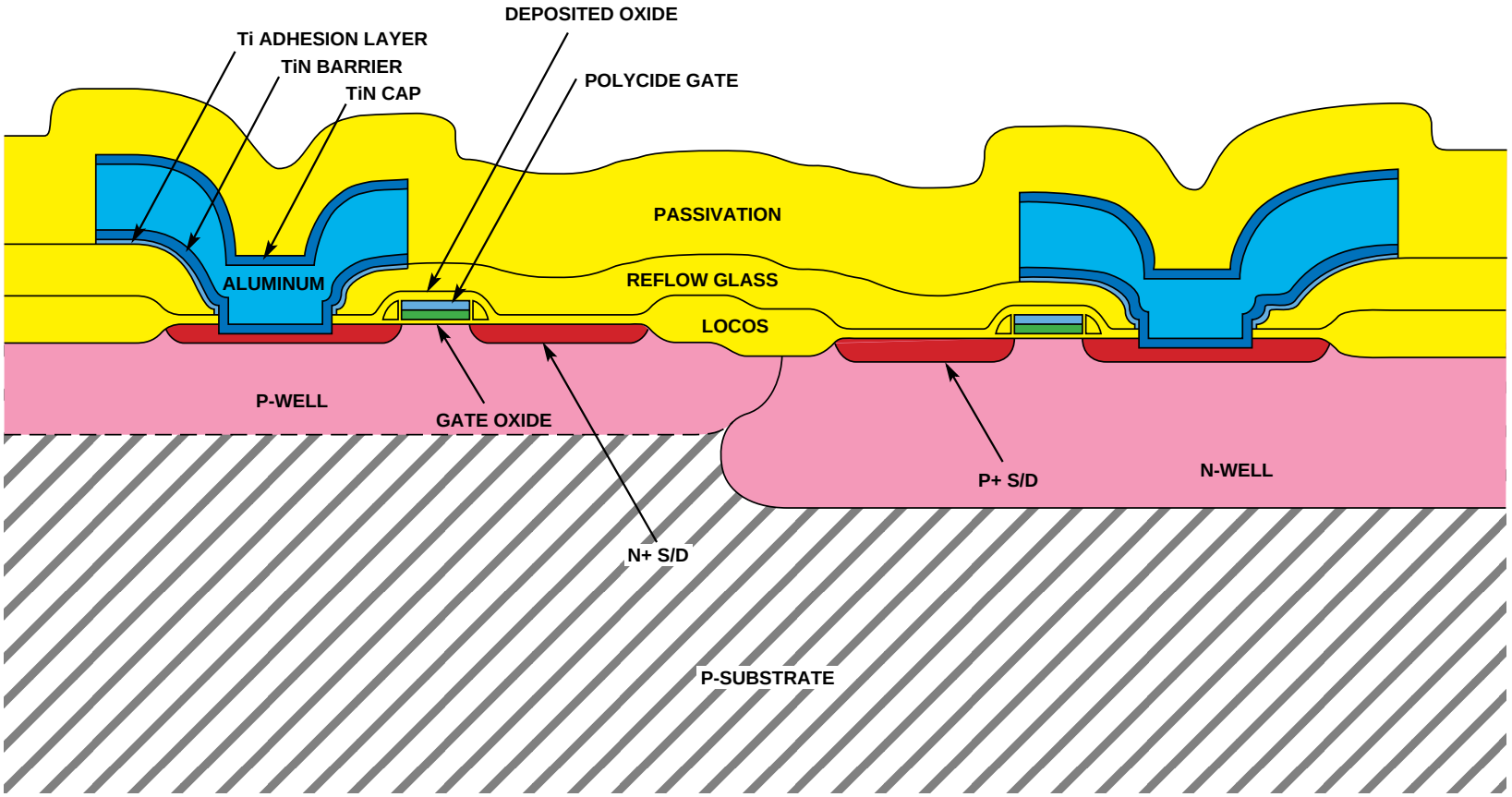


Mag. 1500x



Mag. 13,000x

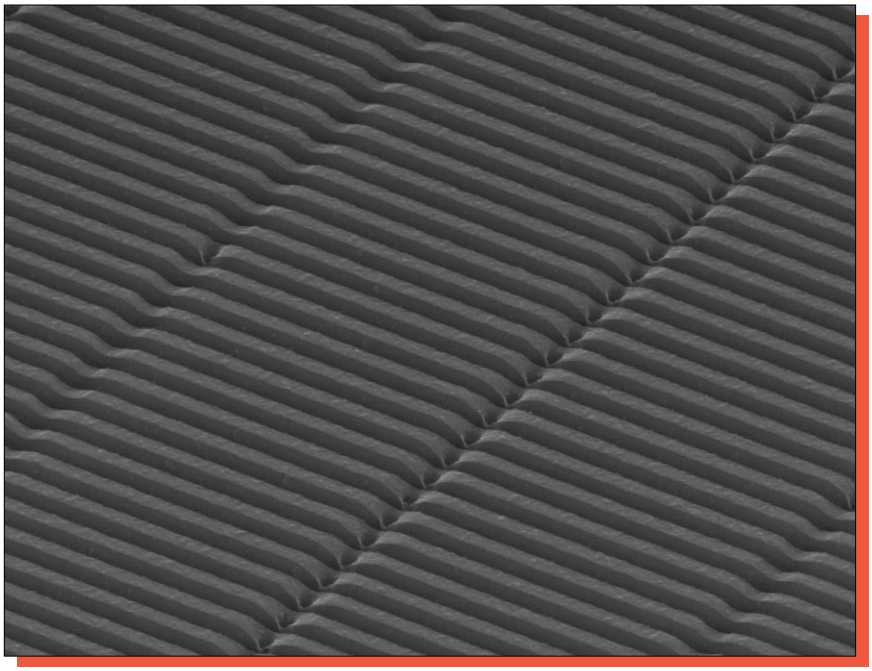
Figure 24. Section views illustrating well structure.



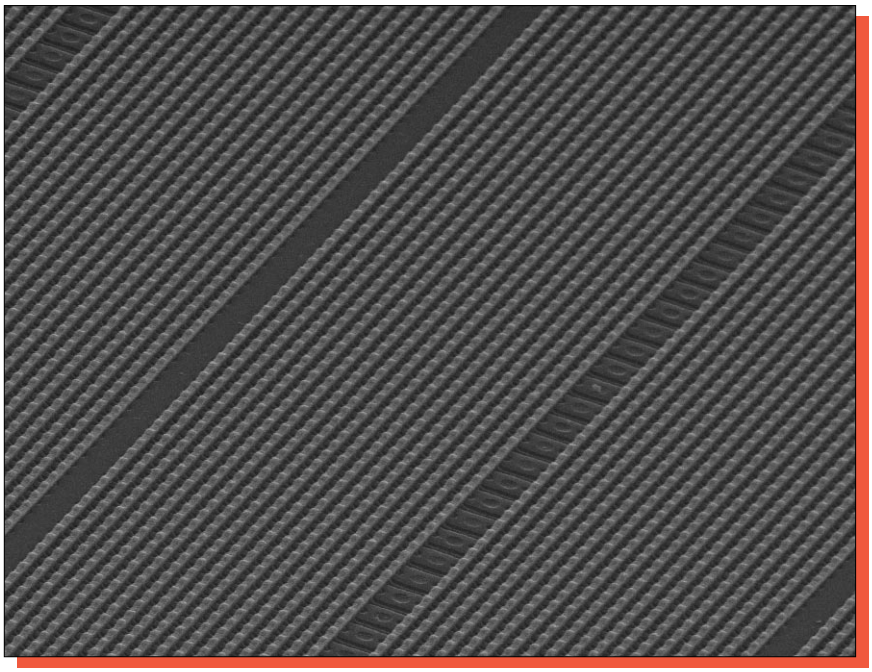
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 25. Color cross section drawing illustrating device structure.

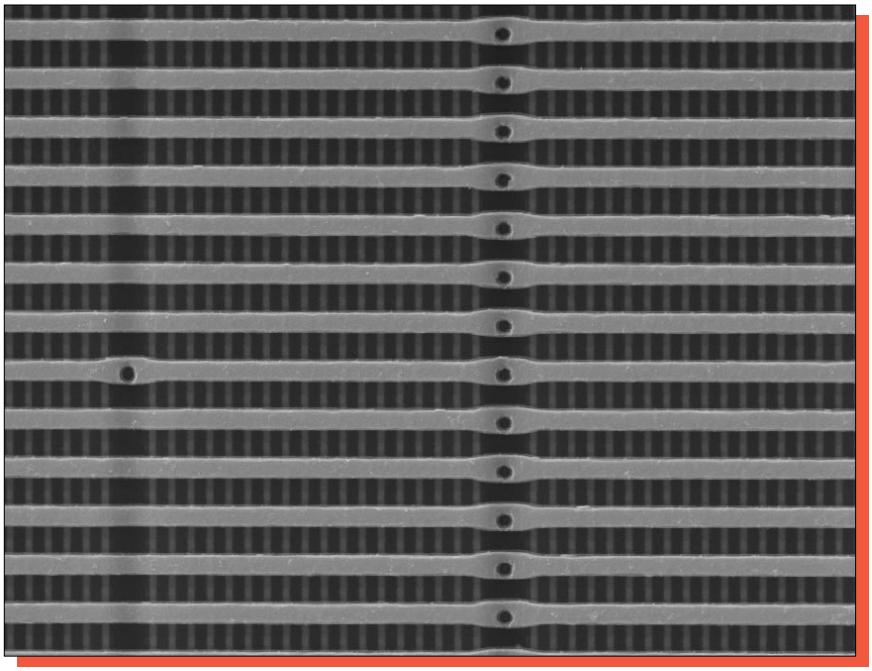


metal

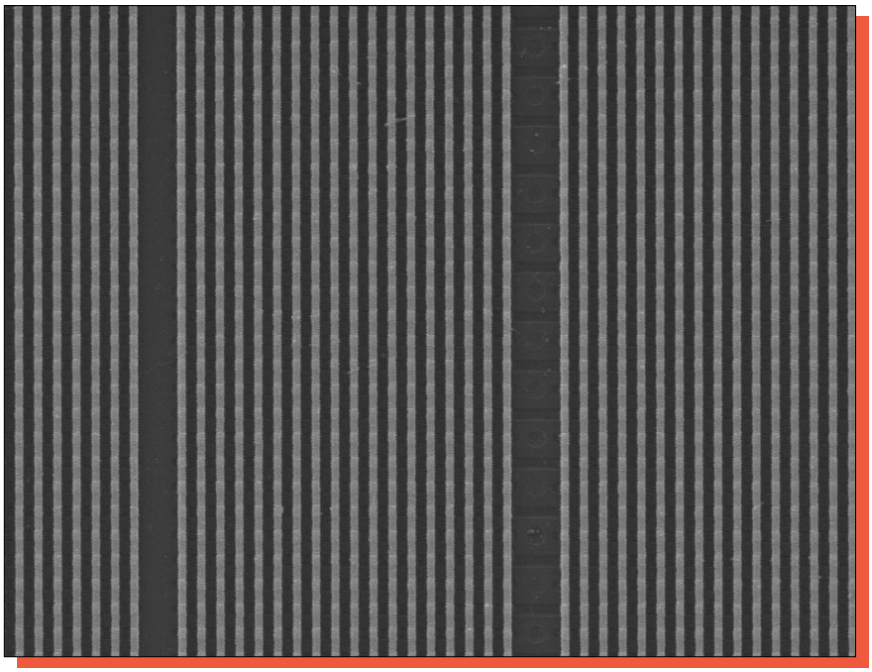


polycide

Figure 26. Perspective SEM views of the NAND ROM array. Mag. 3200x, 60°.

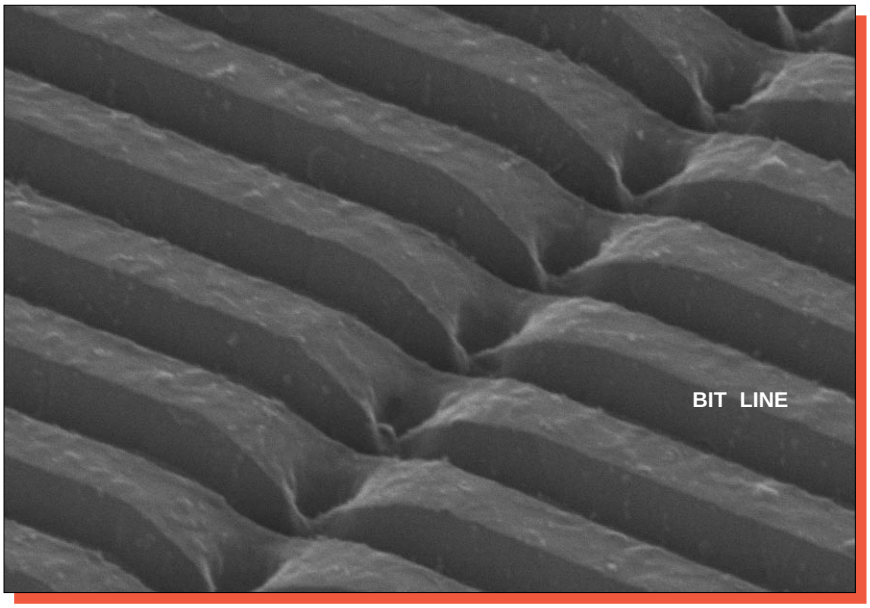


metal

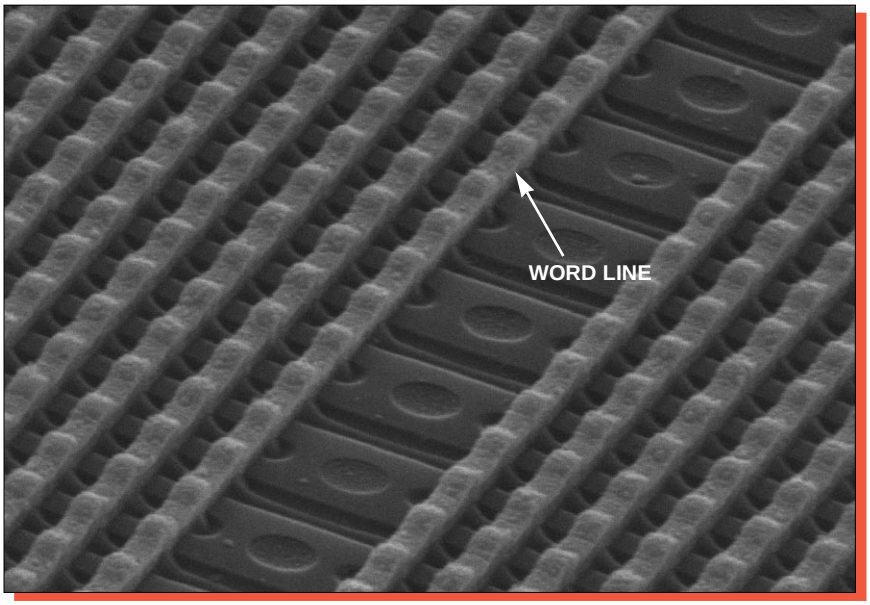


polycide

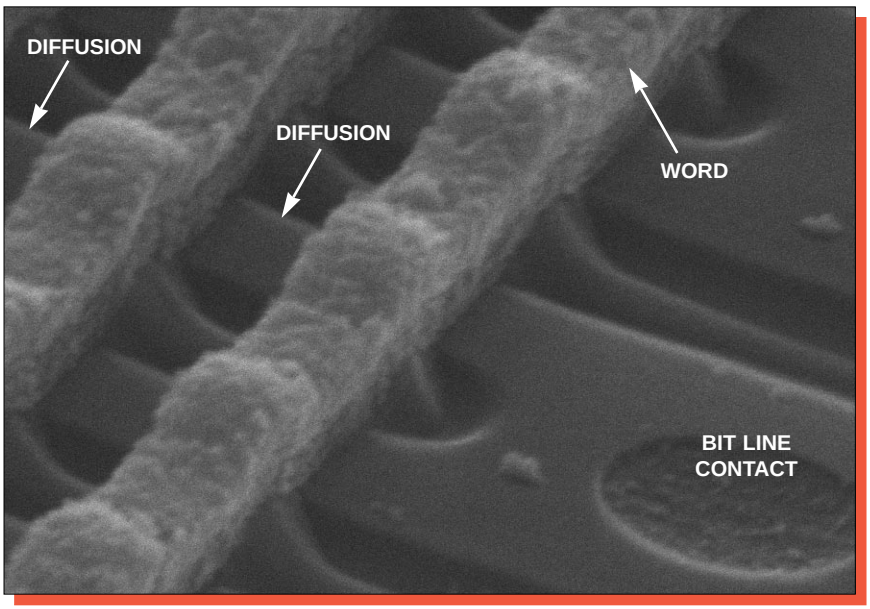
Figure 27. Topological SEM views of the NAND ROM array. Mag. 3200x, 0°.



metal,
Mag. 13,000x

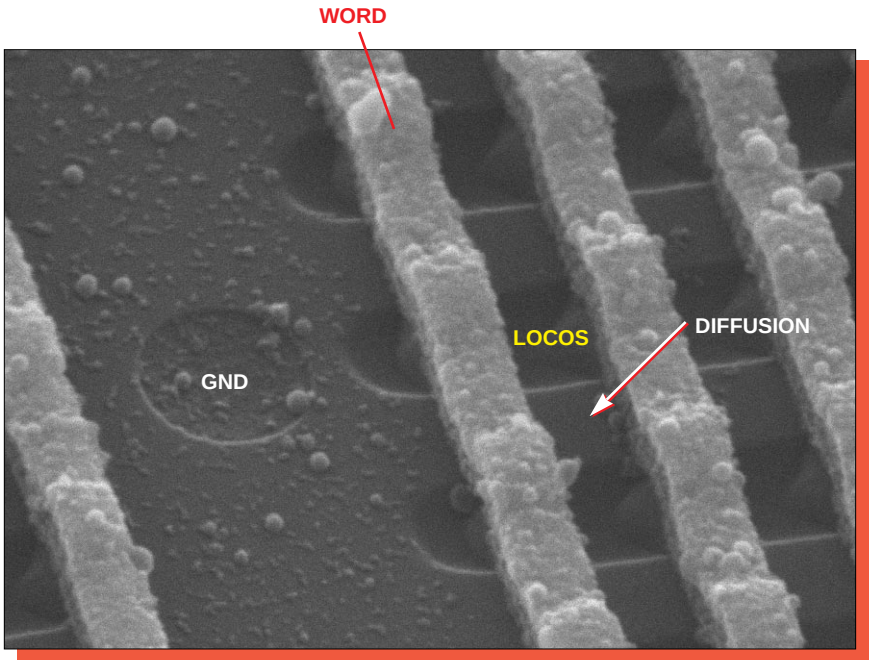


polycide,
Mag. 13,000x



Mag. 52,000x

Figure 28. Detailed perspective SEM views of the NAND ROM array. 60°.



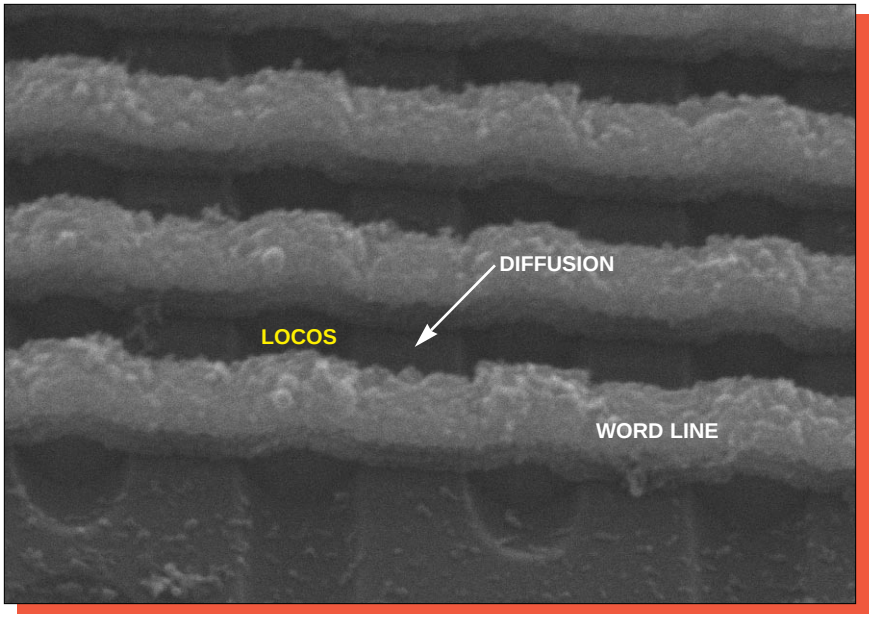
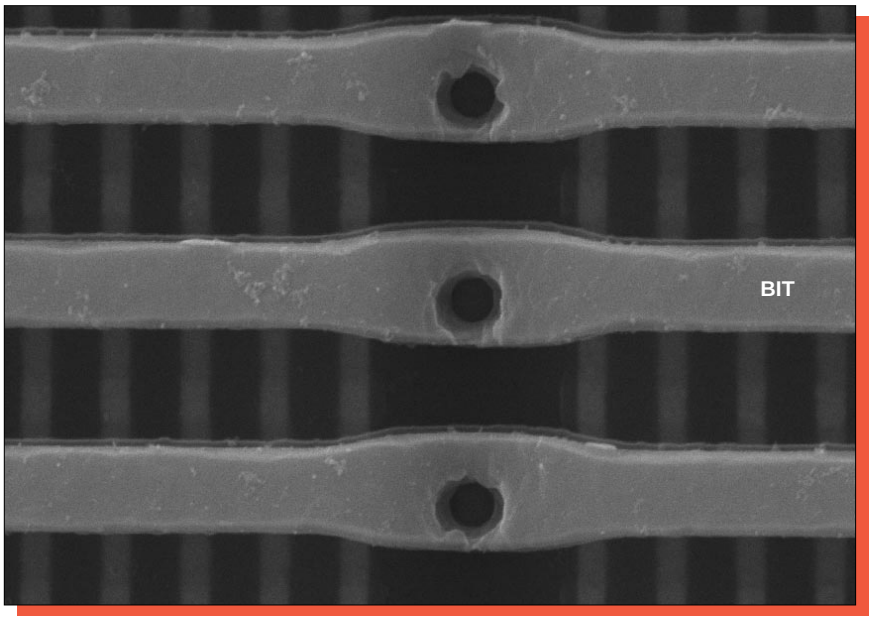


Figure 28a. Additional detailed SEM views of the NAND ROM array.
Mag. 31,000x, 40°.



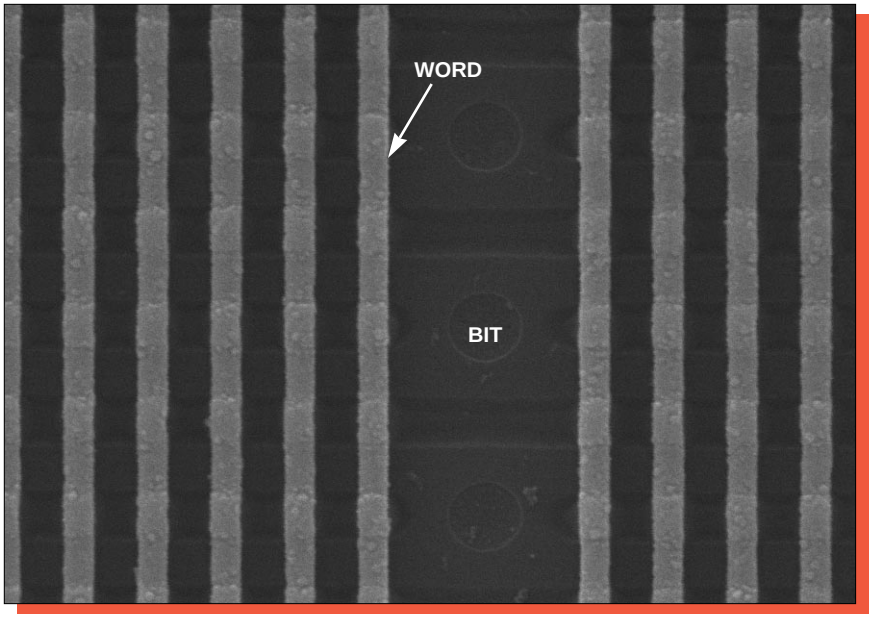
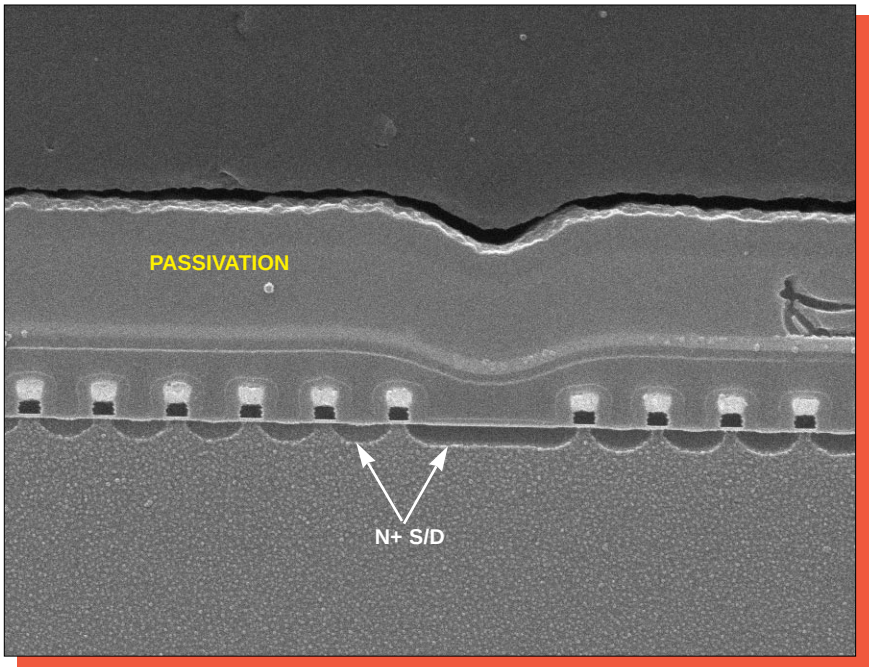
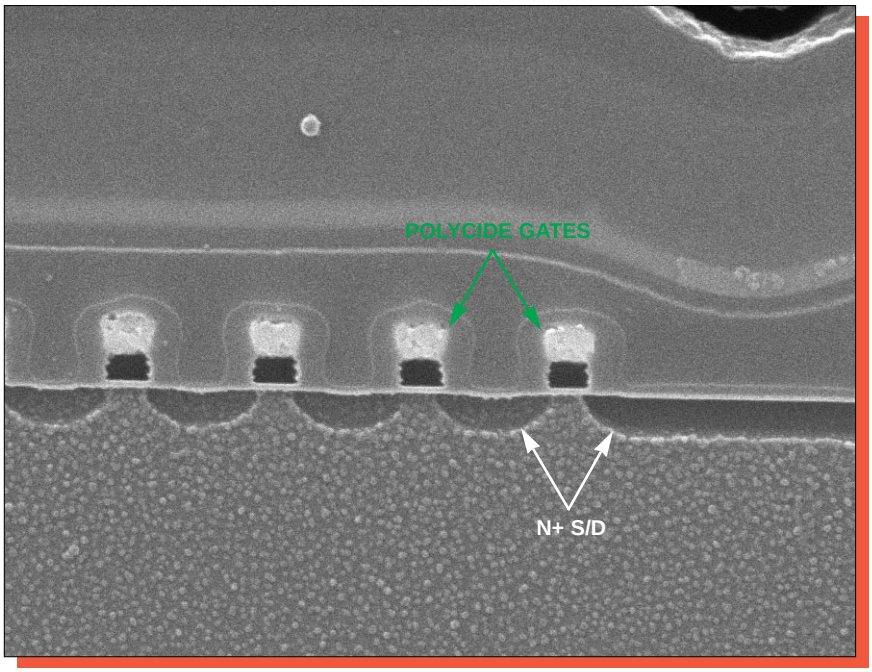


Figure 29. Detailed topological SEM views of the NAND ROM array.
Mag. 13,000x, 0°.

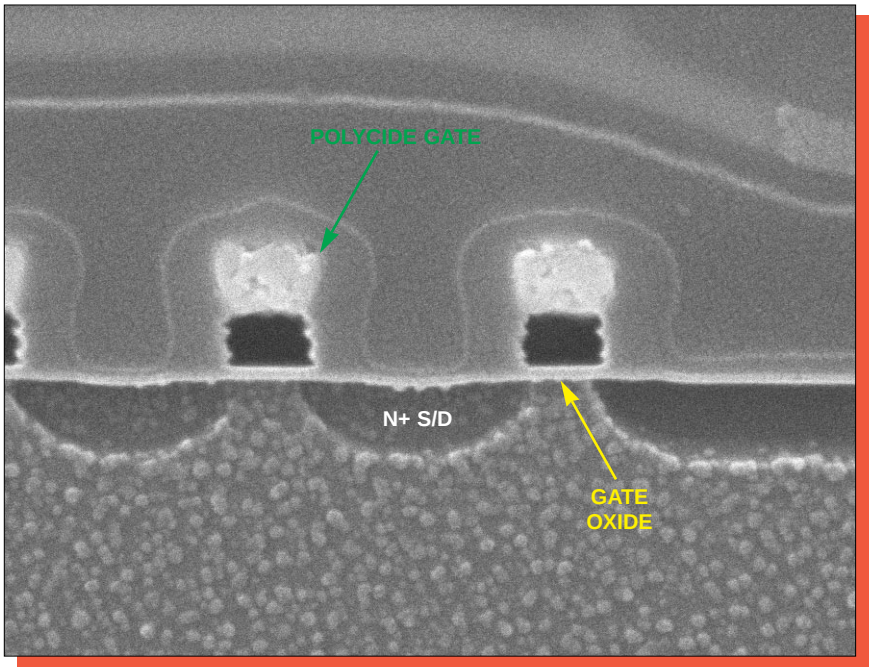


Mag.13,000x

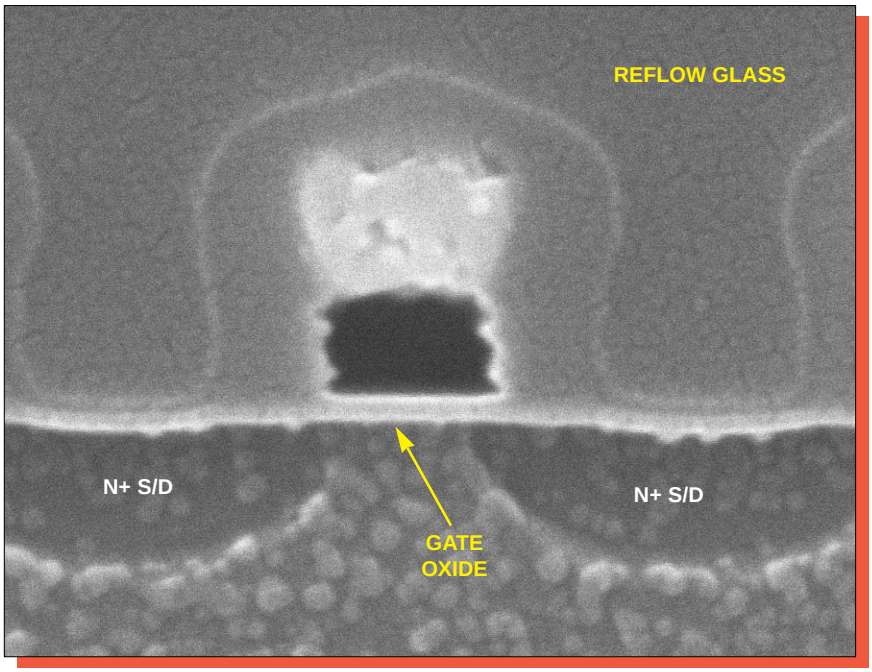


Mag. 26,000x

Figure 30. SEM section views of the NAND ROM array.

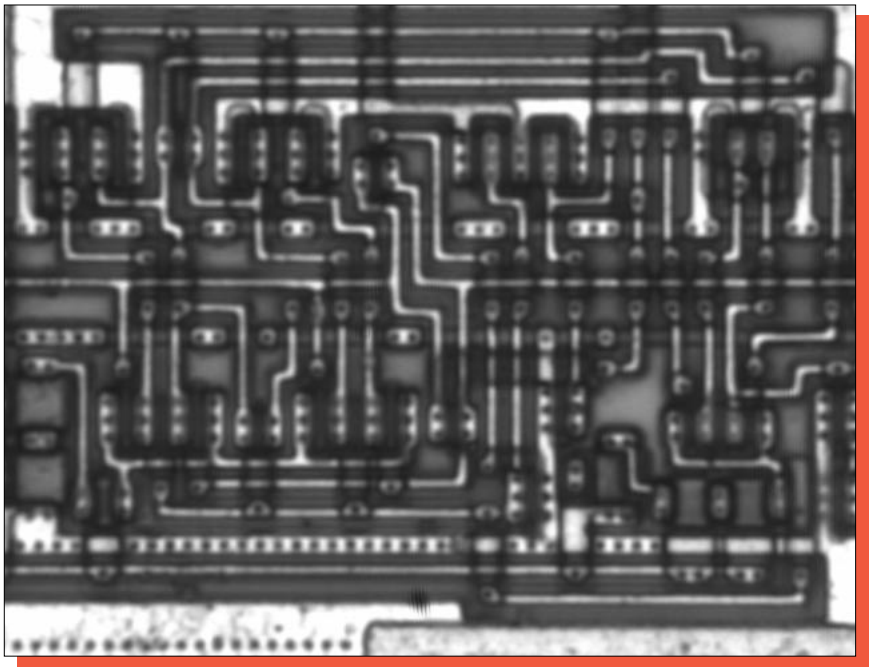


Mag. 52,000x

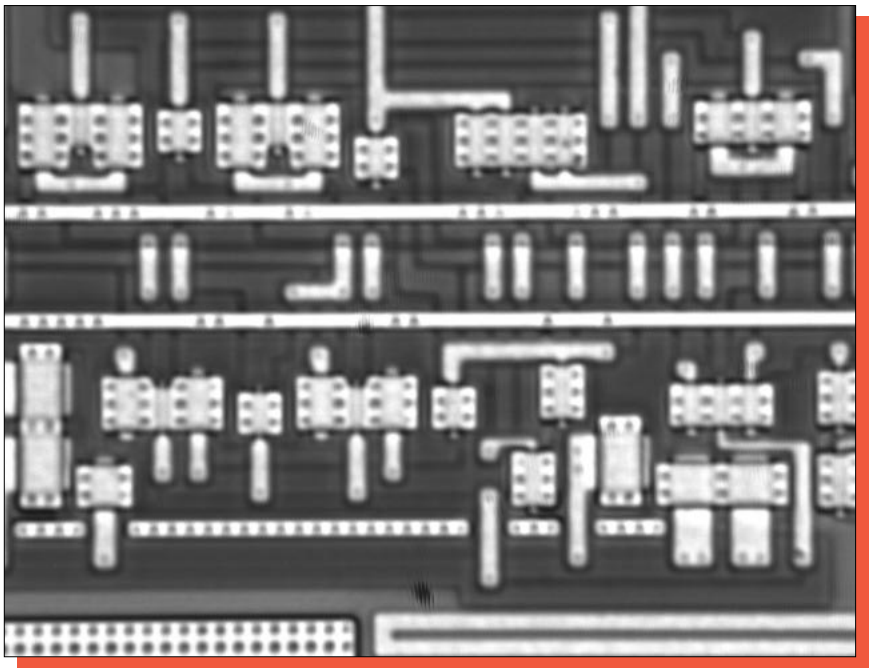


Mag. 104,000x

Figure 31. Detailed SEM section views of the NAND ROM array.



intact



unlayered

Figure 32. Optical views of typical circuitry. Mag. 1500x.