Construction Analysis

NEC D481850GE-A10
8Mb SGRAM

Report Number: SCA 9703-531

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the NEC D41850GE-A10, 8 Meg SGRAM. One decapsulated was received for the analysis. No date code was visible but parts were undoubtedly made in 1996.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Sub-micron gate lengths (0.45 micron).
- Stacked capacitor DRAM cell design.
- Four layers of poly.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Die Process and Design

- Fabrication process: Selective oxidation CMOS process employing twin wells in a P-substrate (no epi was used).

- Final passivation: A single thick layer of nitride.

- Metallization: Metal 2 and metal 1 consisted of silicon-doped aluminum defined by a dry-etch technique. Both metal layers employed a titanium-nitride cap and barrier. Standard vias and tungsten plug contacts were employed.

- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a layer of glass followed by a spin-on-glass (SOG) and another layer of glass.

- Pre-metal dielectric: A single layer of reflow glass over a densified oxide.

- Polysilicon: Four layers of polysilicon were employed. Poly 4 was used to form the common plate of the DRAM capacitors. Poly 3 was used to form the individual plates of the DRAM capacitors. Polycide 2 (poly 2 and tungsten silicide) was used to form interconnect and bit lines in the cell. Polycide 1 (poly 1 and tungsten silicide) was used to form all gates and word lines on the die.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Oxide sidewall spacers were used and were left in place.

- Wells: Twin wells in a P-substrate (no epi). A step in the local oxide was noted at the edge of N-wells.

TECHNOLOGY DESCRIPTION (continued)

- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present.

- Memory cells: A stacked cell design using all four layers of poly as described above. Neither of the metal layers was used directly in the cells (i.e., used as "piggyback" word lines only). Cell size measured 3.1 microns^2.

ANALYSIS RESULTS

Die Process and Design: **Figures 1 - 35**

Questionable Items:[1] None.

Special Features:

- Sub-micron gate lengths (0.45 micron).
- Stacked capacitor DRAM cell design.
- Four layers of poly.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin wells in a P-substrate (no epi was used). No significant problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A single thick layer of nitride.
- Metallization: Metal 2 and metal 1 consisted of silicon-doped aluminum defined by a dry-etch technique. Both metal layers employed a titanium-nitride cap and barrier. Standard vias and tungsten plug contacts were employed. No problems were noted.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS (continued)

- Metal patterning: Both metal layers were defined by a dry-etch of good quality.

- Metal defects: None. No notching of voiding of the metal layers was found. No silicon nodules were found following removal of the aluminum.

- Metal step coverage: Metal 2 aluminum thinned up to 85 percent at vias. Typical metal 2 thinning was 80 percent. Military standards allow up to 70 percent metal thinning at contacts of this size. Virtually no metal 1 thinning was present due to the use of tungsten plugs at contacts.

- Vias and contacts: Via and contact cuts appeared to be defined by a two-step etch. No excessive over-etching or other problems were found.

- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a layer of glass followed by a spin-on glass (SOG) for planarization, and another layer of glass. No problems were found with these layers.

- Pre-metal dielectric: Three layers of reflow glass (BPSG) over a densified oxide in peripheral circuit areas and in the memory array (see Figure 13).

- Polysilicon: Four layers of polysilicon were employed. Poly 4 was in the form of a sheet and used to form the common plate of the DRAM capacitors. Poly 3 was used to form the individual plates of the DRAM capacitors. Polycide 2 (poly 2 and tungsten silicide) was used to form interconnect and bit lines in the cell. Polycide 1 (poly 1 and tungsten silicide) was used to form all gates and word lines on the die. Definition was good at all layers and no problems were noted.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries.

ANALYSIS RESULTS (continued)

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Sidewall spacers were used and left in place. No problems were found in any of these areas.

- Wells: Twin wells were used in a P substrate (no epi was present). A step in the oxide was noted at the edge of the wells (indication of twin-well process) and no problems were found. The P-well could not be delineated.

- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present.

- Memory cells: A stacked cell design using all four layers of poly as described above. Capacitors were formed over the bit line. Neither of the metal layers was used directly in the cells (i.e., used as "piggyback" word lines only). Cell pitch was 1.3 x 2.4 microns (3.12 microns^2).

PROCEDURE

The devices were subjected to the following analysis procedures:

Internal optical inspection and photography

SEM inspection of passivation

Delayer to metal 2 and inspect

Aluminum removal (metal 2) and inspect

Delayer to metal 1 and inspect

Aluminum removal (metal 1) and inspect

Delayer to poly 4, poly 3, poly 2 and inspect

Delayer to poly 1/substrate and inspect poly and substrate

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Metal registration	G
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MATERIAL ANALYSIS

Overlay passivation:	Nitride.
Metallization 2:	Aluminum with a titanium-nitride (TiN) cap and barrier.
Intermetal dielectric (IMD):	Two layers of silicon-dioxide with a planarizing glass (SOG) between.
Metallization 1:	Aluminum with a titanium-nitride (TiN) cap and barrier.
Pre-metal glass:	Three layers of reflow glass over a densified oxide.
Polycide:	Tungsten-silicide.

HORIZONTAL DIMENSIONS

Die size:	6.8 x 9.9 mm (271 x 393 mils)
Die area:	69 mm^2 (106,503 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.3 x 4.3 mils)
Min pad window:	0.09 x 0.09 mm (3.8 x 3.8 mils)
Min pad space:	0.05 mm (2.0 mils)
Min metal 2 width:	1.3 micron
Min metal 2 space:	1.5 micron
Min metal 2 pitch:	2.8 microns
Min via:	1.1 micron
Min via pitch:	2.0 microns
Min metal 1 width:	0.6 micron
Min metal 1 space:	0.5 micron
Min metal 1 pitch:	1.1 micron
Min contact:	0.7 micron
Min contact pitch:	1.4 micron
Min poly 3 width:	0.8 micron
Min poly 3 space:	0.4 micron
Min polycide 2 width:	0.2 micron
Min polycide 2 space:	0.7 micron
Min polycide 1 width - (cell):	0.2 micron
Min polycide 1 space:	0.5 micron
Min gate length* - (N-channel):	0.6 micron
- (P-channel):	0.8 micron
Cell size:	3.12 $microns^2$
Cell pitch:	1.3 x 2.4 microns

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.4 mm (15.5 mils)

Layers

Passivation:	0.8 micron
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.9 micron
- barrier:	0.1 micron
Intermetal dielectric - glass 3:	0.4 micron
- glass 2 (SOG):	0 - 0.6 micron
- glass 1:	0.5 micron
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.4 micron
- barrier:	0.1 micron
Reflow glass 3:	0.5 - 0.9 micron
Reflow glass 2:	0.3 - 0.5 micron
Reflow glass 1:	0.1 - 0.3 micron
Poly 4 (sheet):	1.3 micron
Poly 3:	0.35 micron
Polycide 2:	0.1 micron
Polycide 1:	0.2 micron
Local oxide:	0.25 micron
N+ S/D diffusion:	0.25 micron
P+ S/D diffusion:	0.3 micron (approximate)
N-well:	5 microns

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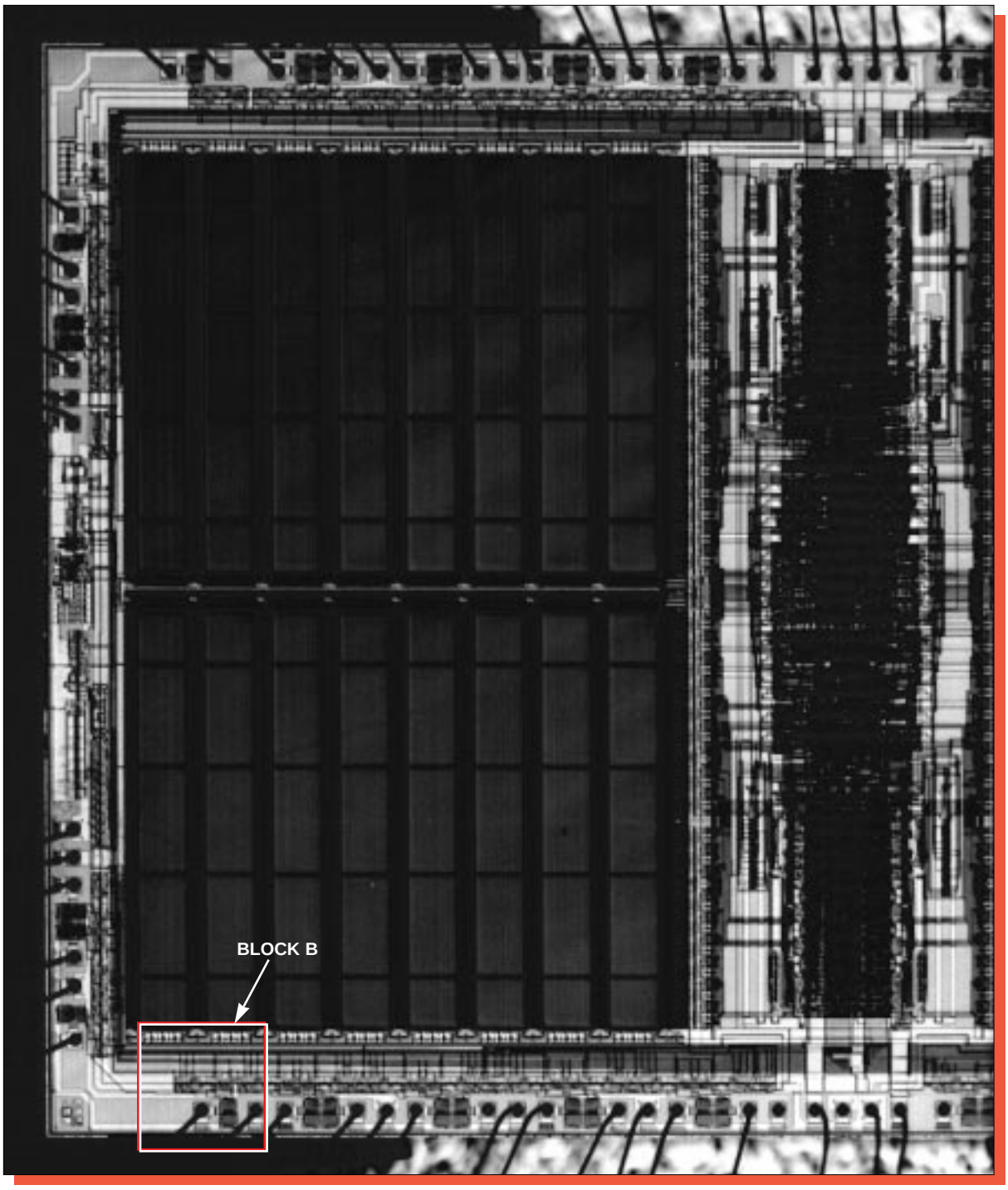


Figure 1. Portion of the NEC D481850GE-A10 intact die. Mag. 26x.

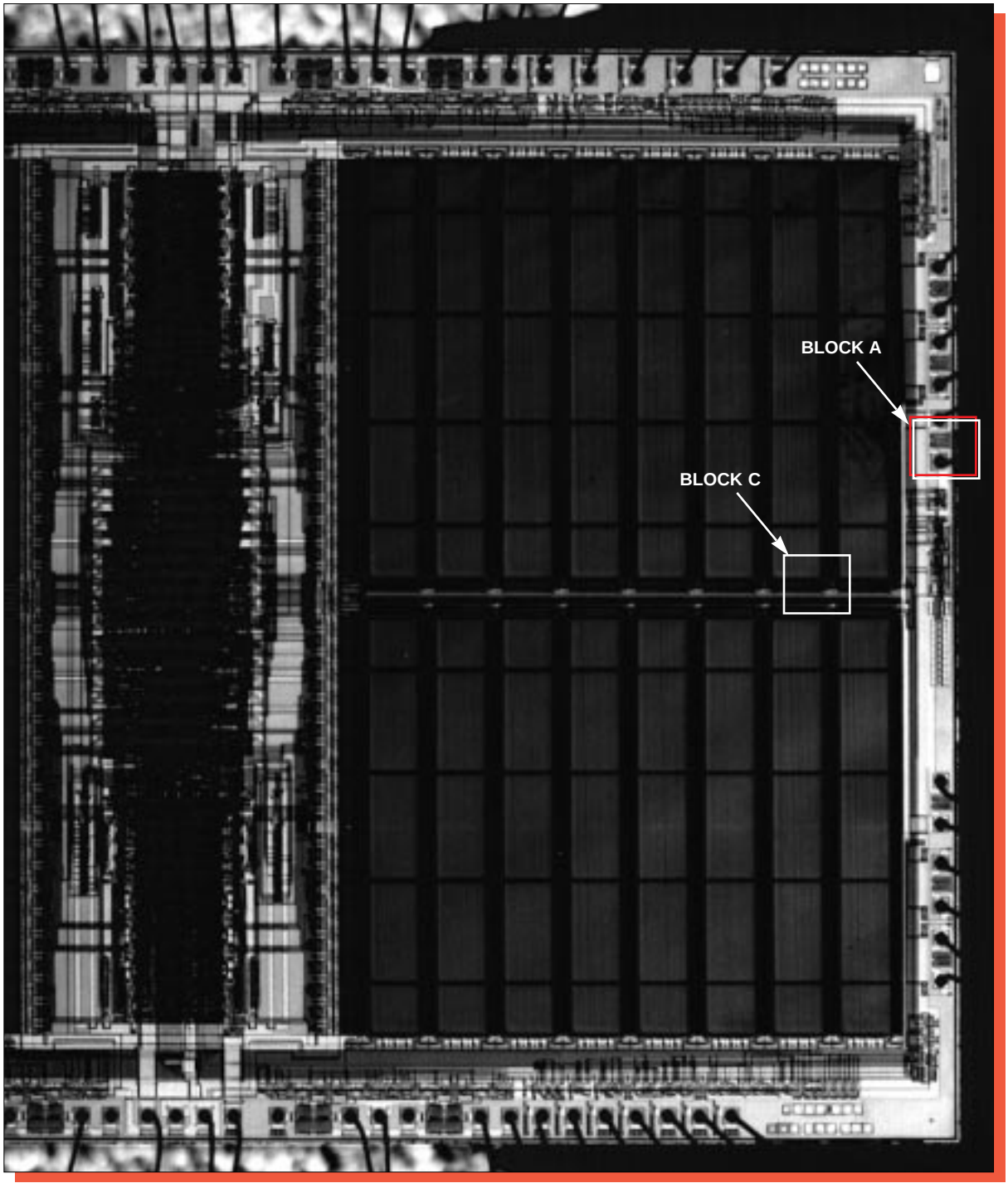
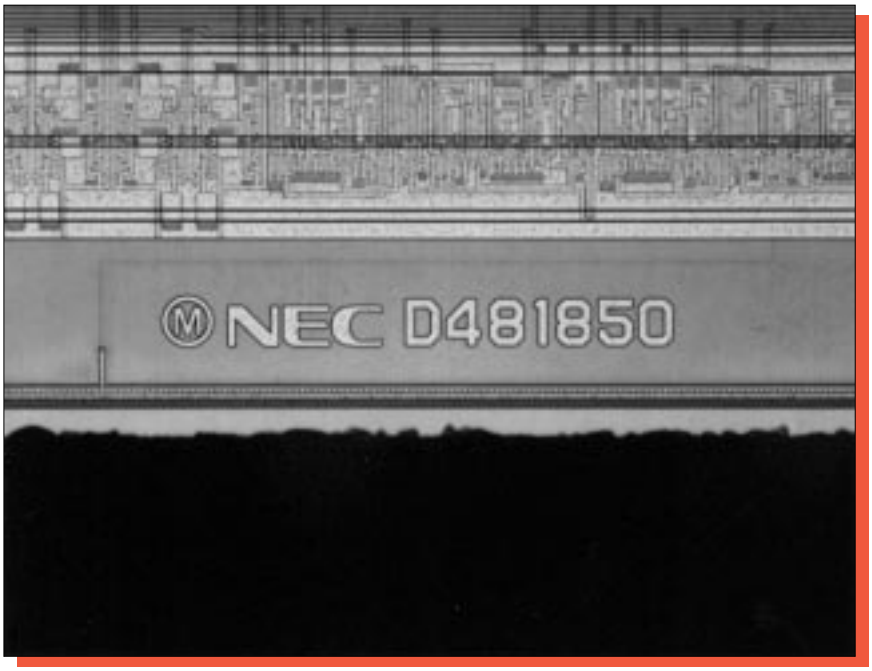


Figure 1a. Remaining portion of the NEC D481850GE-A10 intact die. Mag. 26x.



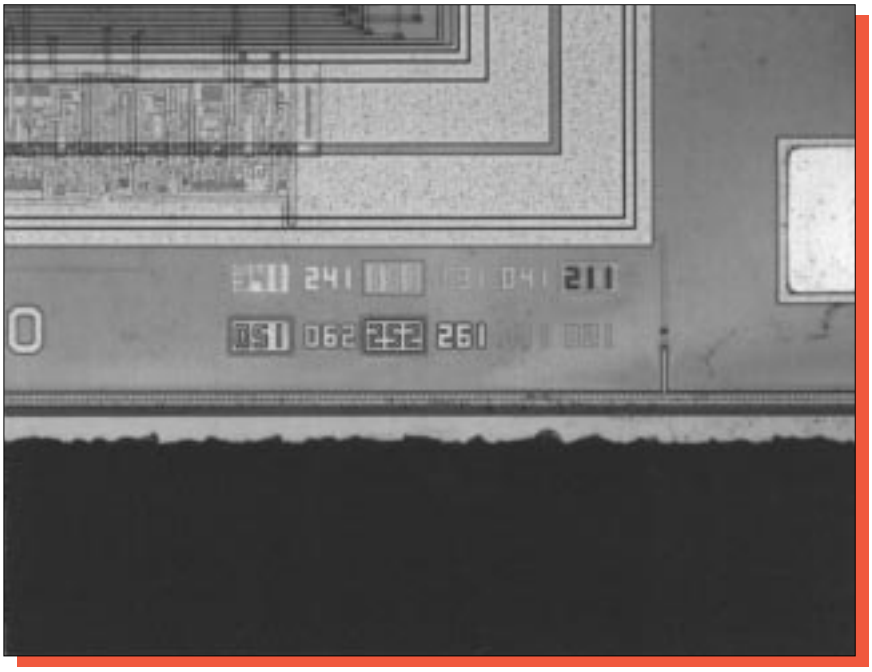


Figure 2. Optical views illustrating die markings. Mag. 200x.

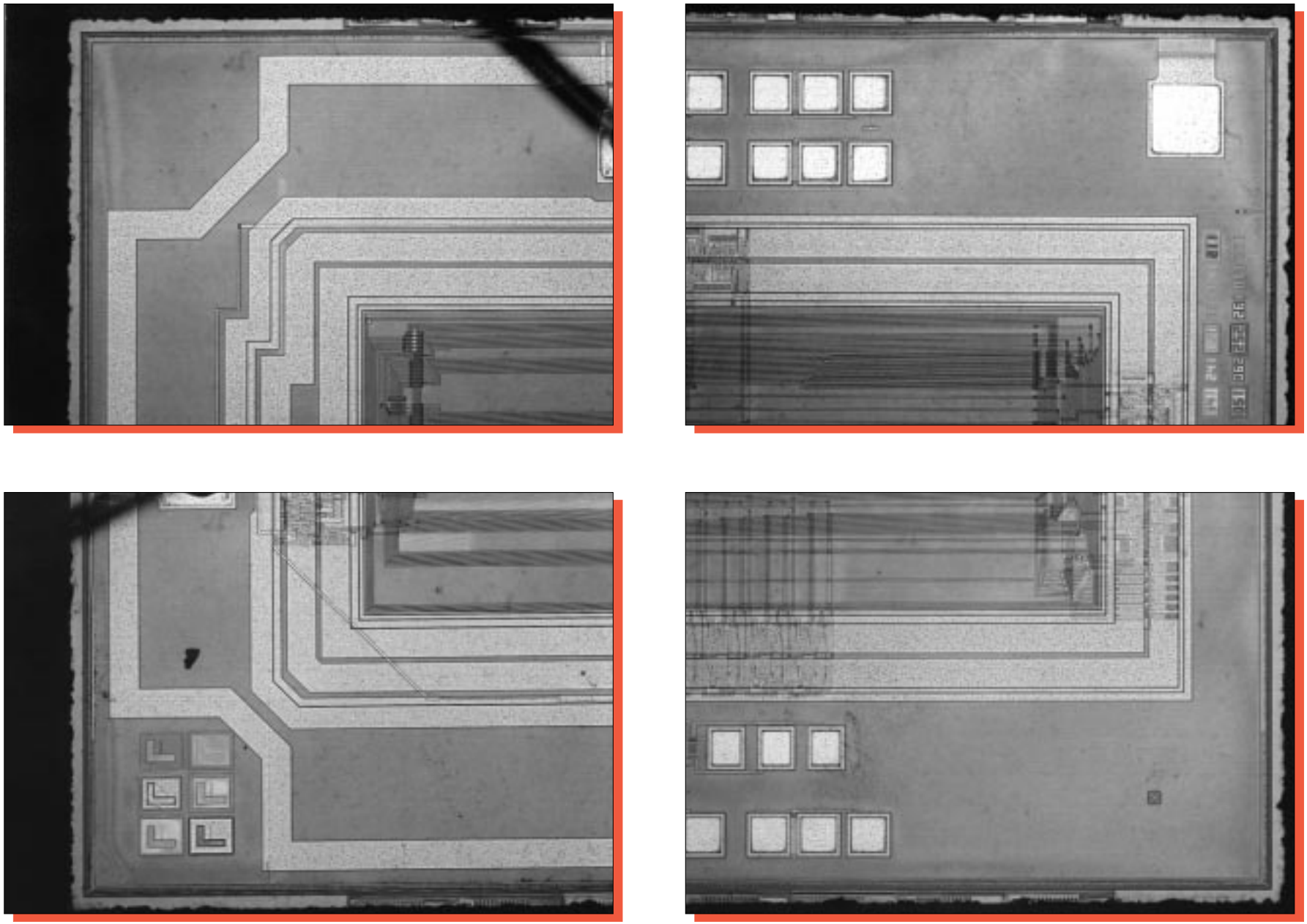
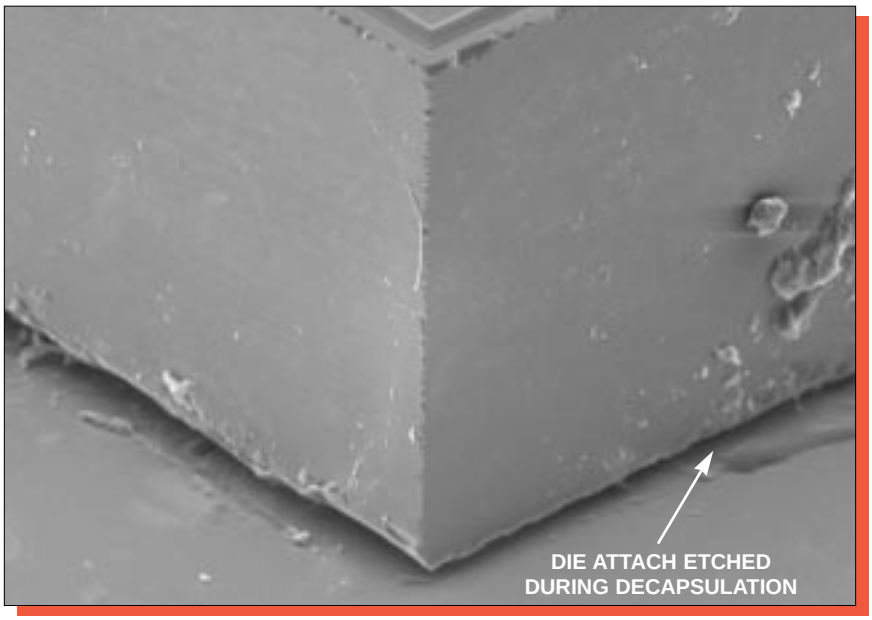
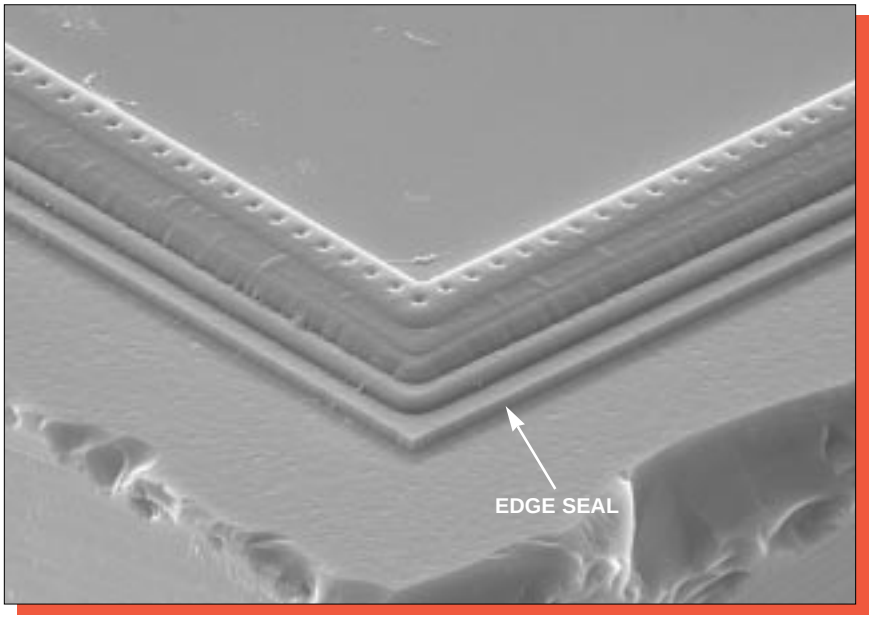


Figure 3. Optical views illustrating die corners. Mag. 130x.

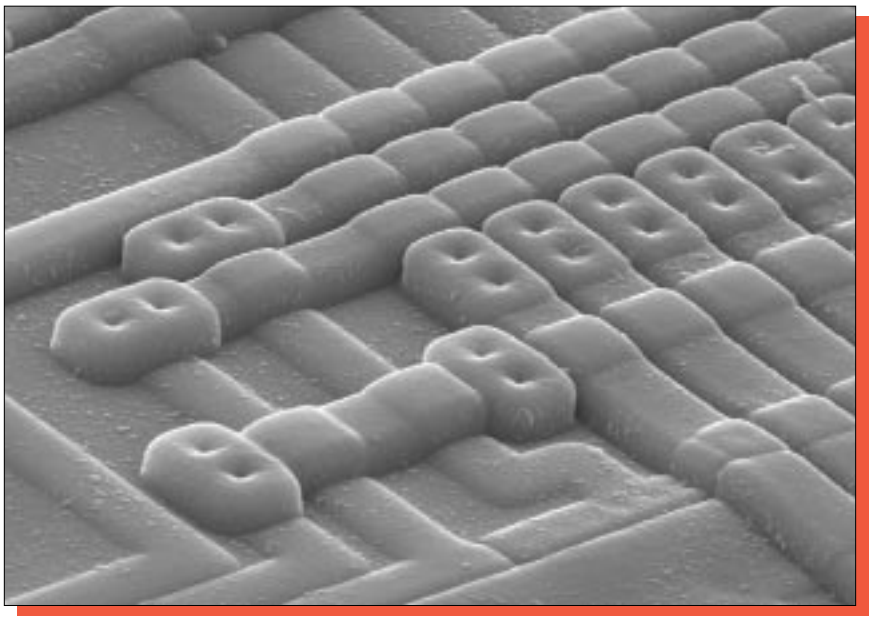


Mag. 200x

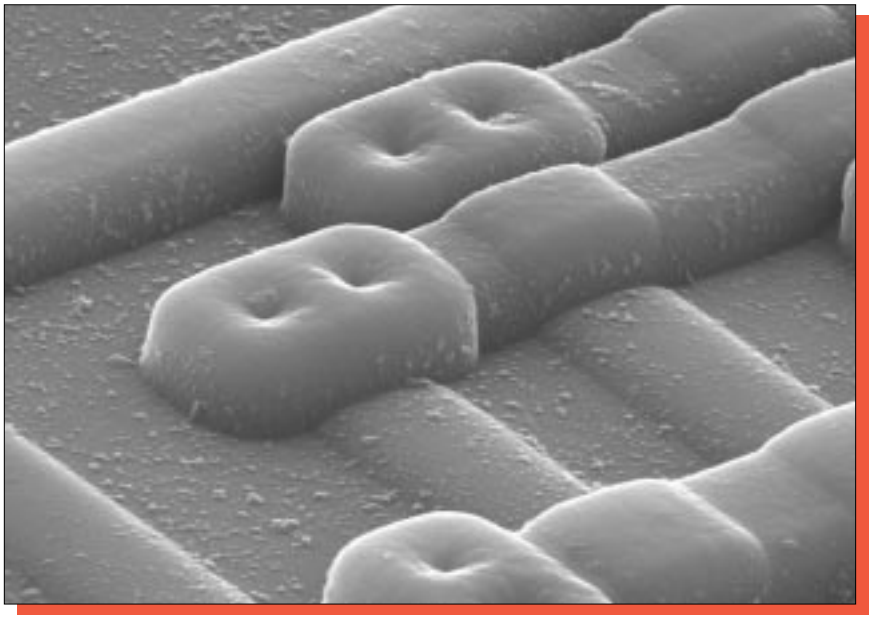


Mag. 1600x

Figure 4. SEM views illustrating die corner and edge seal. 60°.



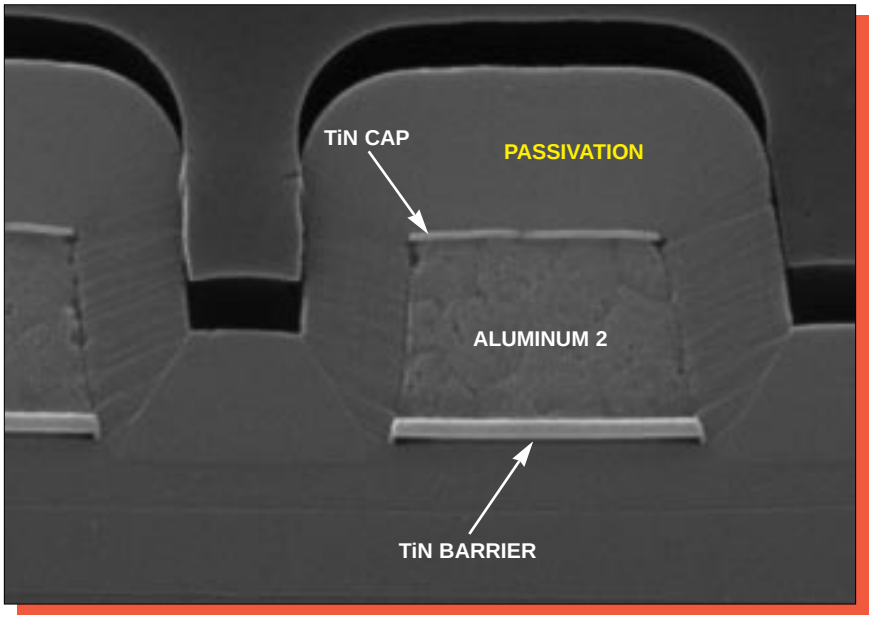
Mag. 4000x



Mag. 8000x

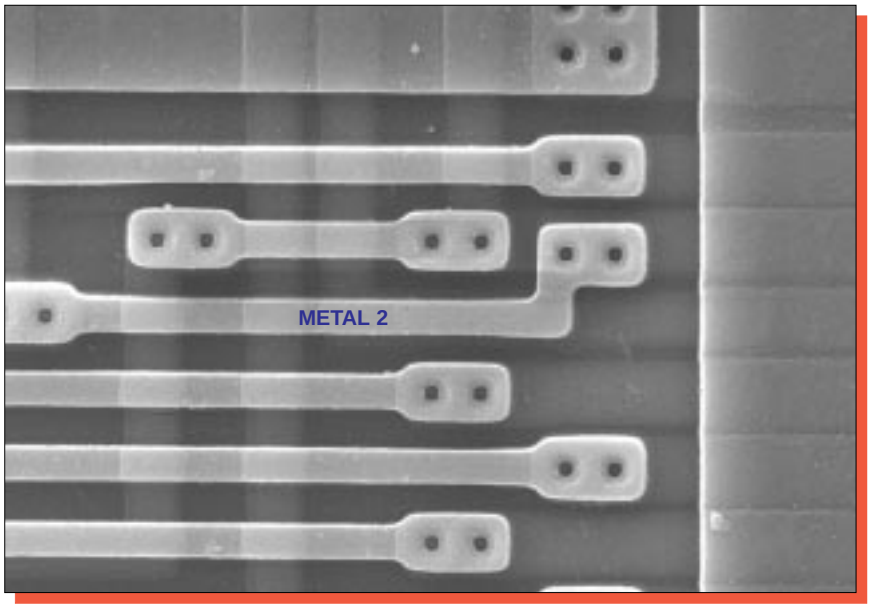
Figure 5. SEM views illustrating passivation coverage. 60°.

Mag. 13,000x

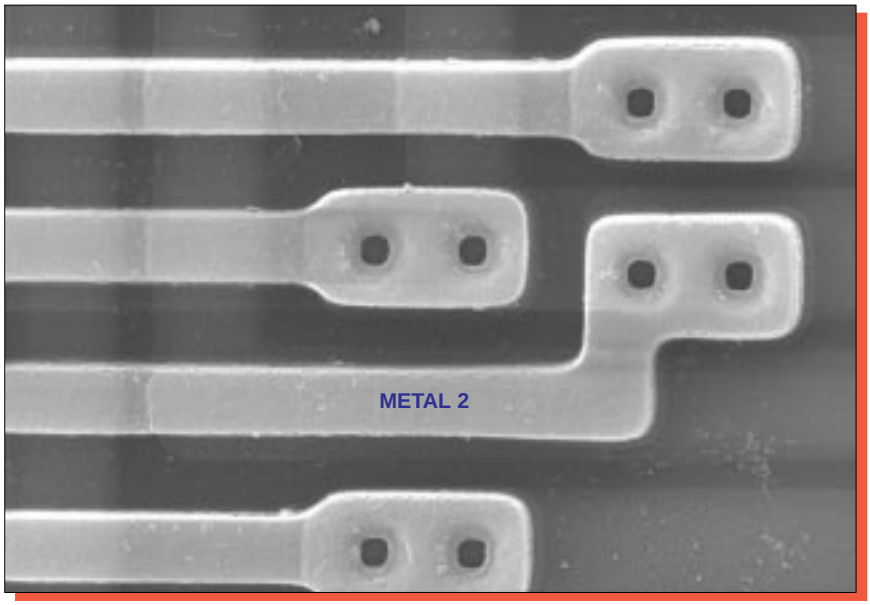


Mag. 26,000x

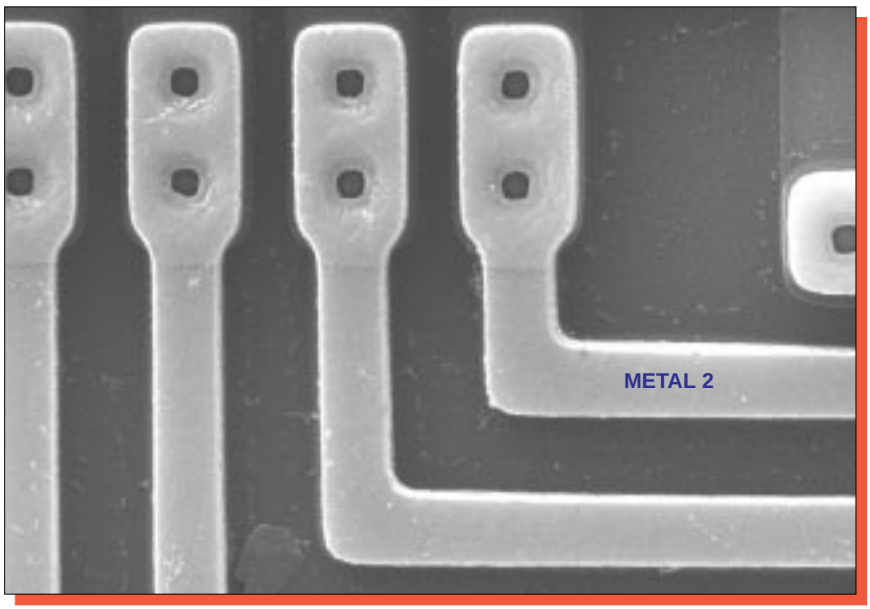
Figure 6. SEM section views illustrating metal 2 line profiles.



Mag. 3250x

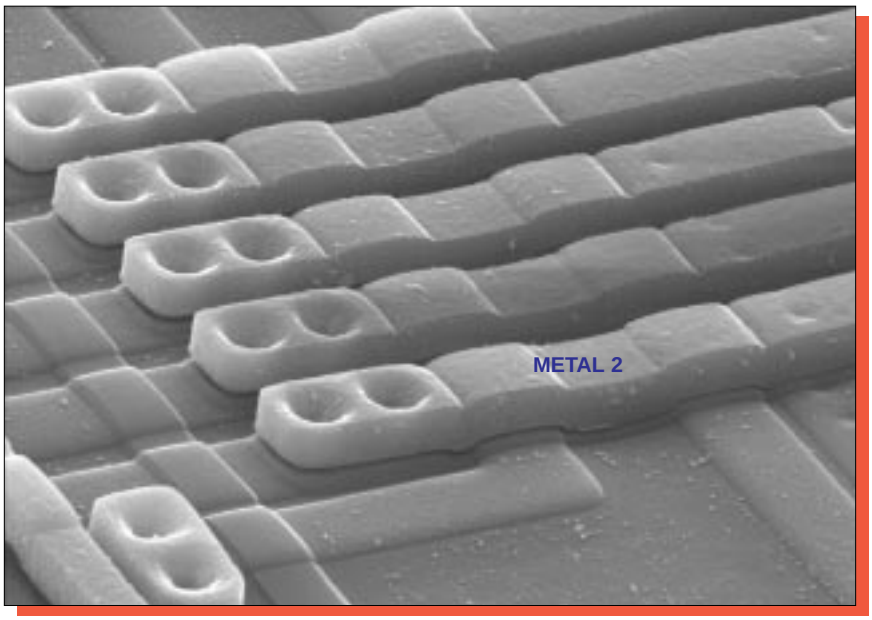


Mag. 6500x

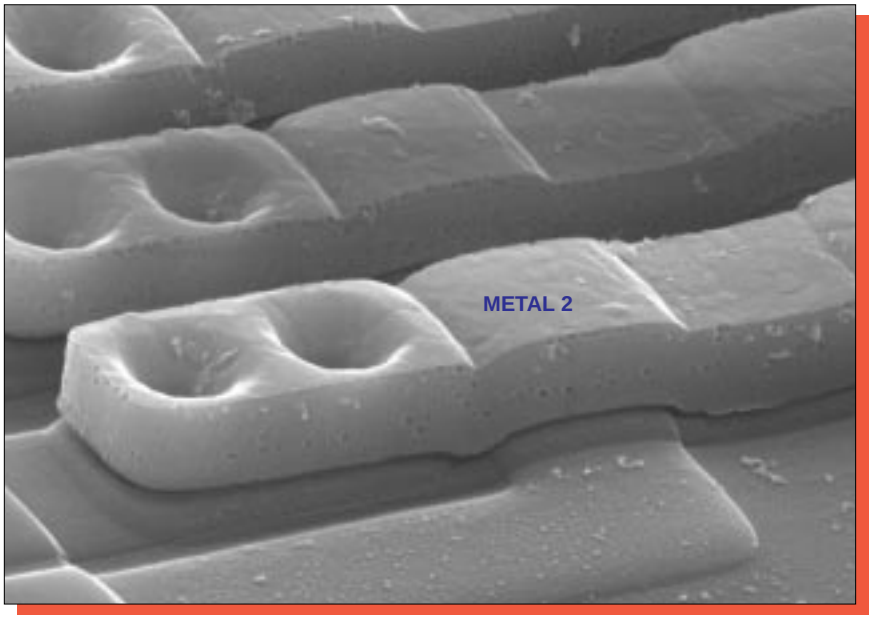


Mag. 6500x

Figure 7. Topological SEM views illustrating metal 2 patterning. 0°.

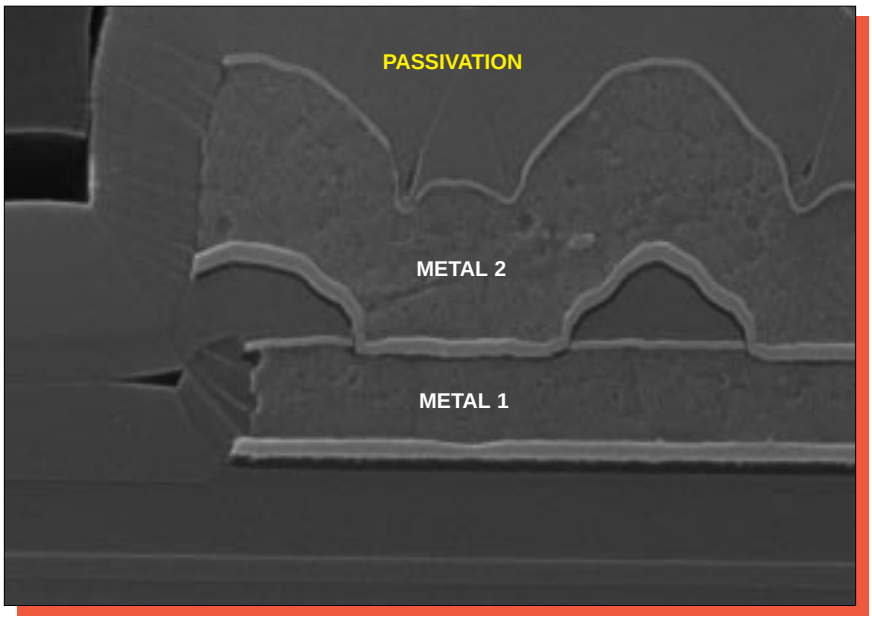


Mag. 6000x

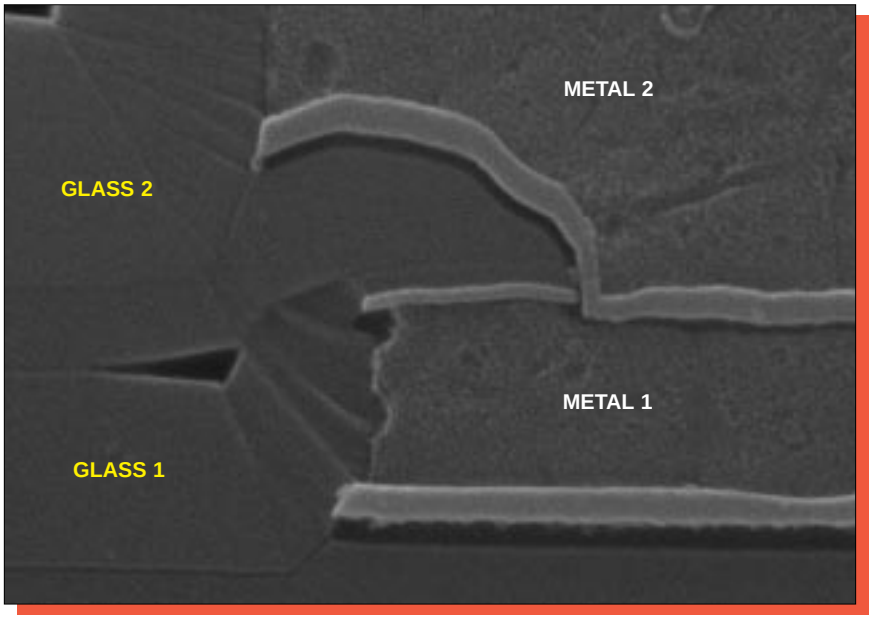


Mag. 12,000x

Figure 8. SEM views illustrating metal 2 step coverage. 60°.

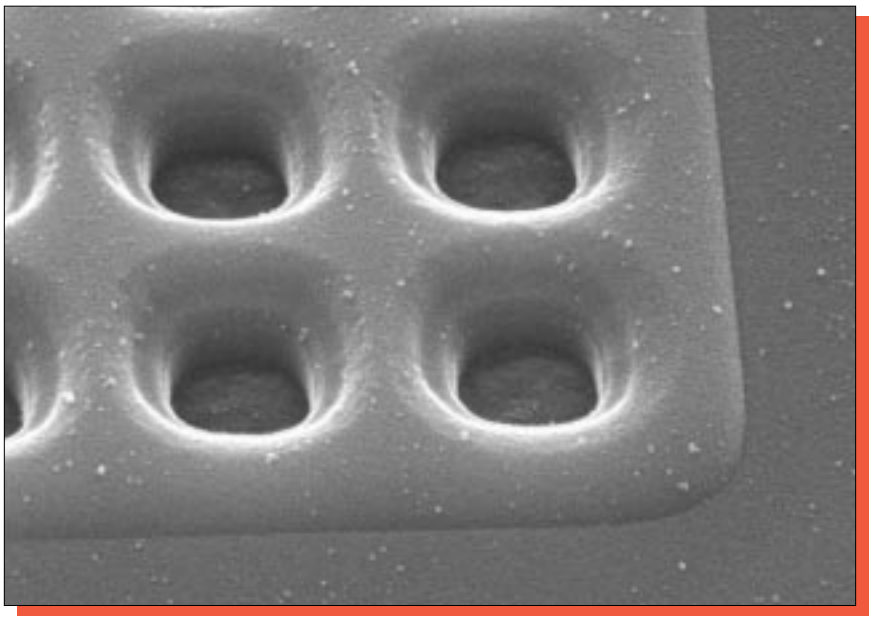


Mag. 26,000x

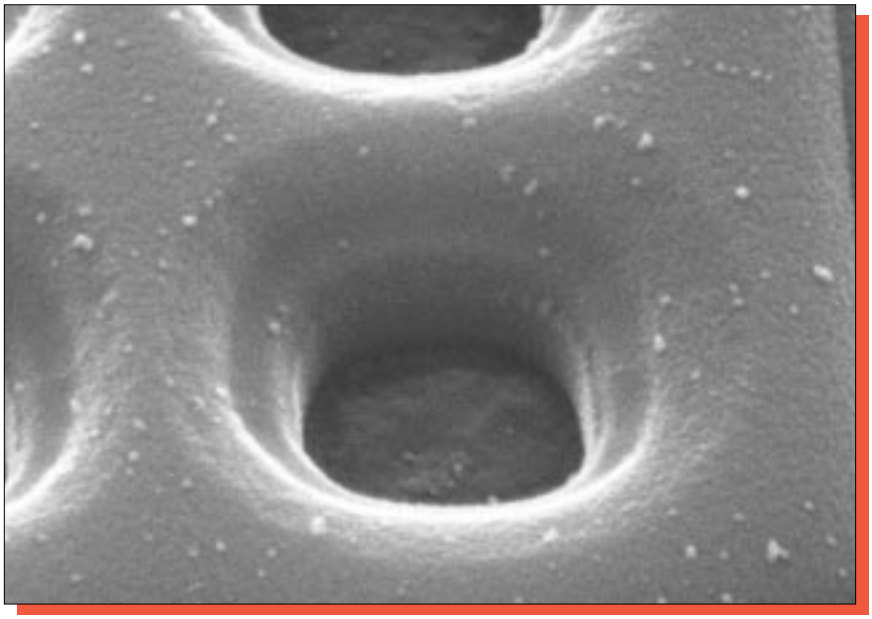


Mag. 52,000x

Figure 9. SEM section views illustrating M2-M1 via and intermetal dielectric.

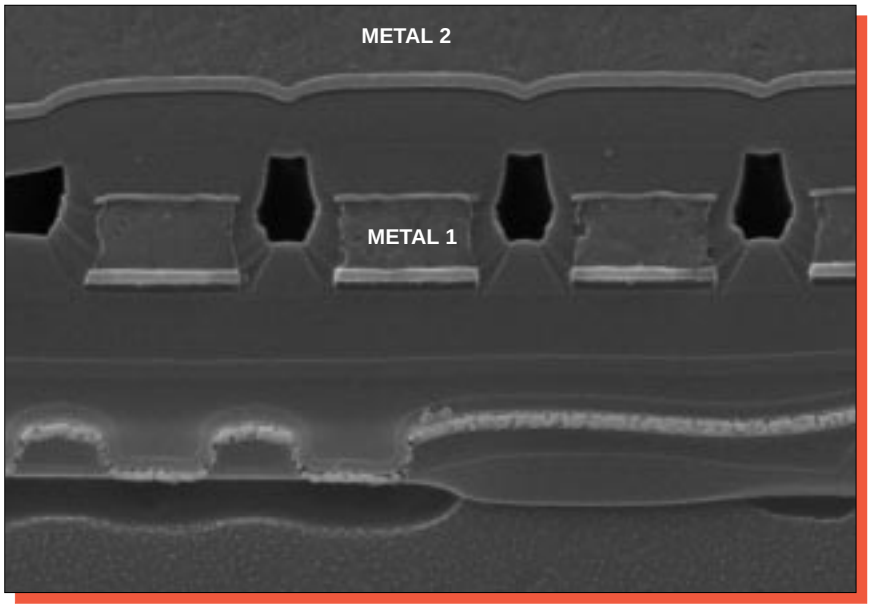


Mag. 20,000x



Mag. 40,000x

Figure 9a. SEM views illustrating metal 2 barrier. 45°.



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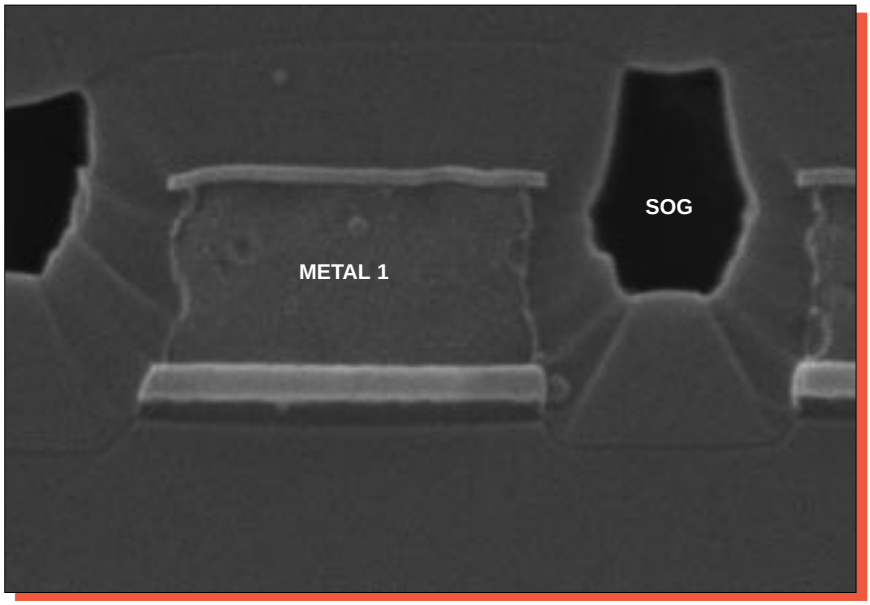

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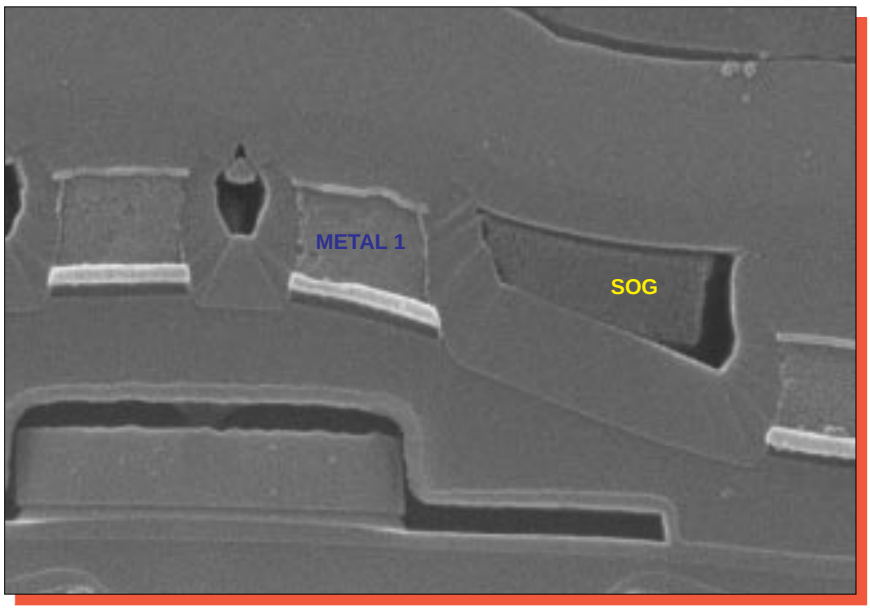
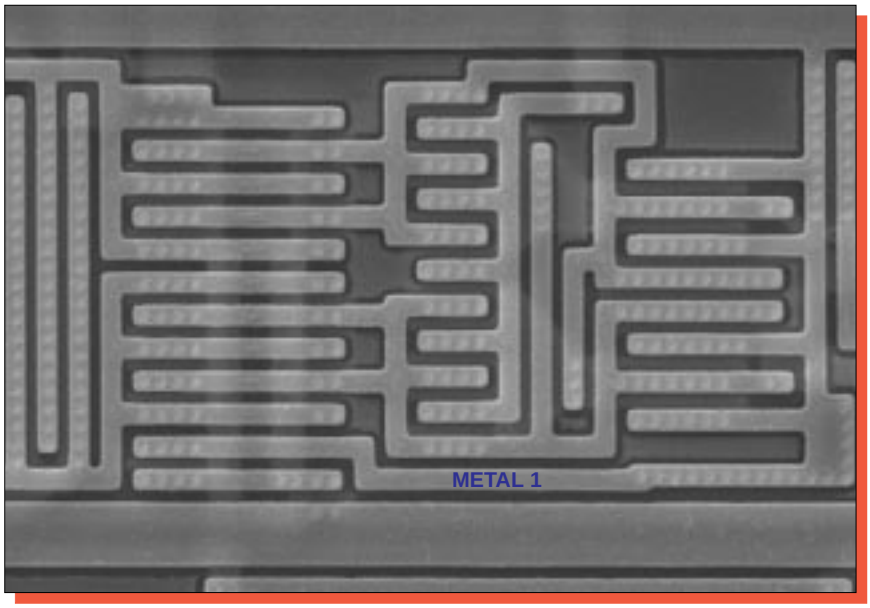
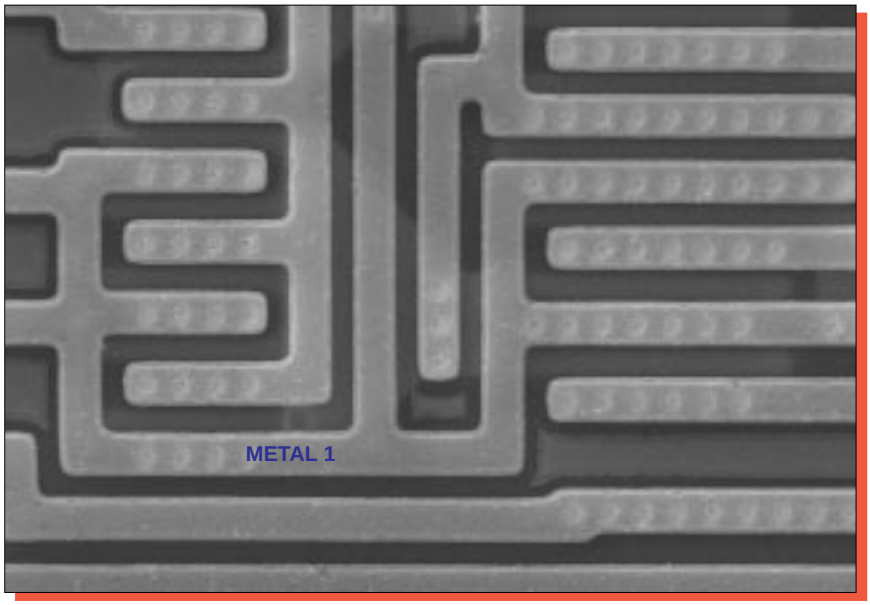


Mag. 26,000x

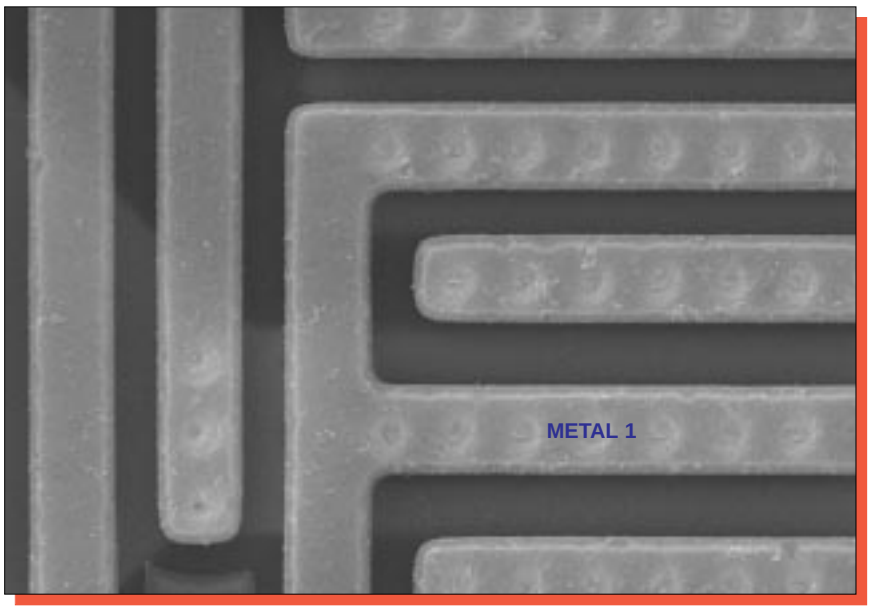
Figure 10. SEM section views illustrating metal 1 line profiles.



Mag. 1600x

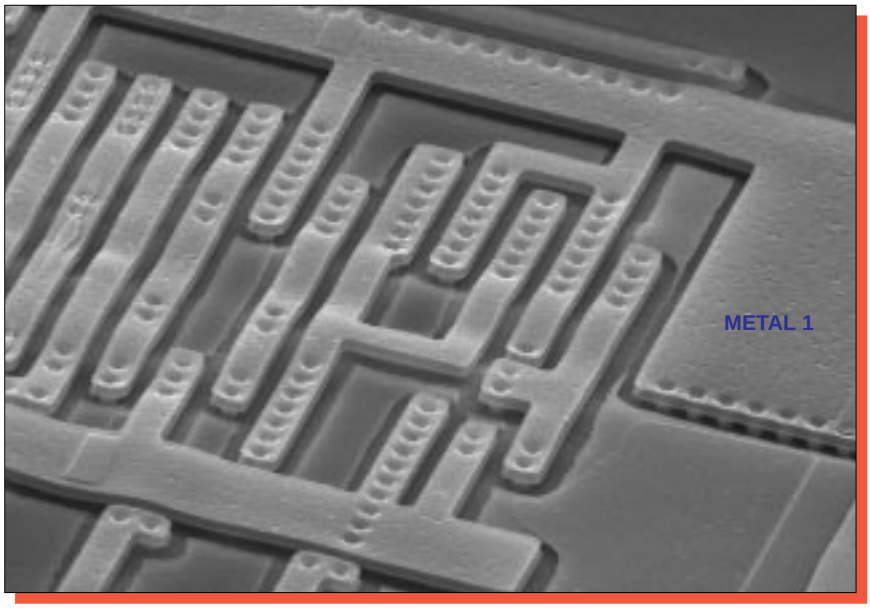


Mag. 3250x



Mag. 6500x

Figure 11. Topological views illustrating metal 1 patterning. 0°.



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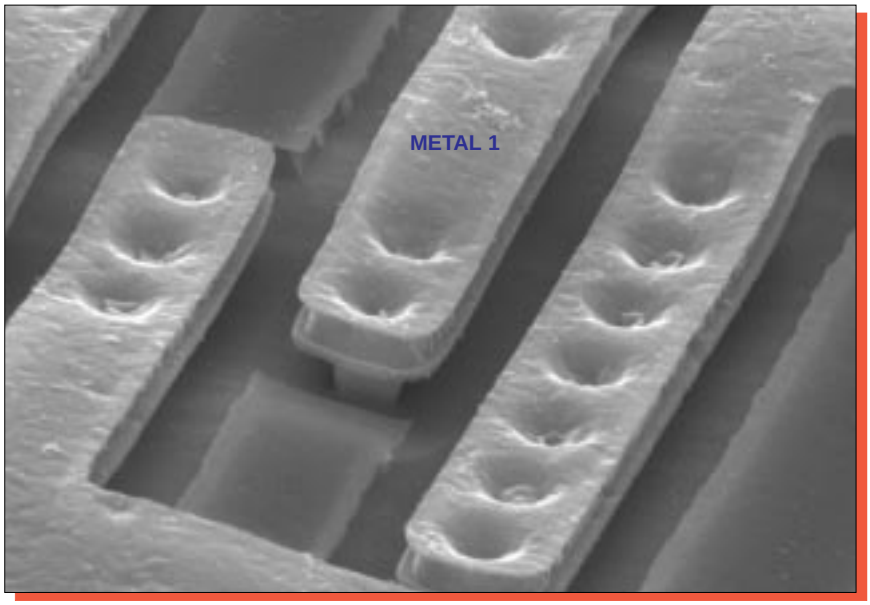
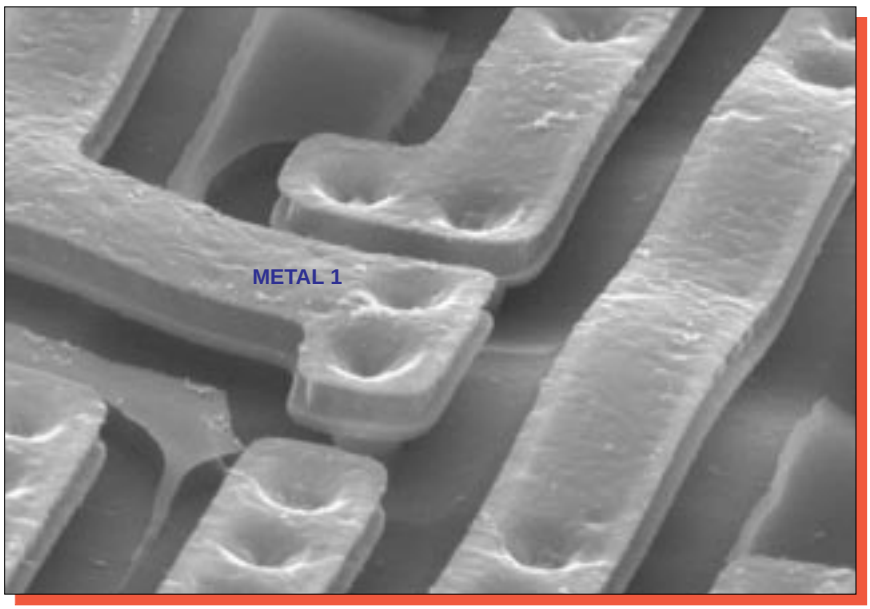
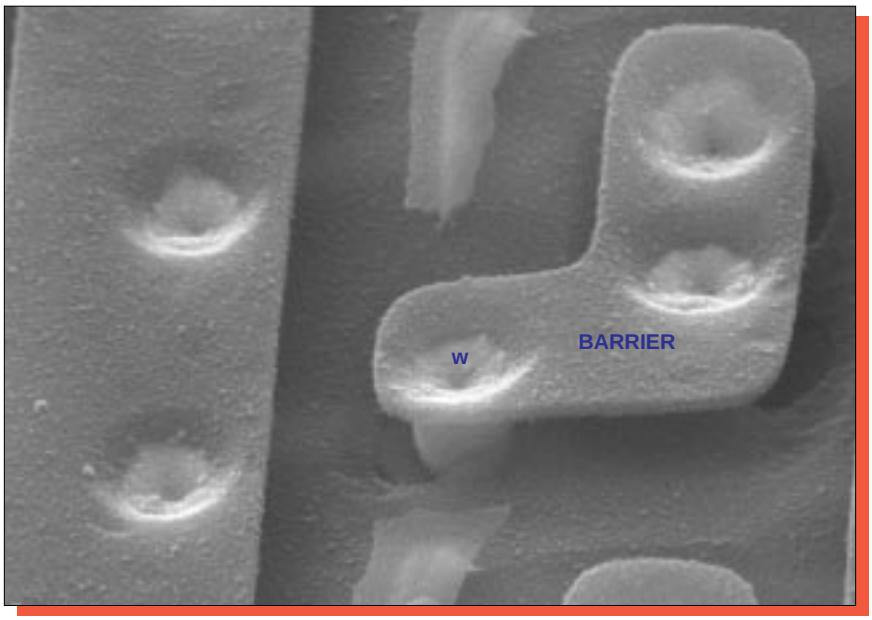


Mag. 12,000x

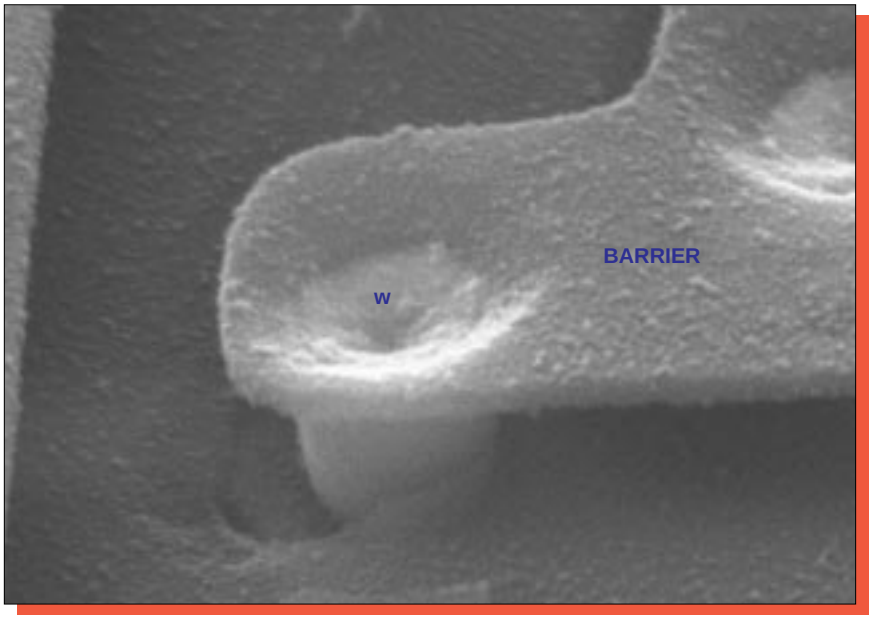


Mag. 12,000x

Figure 12. SEM views illustrating metal 1 step coverage. 60°.

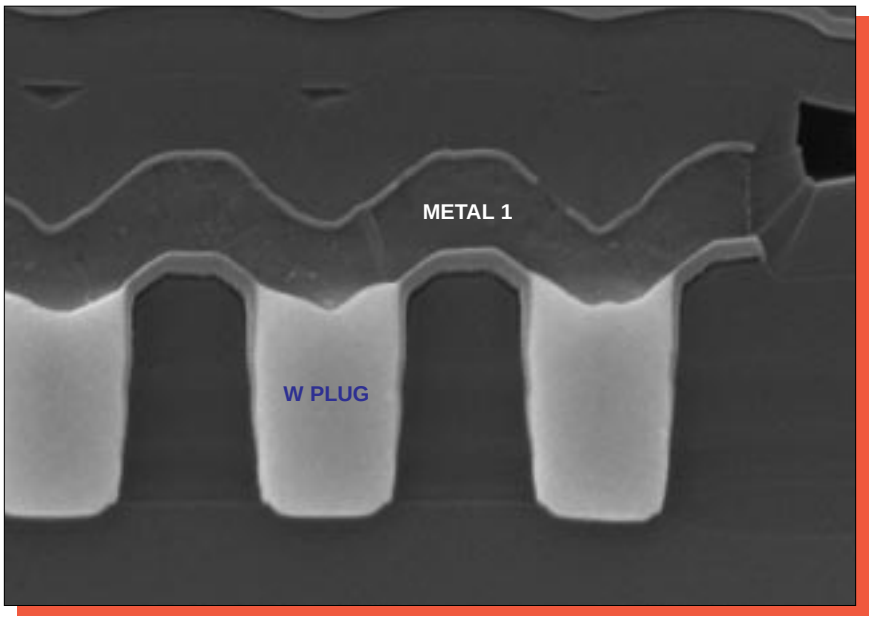


Mag. 20,000x



Mag. 40,000x

Figure 12a. SEM views illustrating metal 1 barrier. 45°.



glass etch

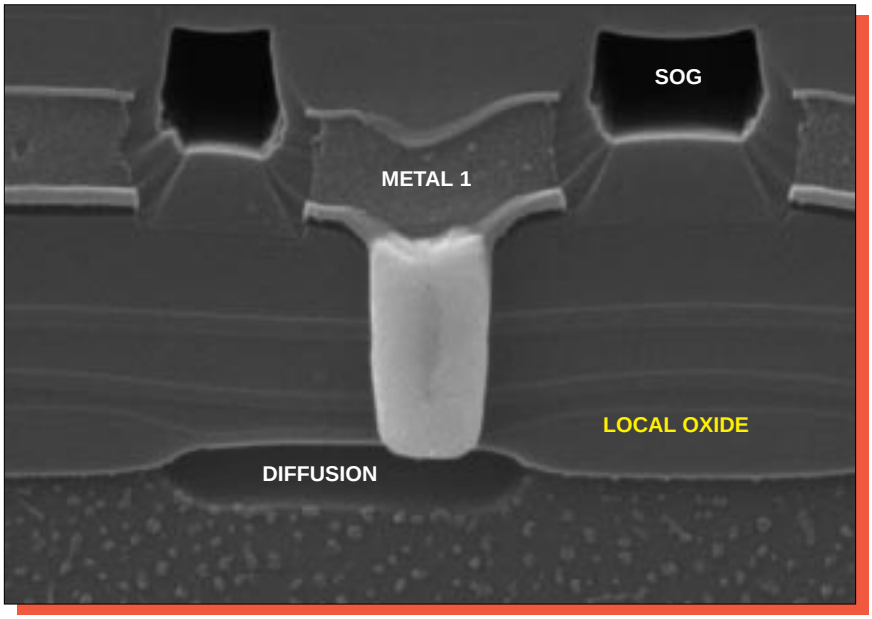
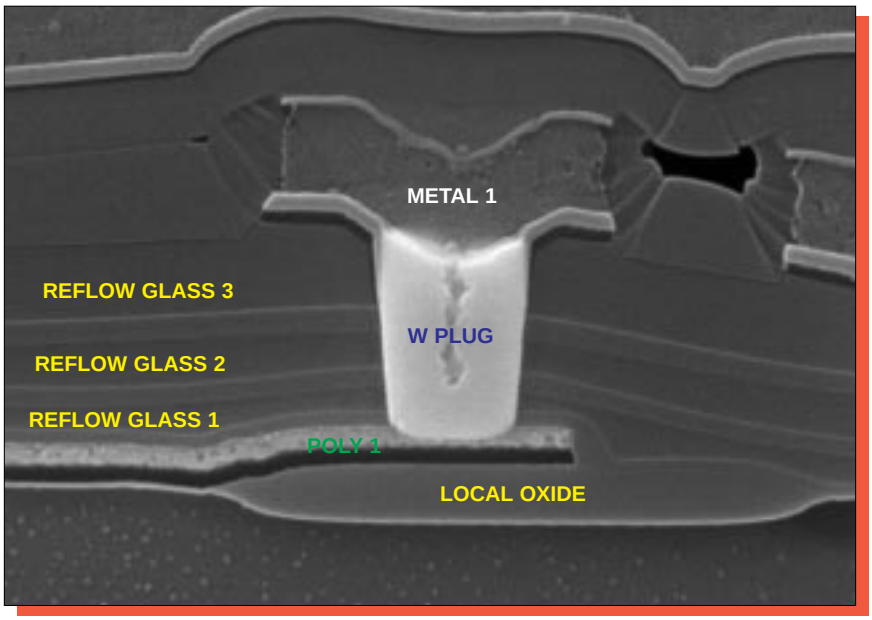
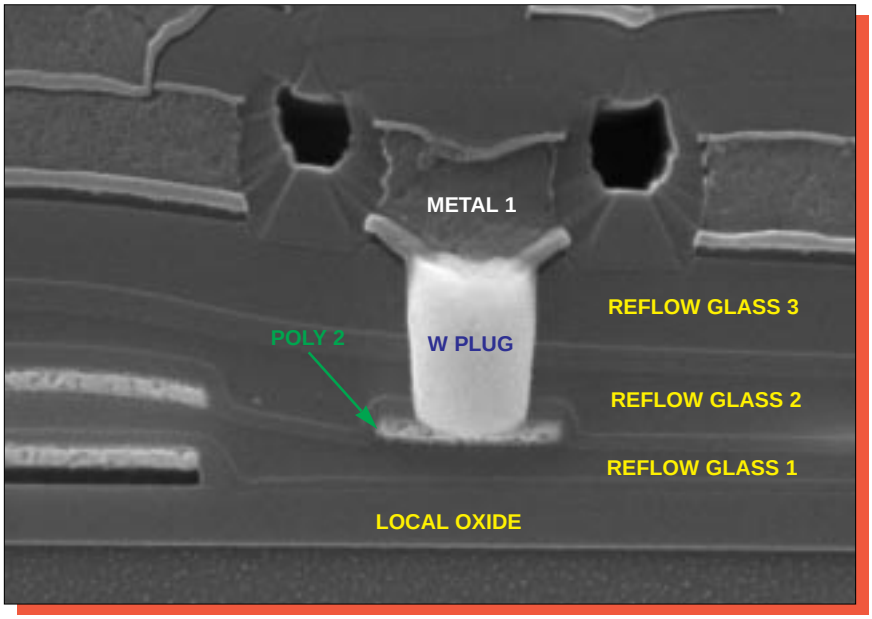


Figure 13. SEM section views illustrating typical metal 1 contacts. Mag. 26,000x.

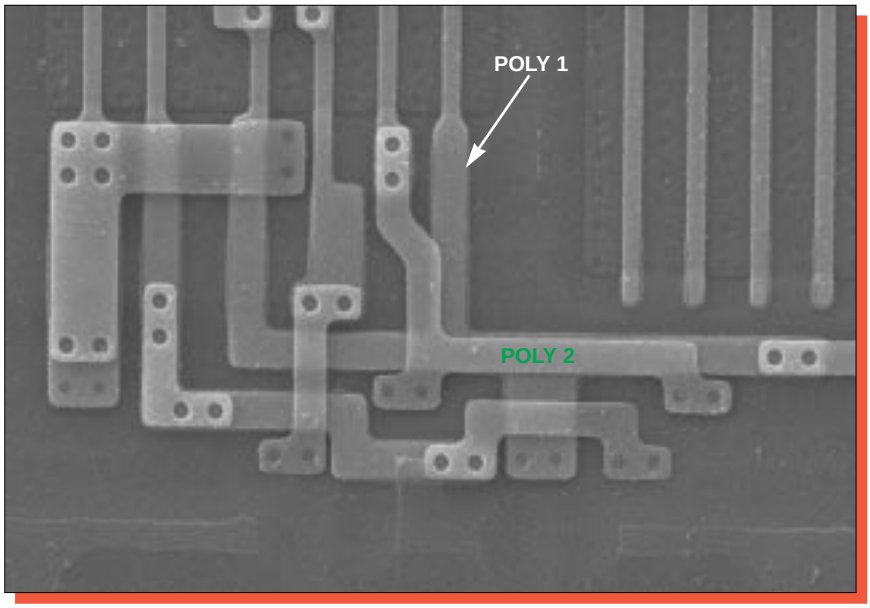


metal 1-to-poly 1

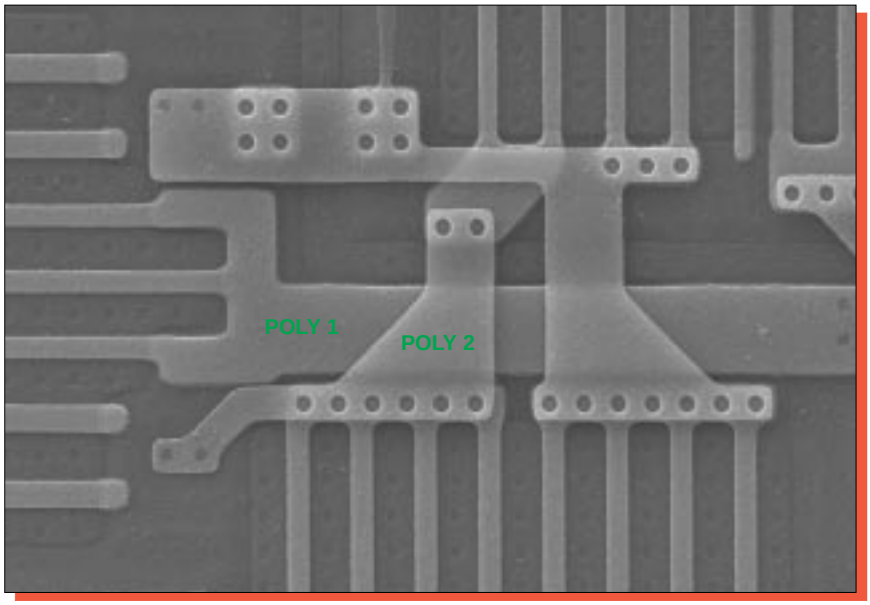


metal 1-to-poly 2

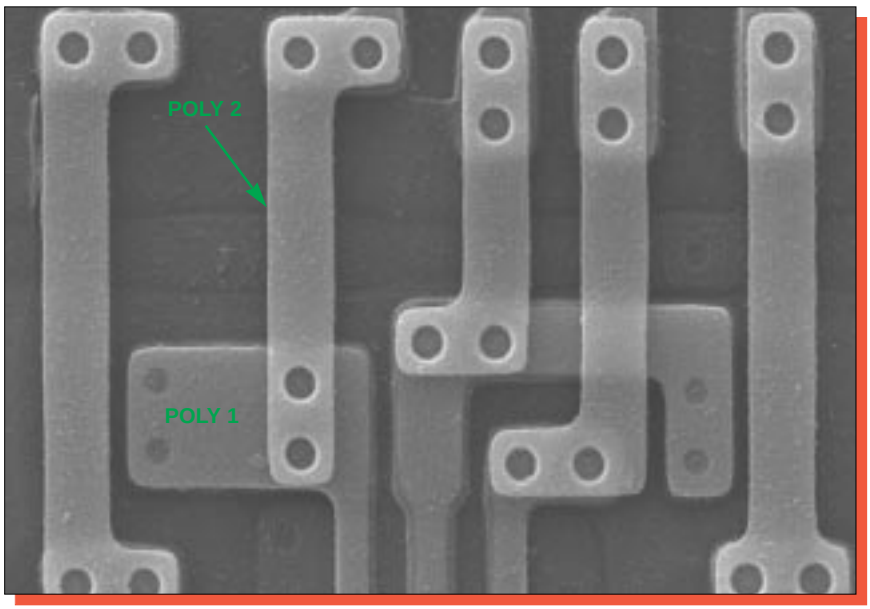
Figure 13a. SEM section views illustrating metal 1 contacts. Mag. 26,000x.



Mag. 3250x

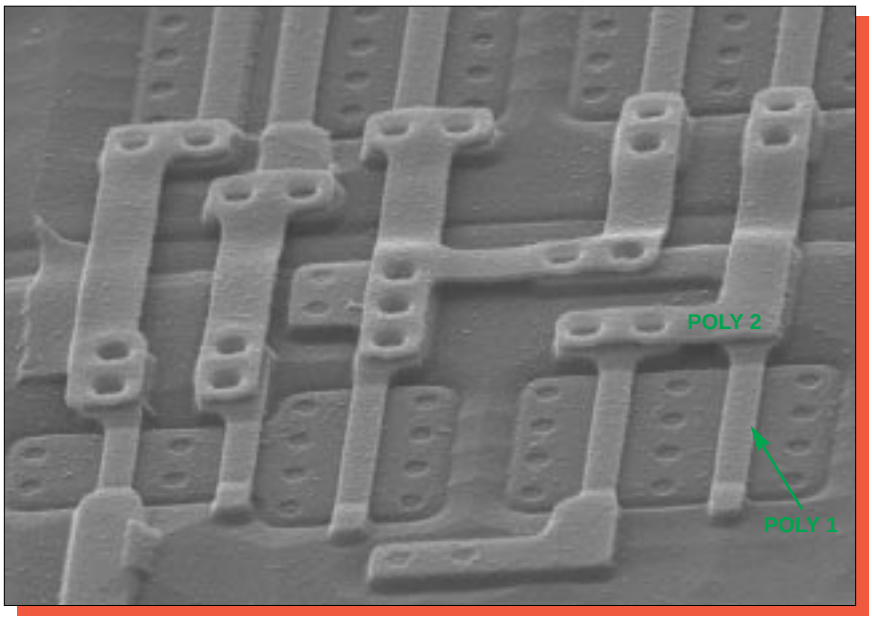


Mag. 3250x

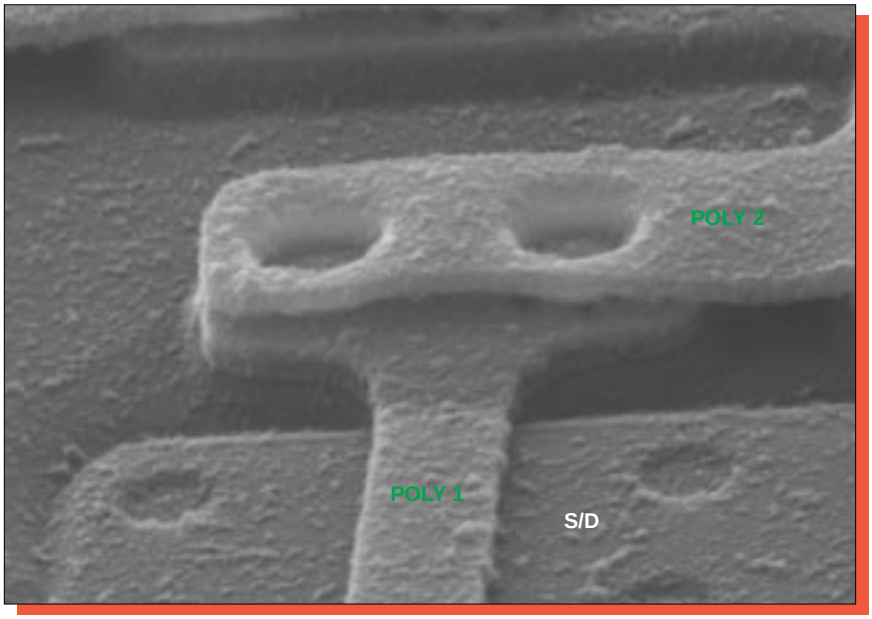


Mag. 6500x

Figure 14. Topological SEM views illustrating poly patterning. 0°.

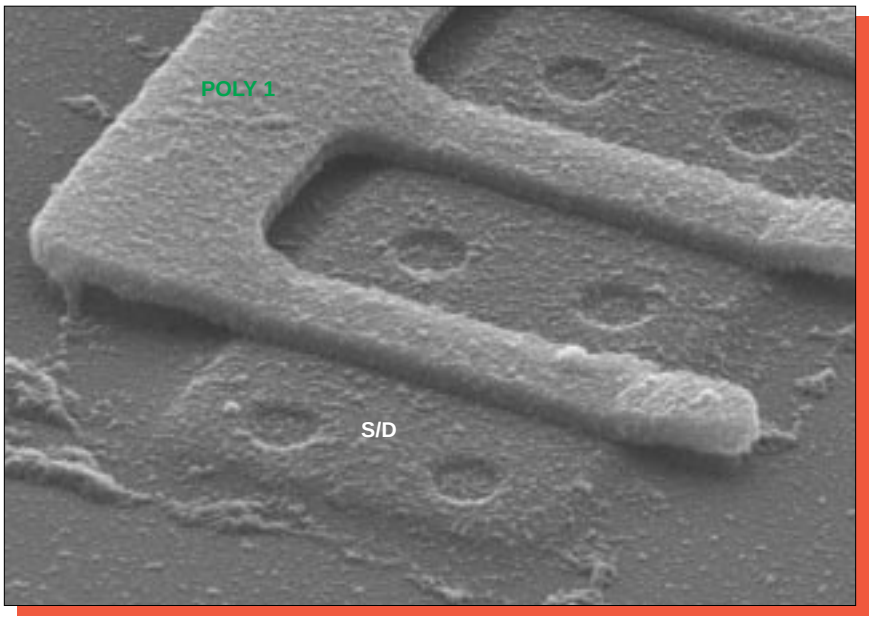


Mag. 6000x

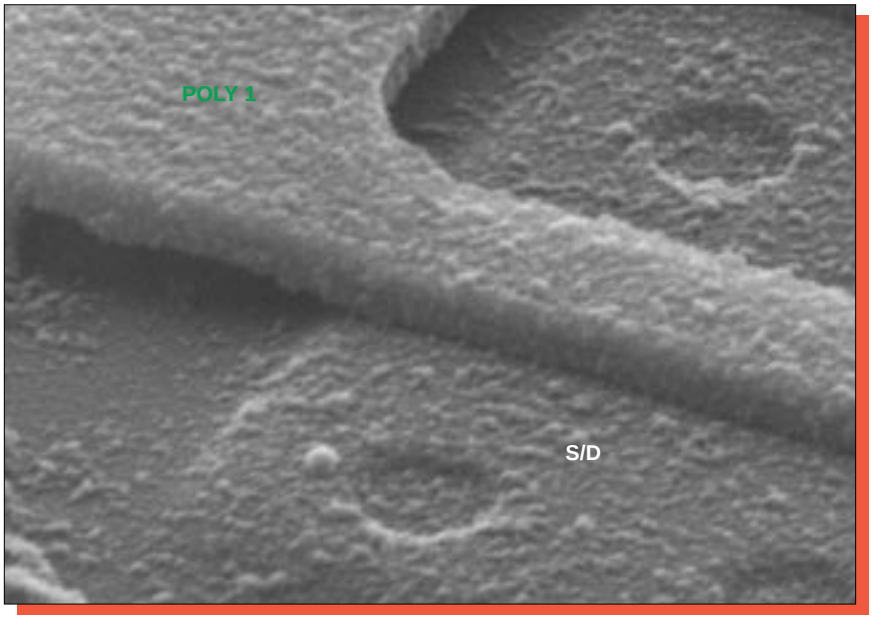


Mag. 24,000x

Figure 15. SEM views illustrating poly step coverage. 60°.

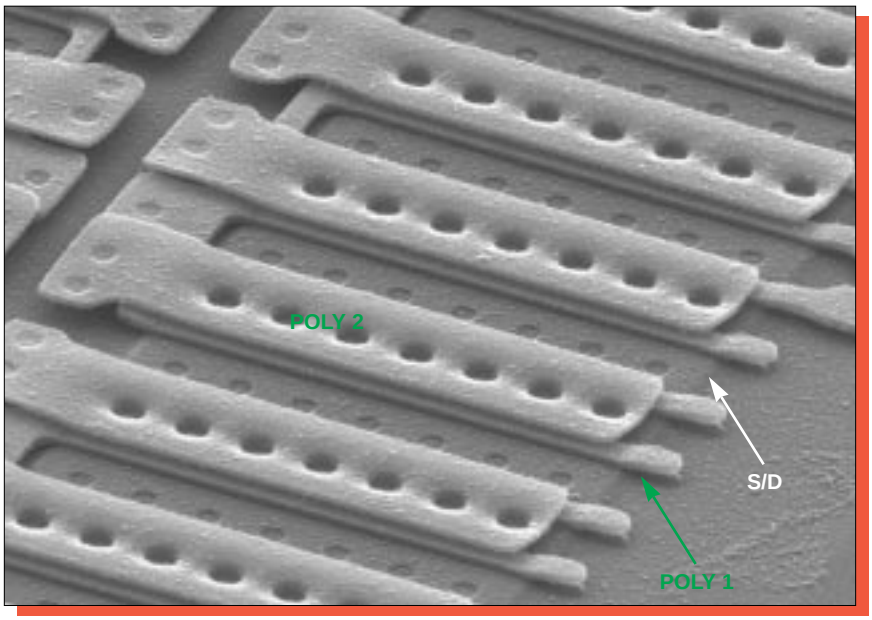


Mag. 20,000x

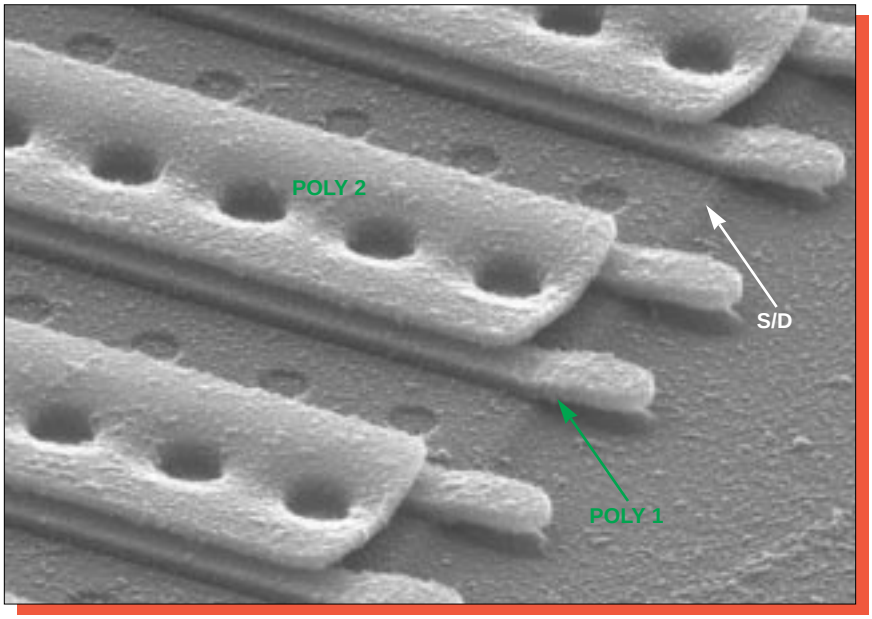


Mag. 40,000x

Figure 15a. Additional SEM views illustrating poly 1 step coverage. 60°.

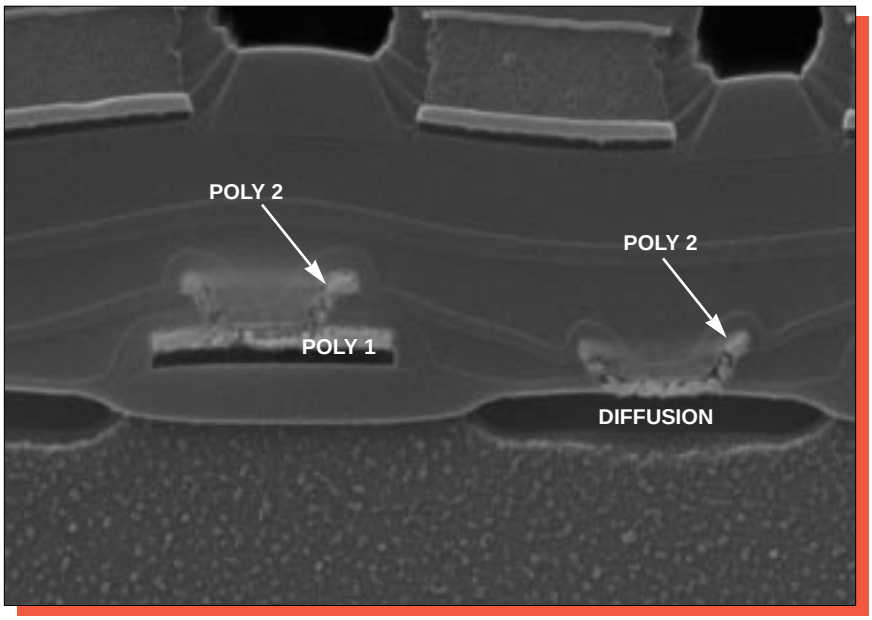


Mag. 7000x

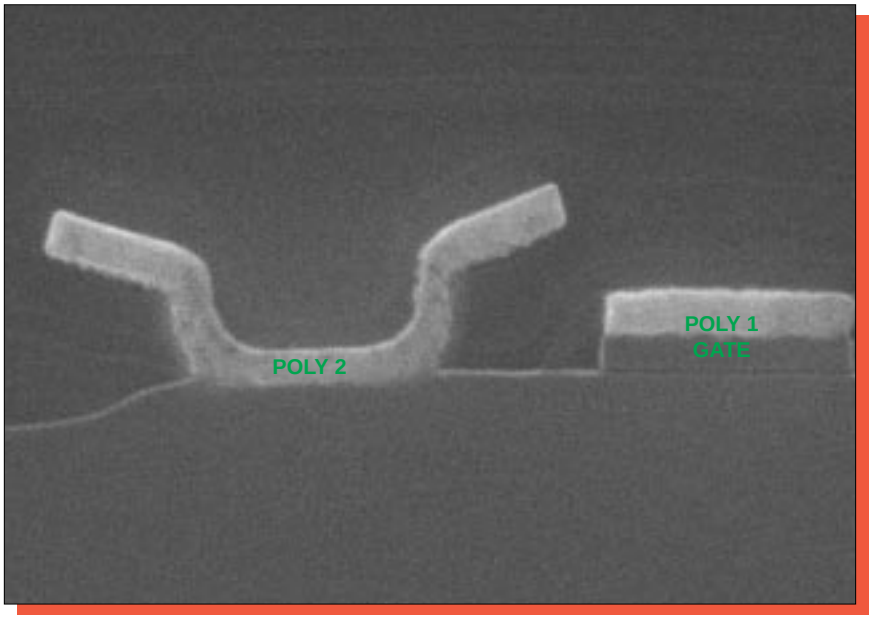


Mag. 14,000x

Figure 15b. Additional SEM views illustrating poly step coverage. 60°.

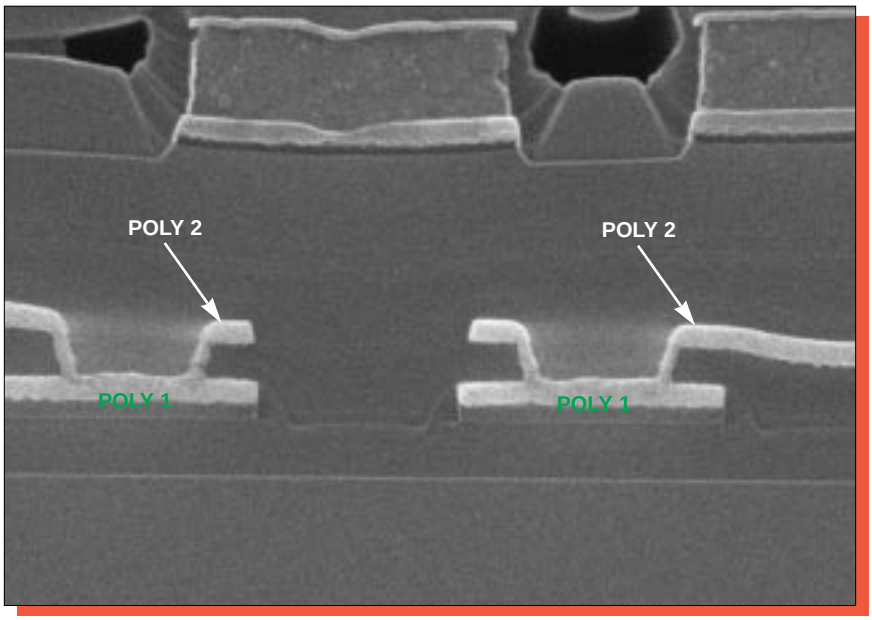


Mag. 26,000x

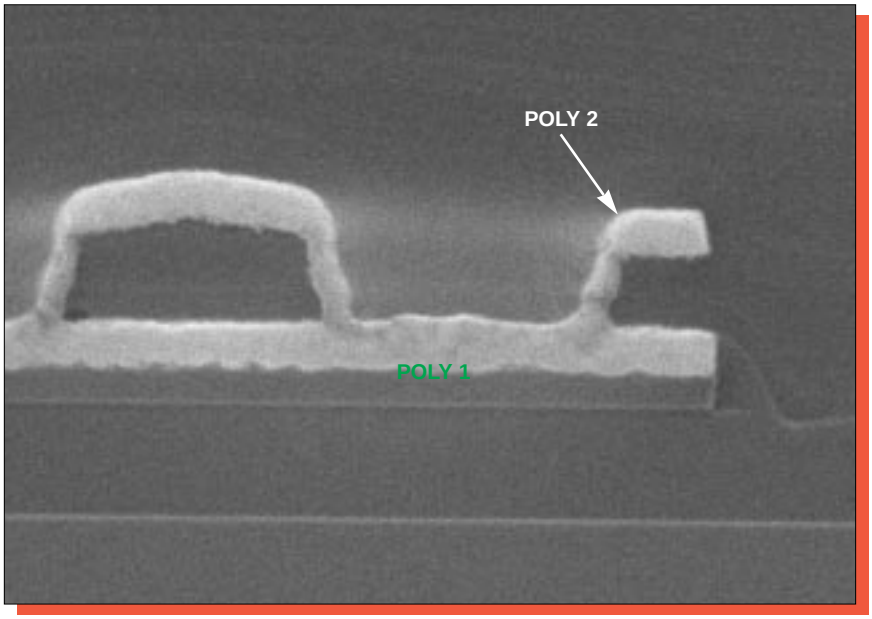


glass etch, Mag. 52,000x

Figure 16. SEM section views illustrating poly 2 contacts.

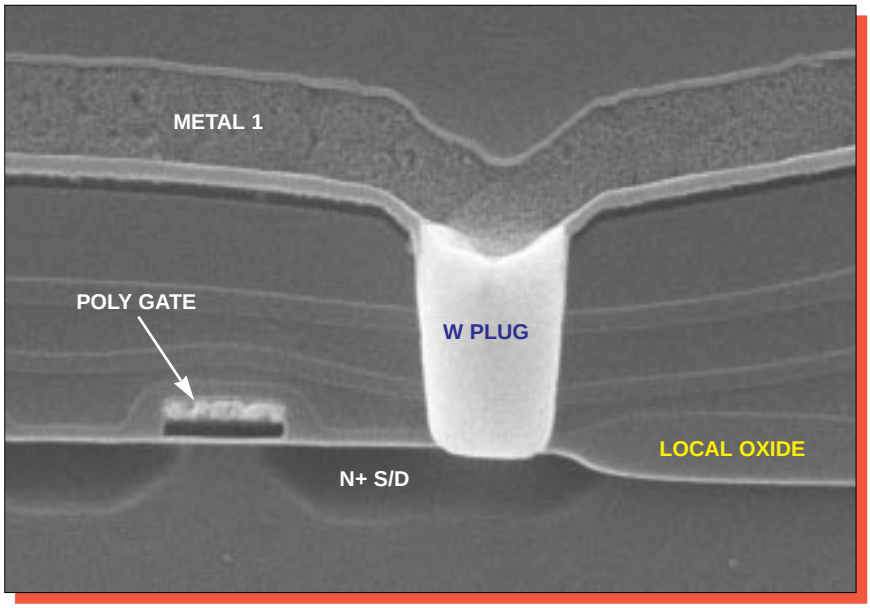


Mag. 26,000x

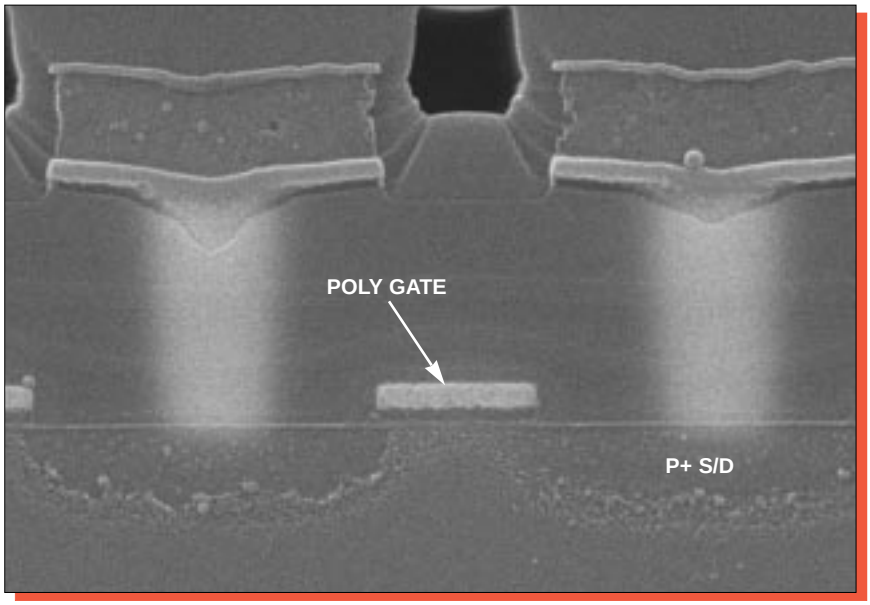


Mag. 52,000x

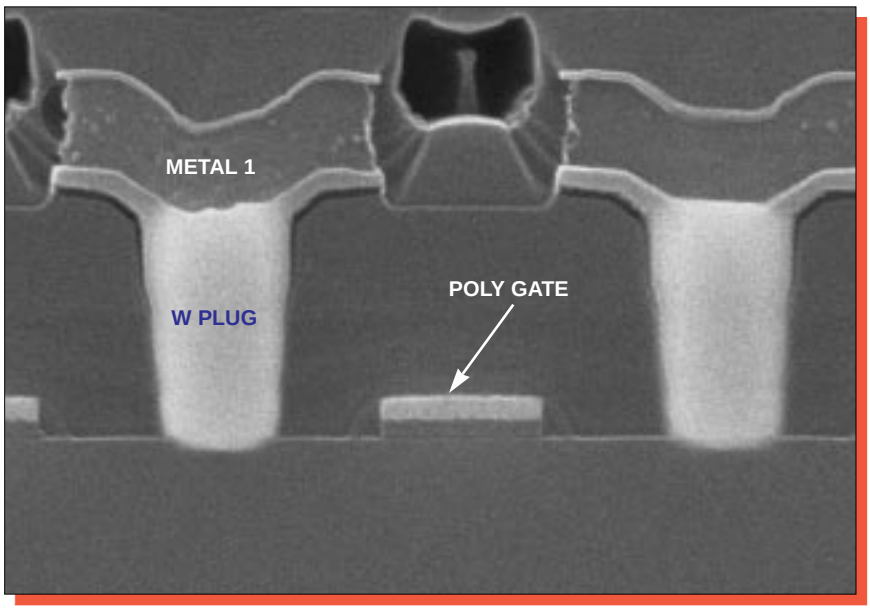
Figure 16a. Additional SEM section views illustrating poly 2 contacts. Glass etch.



N-channel

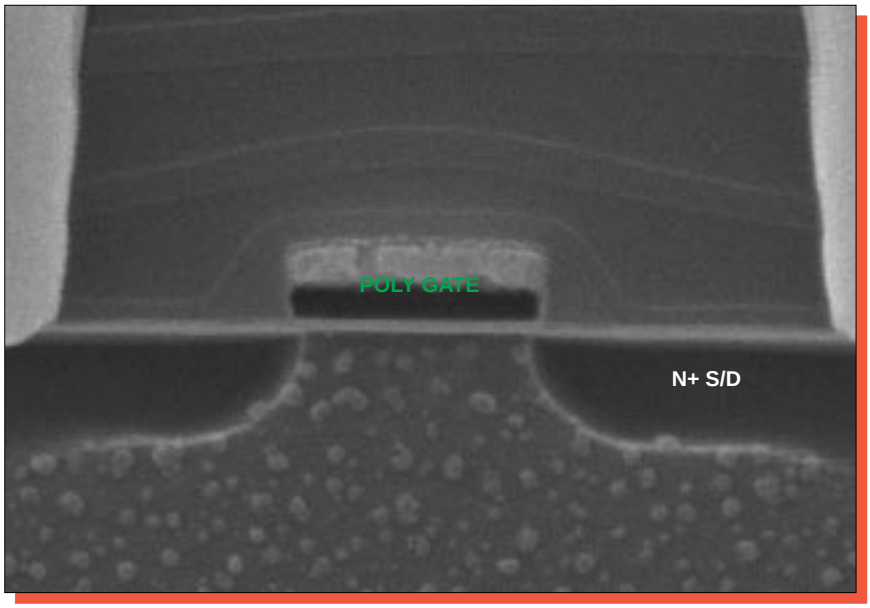


P-channel

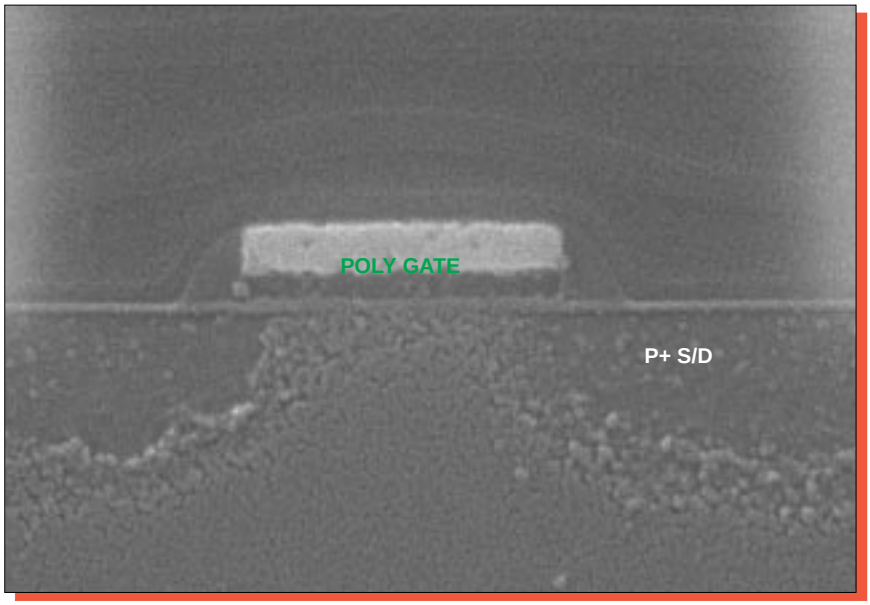


glass etch

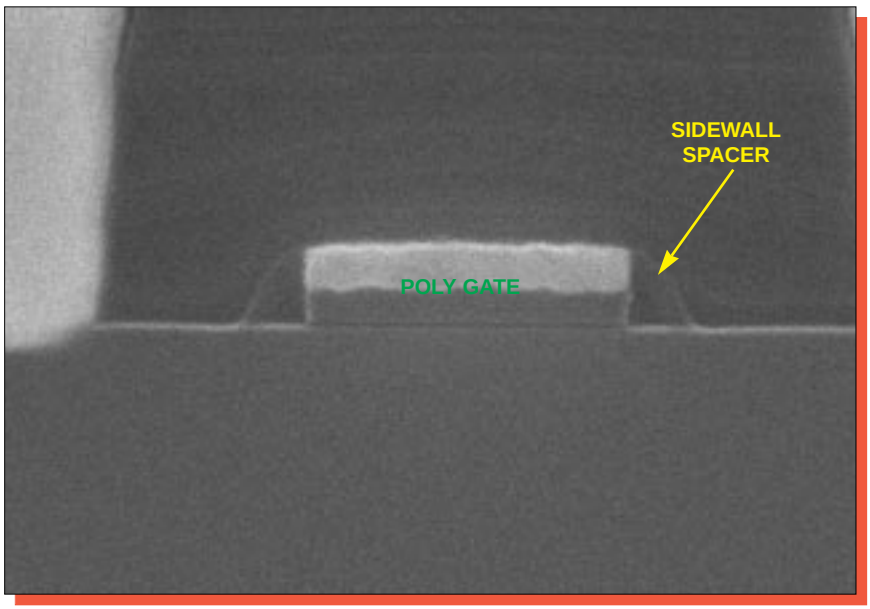
Figure 17. SEM section views illustrating typical gate structures. Mag. 26,000x.



N-channel

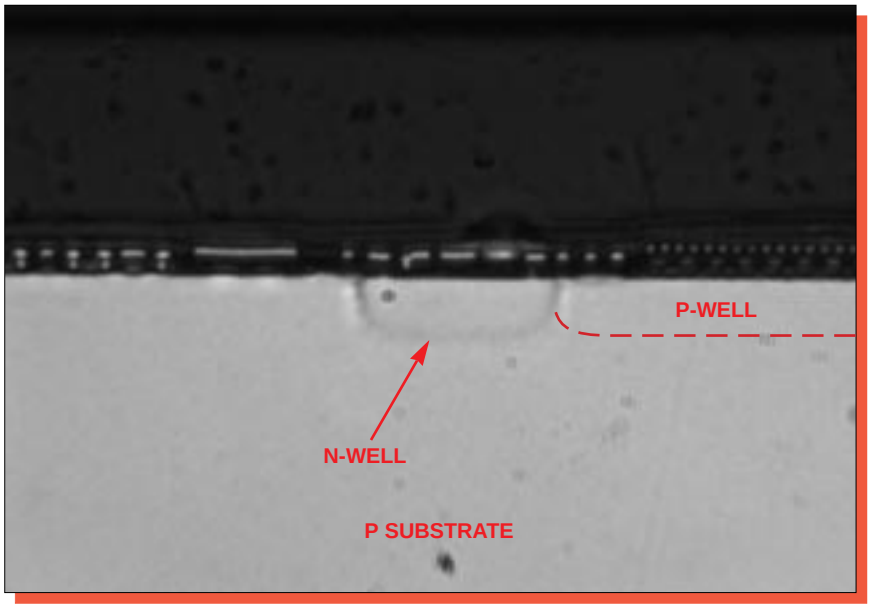


P-channel

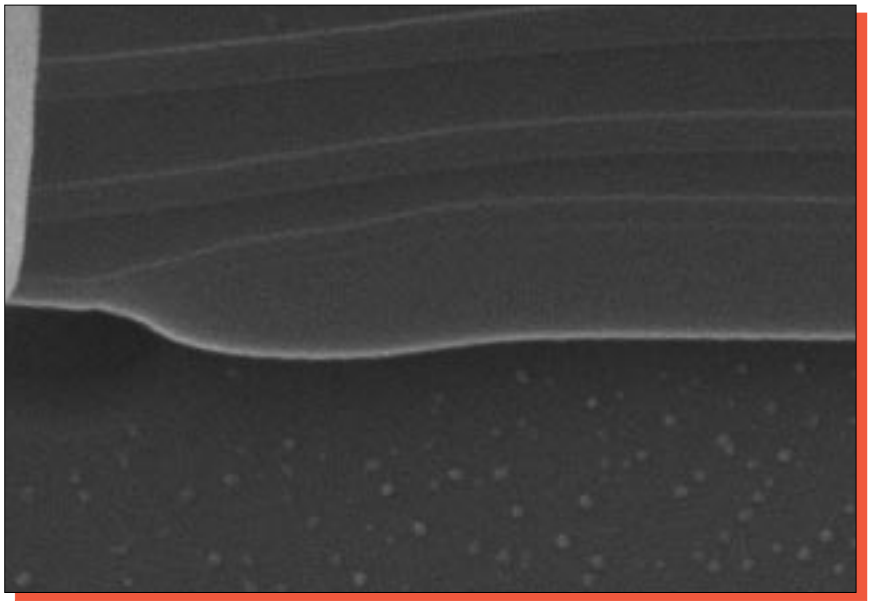


glass etch

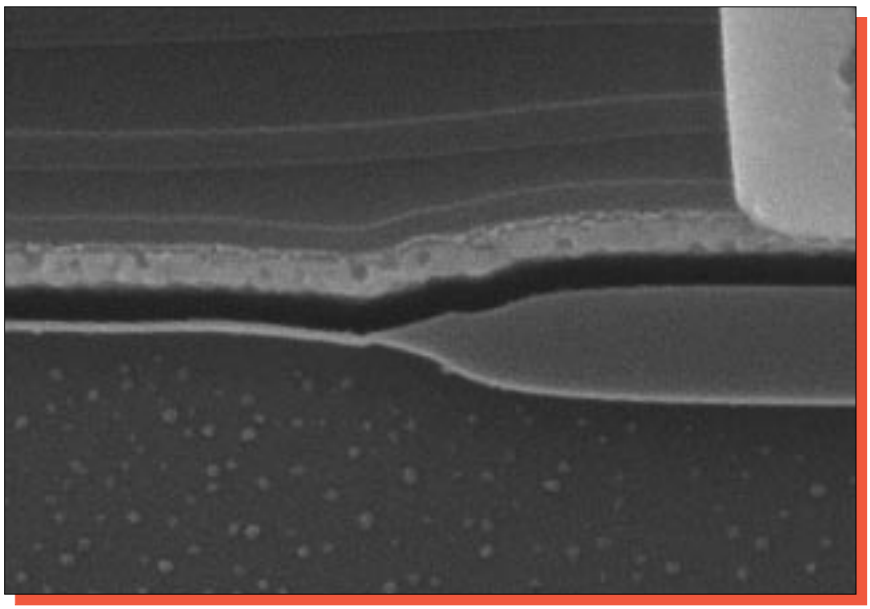
Figure 17a. Detailed SEM views illustrating typical gates. Mag. 52,000x.



Mag. 800x

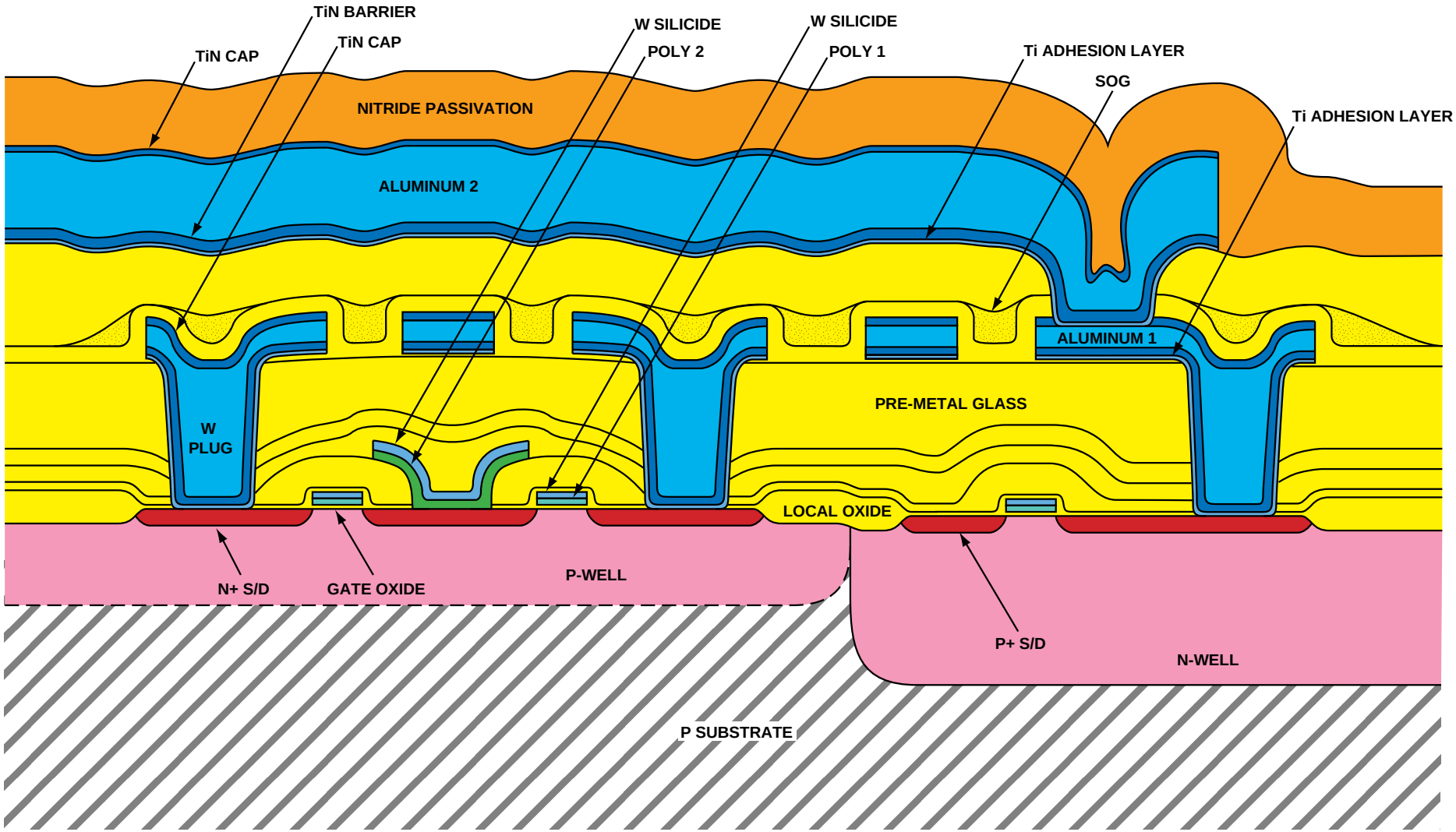


Mag. 52,000x



Mag. 52,000x

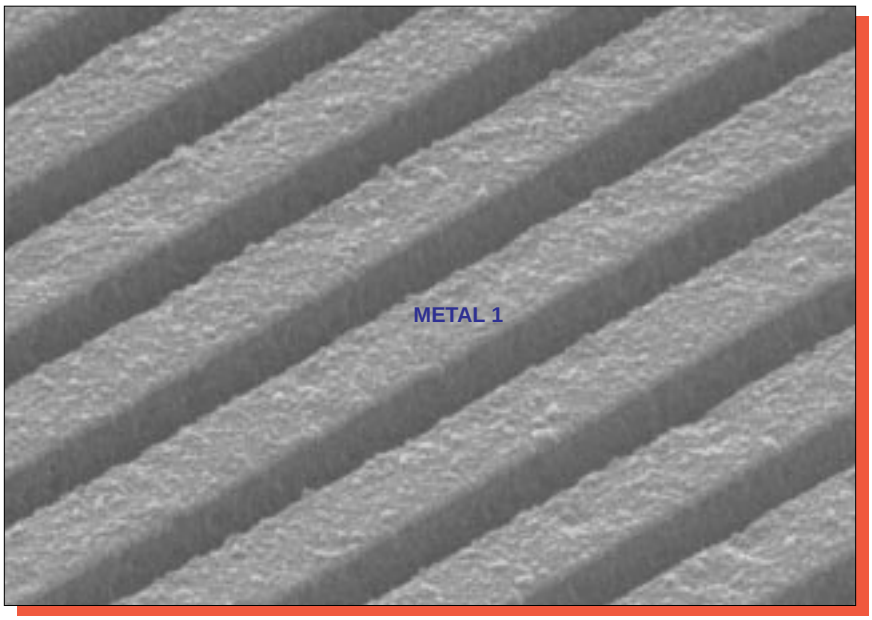
Figure 18. Section views illustrating well structure, step in oxide, and typical birdsbeak.



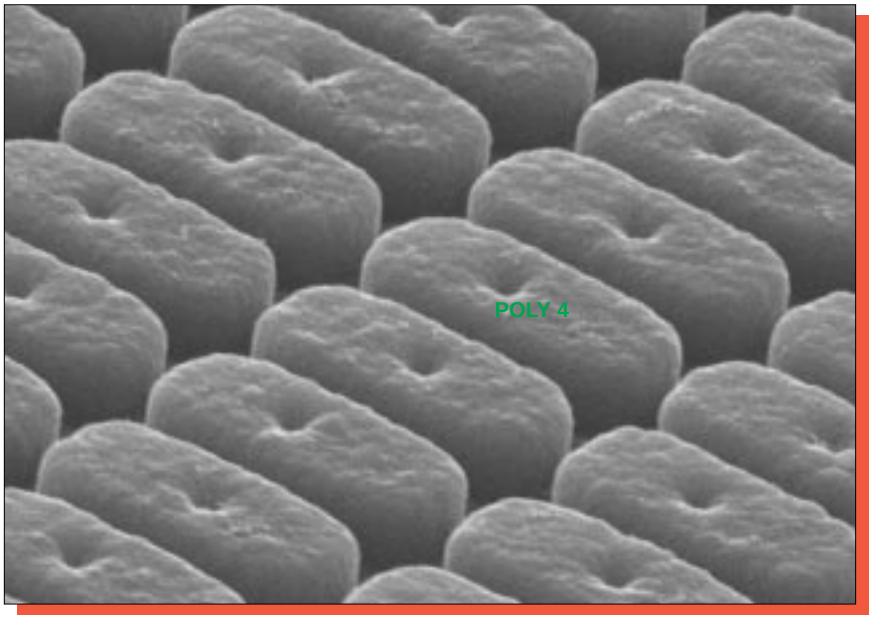
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 19. Color cross section drawing illustrating device structure.

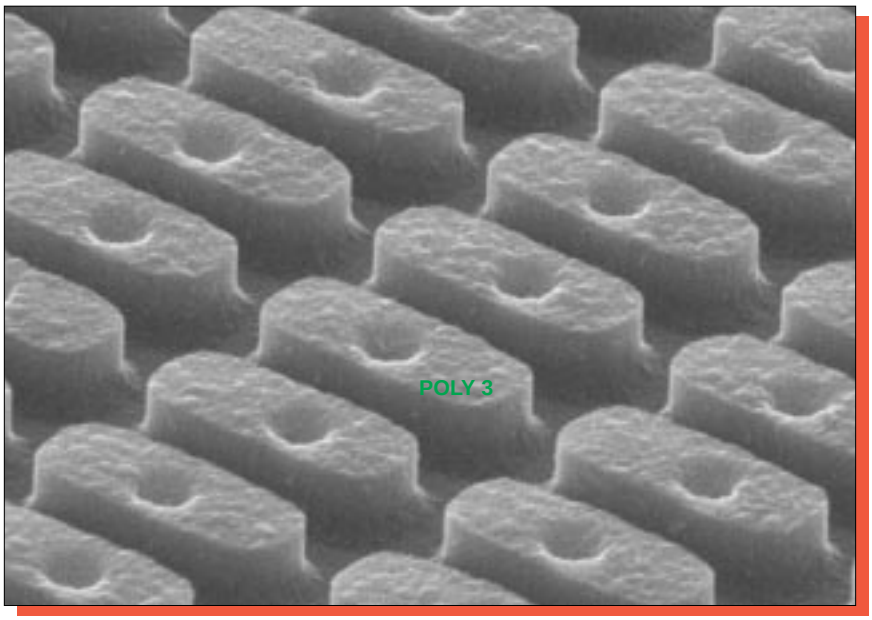


metal 1

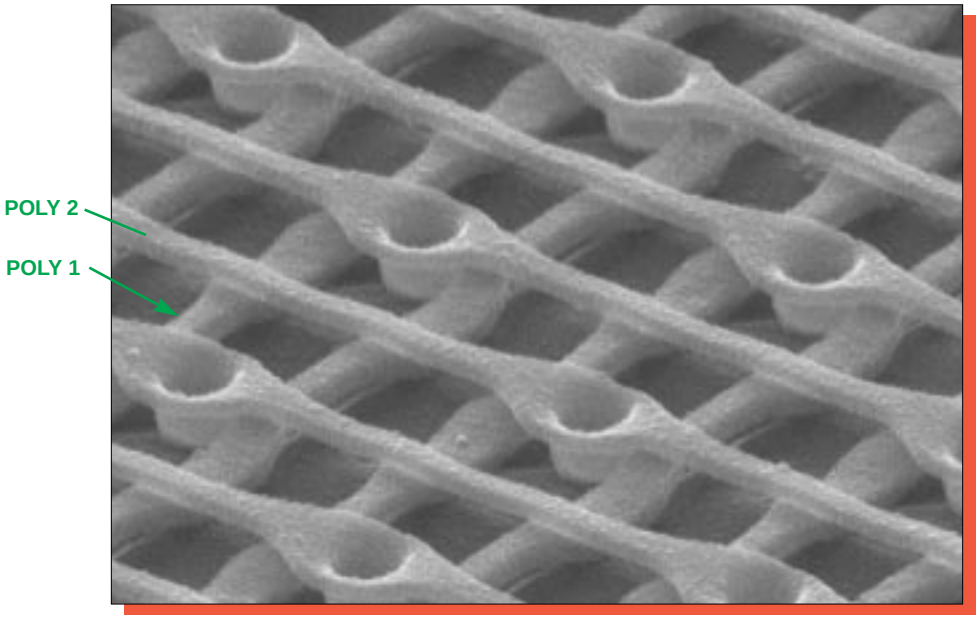


poly 4

Figure 20. Detailed SEM views illustrating SGRAM cell. Mag. 20,000x, 60°.

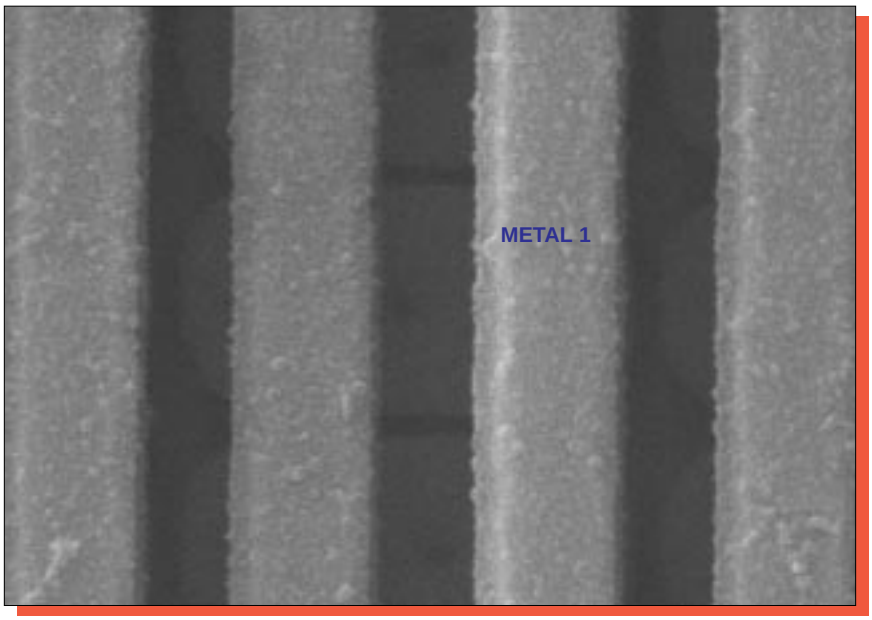


poly 3

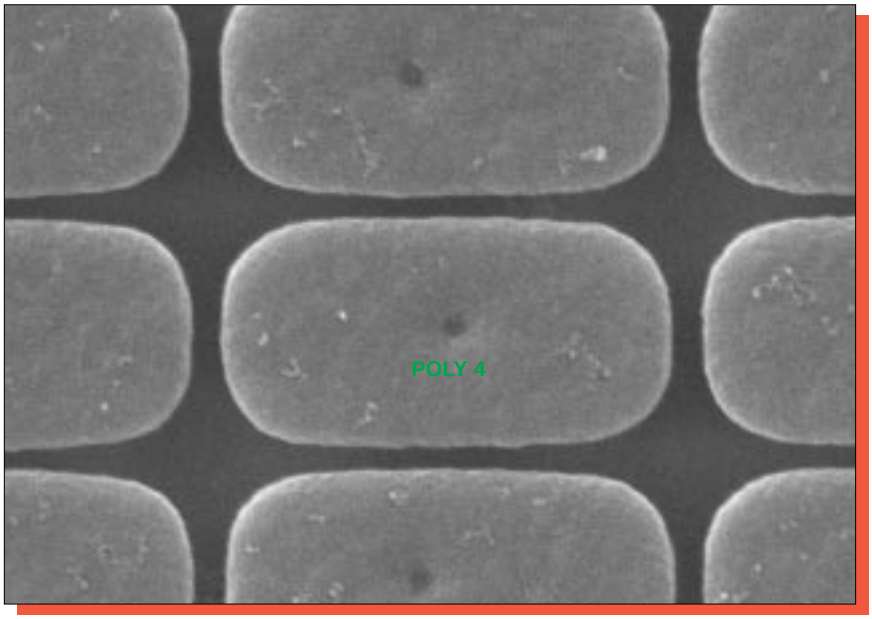


poly 1 and 2

Figure 21. Remaining detailed SEM views illustrating SGRAM cells. Mag. 20,000x, 60°.

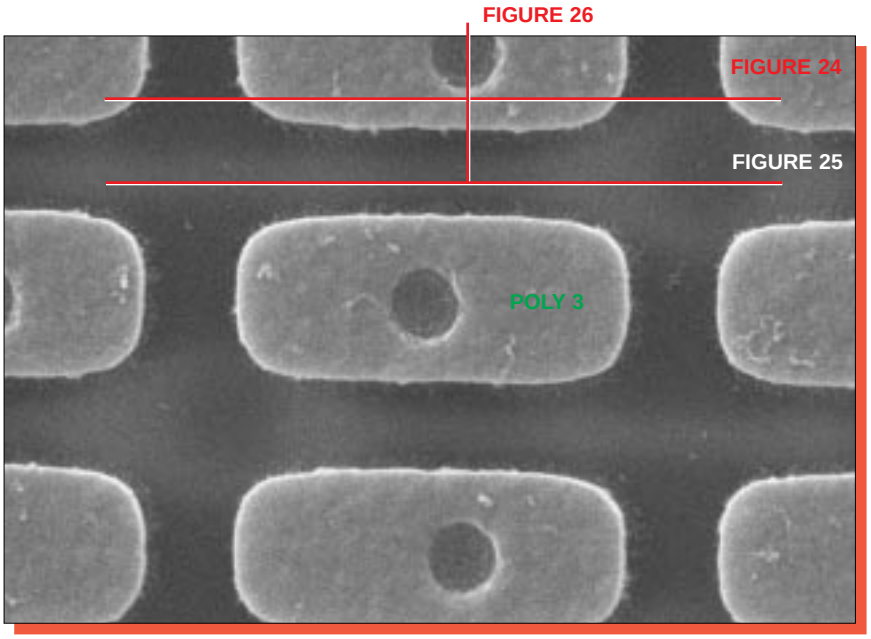


metal 1

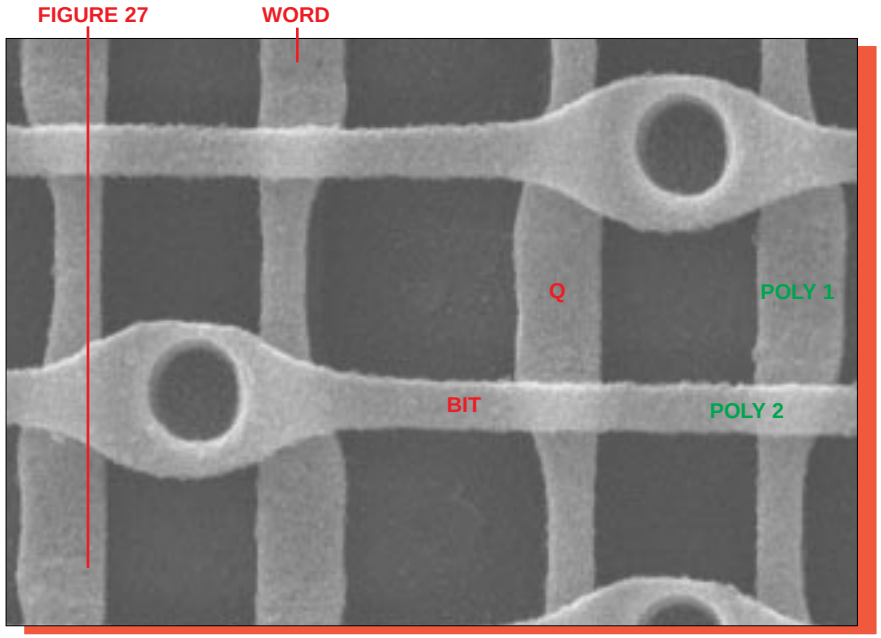


poly 4

Figure 22. Detailed topological SEM views illustrating SGRAM cell. Mag. 26,000x, 0°.



poly 3



unlayered

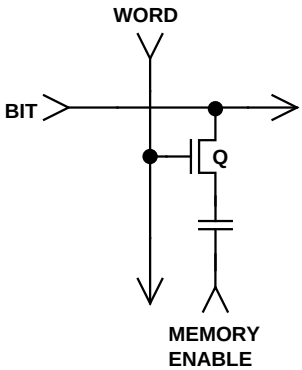
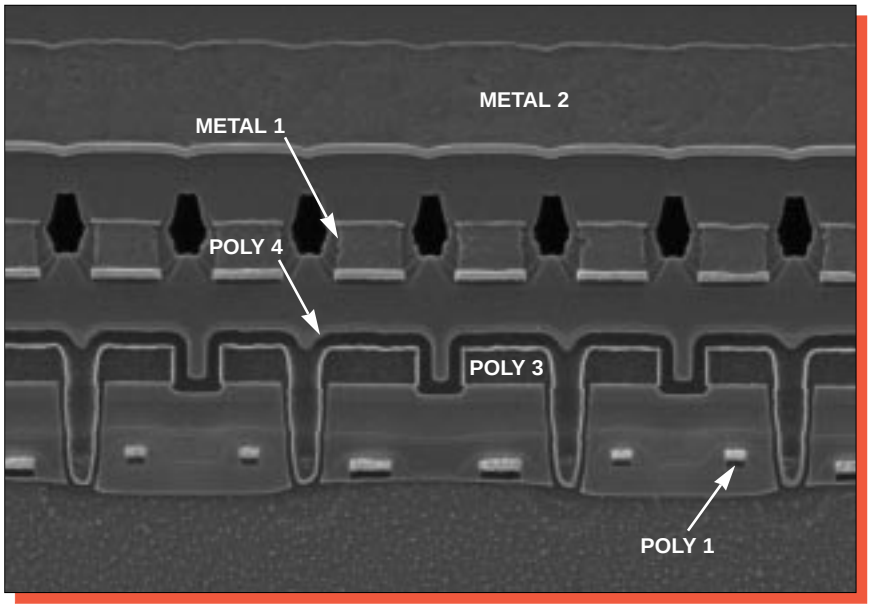
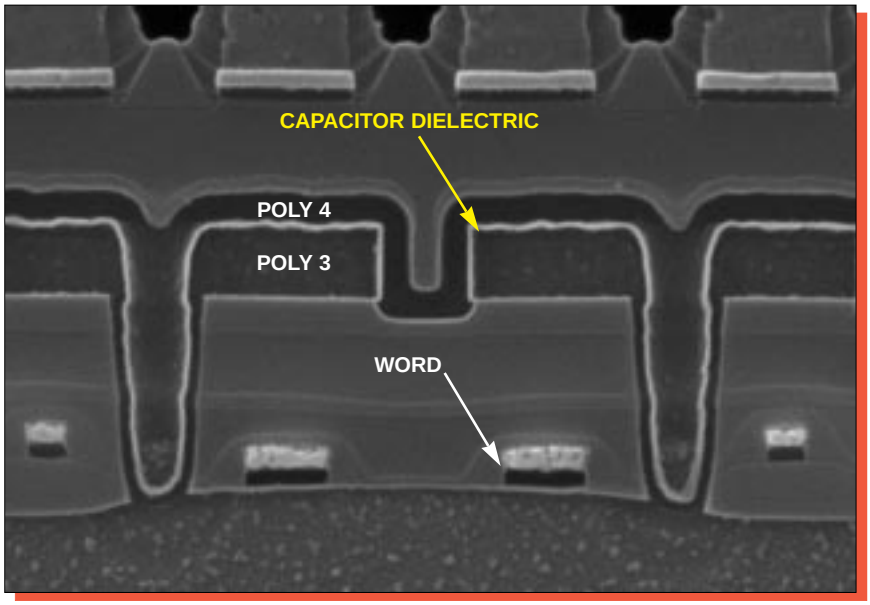


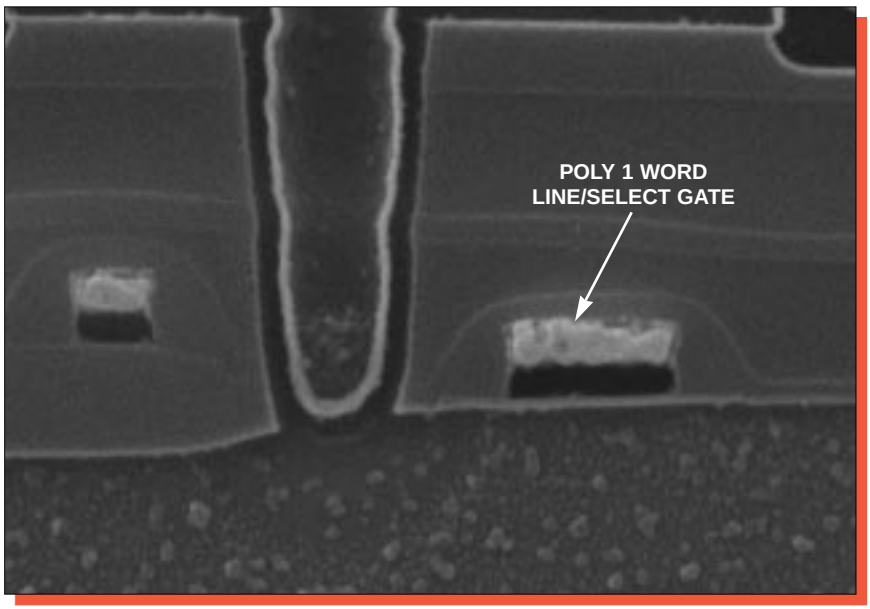
Figure 23. Remaining detailed topological views illustrating SGRAM cell and schematic. Mag. 26,000x.



Mag. 13,000x

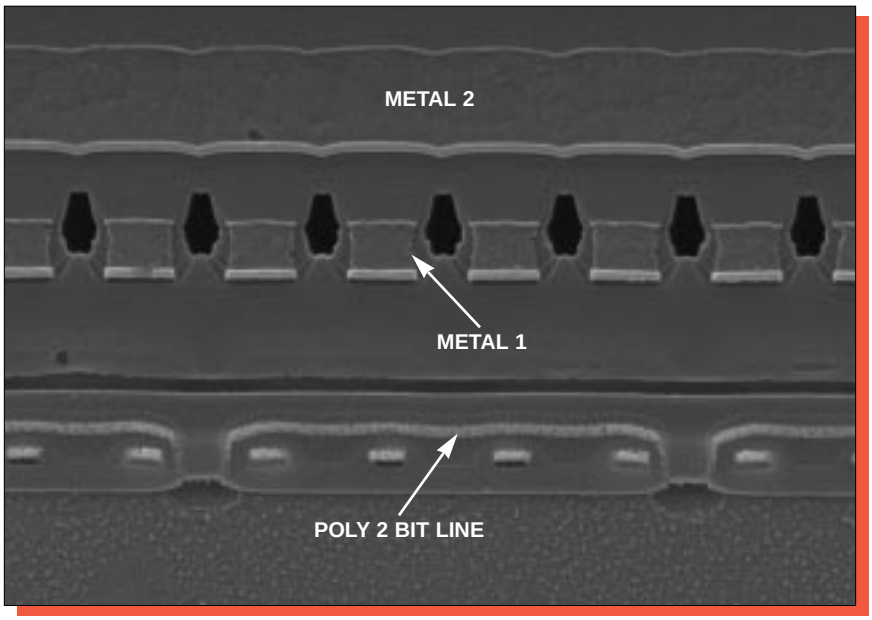


Mag. 26,000x

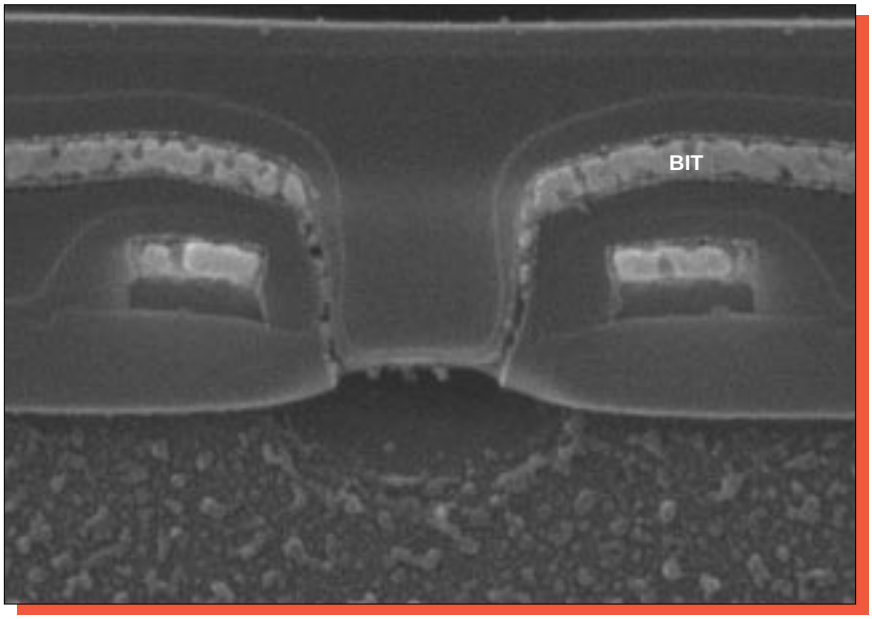


Mag. 52,000x

Figure 24. SEM section views illustrating SGRAM cell.

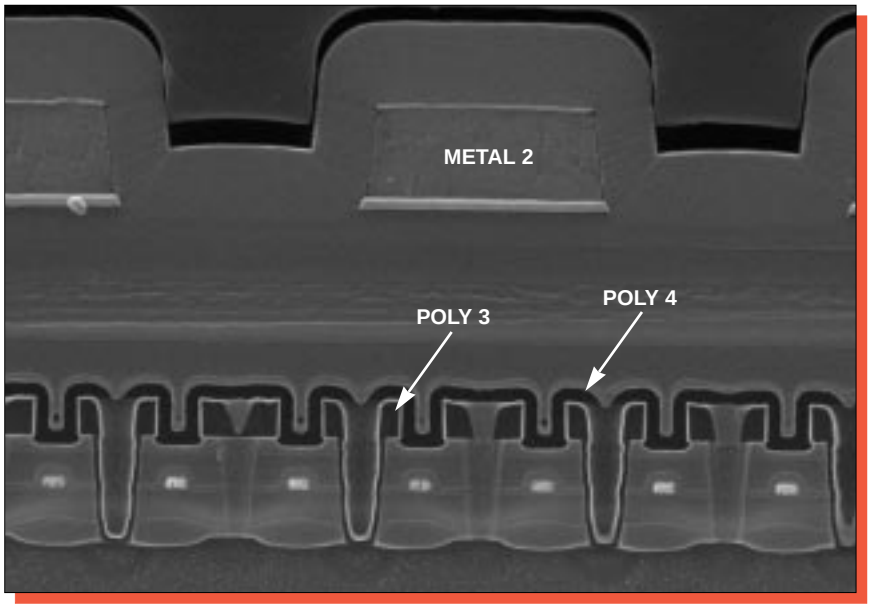


Mag. 13,000x

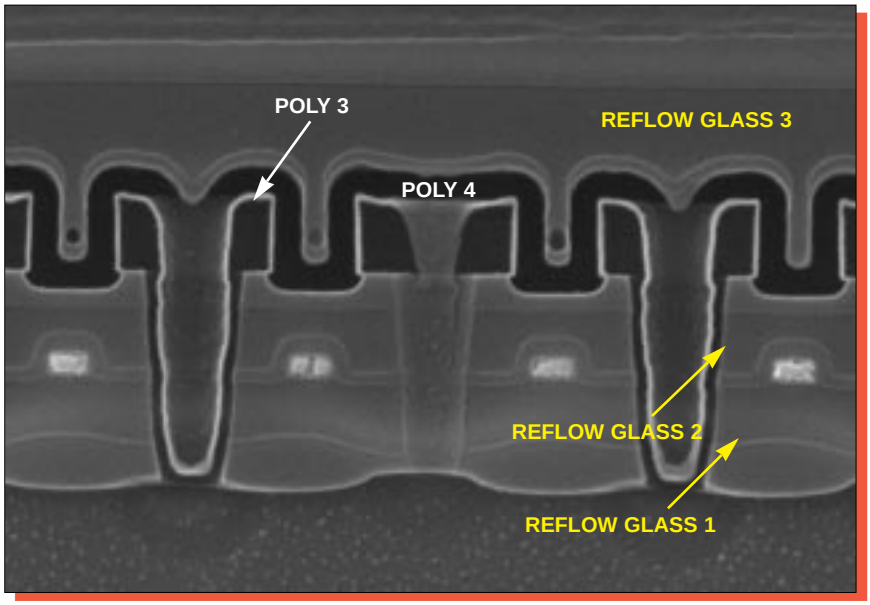


Mag. 52,000x

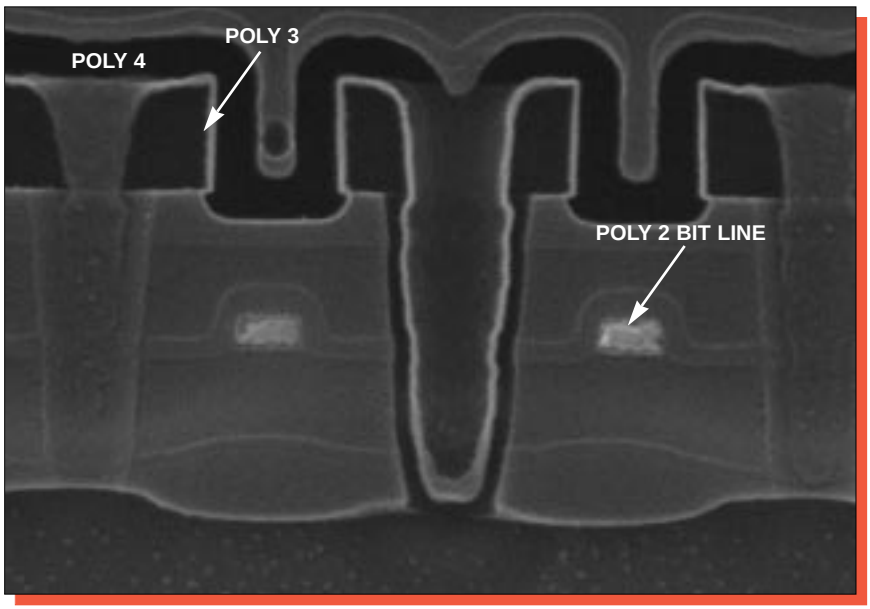
Figure 25. SEM section views illustrating SGRAM cell.



Mag. 13,000x

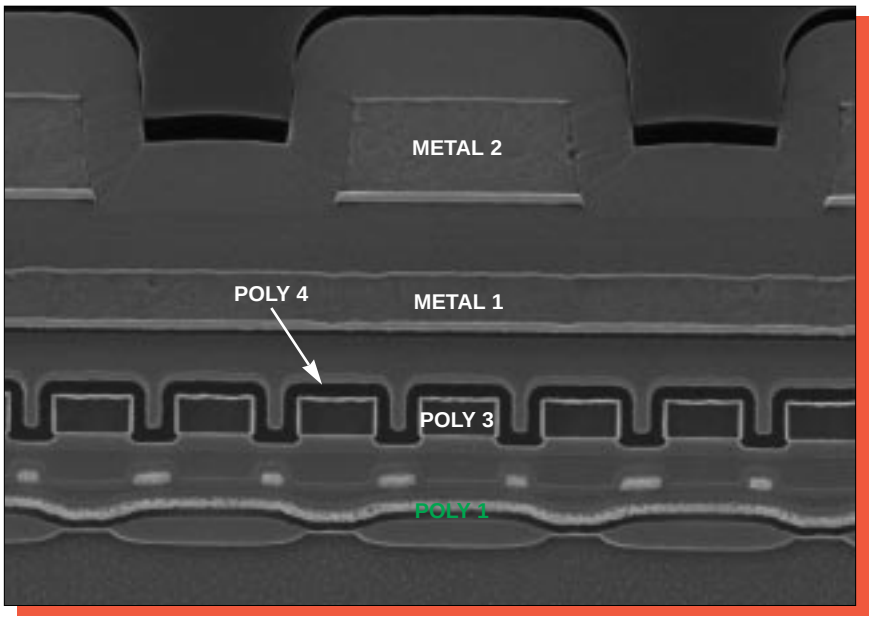


Mag. 26,000x

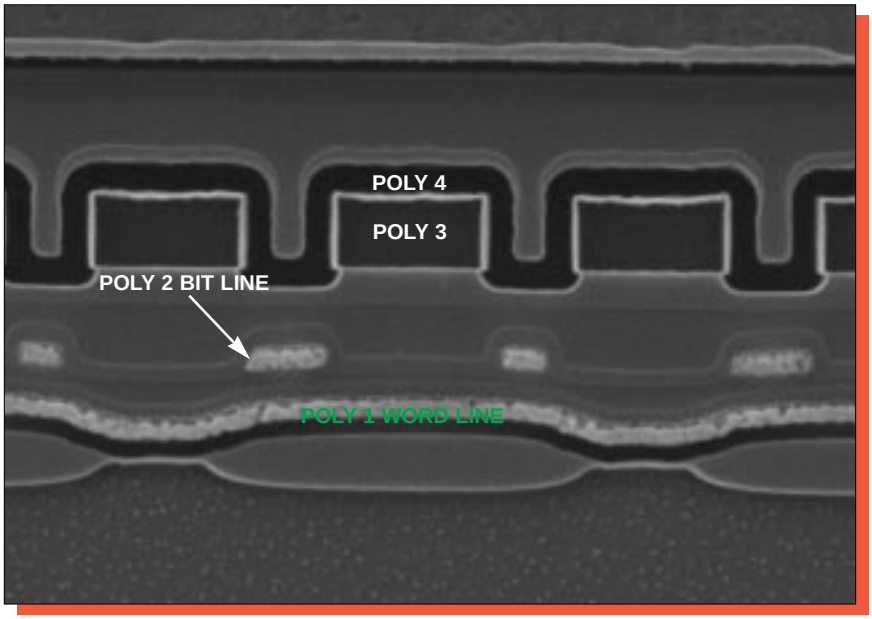


Mag. 40,000x

Figure 26. SEM section views illustrating SGRAM cell.

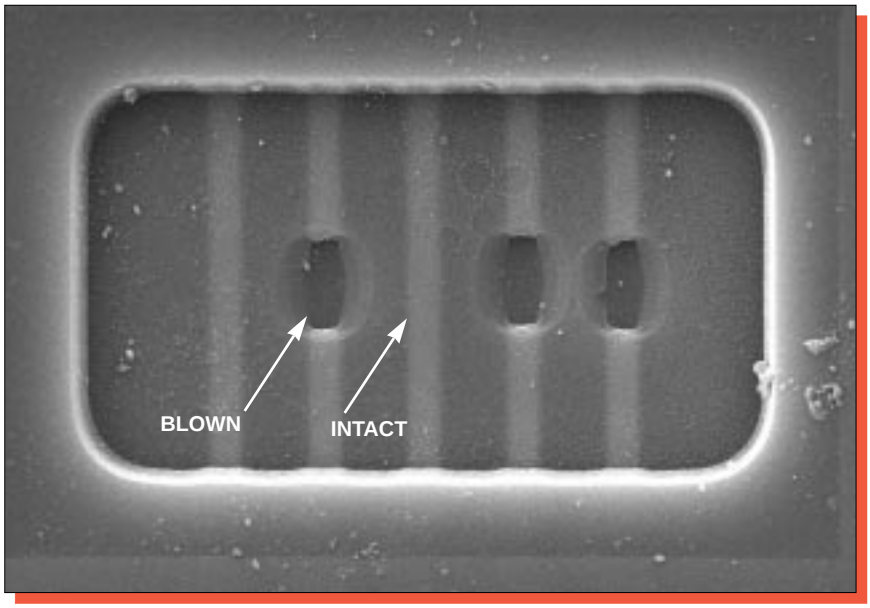


Mag. 13,000x

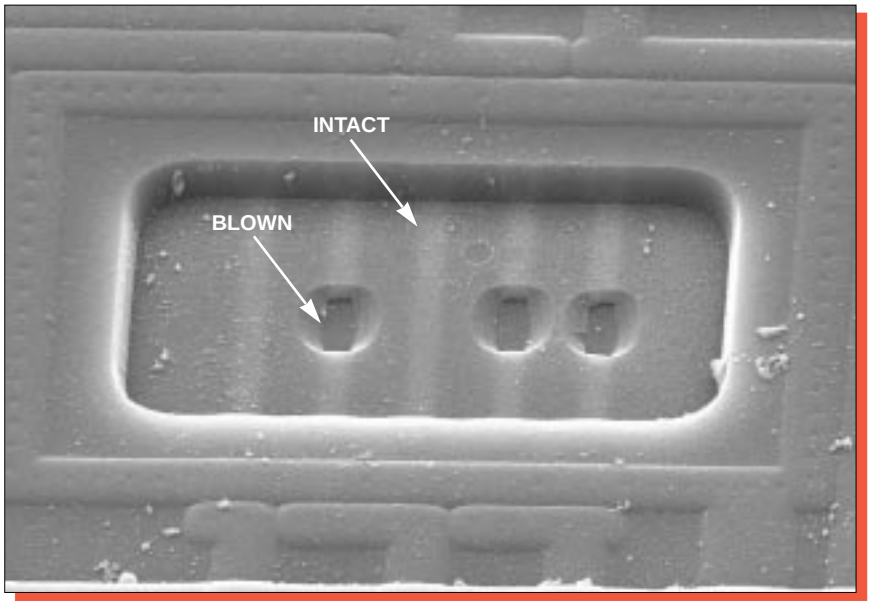


Mag. 26,000x

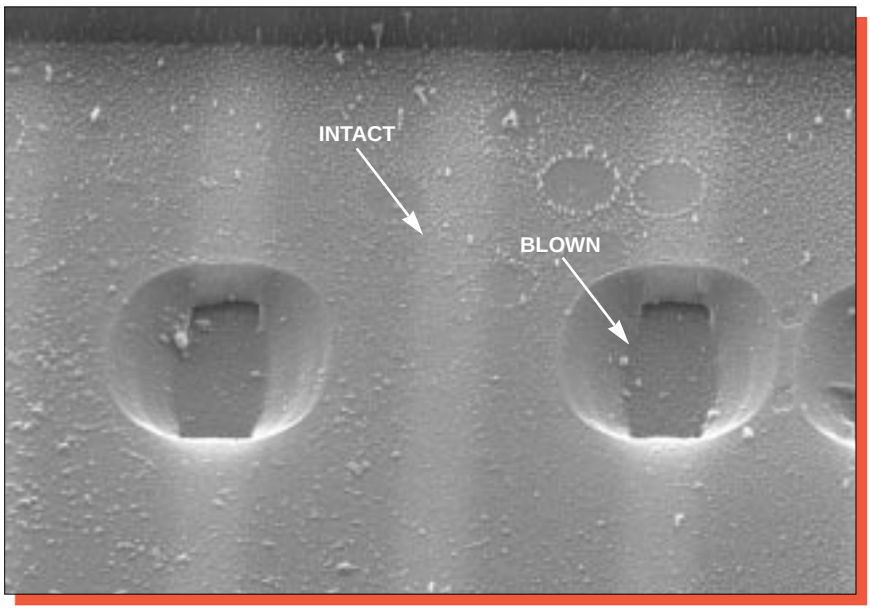
Figure 27. SEM section views illustrating SGRAM cell.



Mag. 3250x, 0°



Mag. 3000x, 45°



Mag. 8000x, 45°

Figure 28. SEM views illustrating fuses.

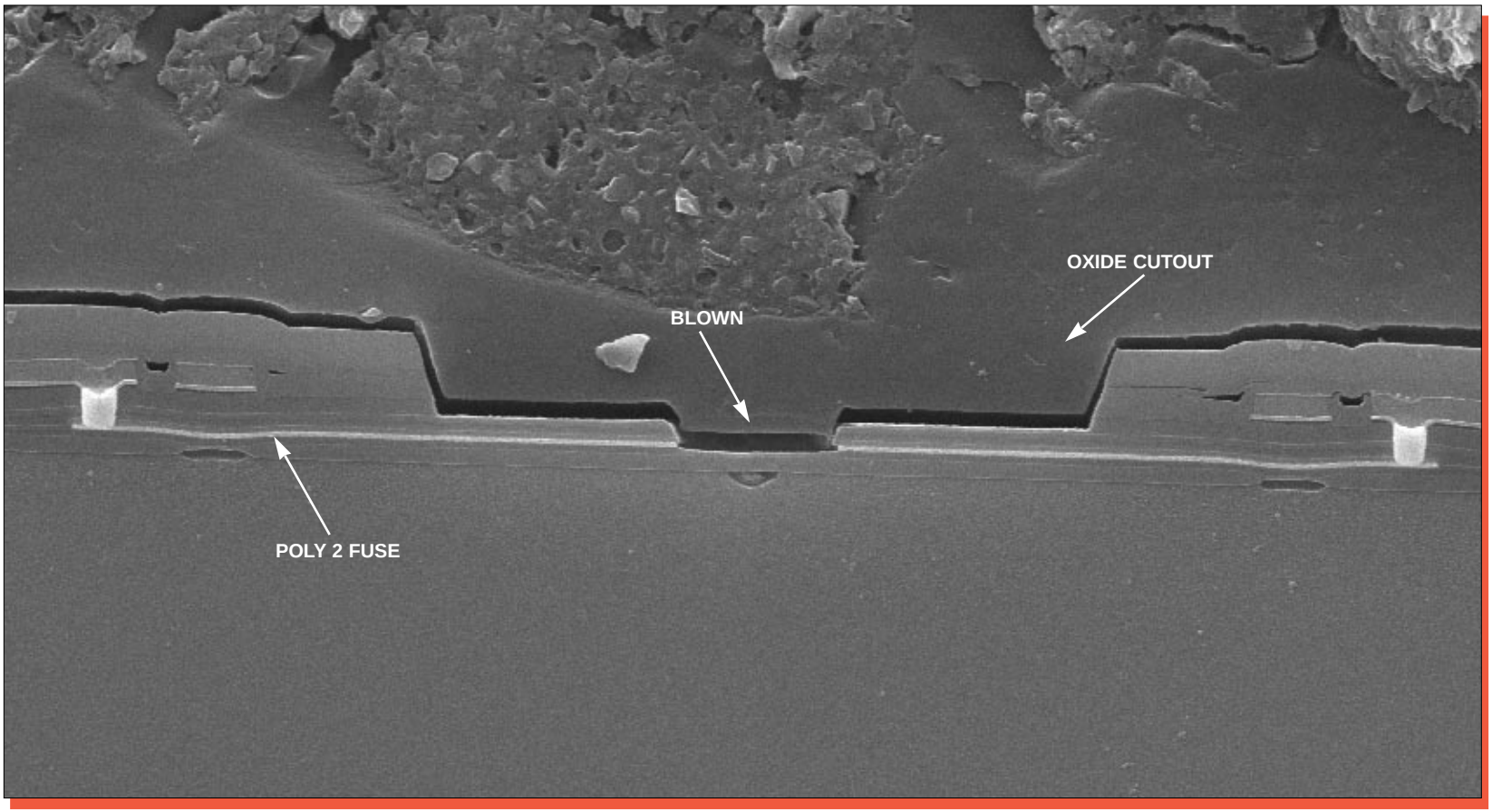
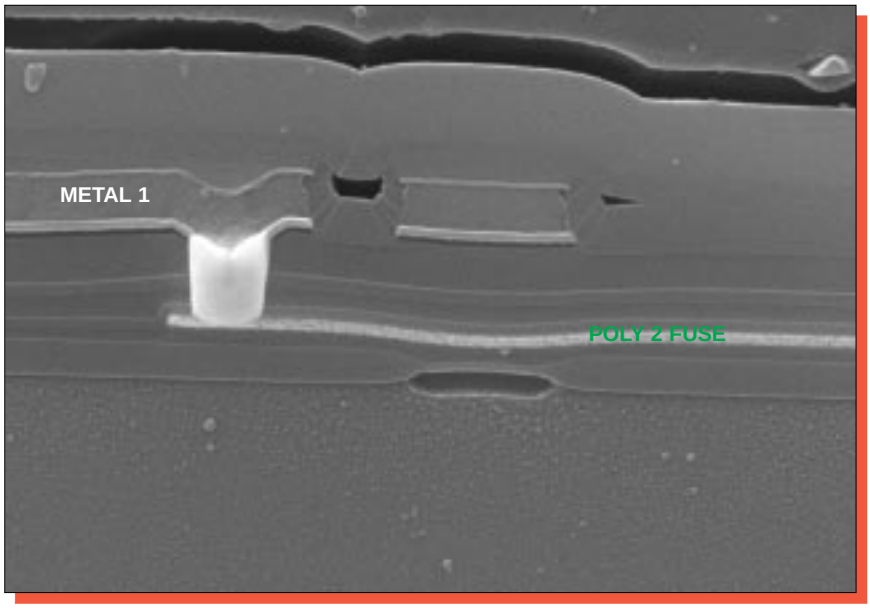
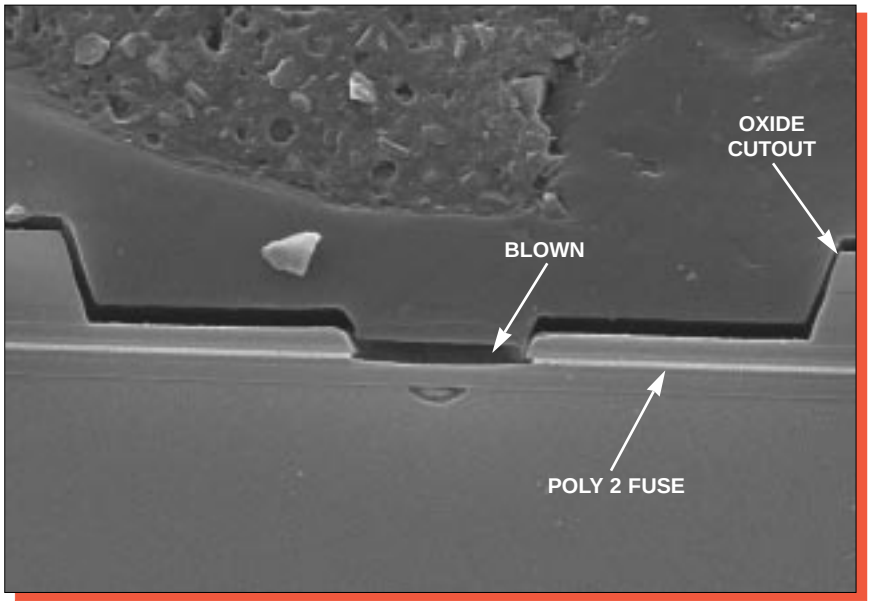


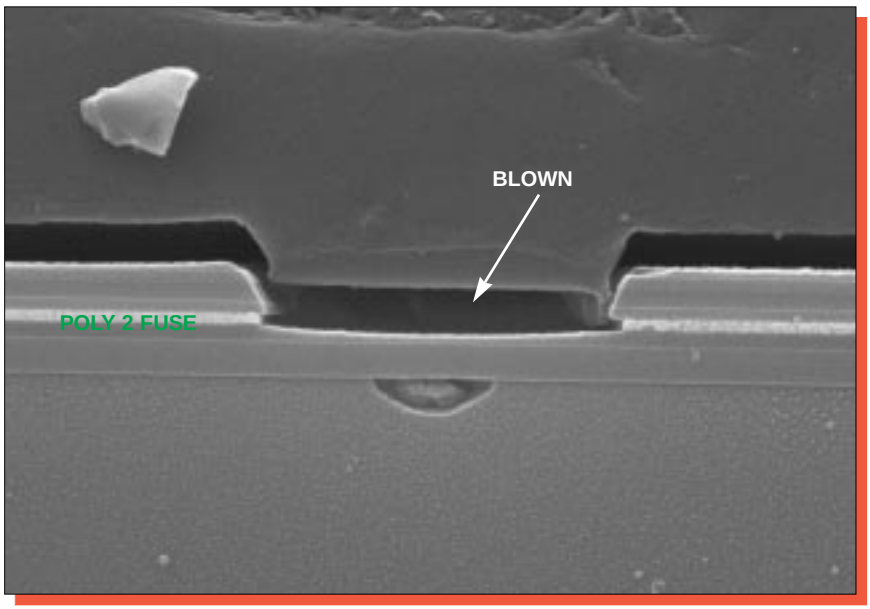
Figure 29. SEM section view illustrating blown fuse. Mag. 6500x.



Mag. 13,000x

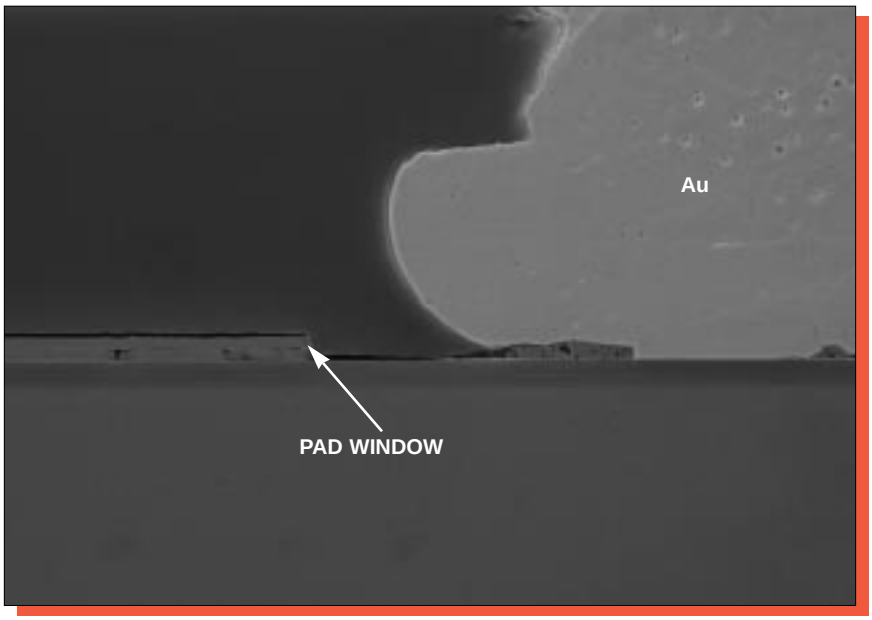


Mag. 6500x

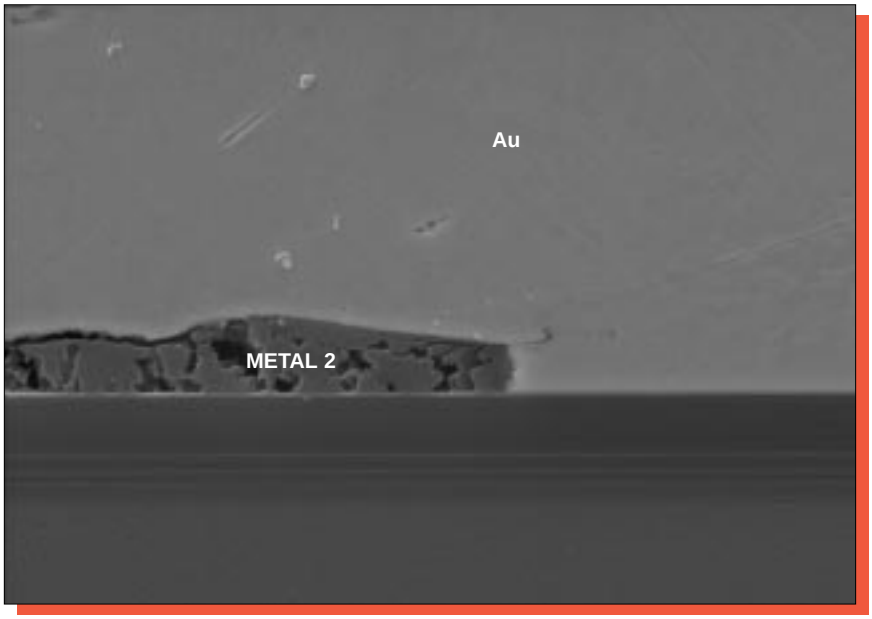


Mag. 13,000x

Figure 29a. Detailed SEM views illustrating fuse.

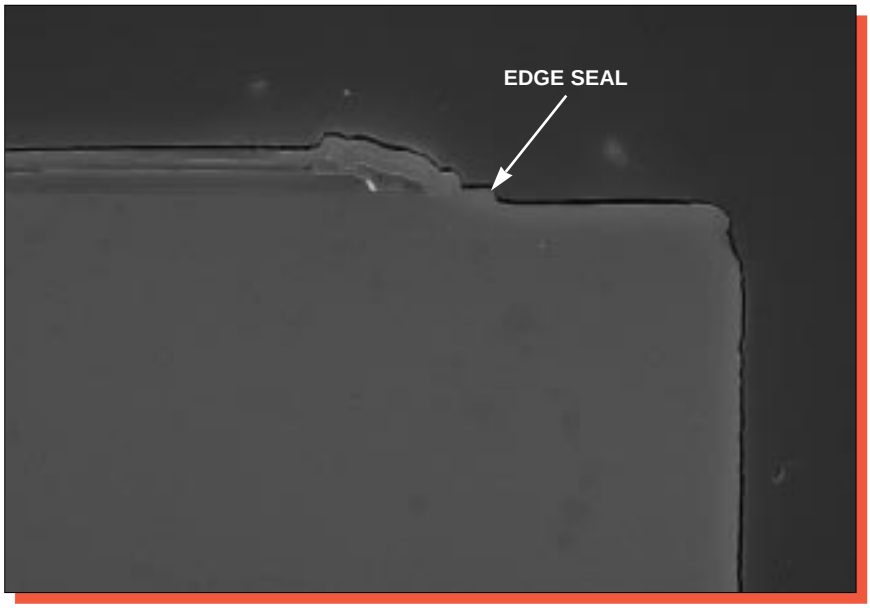


Mag. 1600x

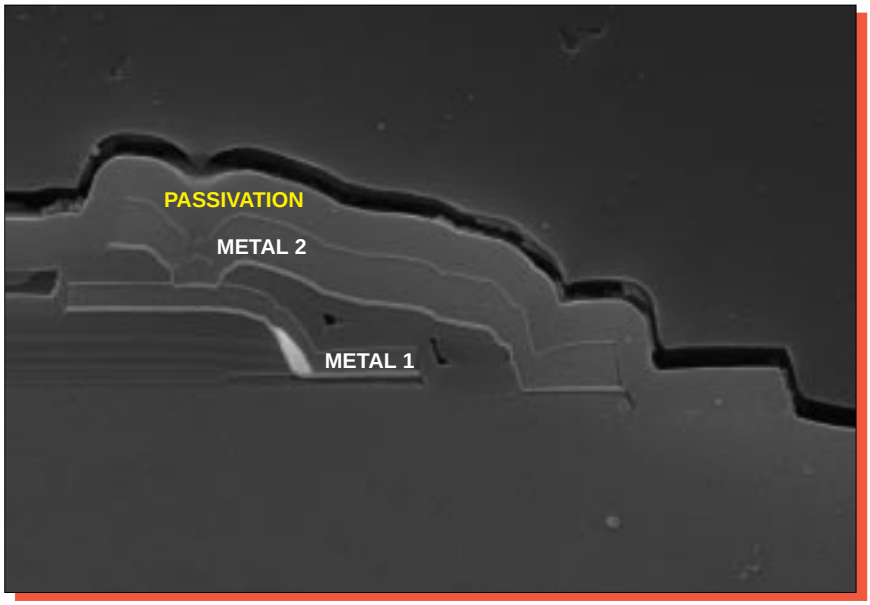


Mag. 6500x

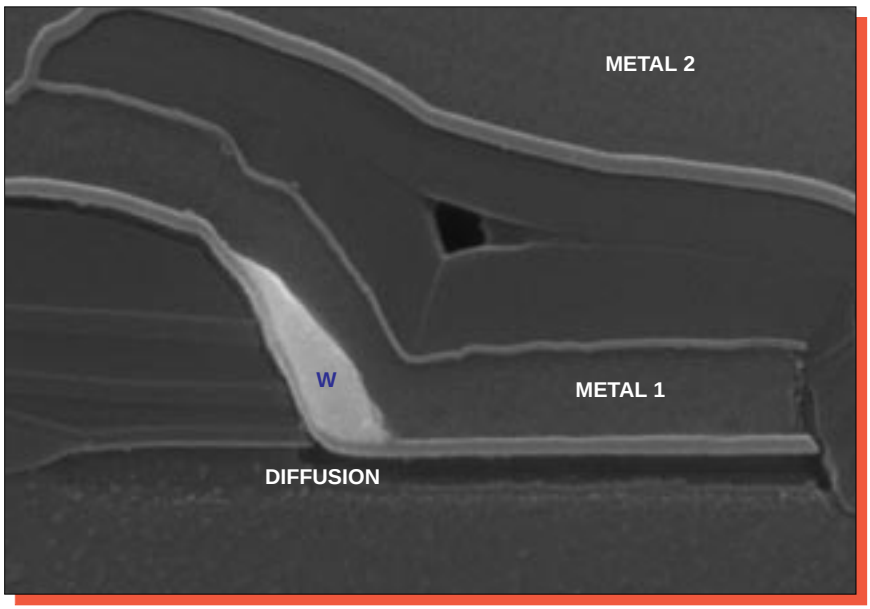
Figure 30. SEM section views illustrating typical bond pad.



Mag. 1600x

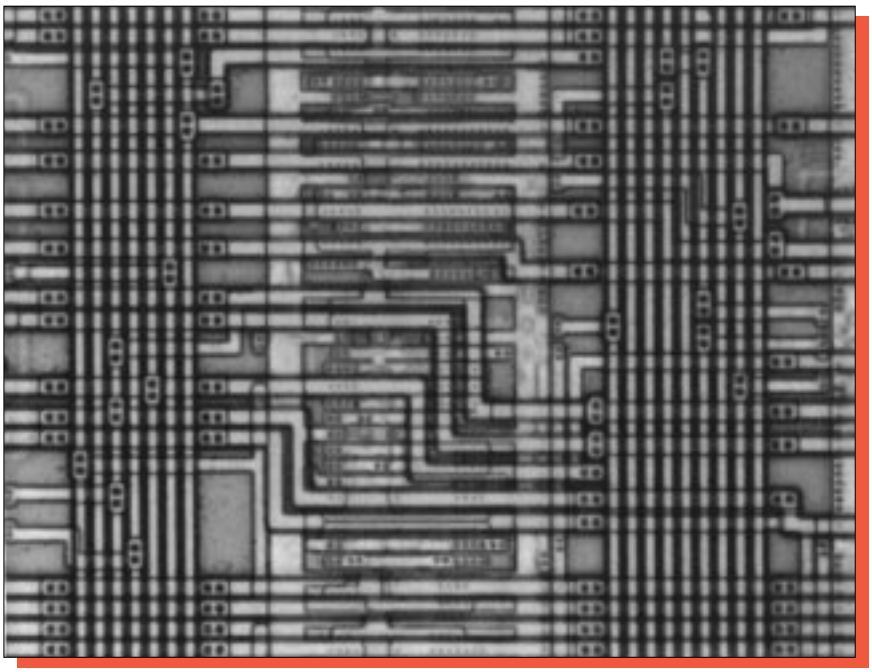


Mag. 6500x

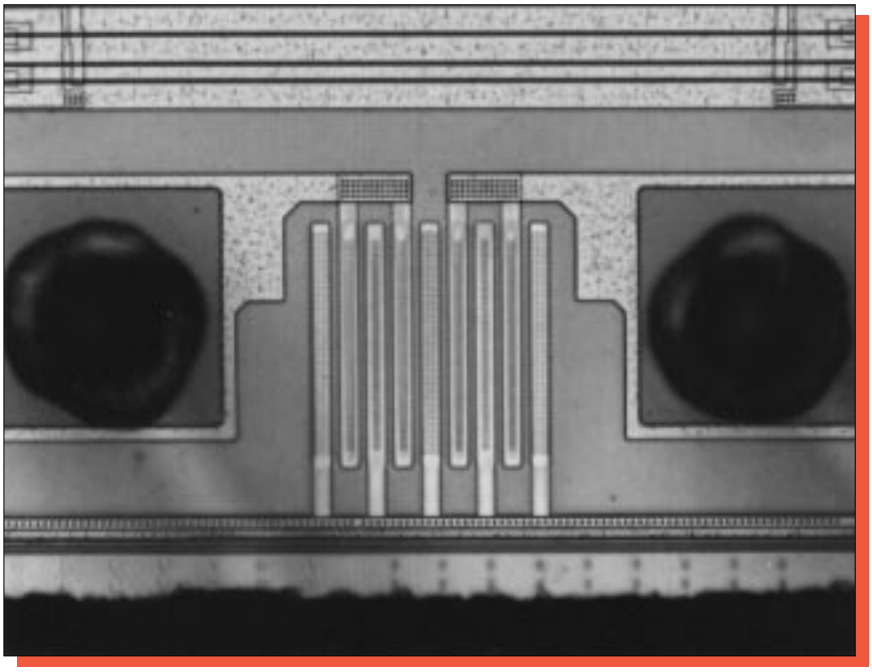


Mag. 26,000x

Figure 31. SEM section views illustrating edge seal.



Mag. 800x



Mag. 320x

Figure 32. Optical views of typical circuitry and I/O structure.

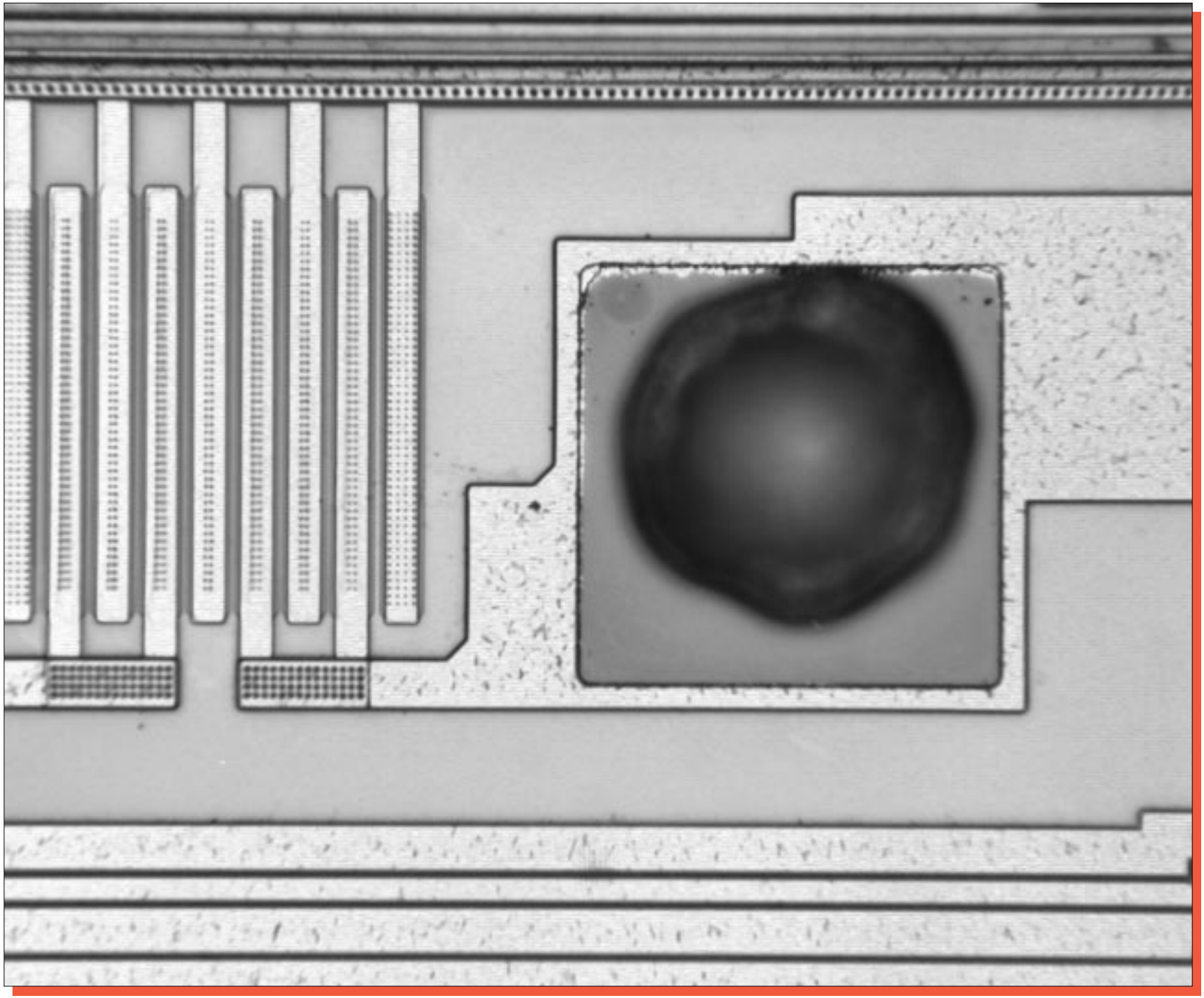


Figure 33. Optical view of Block A. Intact, Mag. 820x.

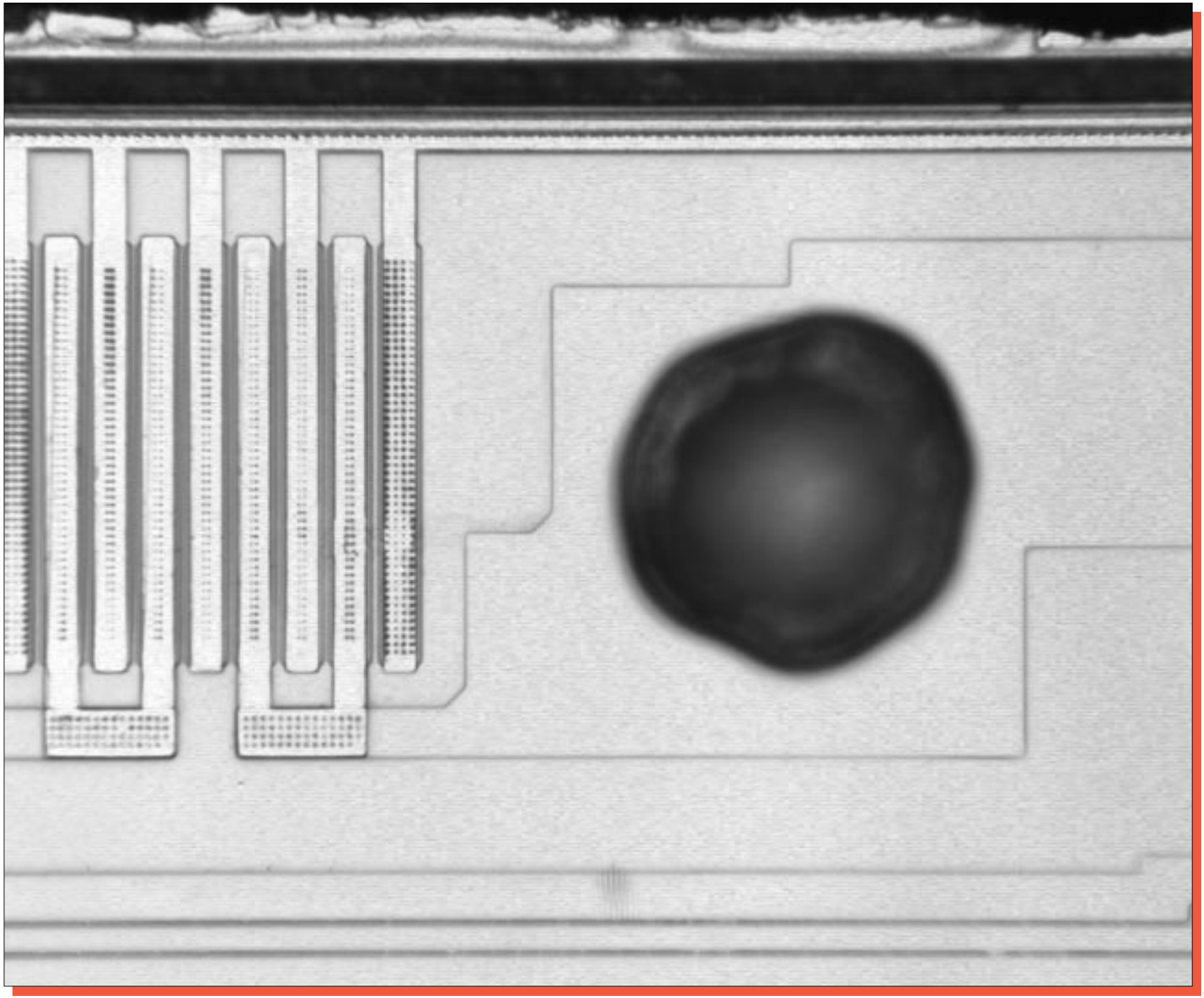


Figure 33a. Optical view of Block A. Metal 1, Mag. 820x.

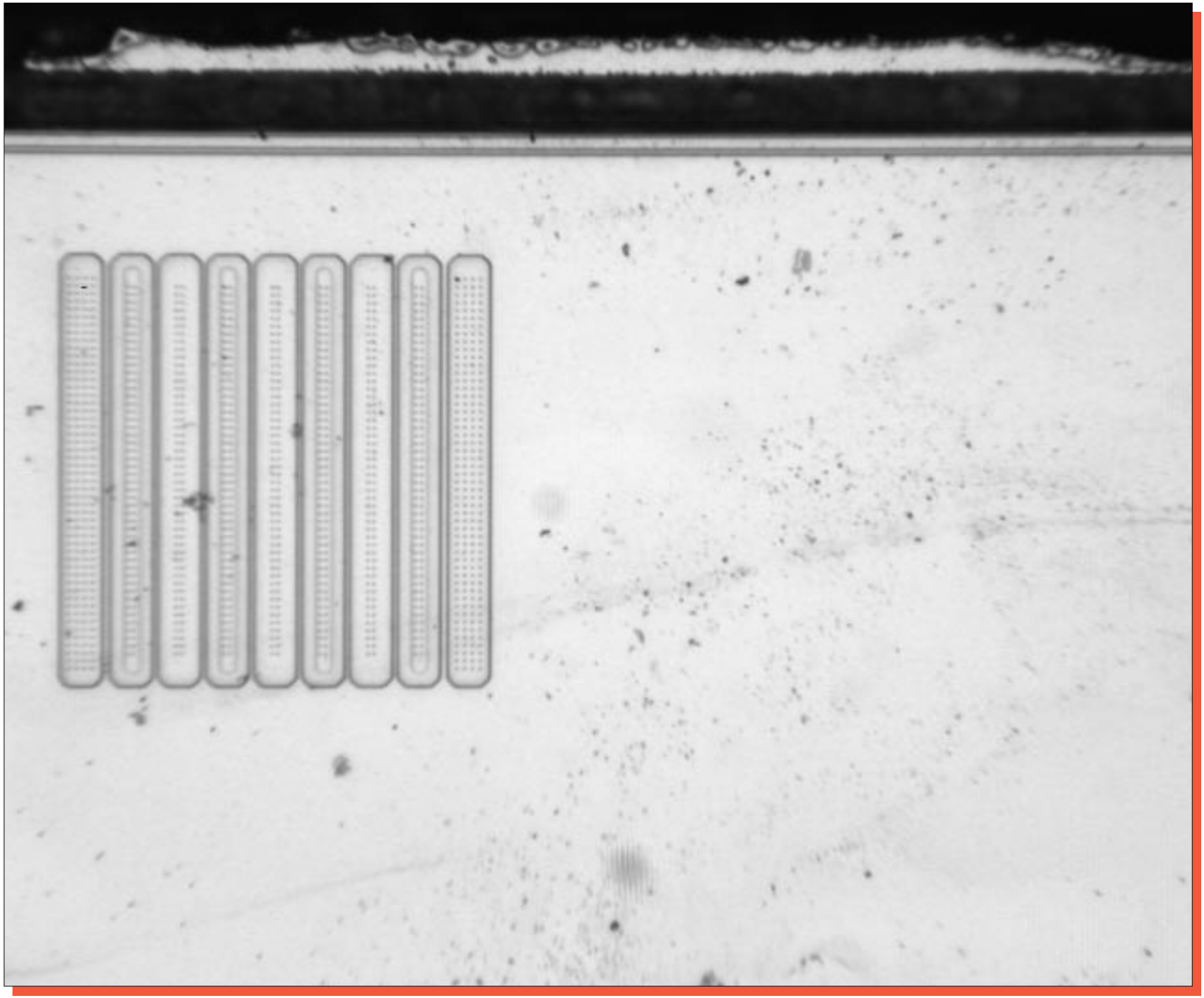


Figure 33b. Optical view of Block A. Unlayered, Mag. 820x.

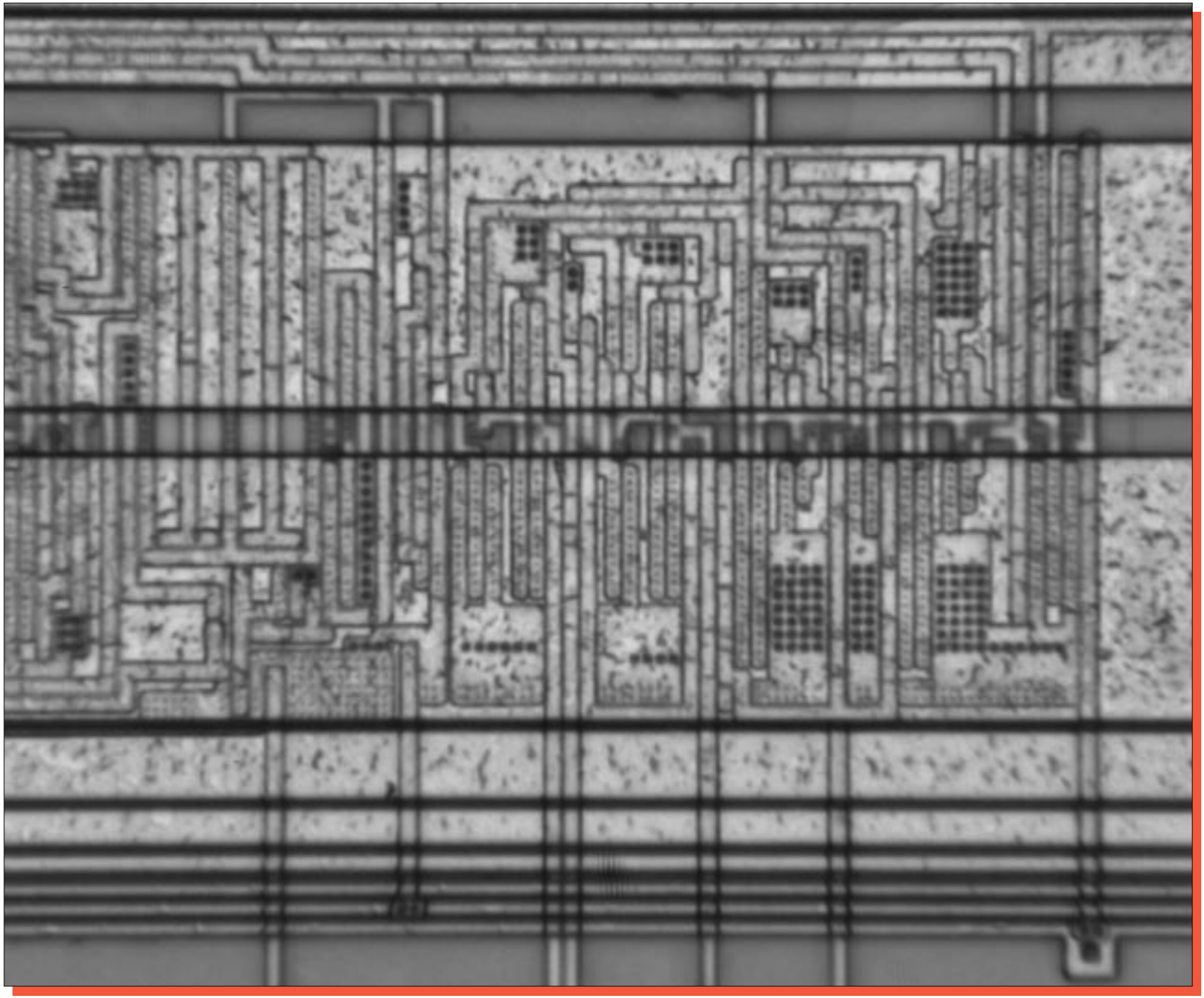


Figure 34. Optical view of Block B. Intact, Mag. 1250x.

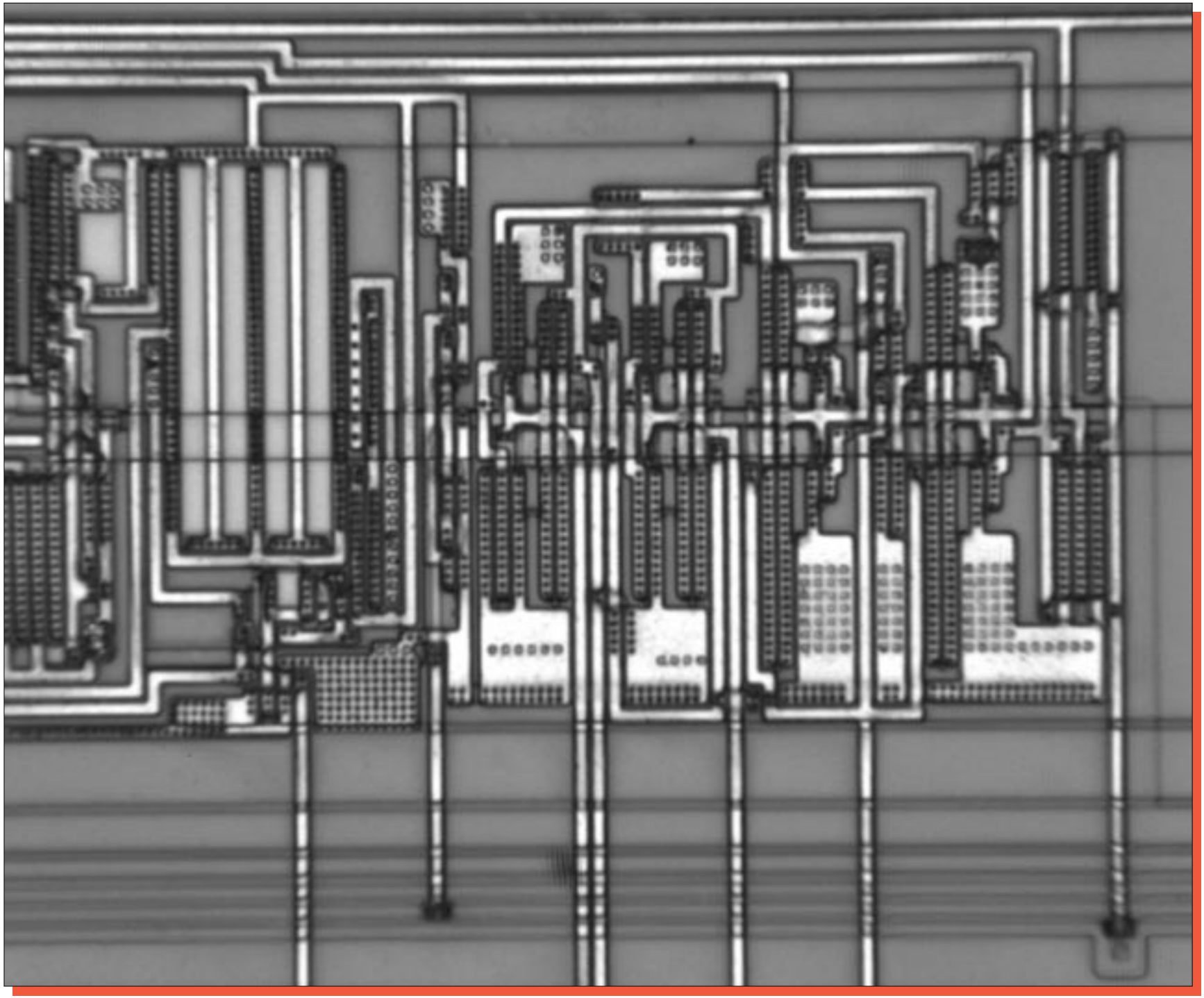


Figure 34a. Optical view of Block B. Metal 1, Mag. 1250x.

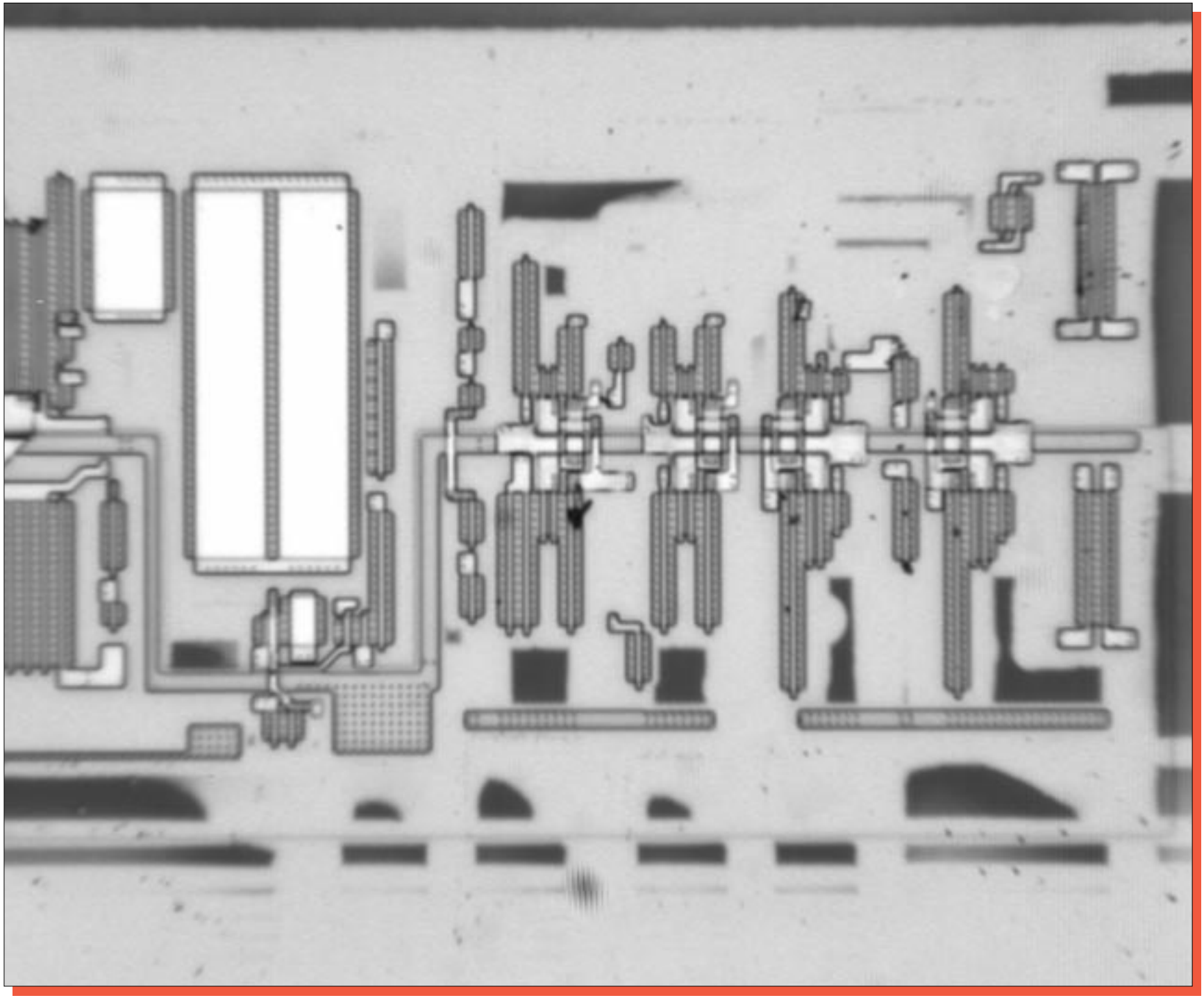


Figure 34b. Optical view of Block B. Unlayered, Mag. 1250x.

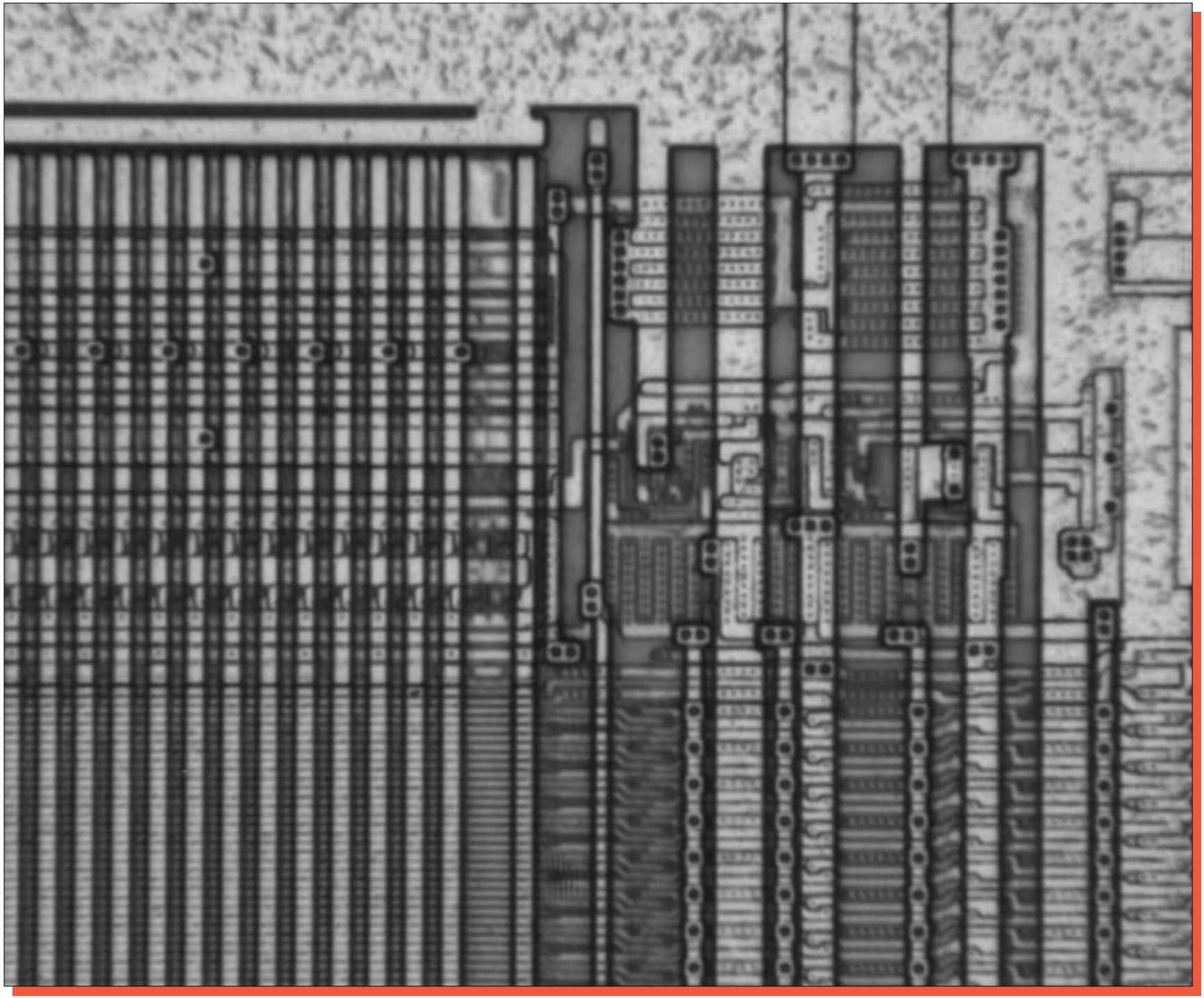


Figure 35. Optical view of Block C. Intact, Mag. 1400x.

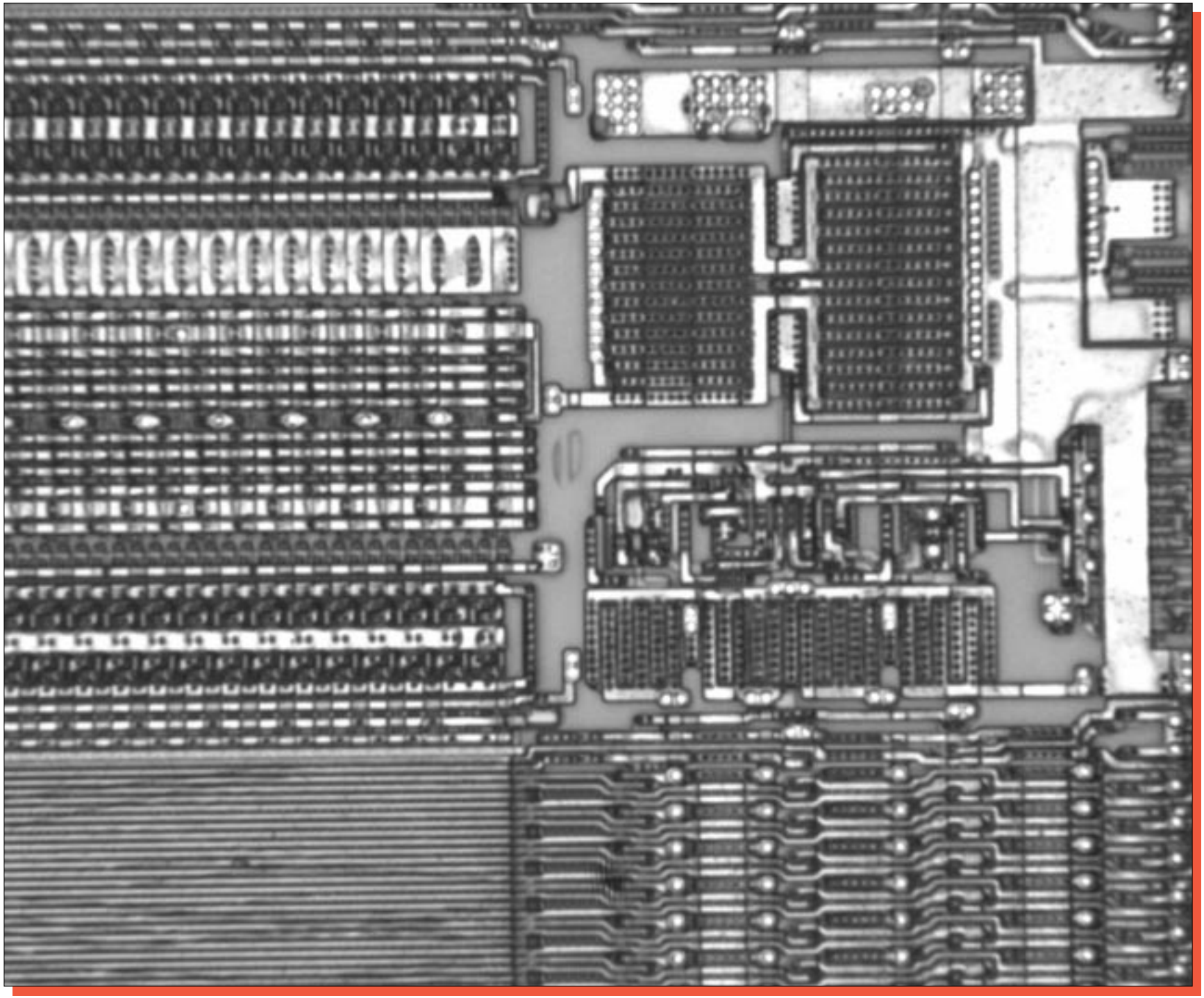


Figure 35a. Optical view of Block C. Metal 1, Mag. 1400x.

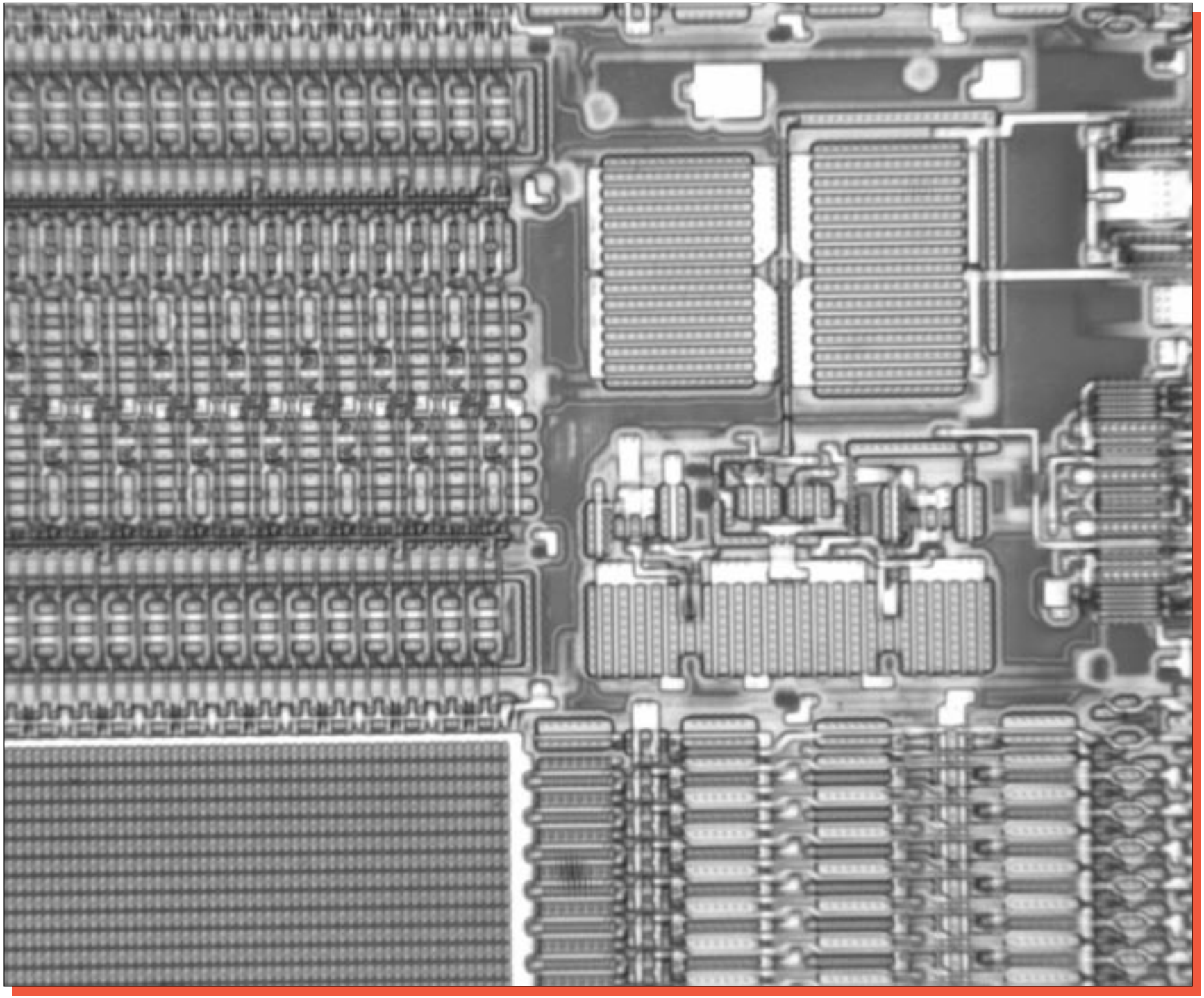


Figure 35b. Optical view of Block C. Unlayered, Mag. 1400x.