

Construction Analysis

Samsung KM4132G271Q-10 8Mb SGRAM

Report Number: SCA 9702-530



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INTRODUCTION

This report describes a construction analysis of the Samsung KM4132G271Q-10, 8 Meg SGRAM. One device packaged in a 120-pin plastic PQFP package was received for the analysis. Package was date coded 546Y (9546).

MAJOR FINDINGS

Questionable Items:¹

- Metal 2 aluminum thinning up to 85 percent² at vias (Figure 14).

Special Features:

- Sub-micron gate lengths (0.45 micron).
- Stacked capacitor DRAM cell design.
- Five layers of poly (four layers effective).
- Reflowed aluminum 1 contacts.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Die Process and Design

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate (no epi was used). No evidence of P-wells was found but this does not rule out their possible presence.
- Final passivation: A layer of nitride over a thin layer of glass.
- Metallization: Metal 2 consisted of silicon-doped aluminum defined by a dry-etch technique. Metal 2 did not use a cap or barrier. Metal 1 consisted of aluminum and employed a titanium-nitride cap and barrier. Standard vias and aluminum-filled (reflowed) contacts were employed. Special patterning of metal 2 and 1 bus lines was used at the corners of the die. Both metals employed slotted lines, beveled (angled) lines at corners and multiple contact arrays. Metal 2 also contained some cutouts.
- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a multilayered glass followed by a spin-on glass (SOG) and another layer of glass.
- Pre-metal dielectric: A single layer of reflow glass over a densified oxide.
- Polysilicon: Five layers of polysilicon were employed. Polycide 4 (poly 4 and tungsten silicide) was used to form bit lines and general interconnect in the peripheral circuitry. Polycide 4 contacted poly 1 and N+ diffusions. Poly 3 (sheet) and Poly 2 (which uses 2 poly depositions)were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die.

TECHNOLOGY DESCRIPTION (continued)

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Oxide sidewall spacers were used and were left in place.
- Wells: N-wells in a P-substrate (no epi). No step in the oxide was noted at the edge of N-wells. Although this is not an absolute indication of a single polarity well process it means we have no proof of twin-wells although it is probable a P-well exist in the cell array.
- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present. (Figures 39 and 40).
- Memory cells: Four layers of polysilicon were employed. Polycide 4 (poly 4 and tungsten silicide) was used to form the bit lines. Poly 3 (sheet) was used to form the common plate of the capacitors and was tied to memory enable. Poly 2 formed the individual plate of the capacitors. As mentioned, Poly 2 is made using two separate depositions (one for each “wing” of the cell plate); but we refer to all of it as Poly 2 for convenience. Poly 1 provided word lines/select gates.

ANALYSIS RESULTS

Die Process and Design:

Figures 8 - 43

Questionable Items:¹

- Metal 2 aluminum thinning up to 85 percent² at vias (Figure 14).

Special Features:

- Sub-micron gate lengths (0.45 micron).
- Stacked capacitor DRAM cell design.
- Five layers of poly (counted as 4).
- Reflowed aluminum 1 contacts.

General Items:

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate (no epi was used). No evidence of P-wells was found but this does not rule out their possible presence. No significant problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins

ANALYSIS RESULTS (continued)

- Final passivation: A layer of nitride over a thin layer of glass. Passivation integrity tests indicated defect-free passivation. Edge seal was also good.
- Metallization: Metal 2 consisted of silicon-doped aluminum defined by a dry-etch technique. It did not use a cap or barrier. Metal 1 consisted of aluminum and employed a titanium-nitride cap and barrier. Standard vias (M2-to-M1) and reflowed aluminum contacts (M1-to-silicon) were employed. Both metals employed beveled/angled corners and multiple contact arrays on the corners and edges of the die. Metal 2 and 1 patterned structures were used around the bonding pads.
- Metal patterning: Both metal layers were defined by a dry-etch of good quality.
- Metal defects: None. No notching or voiding of the metal layers was found. No silicon nodules were found following removal of the aluminum.
- Metal step coverage: Metal 2 aluminum thinned up to 85 percent at vias. Typical metal 2 thinning was 80 percent. Military standards allow up to 70 percent metal thinning at contacts of this size. Virtually no metal 1 thinning was present due to the use of aluminum reflow at contacts.
- Vias and contacts: Via and contact cuts appeared to be defined by a two-step etch. No excessive over-etching or other problems were found. Both metals employed multiple contact arrays.
- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of a multilayered glass followed by a spin-on glass (SOG) for planarization, and another layer of glass. No problems were found with these layers.

ANALYSIS RESULTS (continued)

- Pre-metal dielectric: A single layer of reflow glass (BPSG) over a densified oxide in peripheral circuit areas and in the memory array.
- Polysilicon: Five layers of polysilicon were employed. Polycide 4 (poly 4 and tungsten silicide) was used to form bit lines in the array and general interconnect in the peripheral circuitry. Polycide 4 contacted poly 1 and N+ diffusions. Poly 3 (sheet) and Poly 2 (two layers) were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die. Definition was good at all layers and no problems were noted.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. No step was present in the local oxide at the well boundaries.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Sidewall spacers were used and left in place. No problems were found in any of these areas.
- Wells: N-wells were used in a P substrate (no epi was present). No step in the oxide was noted at the edge of the N-wells (indication of twin-well process) and no problems were found. A P-well if present could not be delineated.
- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present.
- Memory cells: Five layers of polysilicon were employed. Polycide 4 was used to form the bit lines. Poly 3 was used to form the common plate of the capacitors (sheet) and was tied to memory enable. Poly 2 formed the dual individual plates of the capacitors. (As mentioned, poly 2 consisted of two separate layers connected together.) Poly 1 formed all gates and word lines. Definition was good and no problems were noted. Cell pitch was 1.1 x 2.5 microns (2.75 microns²).

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM inspection of passivation

Passivation integrity test

Delayer to metal 2 and inspect

Aluminum removal (metal 2)

Delayer to metal 1 and inspect

Aluminum removal (metal 1)

Delayer to poly/substrate and inspect poly and substrate

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	NP*
Metal registration	G
Contact coverage	G
Contact registration	G

**85 percent metal 2 aluminum thinning.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

SEC KOREA
546Y
KM4132G271Q-10

BOTTOM

5PG017THF

DIE MATERIAL ANALYSIS

Overlay passivation:	A layer of nitride over a thin layer of glass.
Metallization 2:	Aluminum.
Intermetal dielectric (IMD):	Two layers of silicon-dioxide with a filler glass (SOG) between.
Metallization 1:	Aluminum with a titanium-nitride (TiN) cap and barrier.
Pre-metal glass:	A single layer of reflow glass over a densified oxide.
Polycide:	Tungsten-silicide.

HORIZONTAL DIMENSIONS

Die size:	6.8 x 9.0 mm (267 x 354 mils)
Die area:	61 mm ² (94,518 mils ²)
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.1 x 0.1 mm (4 x 4 mils)
Min pad space:	0.1 mm (4 mils)
Min pad pitch:	0.2 mm (8.2 mils)
Min pad to metal:	40 microns
Min metal 2 width:	1.1 micron
Min metal 2 space:	1.2 micron
Min metal 2 pitch:	2.3 microns
Min via:	1.0 micron
Min via space:	1.3 micron
Min via pitch:	2.3 micron
Min metal 1 width:	0.6 micron
Min metal 1 space:	0.7 micron
Min metal 1 pitch:	1.3 micron
Min contact:	0.6 micron
Min contact space:	0.6 micron
Min contact pitch:	1.3 micron
Min polycide 4 width:	0.4 micron
Min polycide 4 space:	0.7 micron
Min polycide 4 pitch:	1.1 micron
Min poly 3 width:	0.9 micron
Min poly 3 space:	0.15 micron
Min poly 2 width:	0.8 micron
Min poly 2 space:	0.35 micron
Min poly 1 width - (cell):	0.3 micron
Min poly 1 space:	0.5 micron
Min poly 1 pitch:	0.8 micron
Min gate length* - (N-channel):	0.45 micron
- (P-channel):	0.65 micron
Cell size:	2.75 microns ²
Cell pitch:	1.1 x 2.5 microns

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness: 0.3 mm (11 mils)

Layers

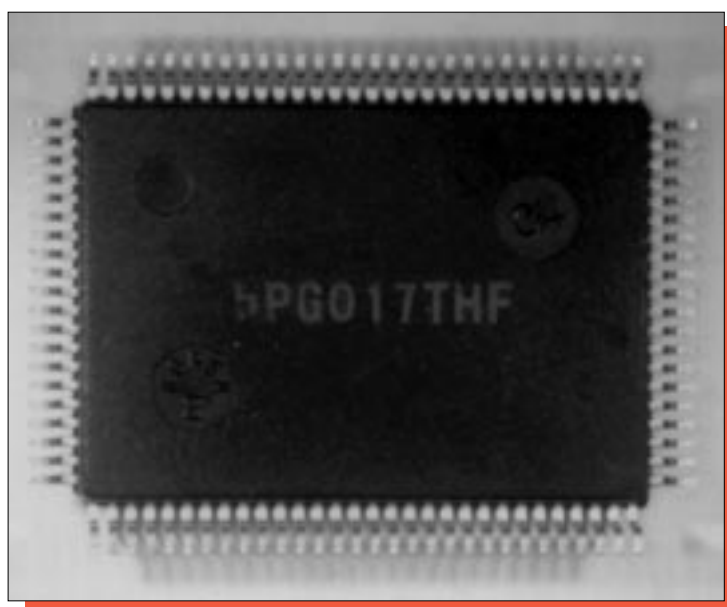
Passivation 2:	0.55 micron
Passivation 1:	0.15 micron
Metal 2 - aluminum:	0.8 micron
Intermetal dielectric - glass 3:	0.4 micron
- glass 2 (SOG):	0 - 0.7 micron
- glass 1:	0.45 micron
Metal 1- cap:	0.05 micron (approximate)
- aluminum:	0.6 micron
- barrier:	0.1 micron
Reflow glass:	0.6 micron
Polycide 4:	0.25 micron
Poly 3 (sheet):	0.1 micron (approximate)
Poly 2 - 2nd layer:	0.06 micron
- 1st layer:	0.15 micron
Poly 1:	0.15 micron
Local oxide:	0.35 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.25 micron
N-well:	2 microns

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GENERAL CIRCUIT LAYOUT	Figures 42 - 42b
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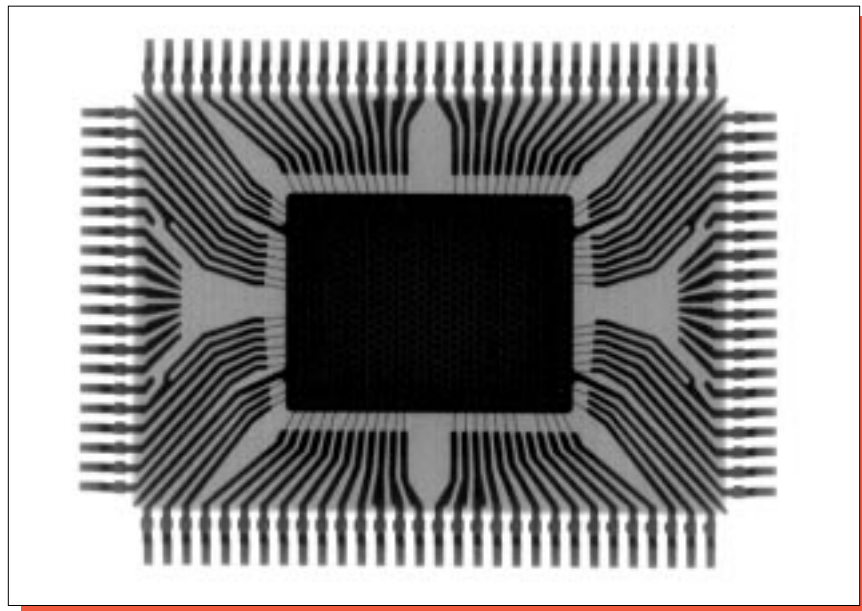


top view



bottom view

Figure 1. Package photographs of the Samsung KM4132G271Q-10 8M Synchronous Graphic RAM. Mag. 3.8x.

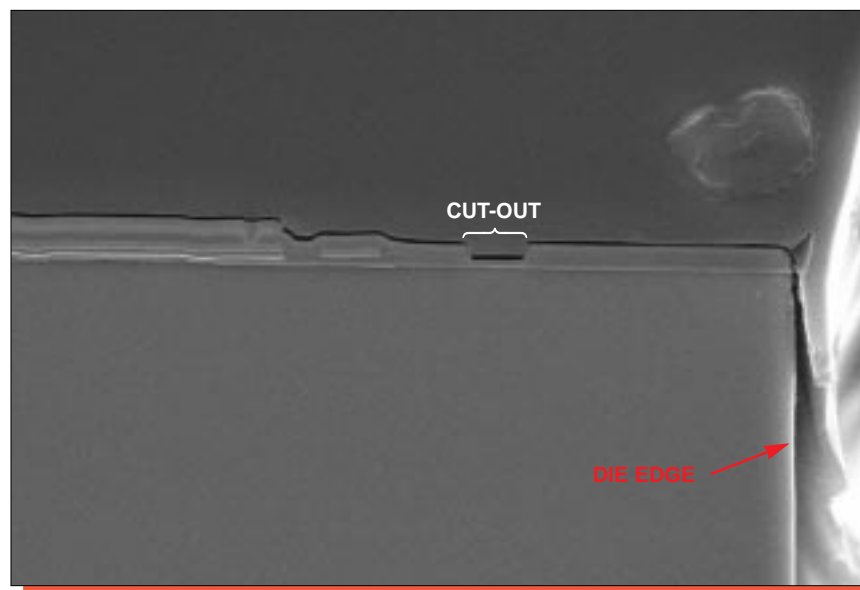


top

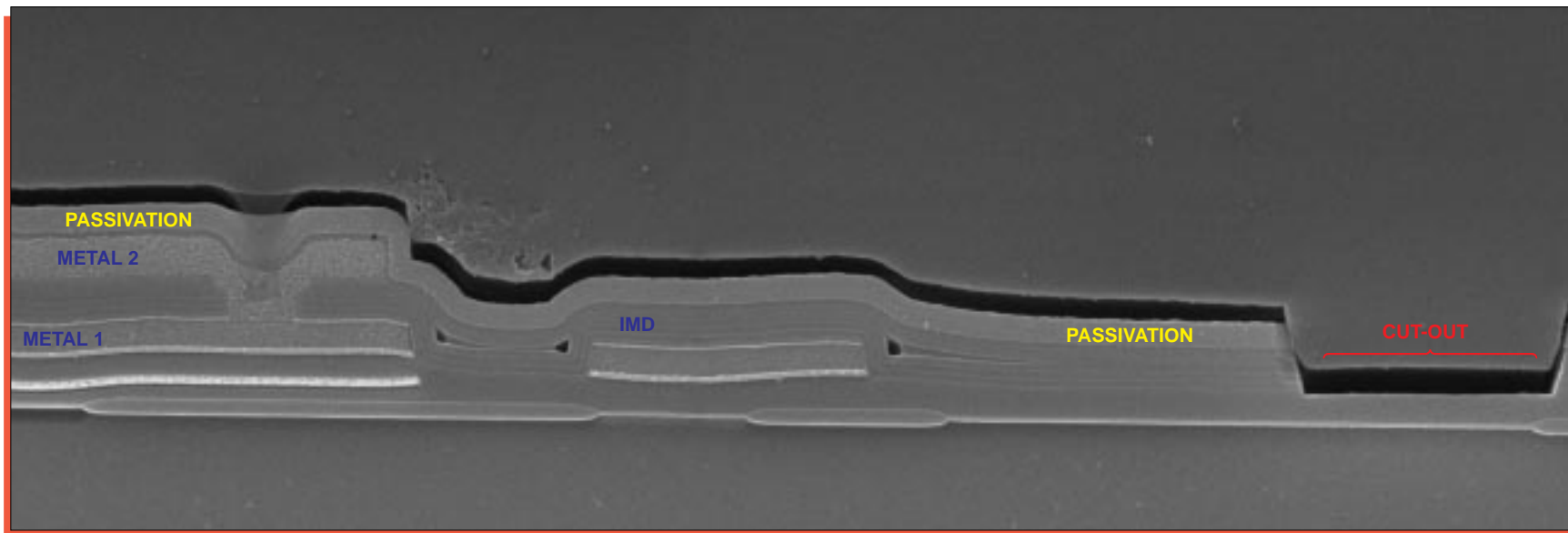


side

Figure 2. X-ray views of the package. Mag. 4x.



Mag. 1300x



Mag. 6000x

Figure 3. SEM section views of the edge seal.

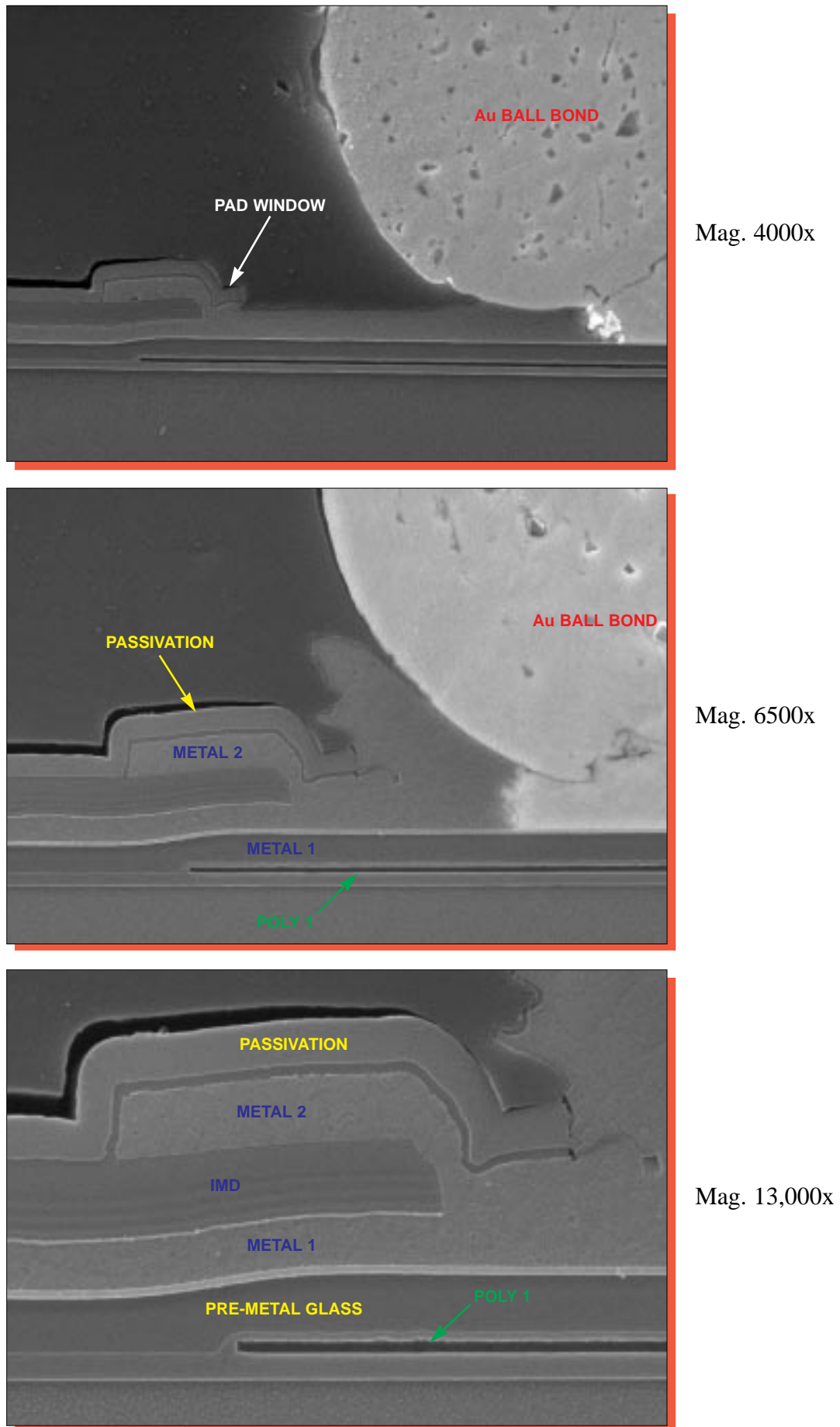


Figure 4. SEM section views of the bond pad structure.

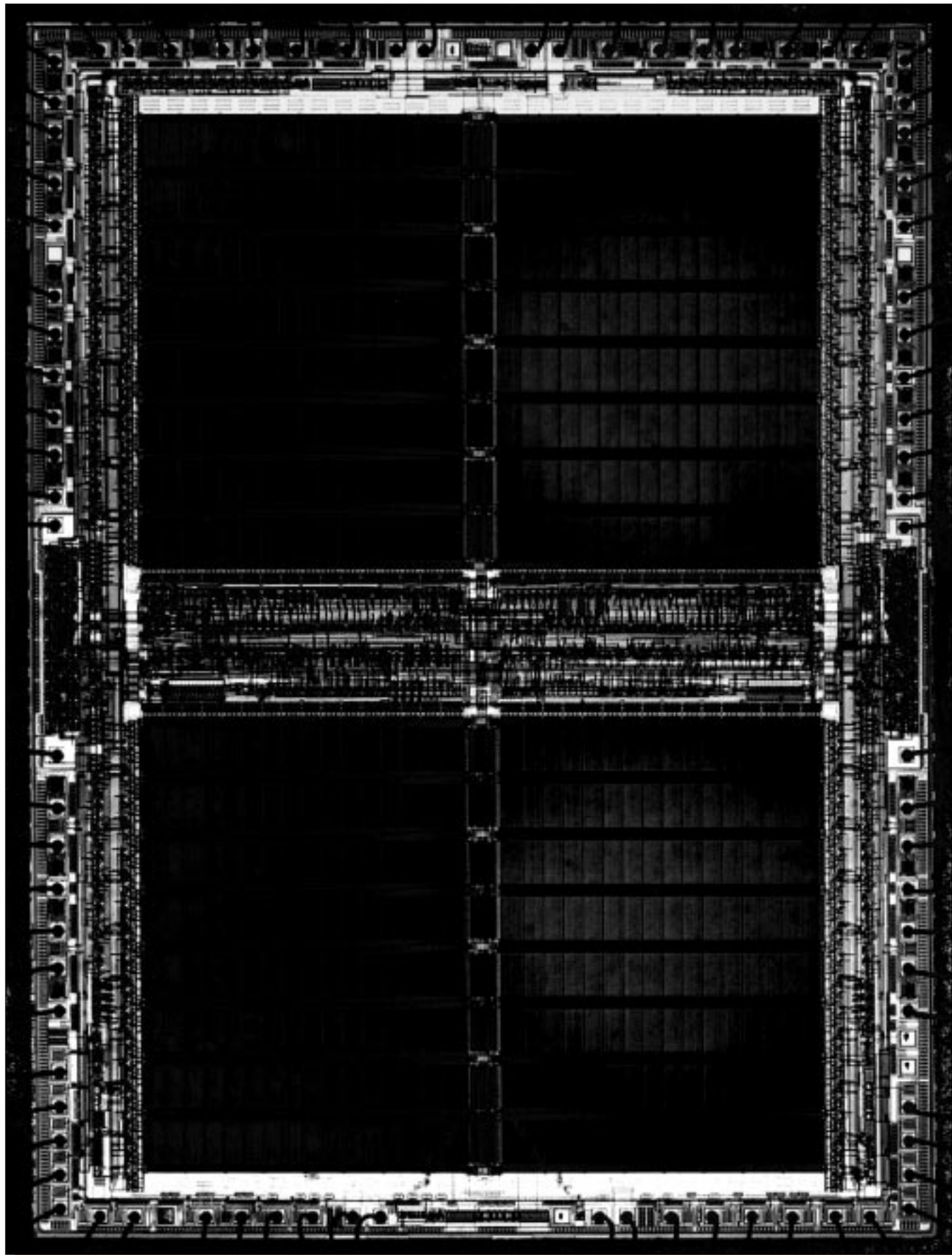


Figure 5. Whole die photograph of the Samsung KM4132G271Q-10 8M Synchronous Graphic RAM. Mag. 26x.

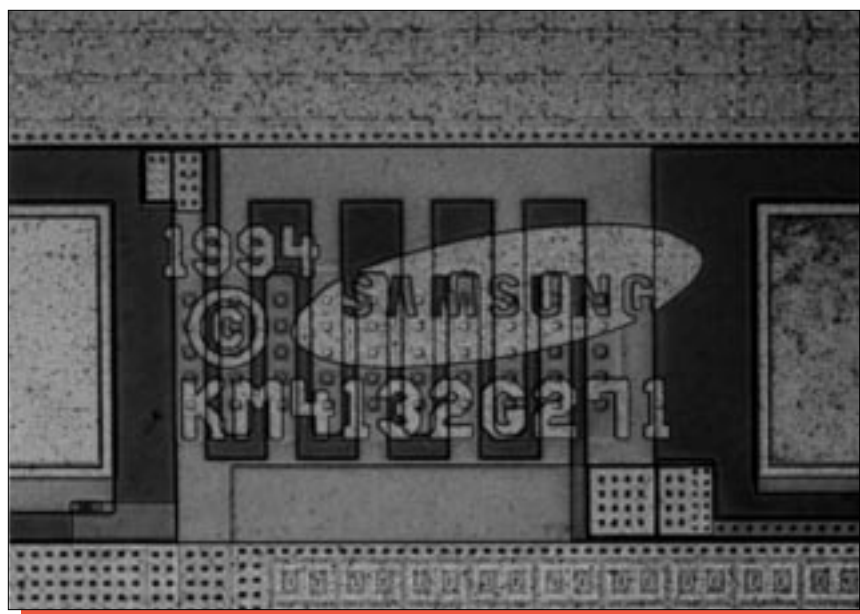


Figure 6. Optical view of the die markings from the surface. Mag. 320x.

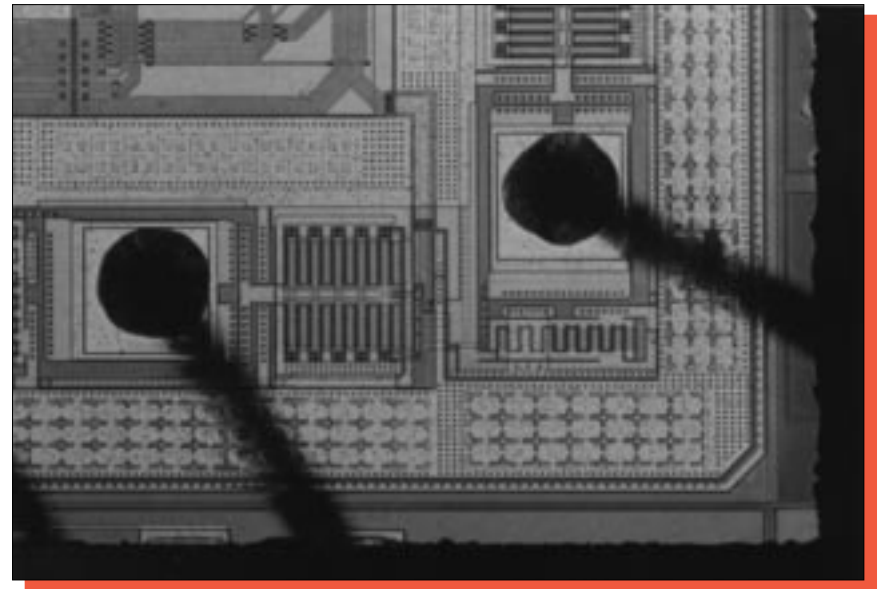
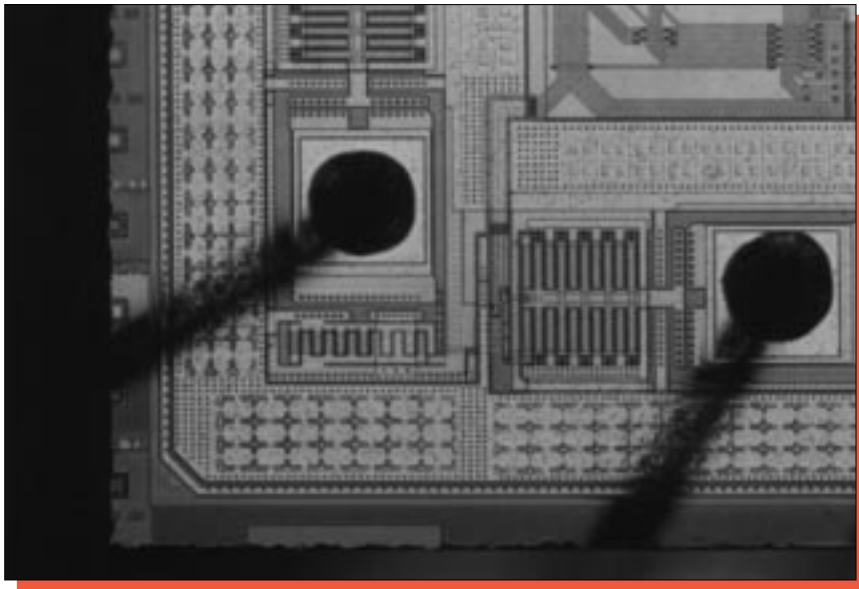
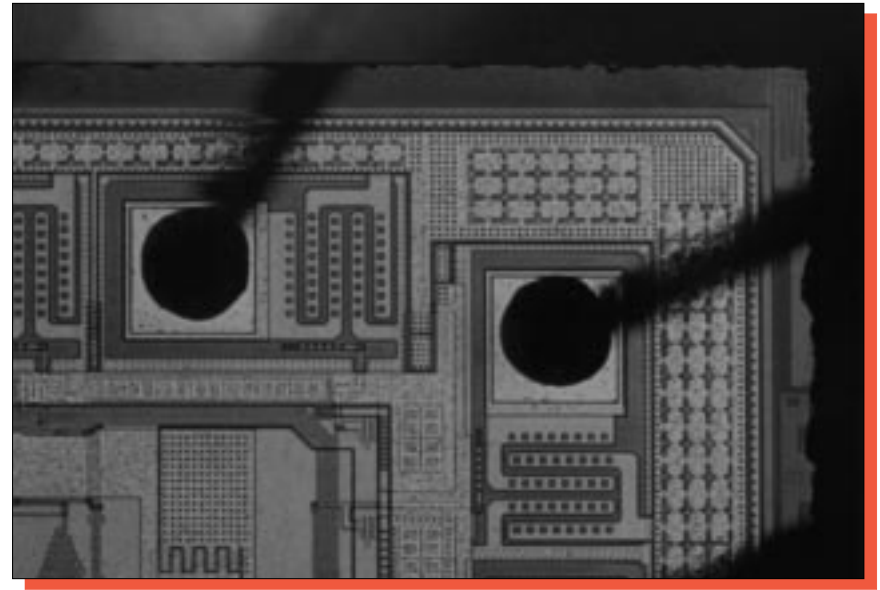
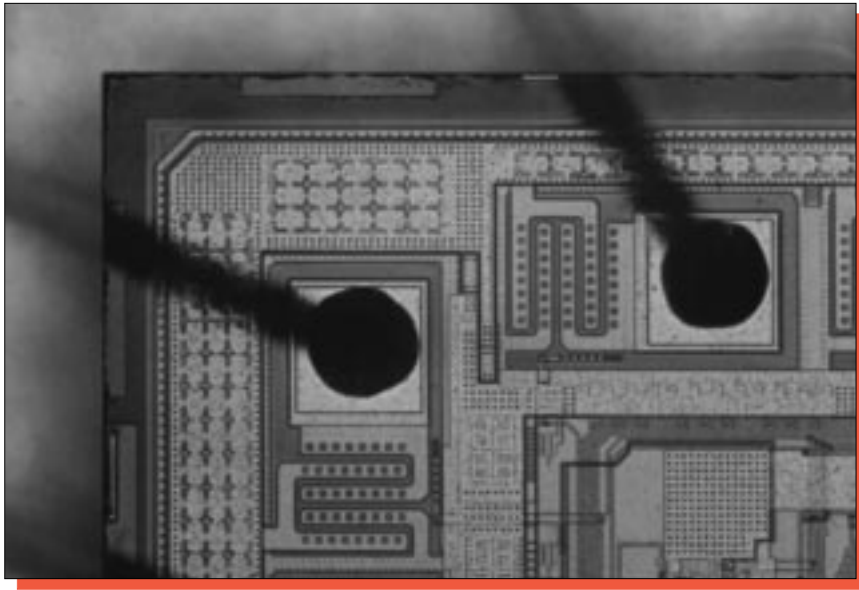


Figure 7. Optical views of the die corners on the Samsung KM4132G271Q-10. Mag. 160x.

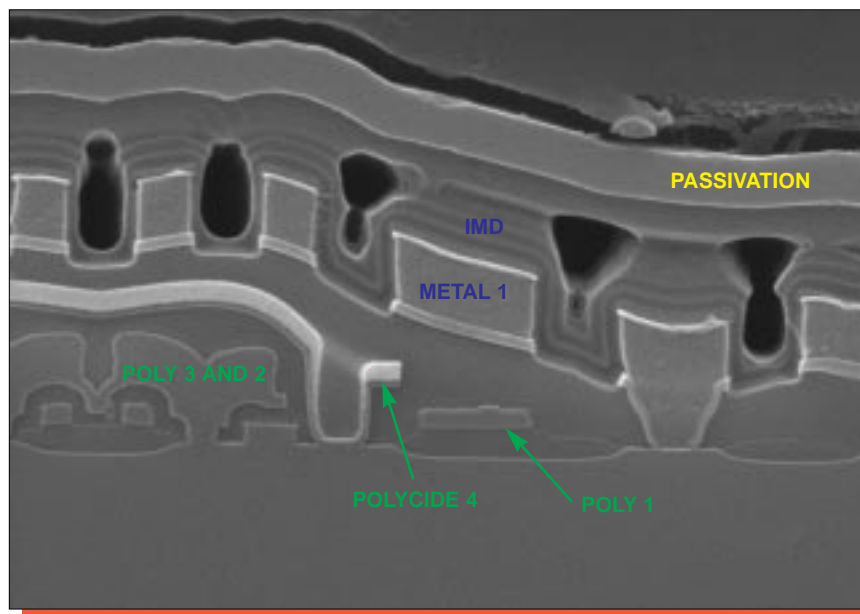
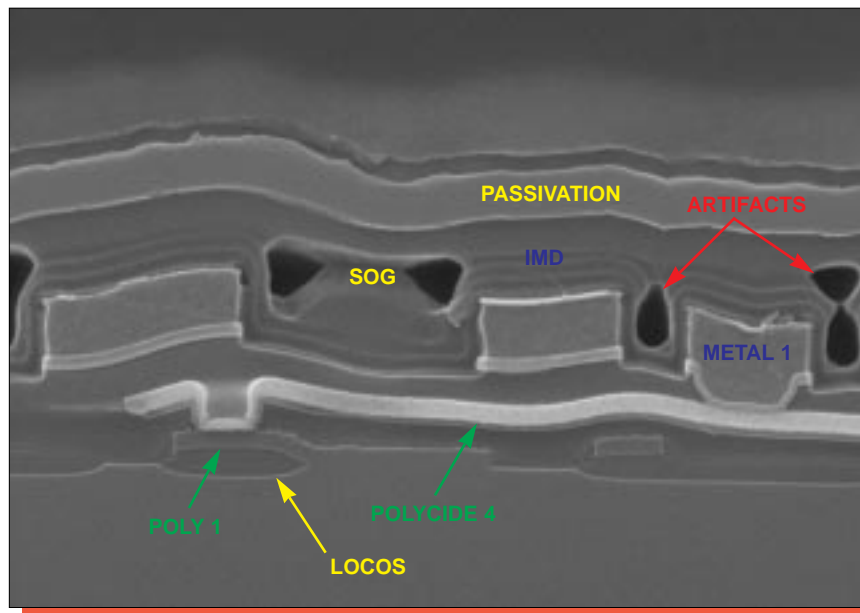
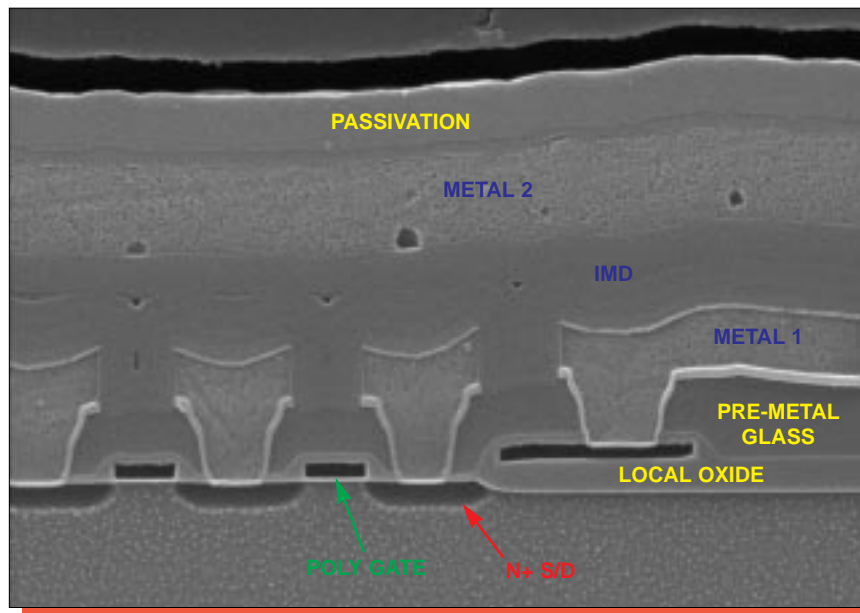
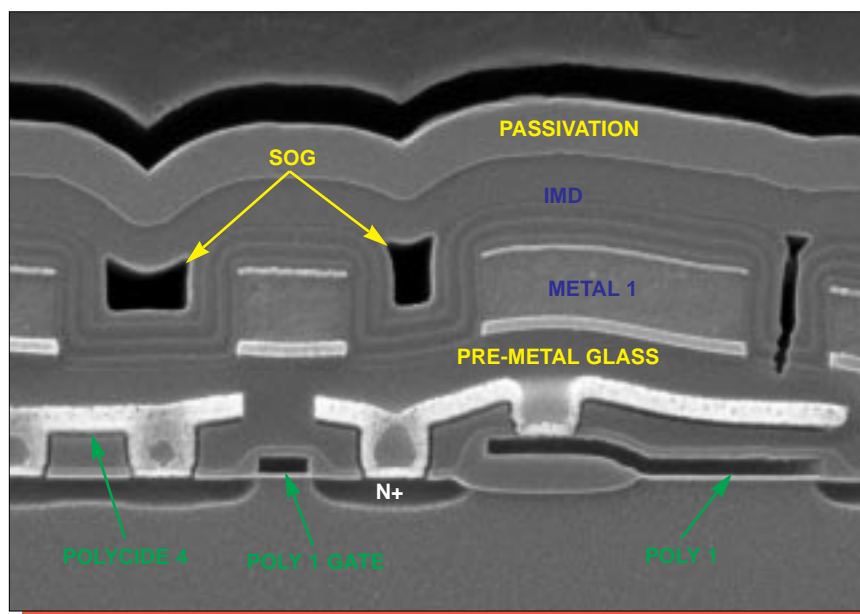


Figure 8. SEM section views of general construction. Glass-etch. Mag. 13,000x.

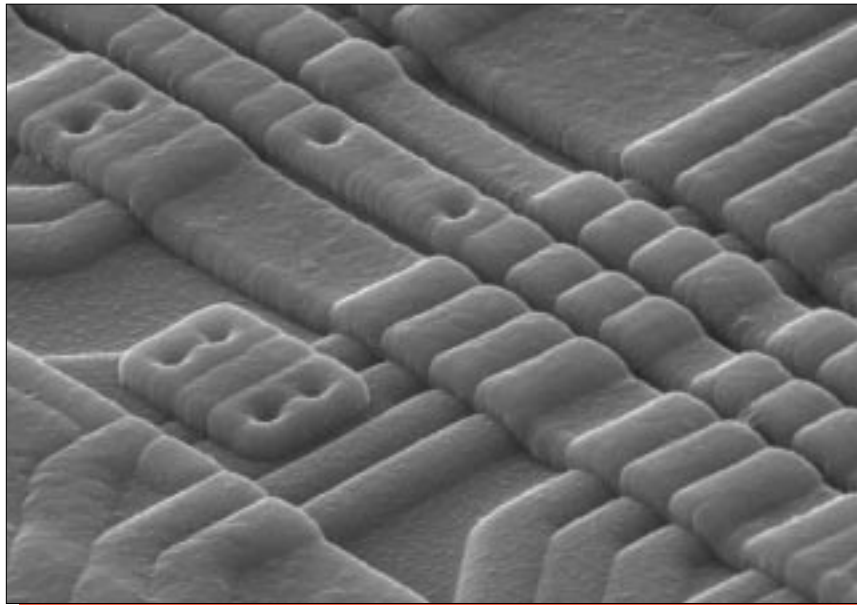


Mag. 13,000x

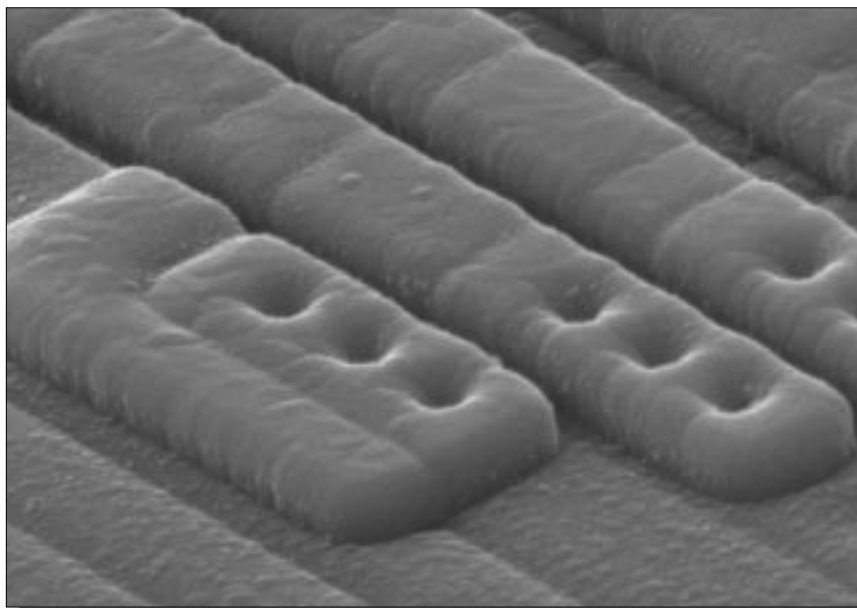


Mag. 15,000x

Figure 9. SEM section views of general construction. Silicon-etch.

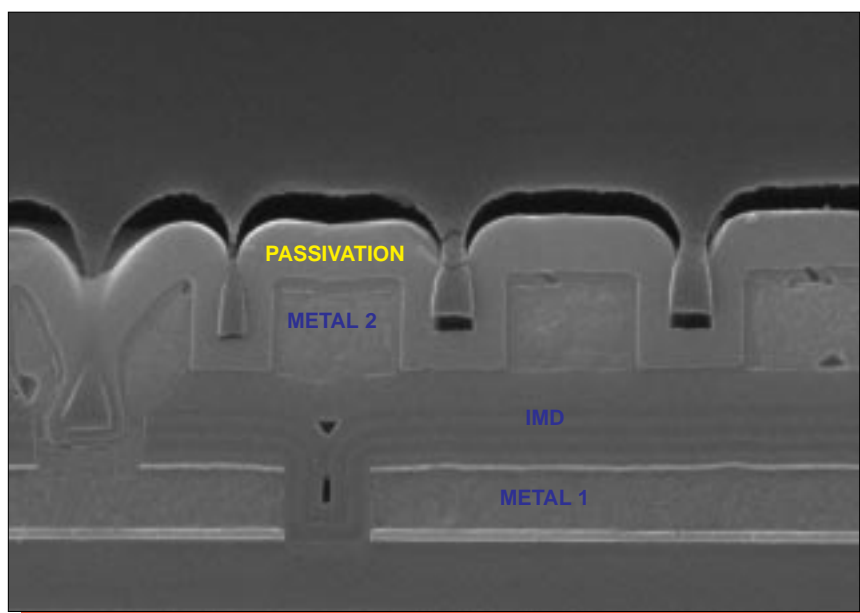


Mag. 4000x

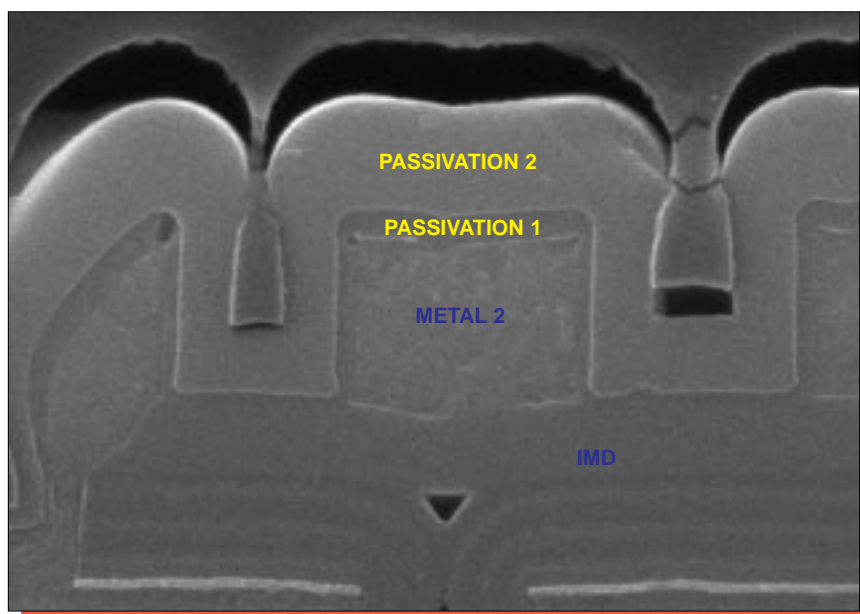


Mag. 8000x

Figure 10. SEM views of overlay passivation coverage. 60°.

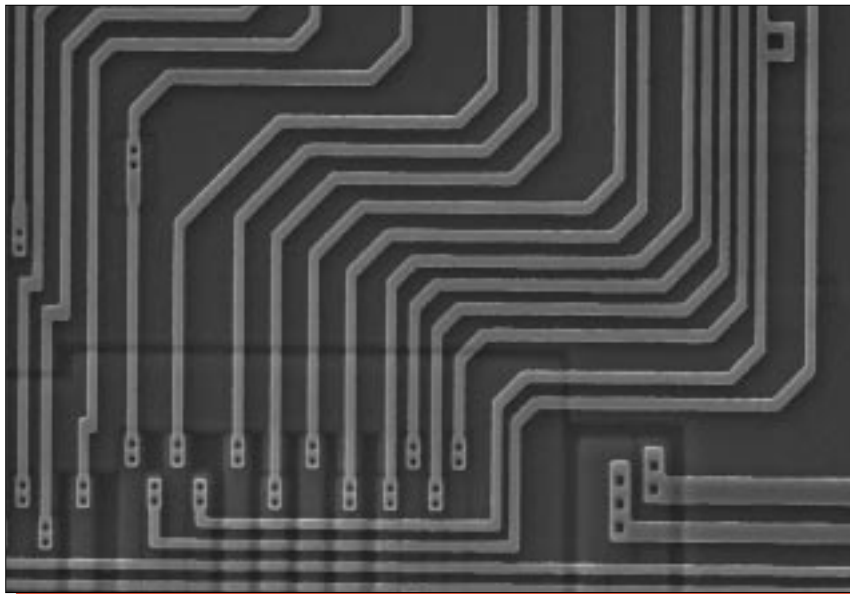


Mag. 13,000x

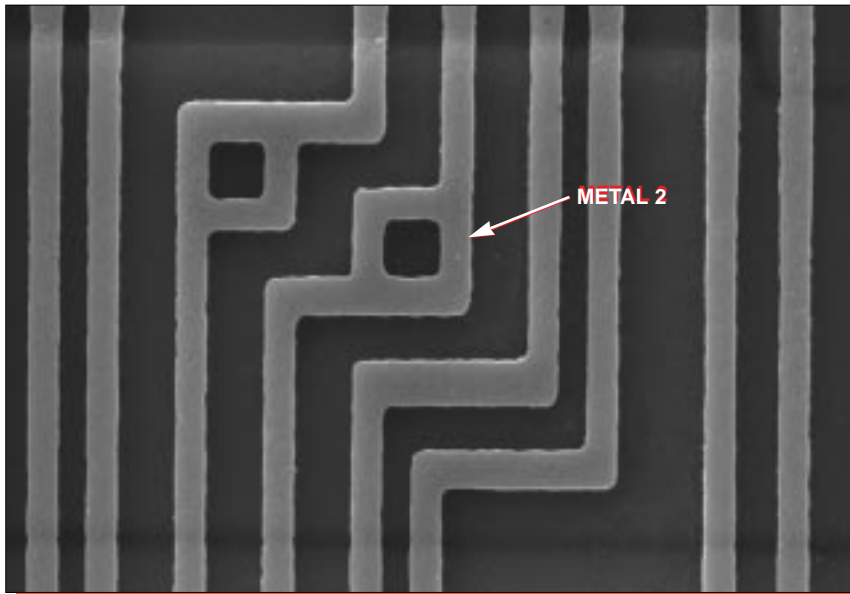


Mag. 26,000

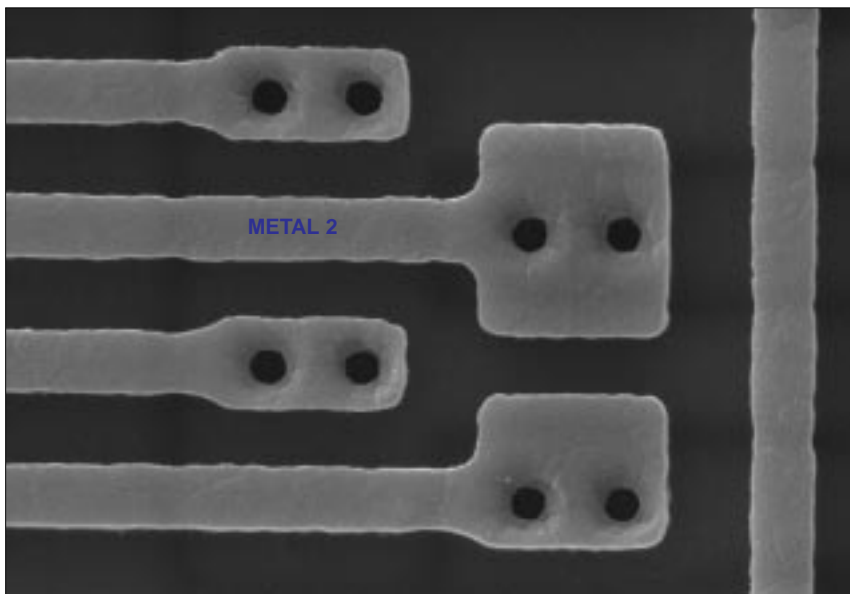
Figure 11. SEM section views of metal 2 line profiles.



Mag. 1000x

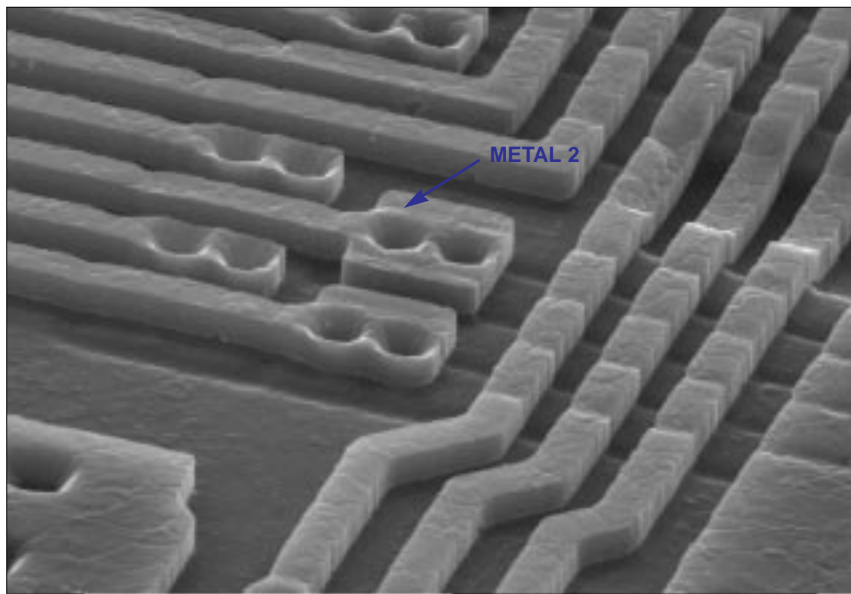


Mag. 3300x

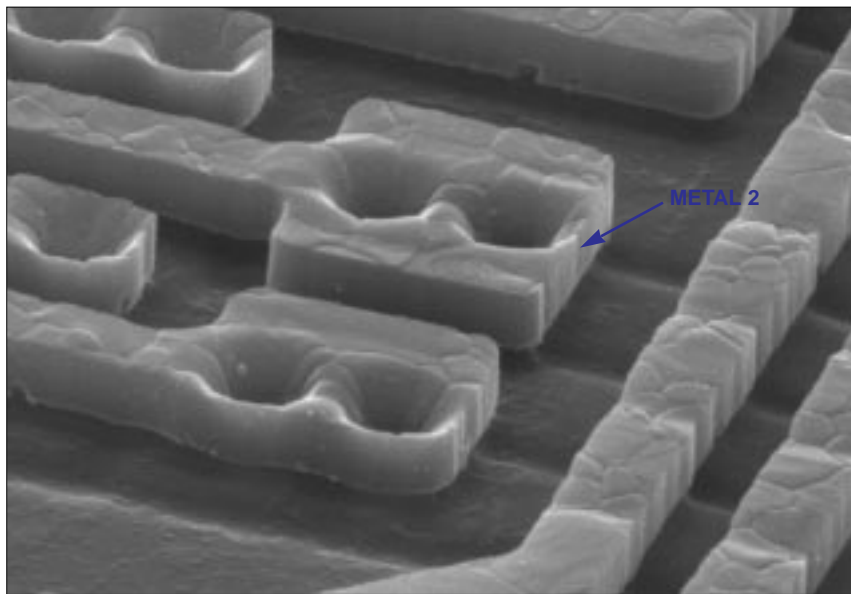


Mag. 6500x

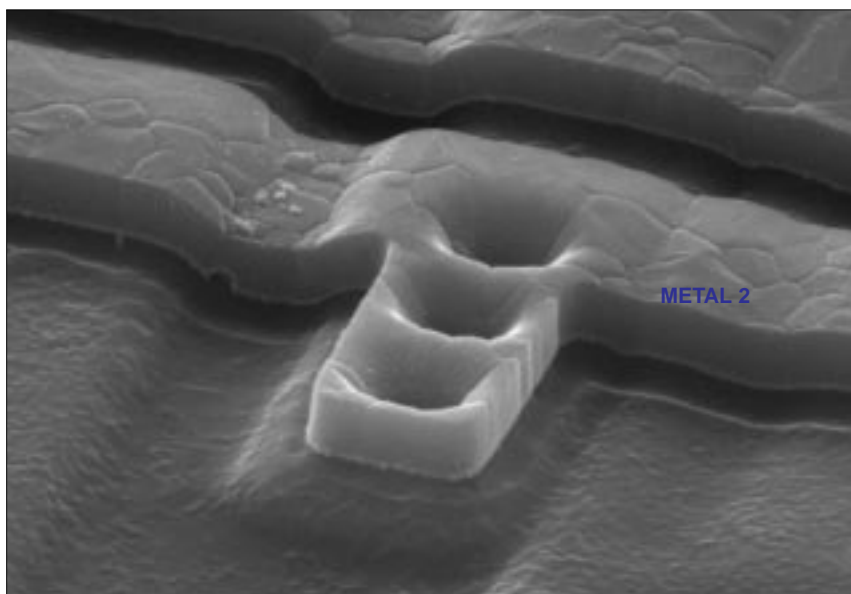
Figure 12. Topological SEM views of metal 2 patterning. 0°.



Mag. 5000x

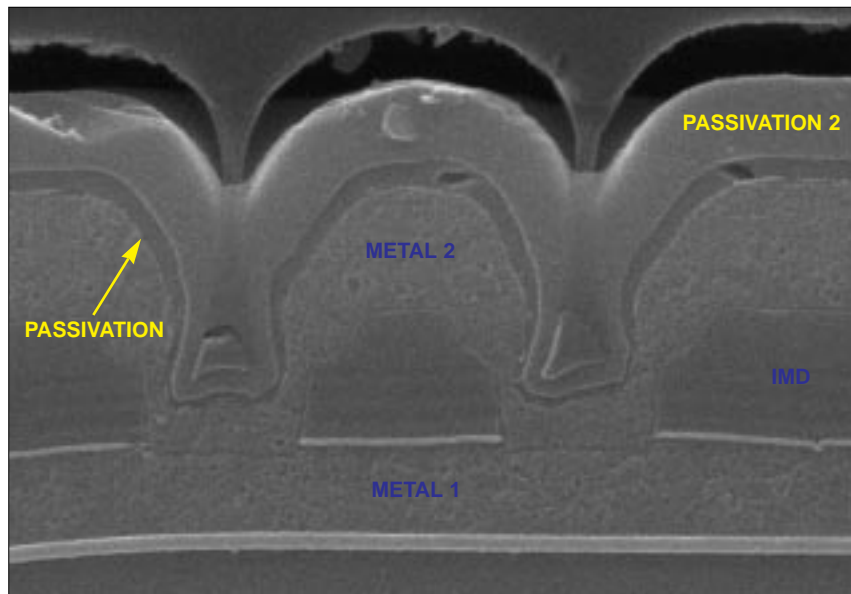


Mag. 10,000x

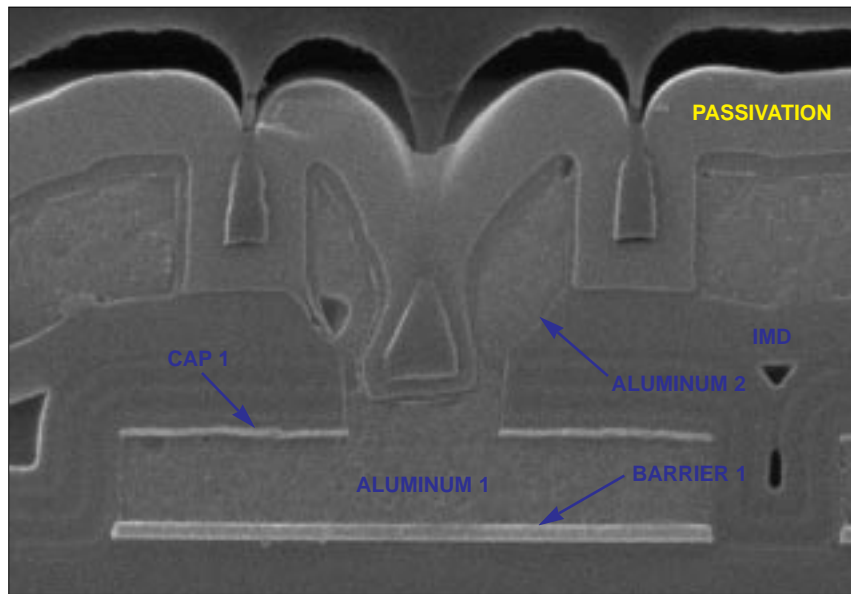


Mag. 10,000x

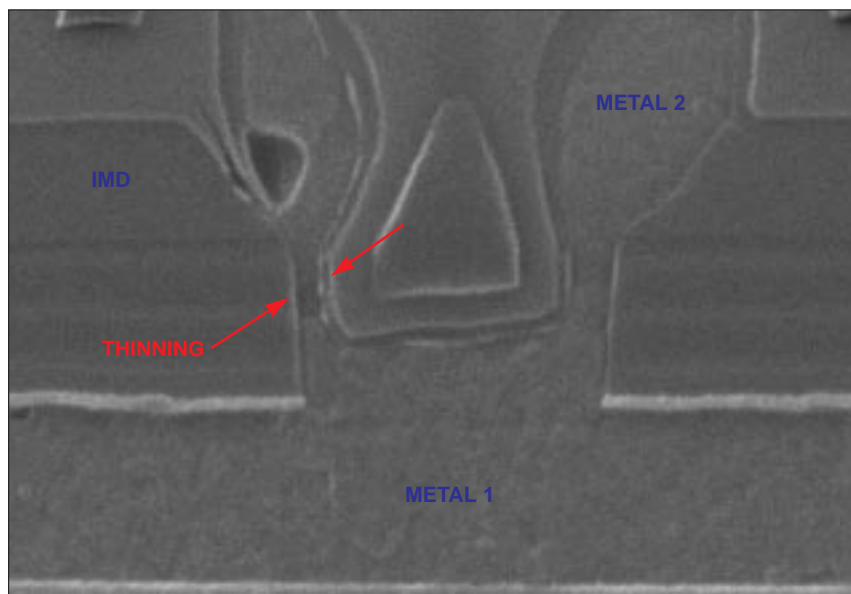
Figure 13. Perspective SEM views of metal 2 coverage. 60°.



Mag. 20,000x

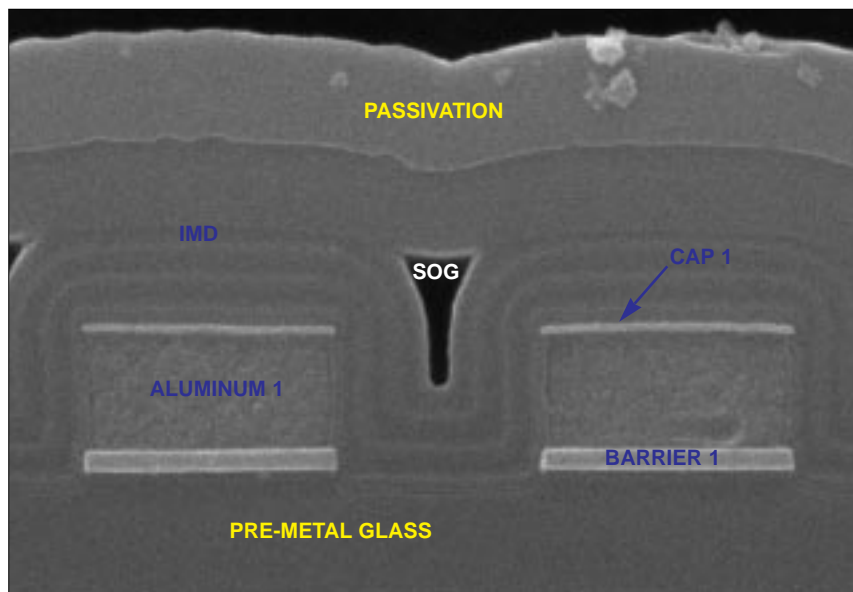


Mag. 20,000x

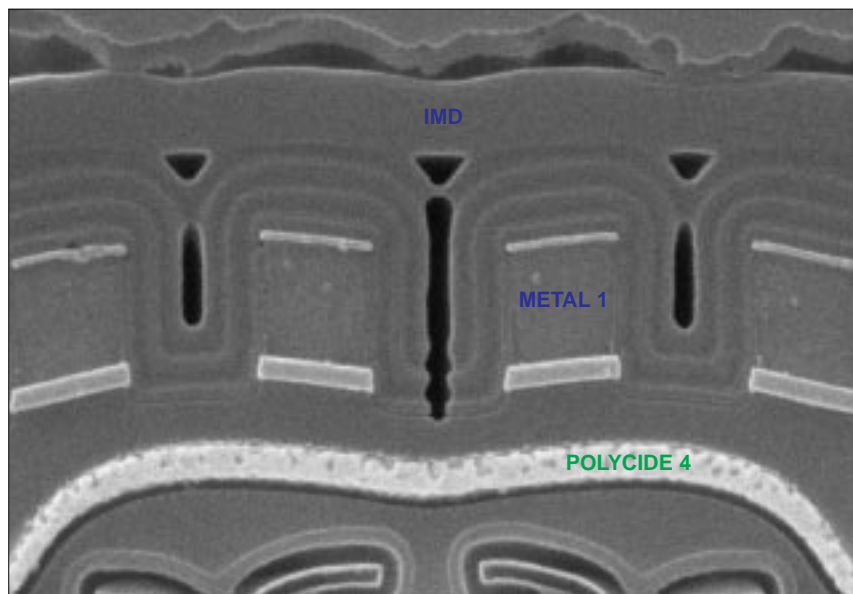


Mag. 40,000x

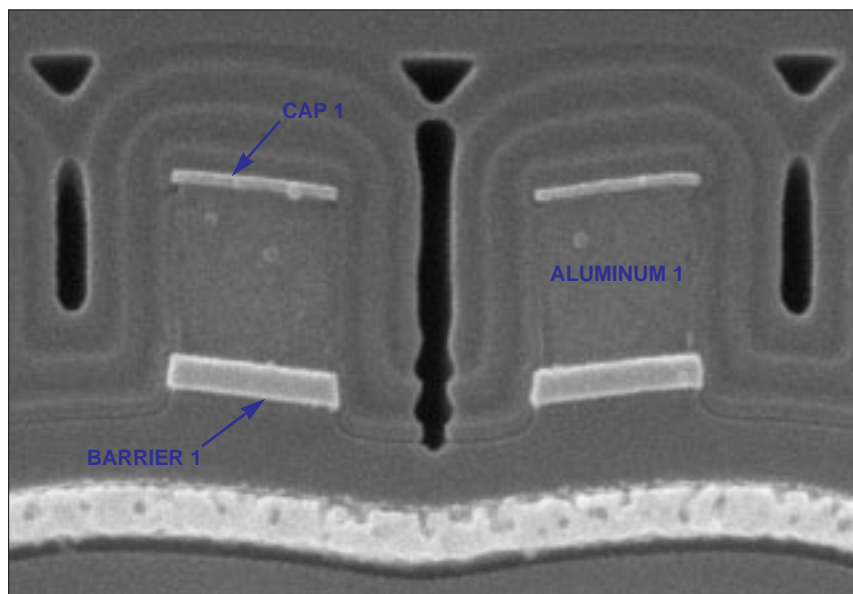
Figure 14. SEM section views of metal 2-to-metal 1 vias.



Mag. 26,000x

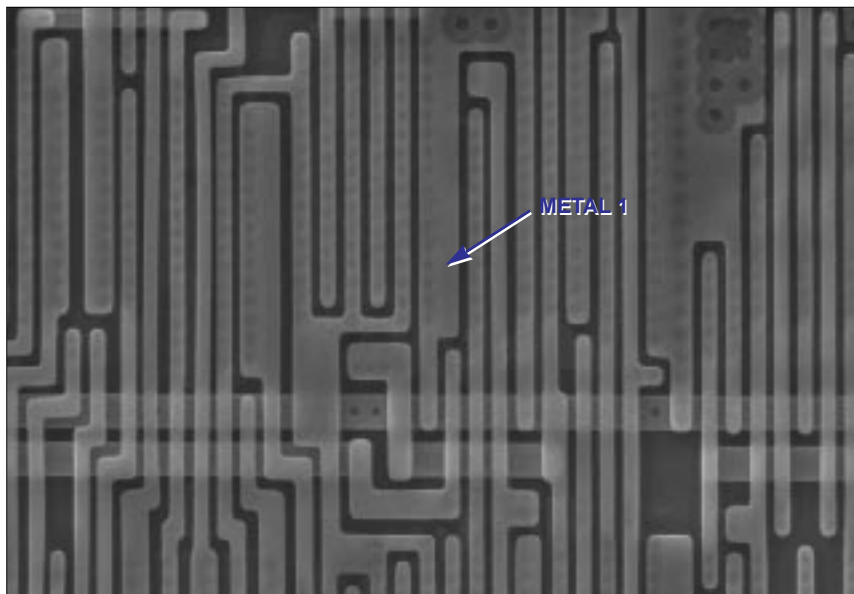


Mag. 26,000x

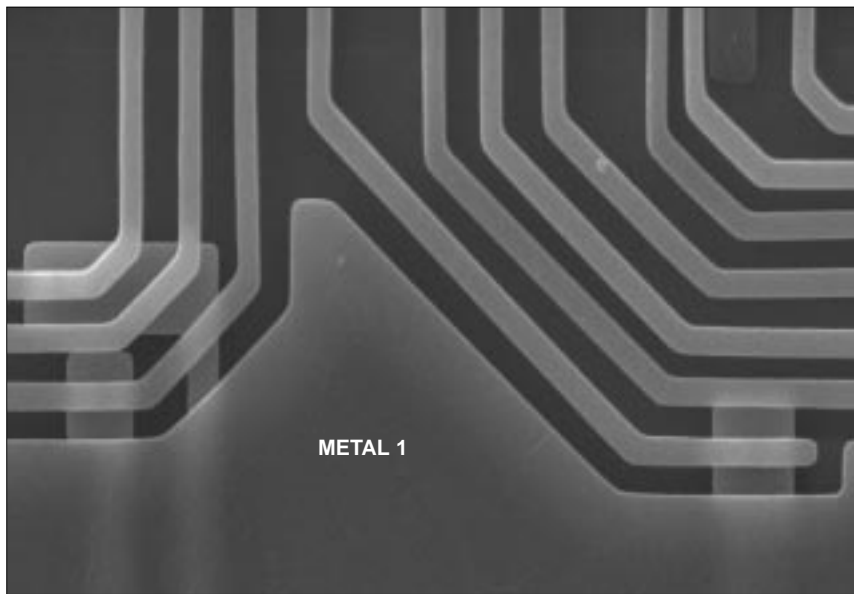


Mag. 40,000x

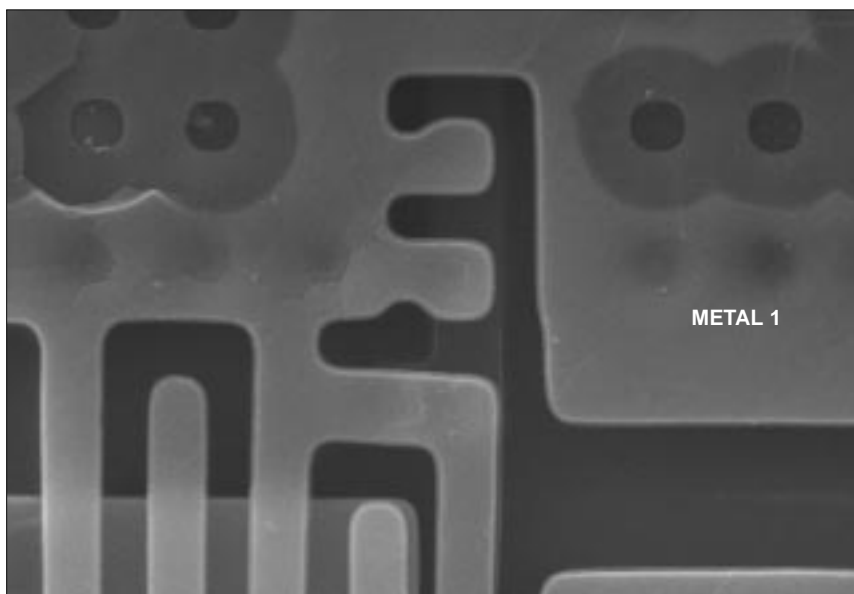
Figure 15. SEM section views of metal 1 line profiles.



Mag. 1600x

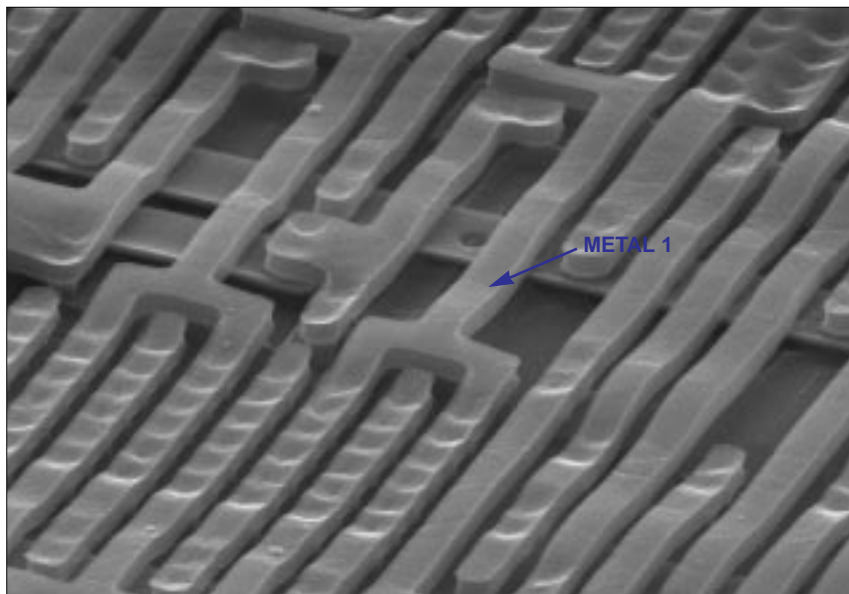


Mag. 3000x

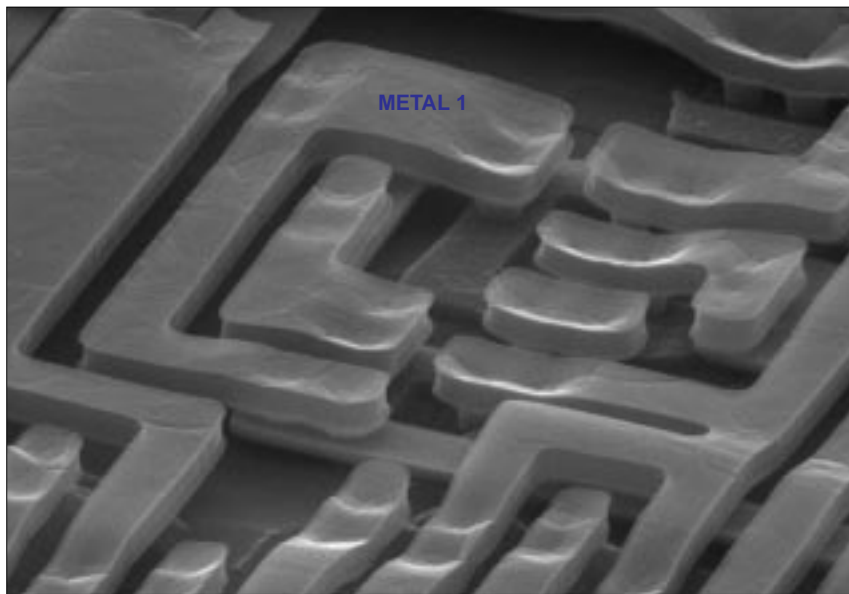


Mag. 6500x

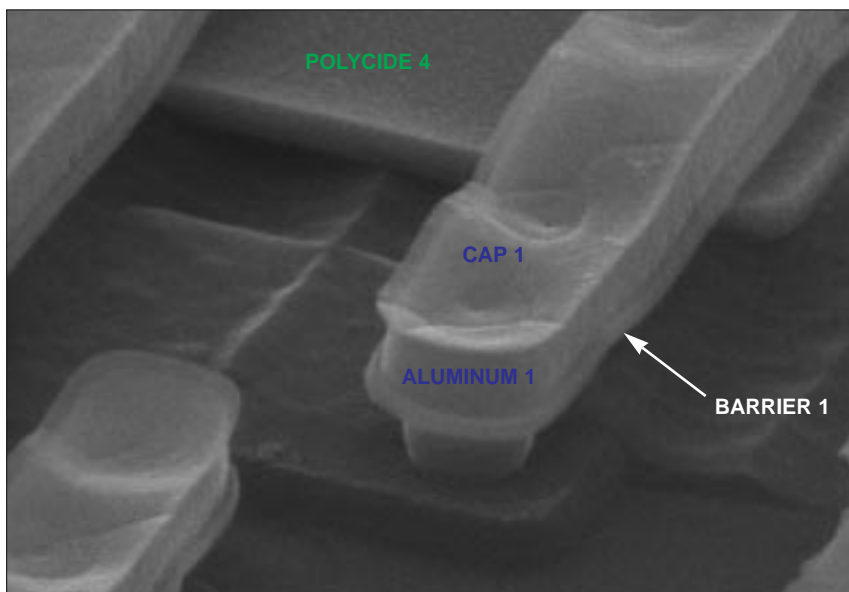
Figure 16. Topological SEM views of metal 1 patterning. 0°.



Mag. 5000x

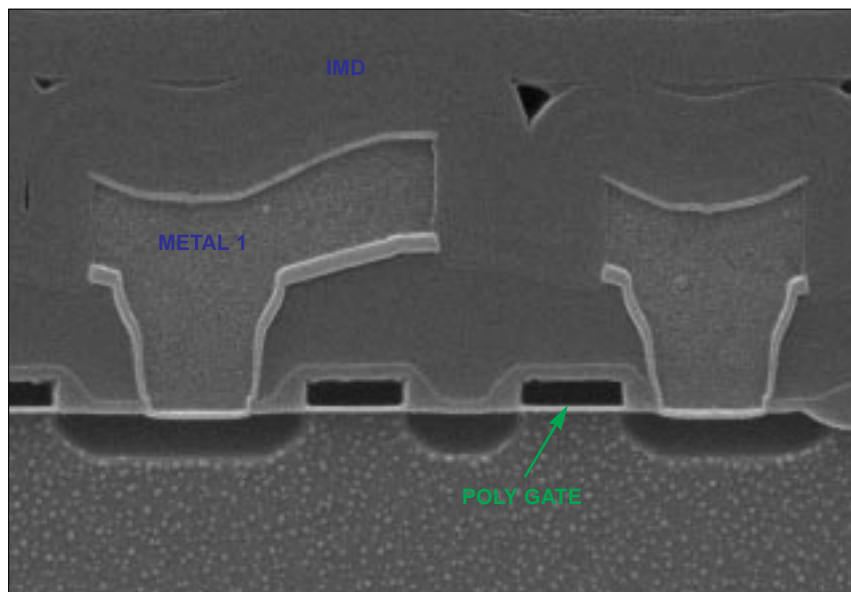


Mag. 7000x



Mag. 20,000x

Figure 17. Perspective SEM views of metal 1 coverage. 60°.



Mag. 24,000x

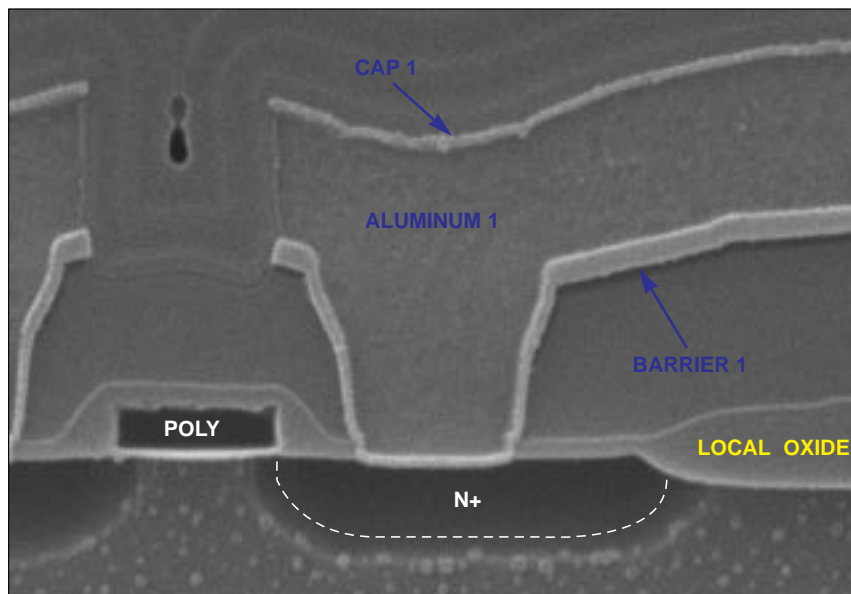
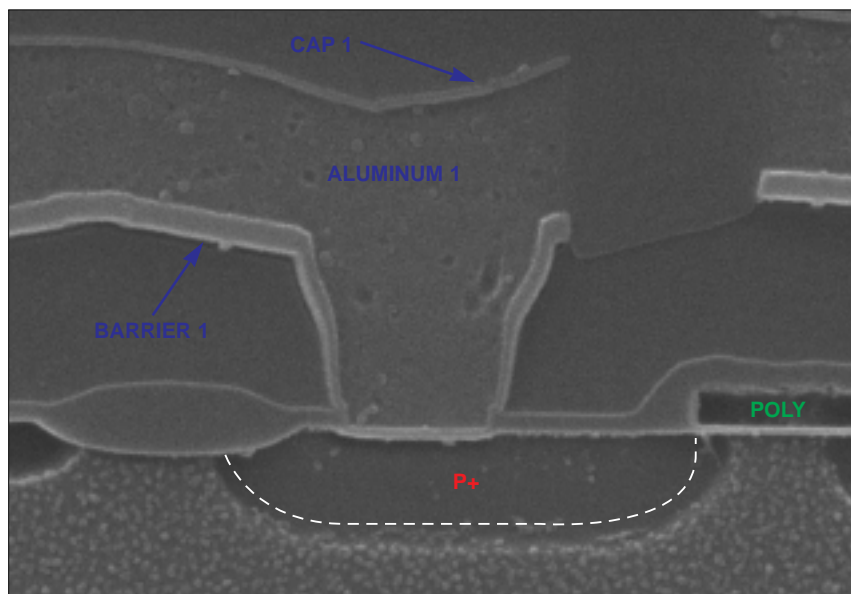
metal 1-to-N+,
Mag. 35,000xmetal-to-P+,
Mag. 35,000x

Figure 18. SEM section views of typical metal 1 contacts-to-diffusion.

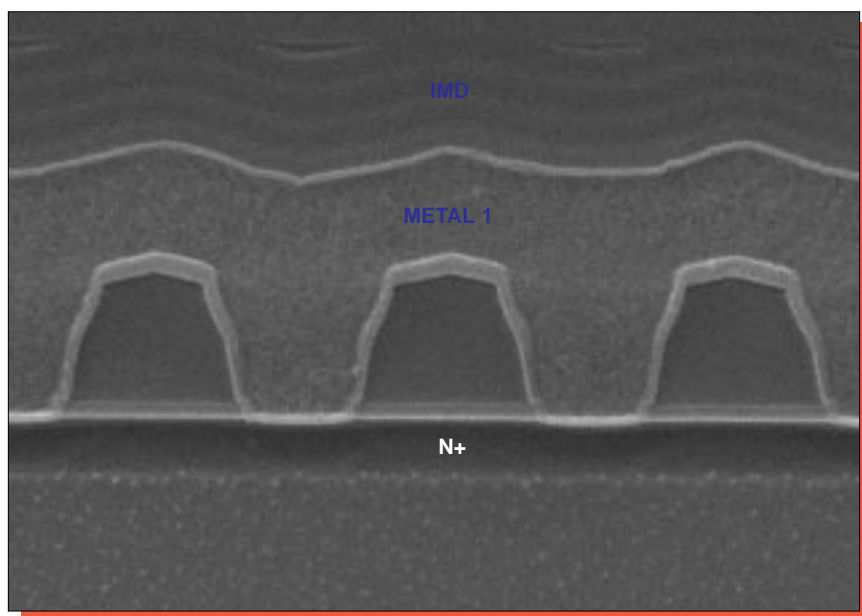
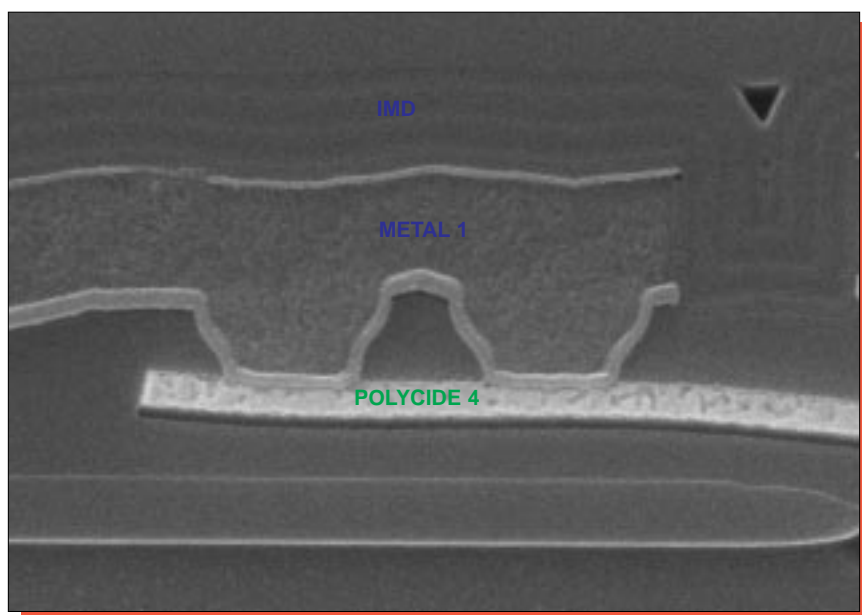
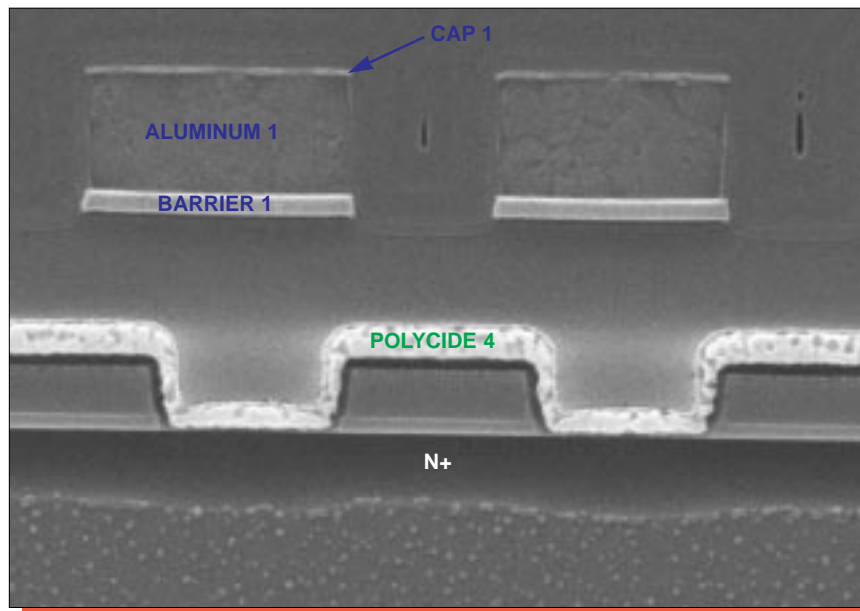
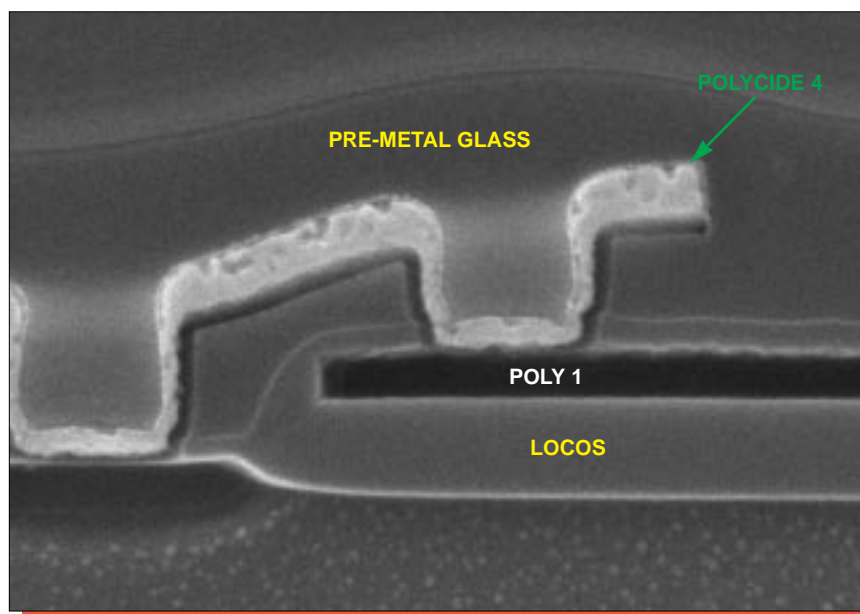


Figure 18a. SEM section views of metal 1 contact spacing. Mag. 26,000x.

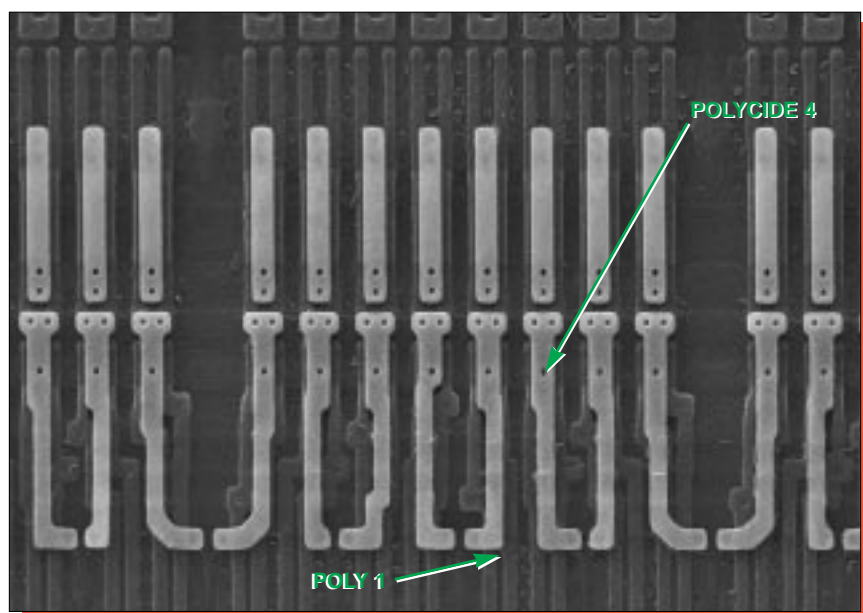


Mag. 26,000x

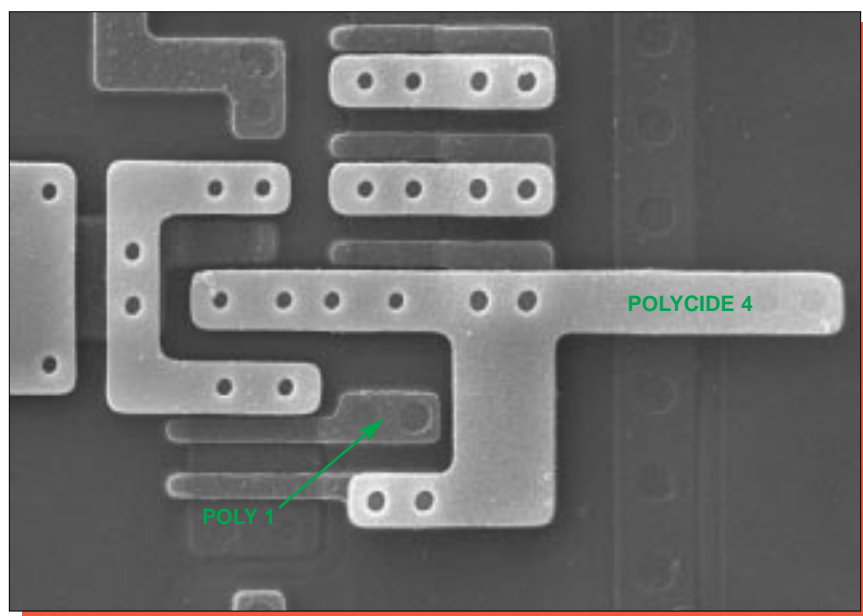


Mag. 40,000x

Figure 18b. SEM section views of polycide contact spacing.

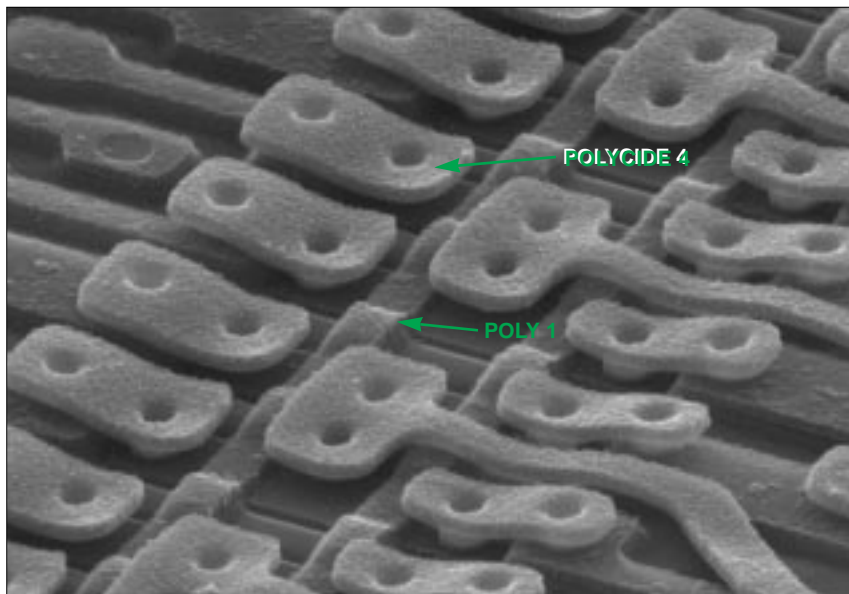


Mag. 2000x

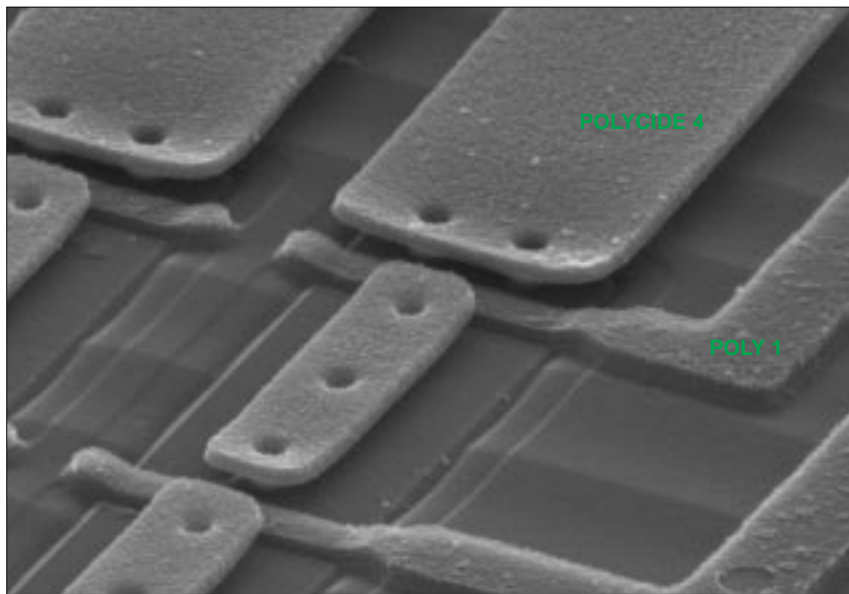


Mag. 5000x

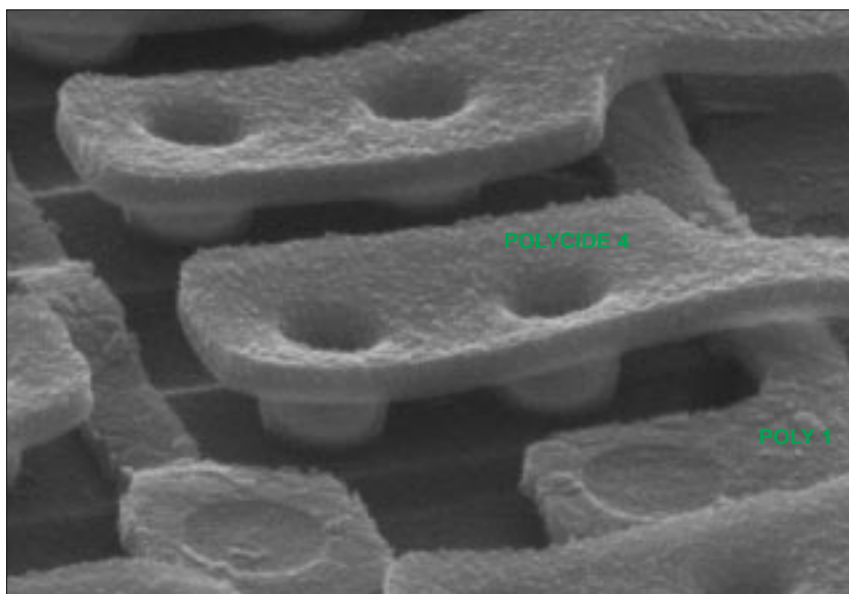
Figure 19. Topological SEM views of polycide 4 patterning. 0°.



Mag. 10,000x

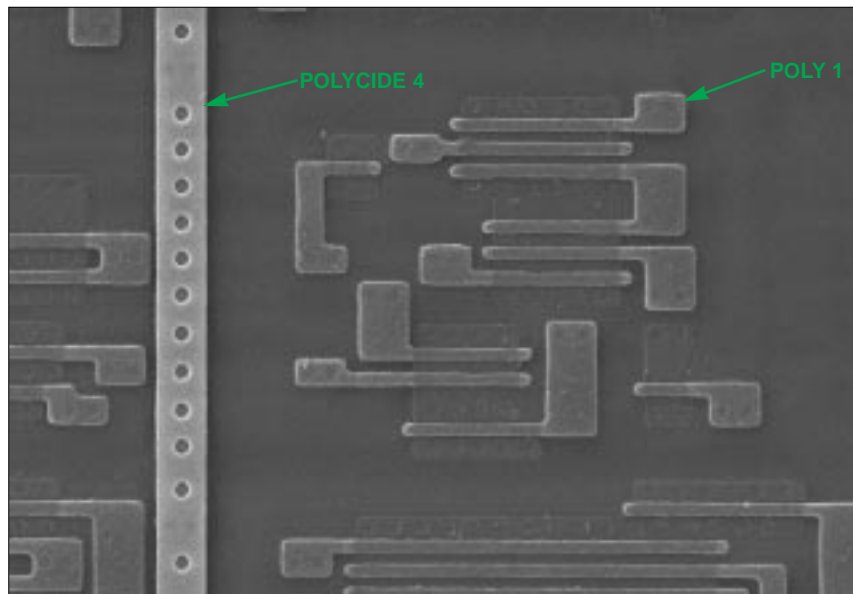


Mag. 10,000x

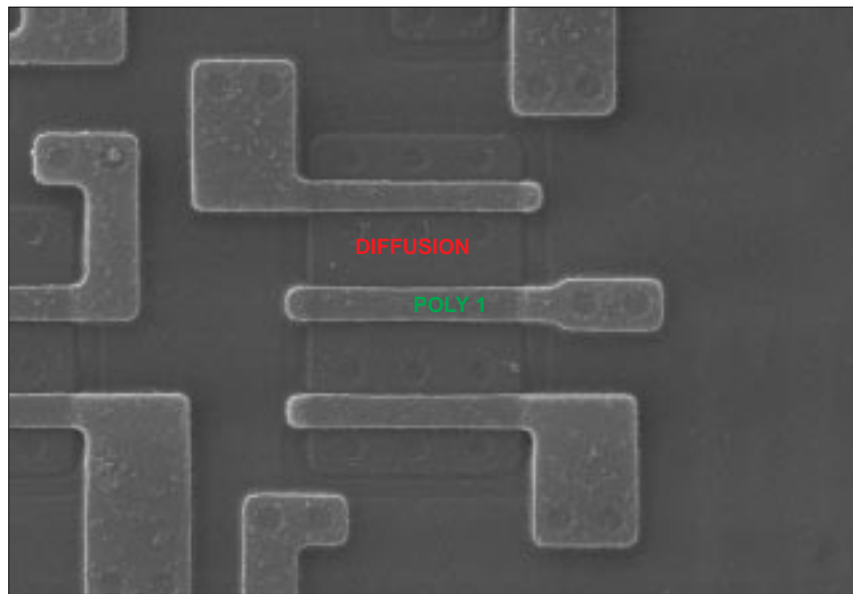


Mag. 26,000x

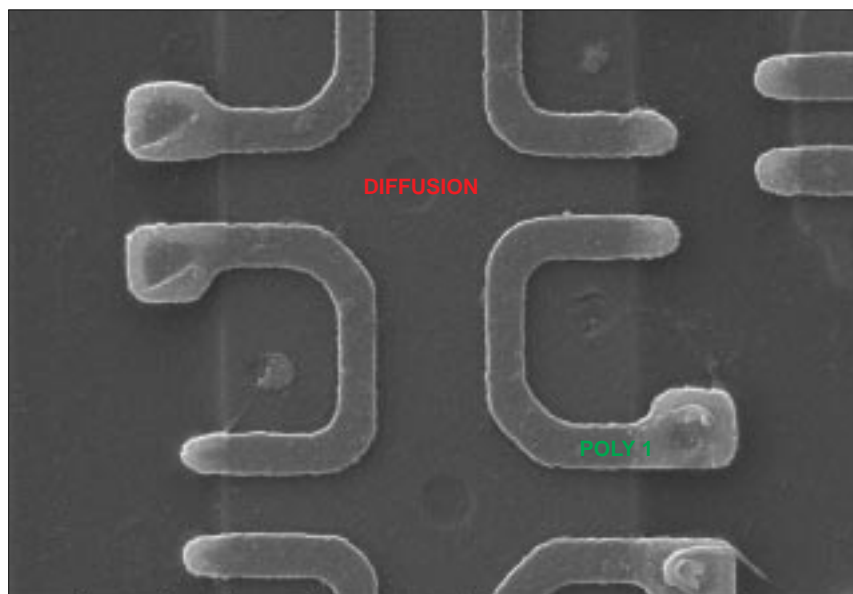
Figure 20. Perspective SEM views of polycide 4 coverage. 60°.



Mag. 2500x

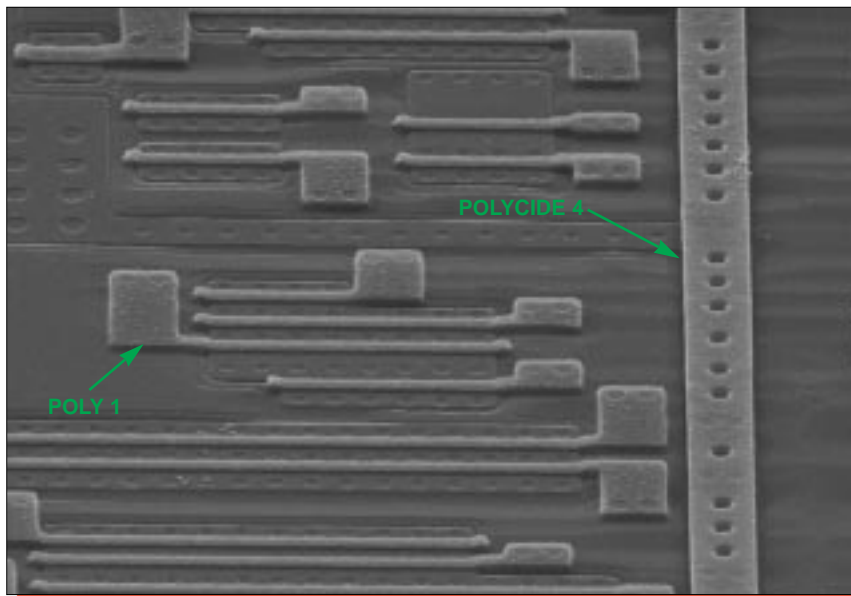


Mag. 5000x

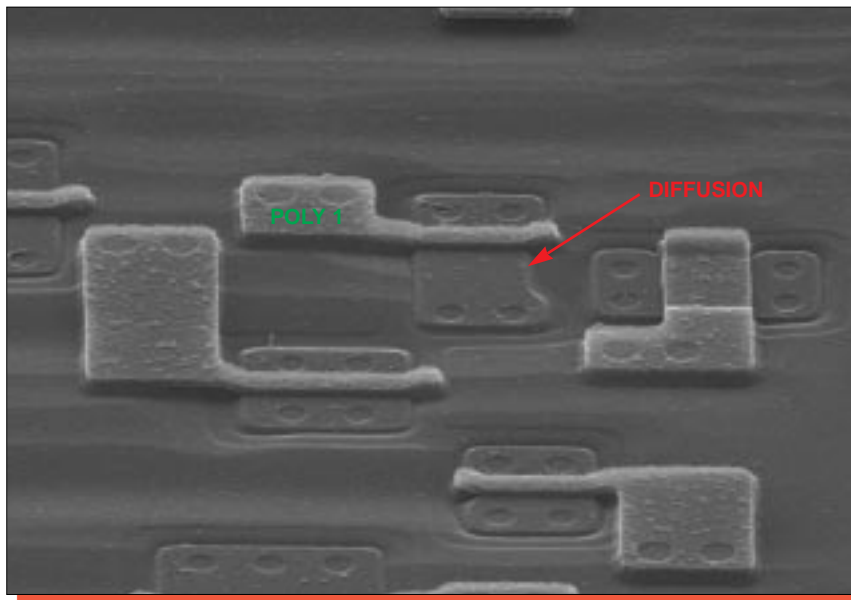


Mag. 10,000x

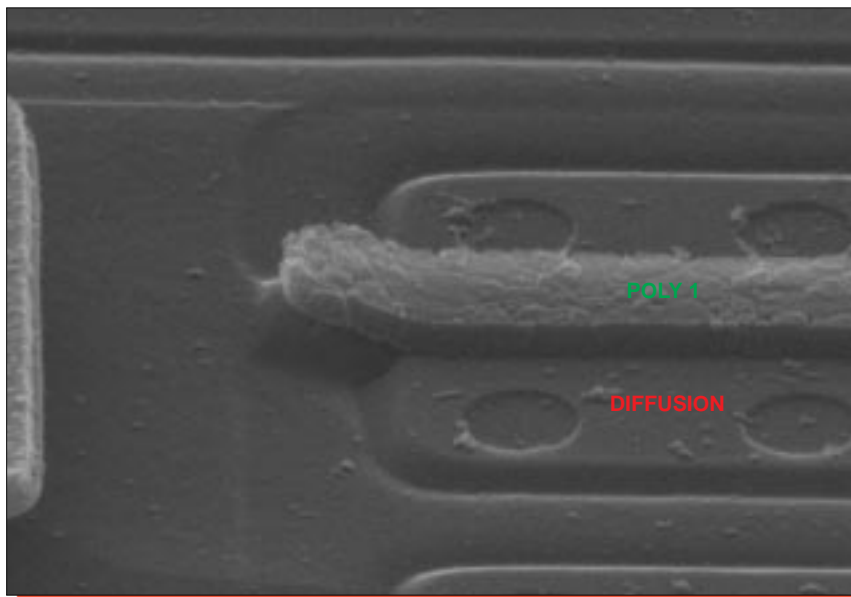
Figure 21. Topological SEM views of poly 1 patterning. 0°.



Mag. 3300x

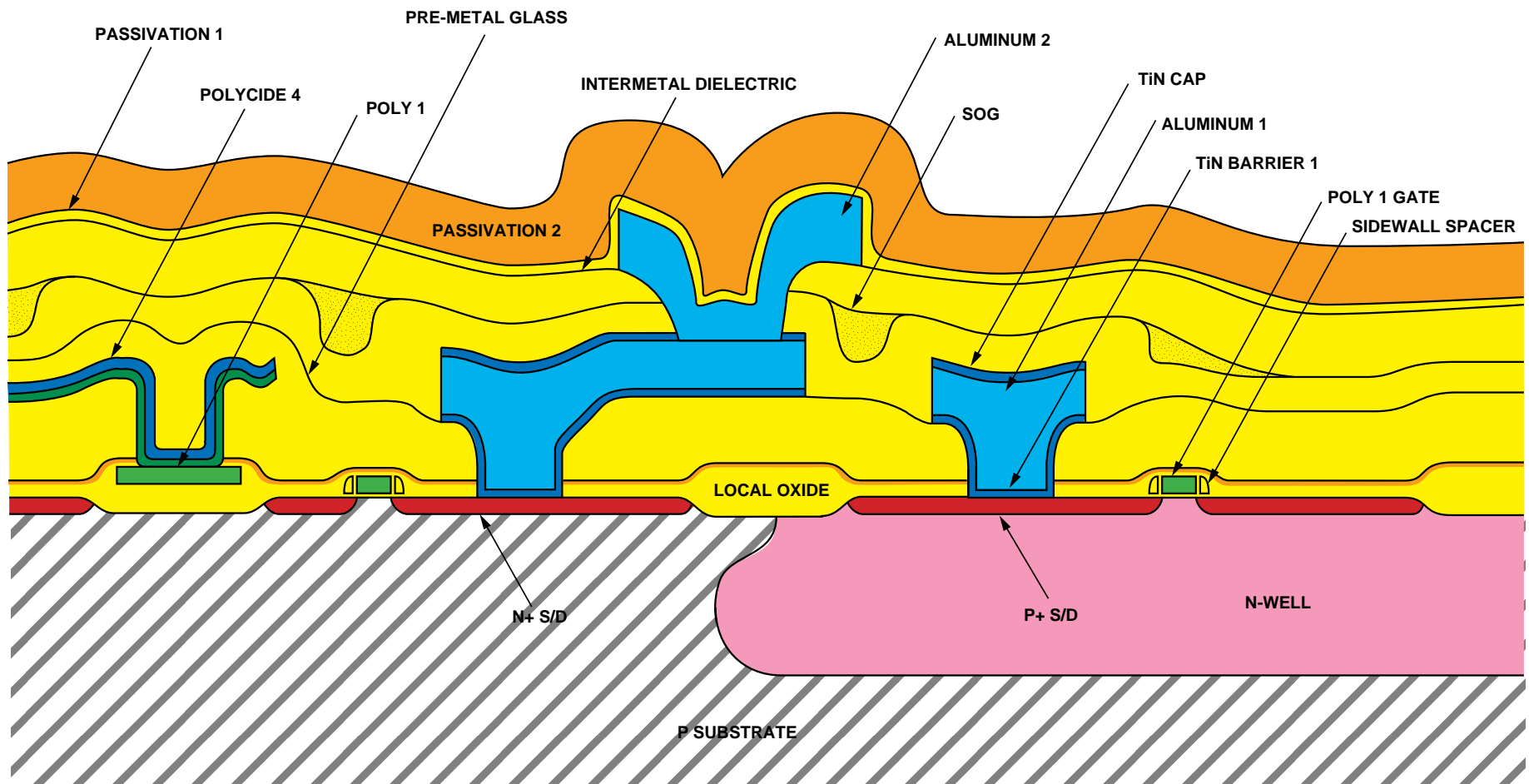


Mag. 6500x



Mag. 26,000x

Figure 22. Perspective SEM views of poly 1 coverage. 60°.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

Figure 23. Color cross section drawing illustrating device structure.

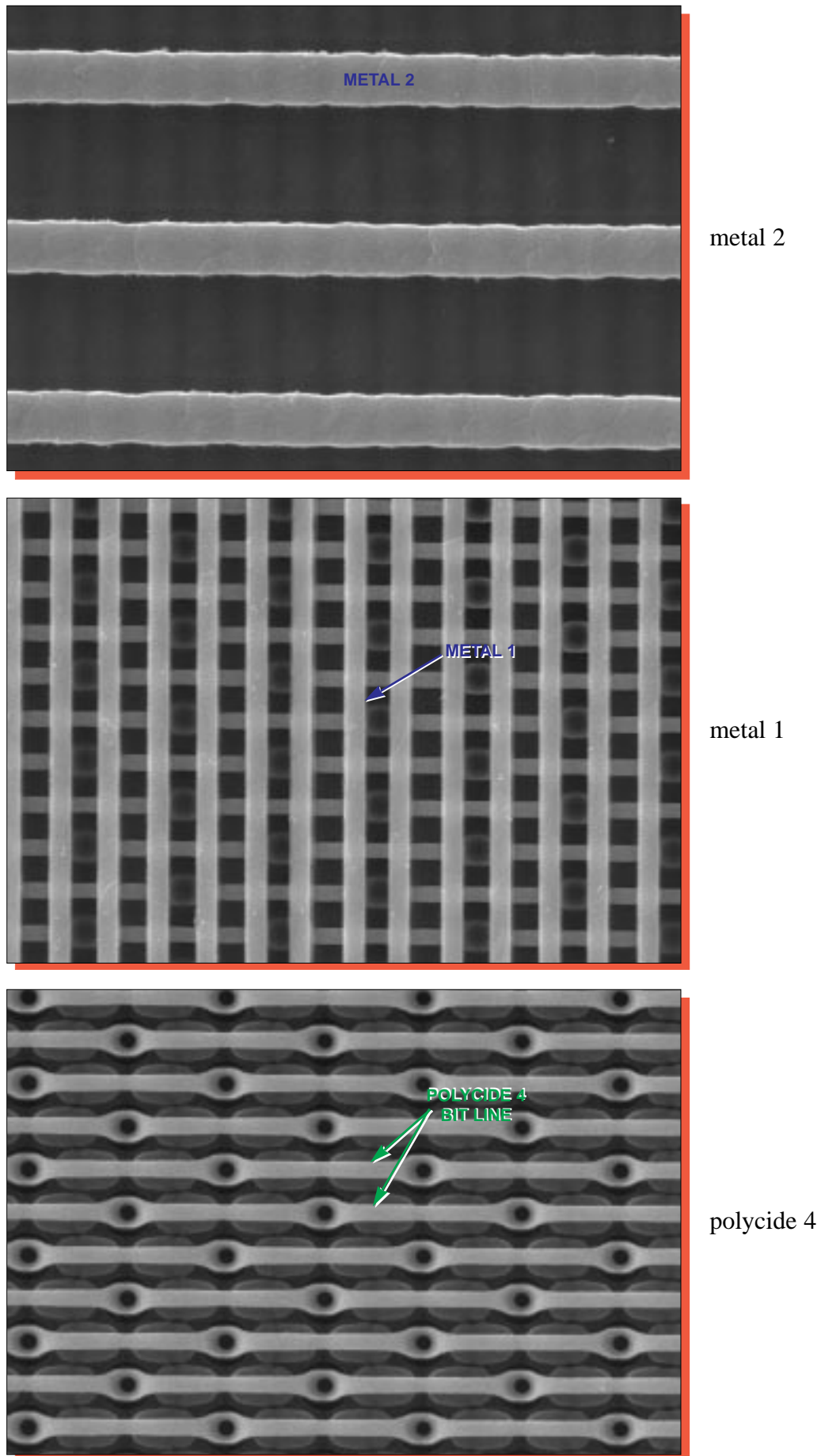
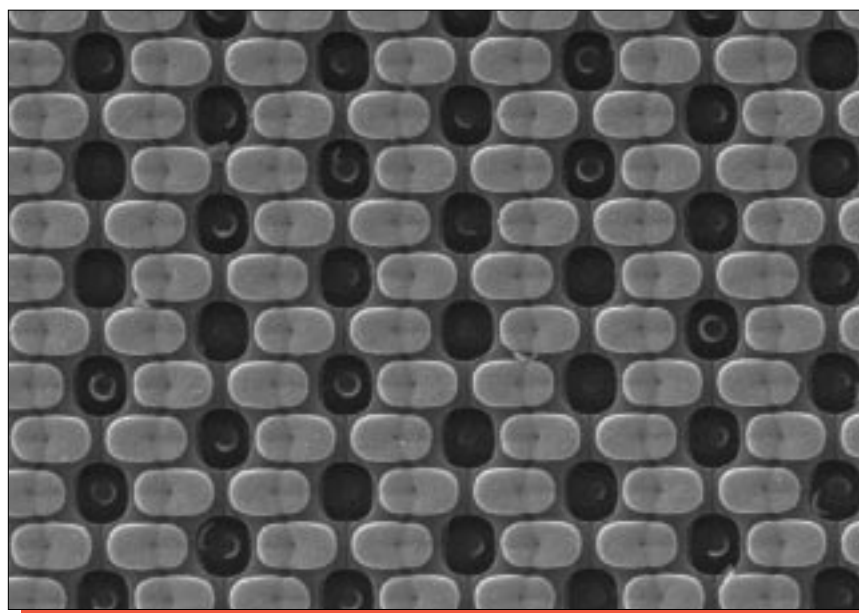
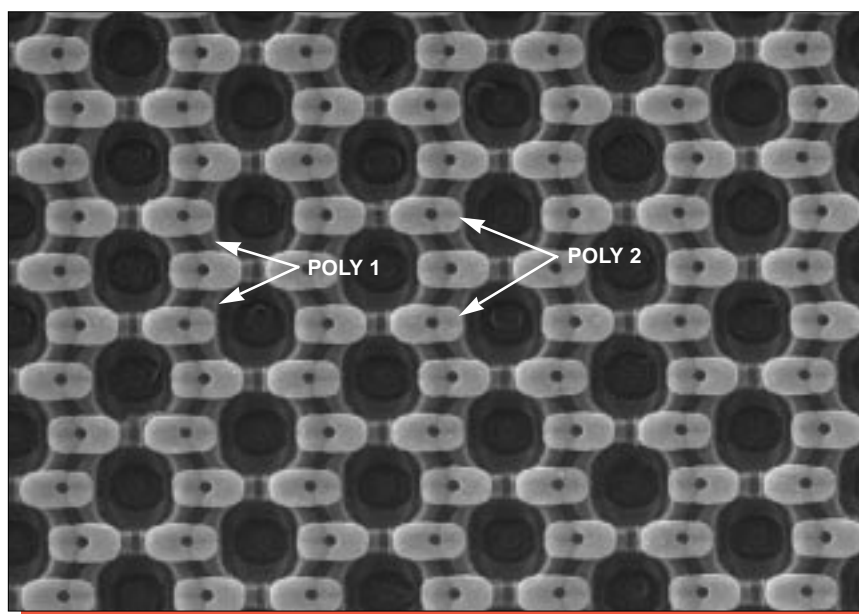


Figure 24. Topological SEM views of the DRAM cell array. Mag. 6500x. 0°.



poly 3 sheet



poly 2 and poly 1

Figure 25. Topological SEM views of the DRAM cell array. Mag. 6500x, 0°.

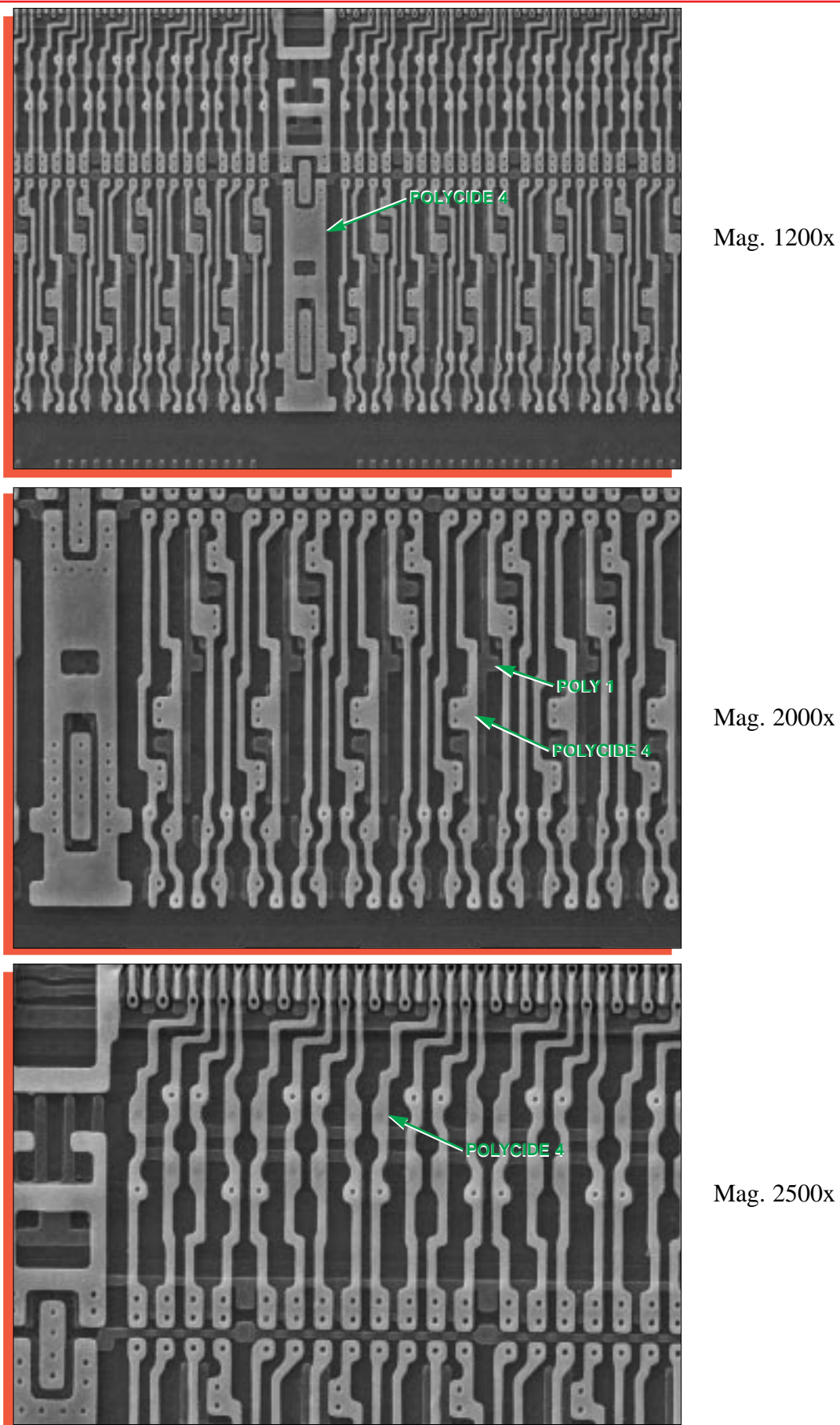
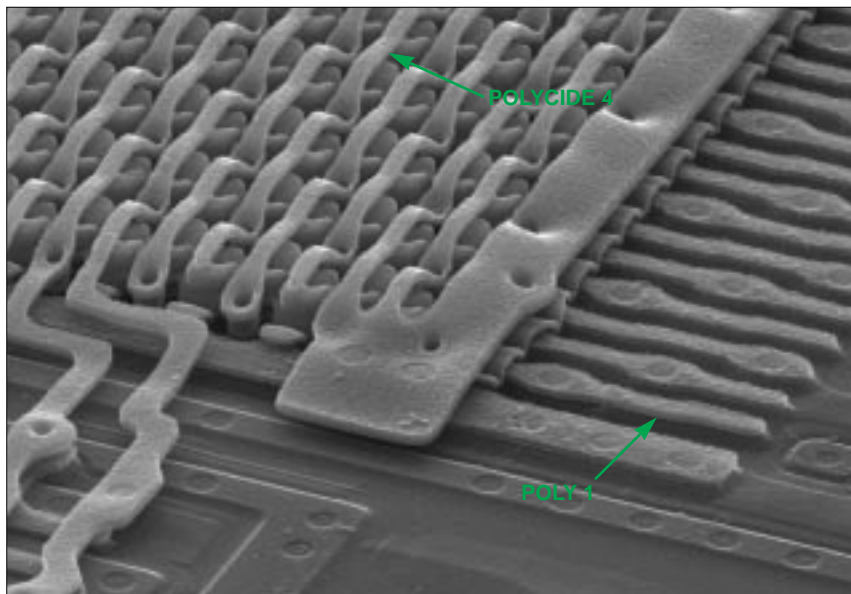
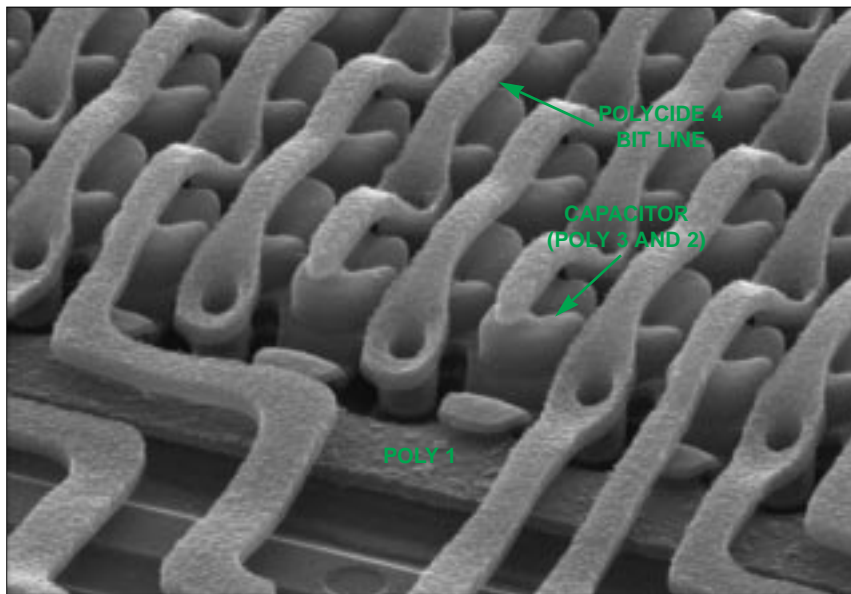


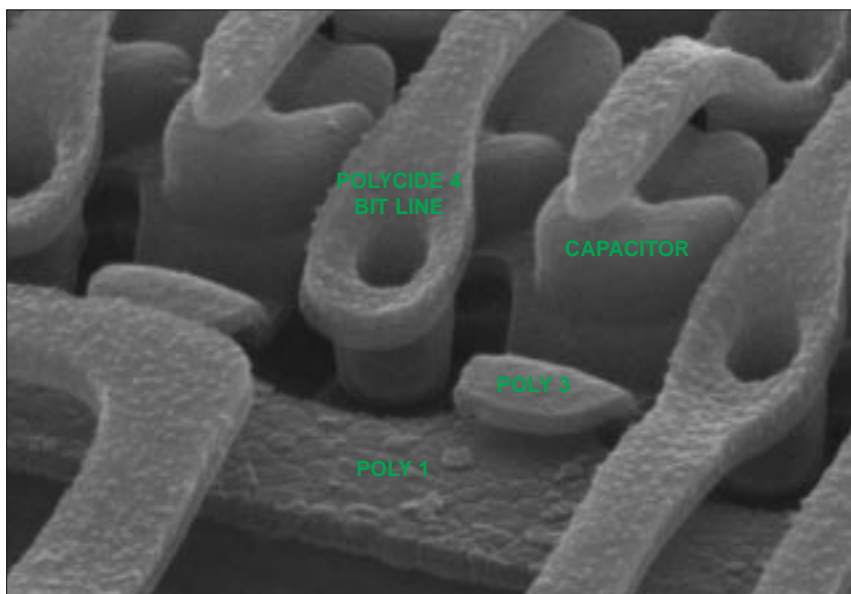
Figure 26. Topological SEM views of polycide 4 patterning along the edge of the DRAM cell array. Column, 0°.



Mag. 6500x

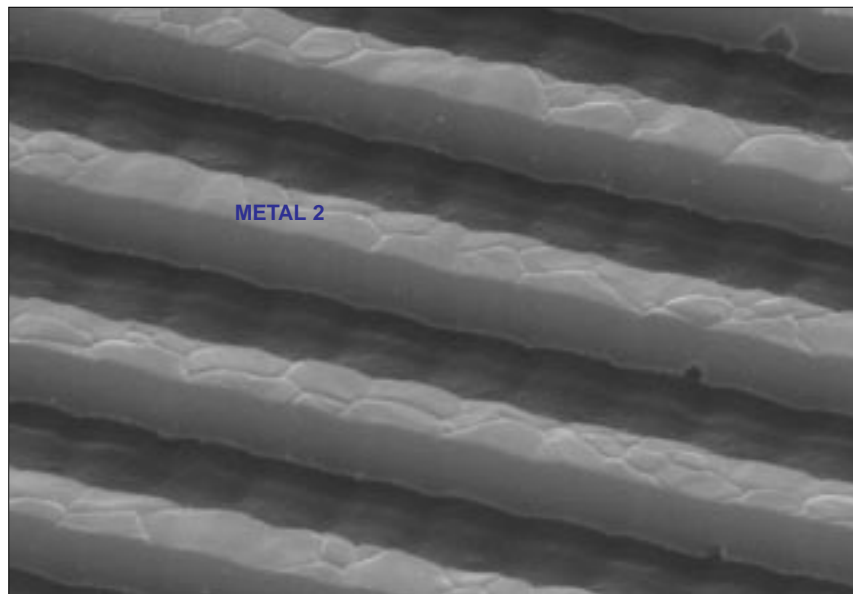


Mag. 13,000x

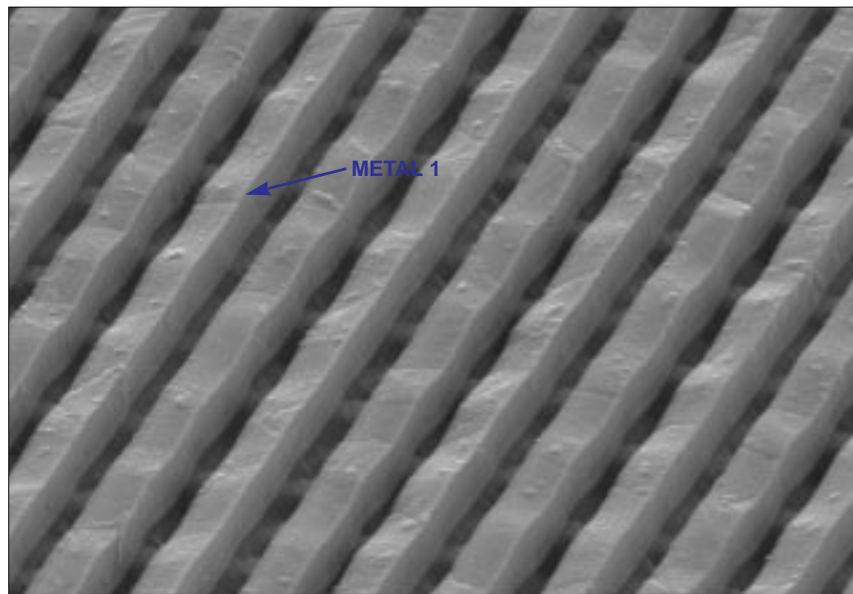


Mag. 26,000x

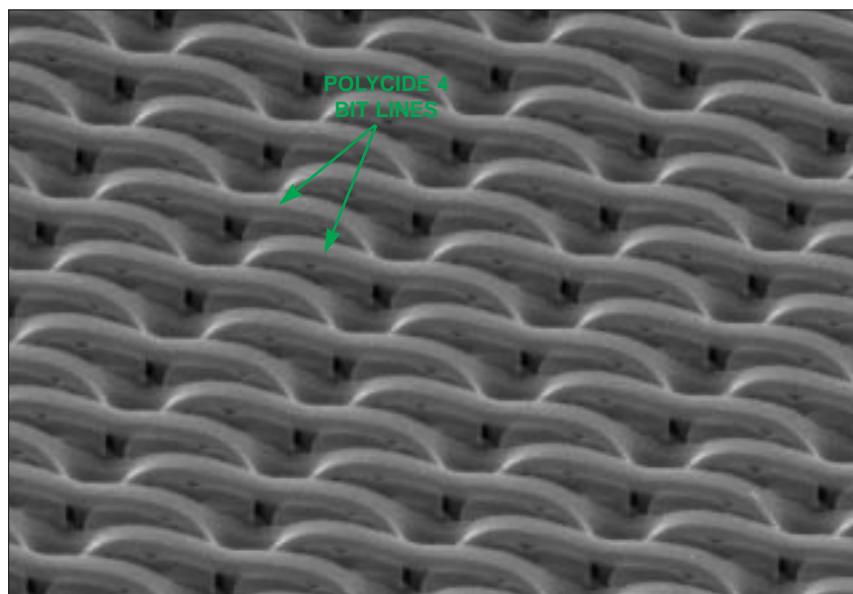
Figure 27. Perspective SEM views of structures at edge of DRAM array. 60°.



metal 2

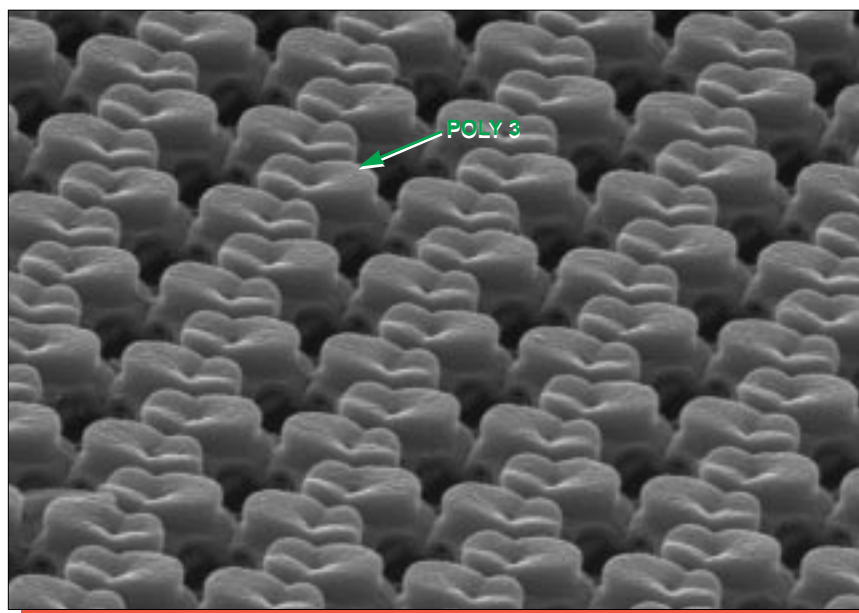


metal 1

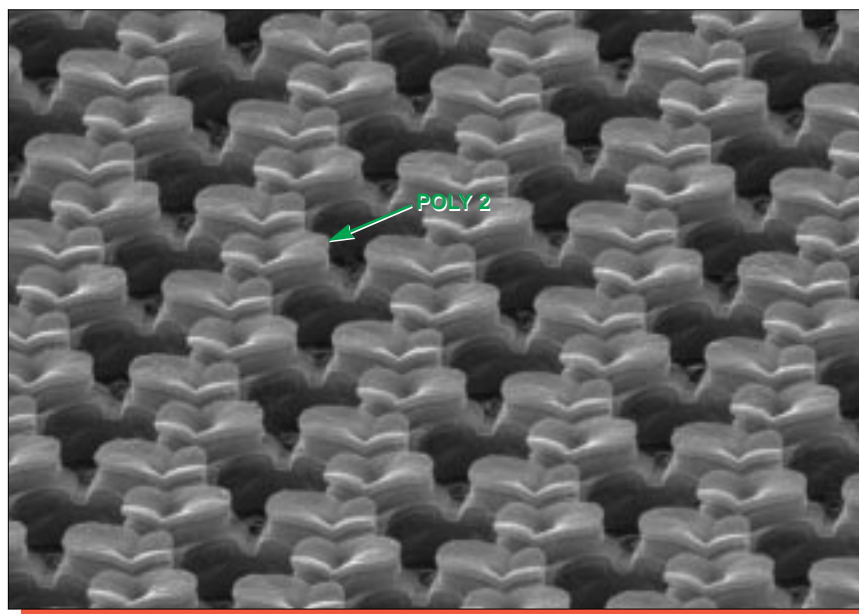


polycide 4

Figure 28. Perspective SEM view of the DRAM cell array. Mag. 10,000x. 60°.

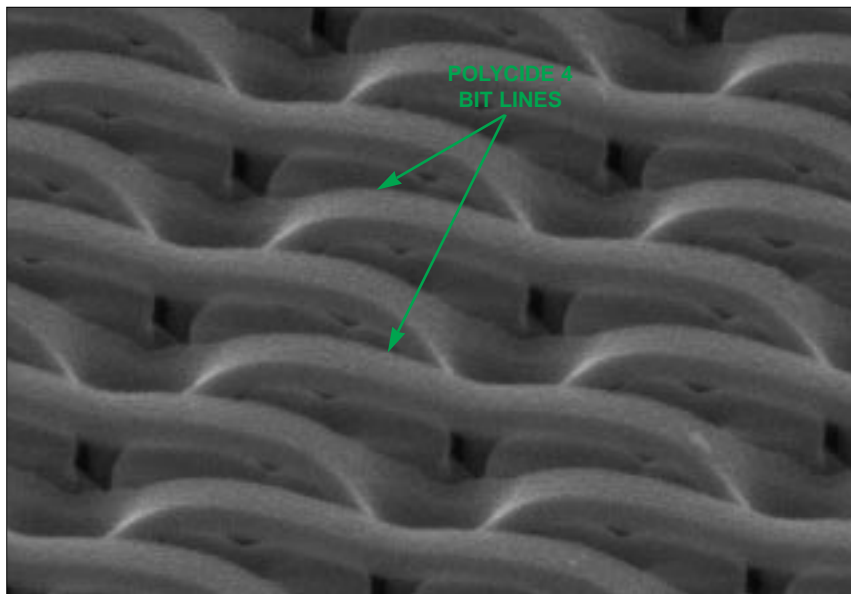


poly 3 sheet

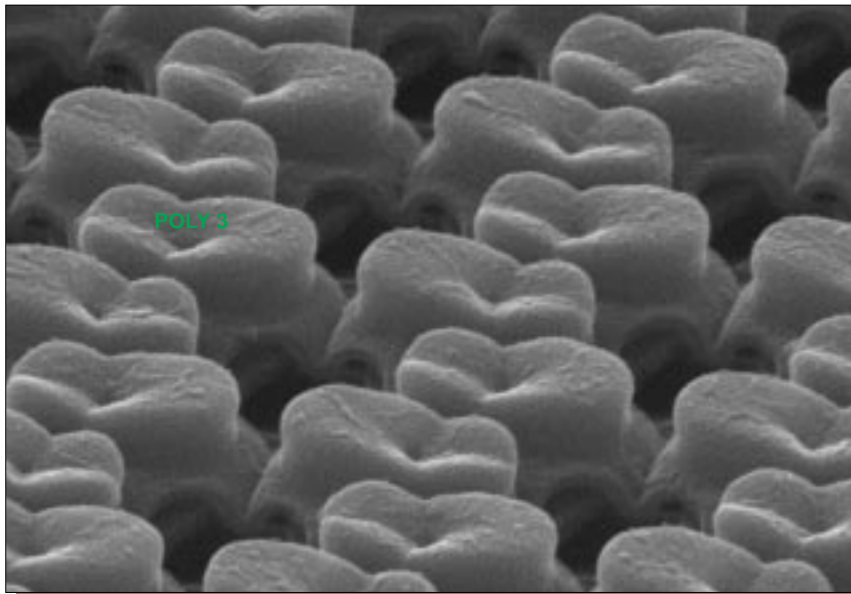


poly 2

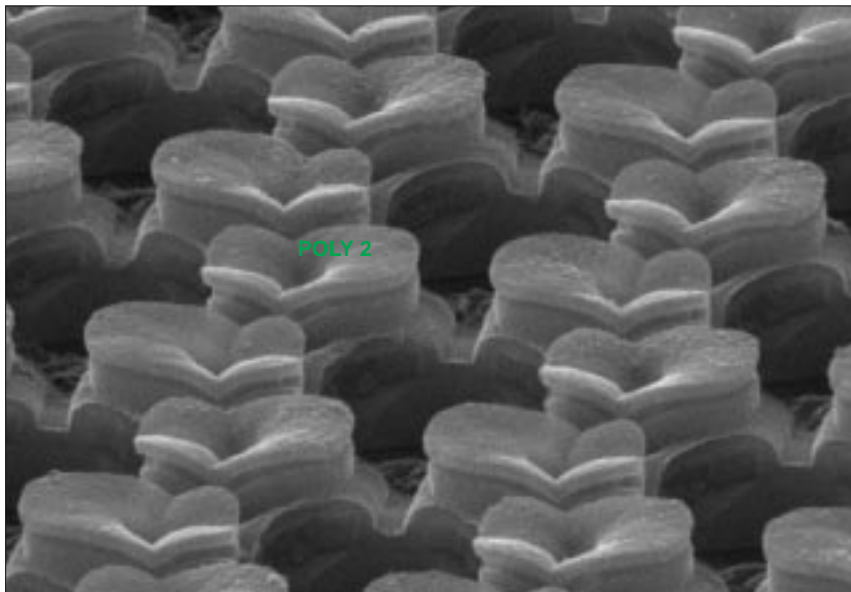
Figure 29. Perspective SEM views of the DRAM cell array. Mag. 10,000x, 60°.



polycide 4

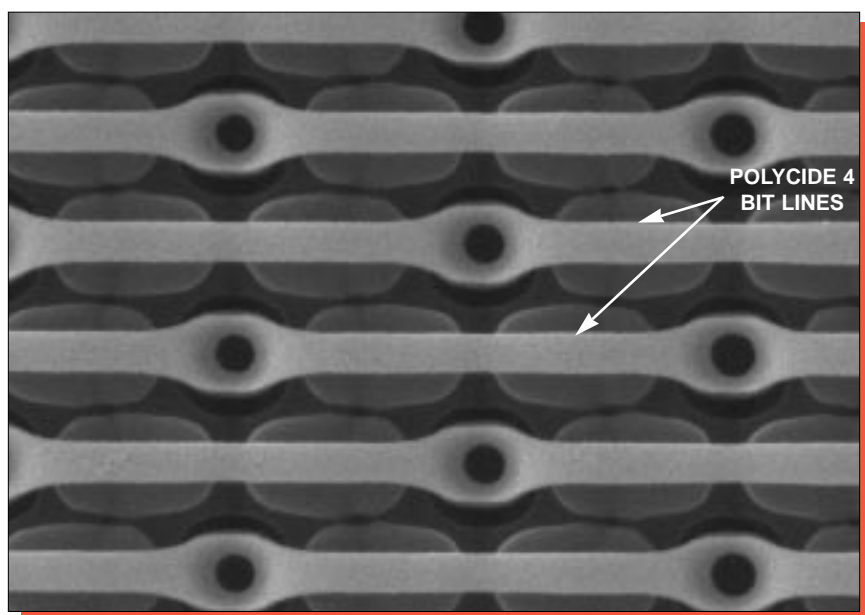


poly 3 sheet

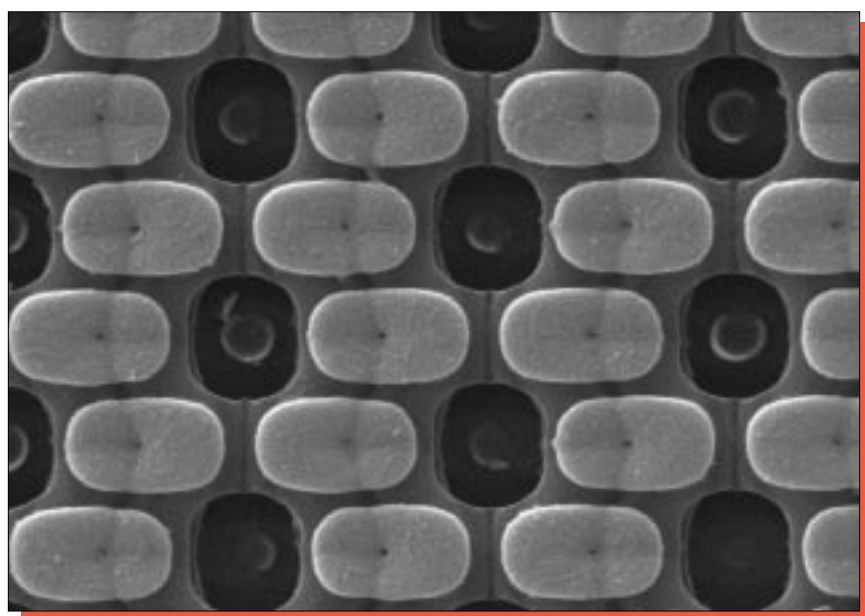


poly 2

Figure 30. Detailed SEM views of the DRAM cell array. Mag. 20,000x. 60°.

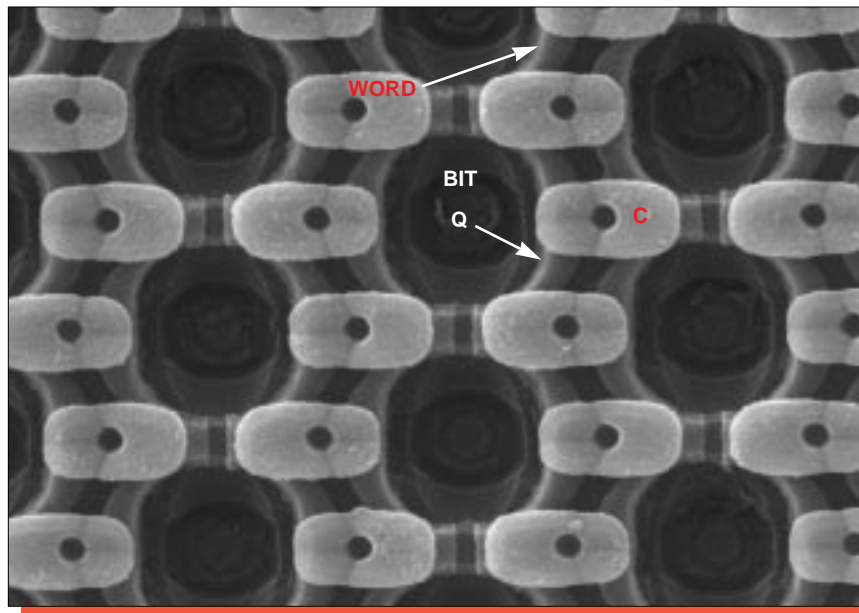


polycide 4



poly 3 sheet

Figure 31. Detailed topological SEM views of the DRAM cell array.
Mag. 13,000x. 0°.



poly 2

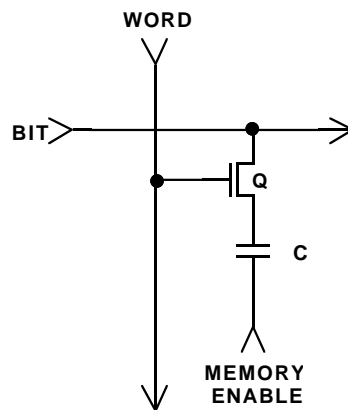
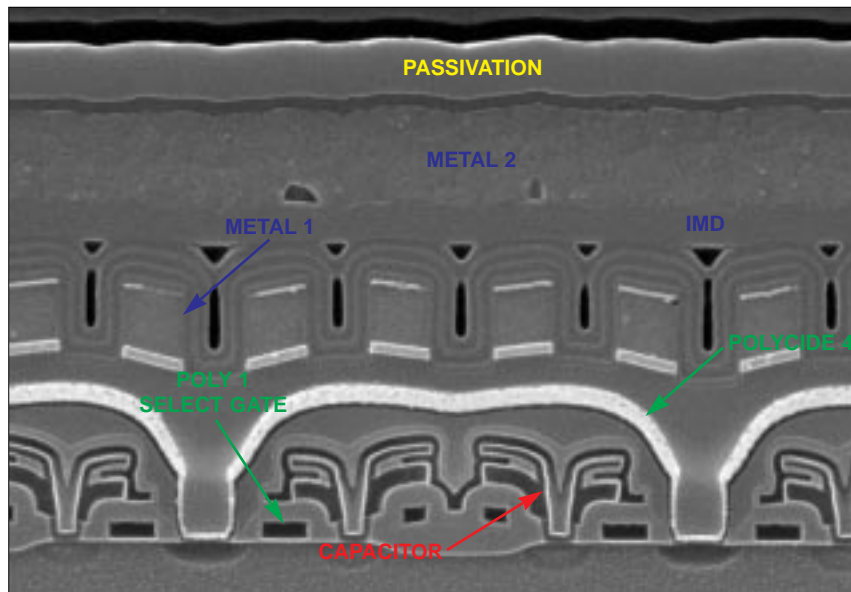
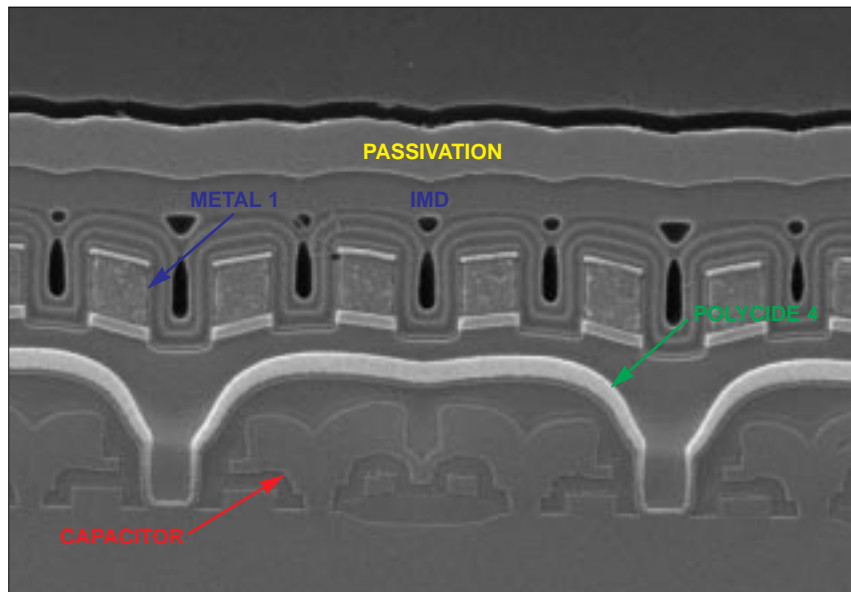


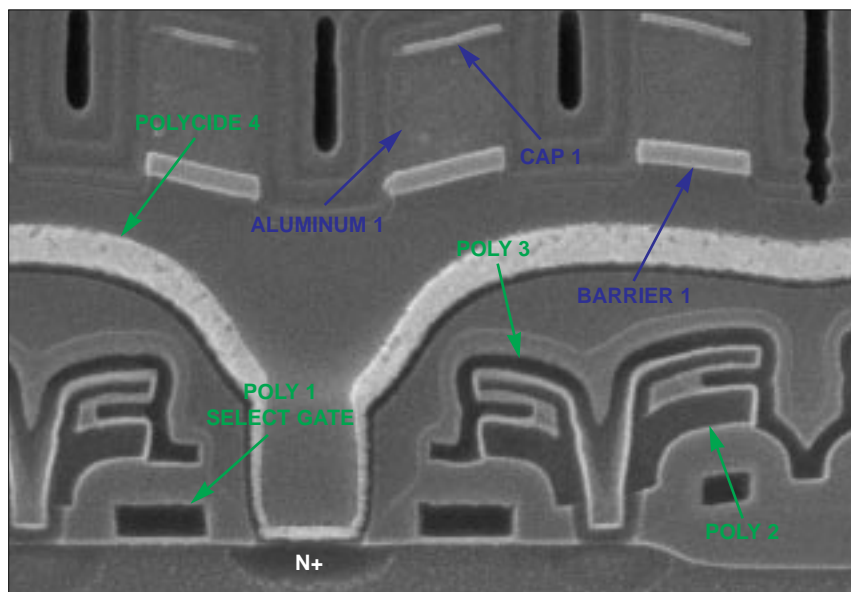
Figure 32. Detailed topological SEM view and schematic of the DRAM cell.
Mag. 13,000x.



silicon-etch,
Mag. 13,000x

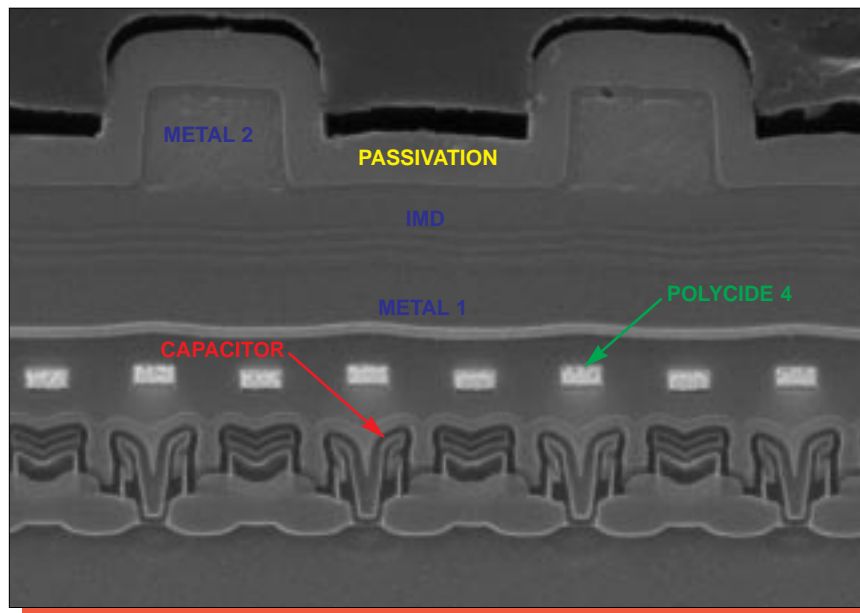


glass-etch,
Mag. 13,000x

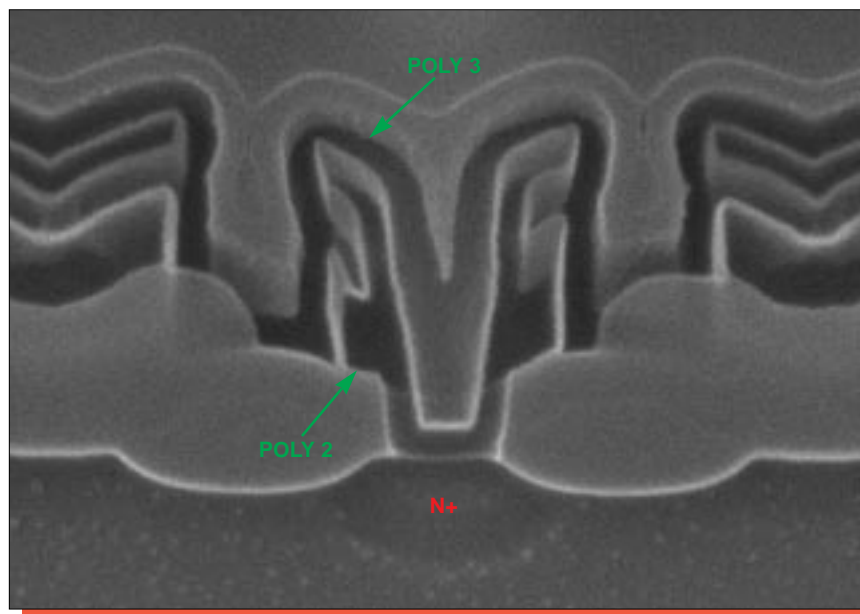


silicon-etch,
Mag. 26,000x

Figure 33. SEM section views of the DRAM cell array (X-direction).

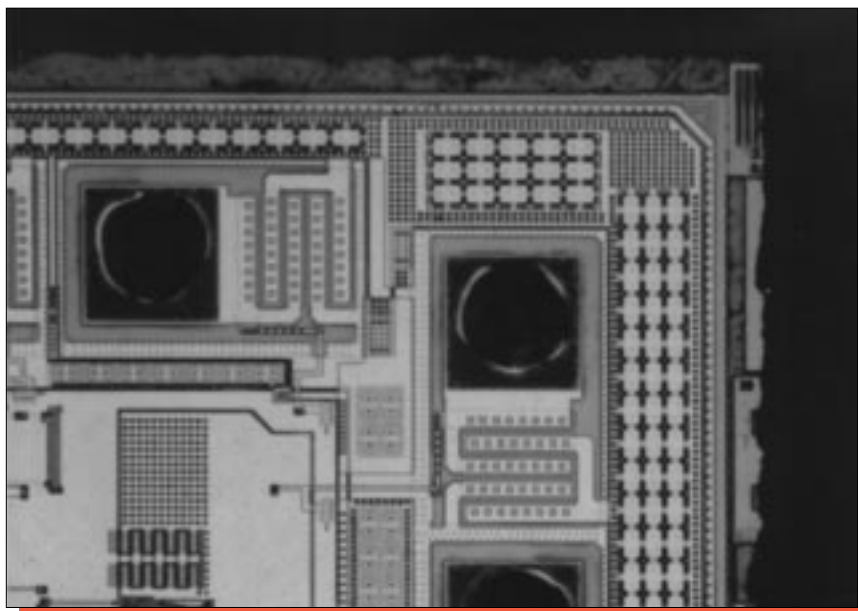


Mag. 13,000x

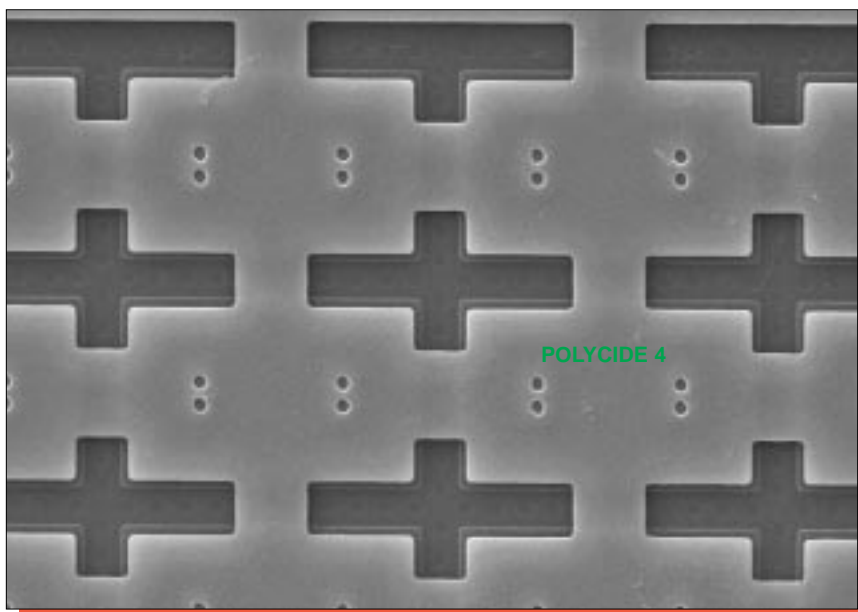


Mag. 50,000x

Figure 34. SEM section views of the DRAM cell array (Y-direction).

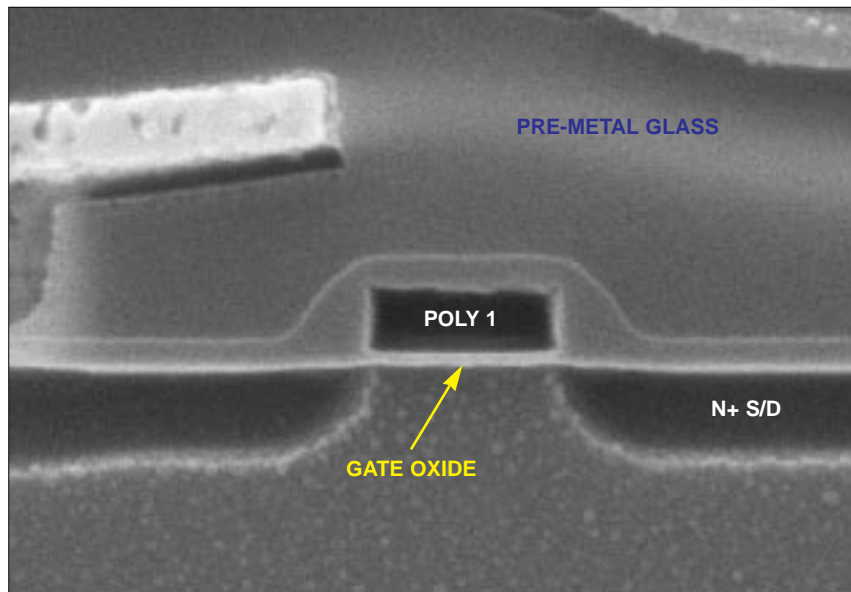


metal 1, Mag. 160x

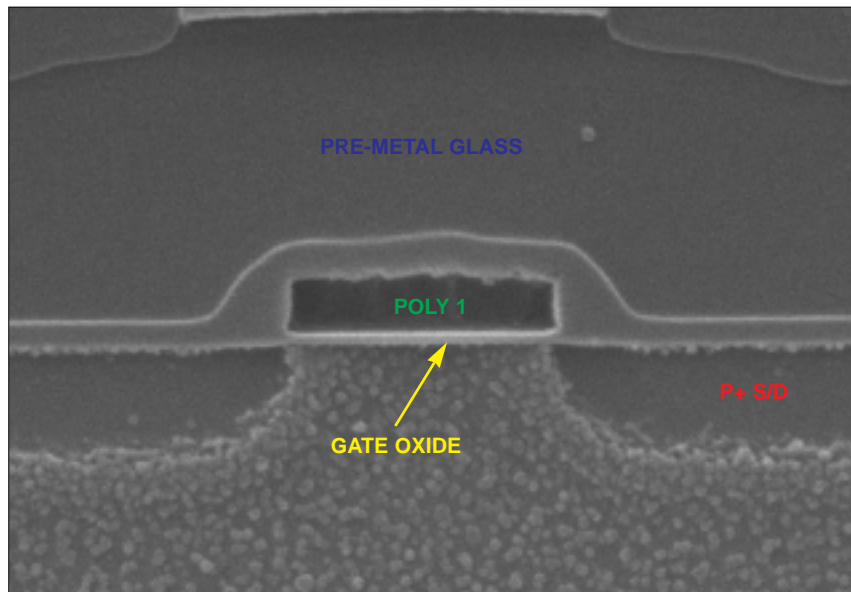


Mag. 1600x, 0°

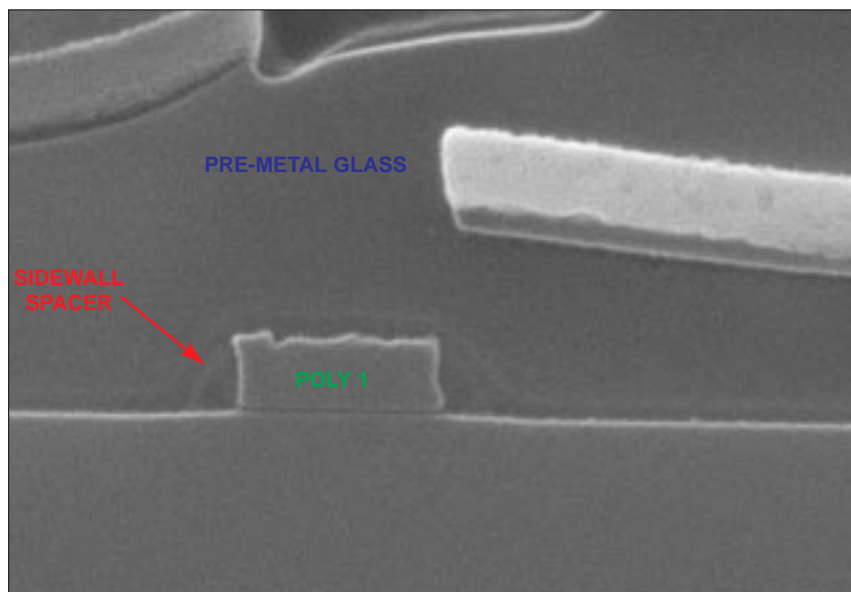
Figure 35. Optical and SEM views of metal 1 and polycide 4 patterning around bonding pads.



N-channel,
silicon-etch



P-channel,
silicon-etch



glass-etch

Figure 36. SEM section views of typical transistors. Mag. 52,000x.

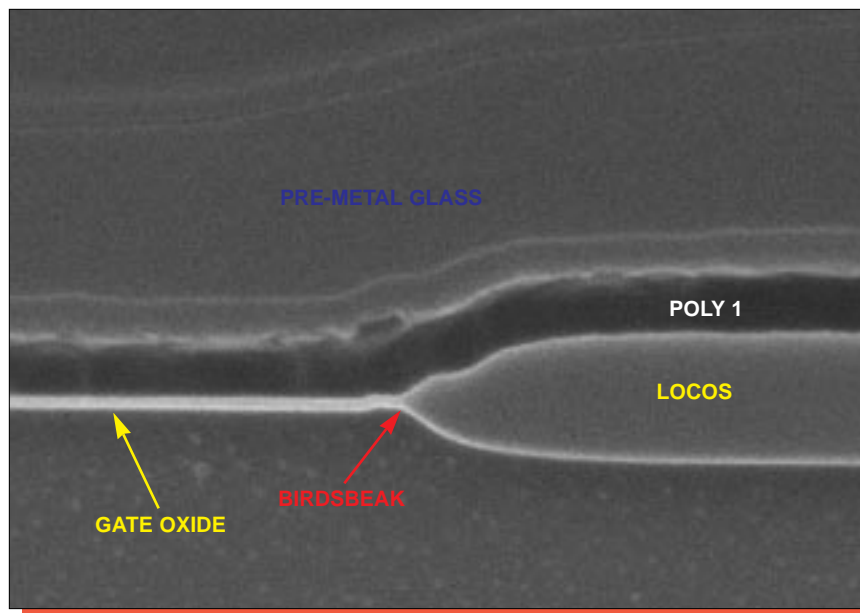


Figure 37. SEM section view of a local oxide birds beak. Mag. 52,000x.

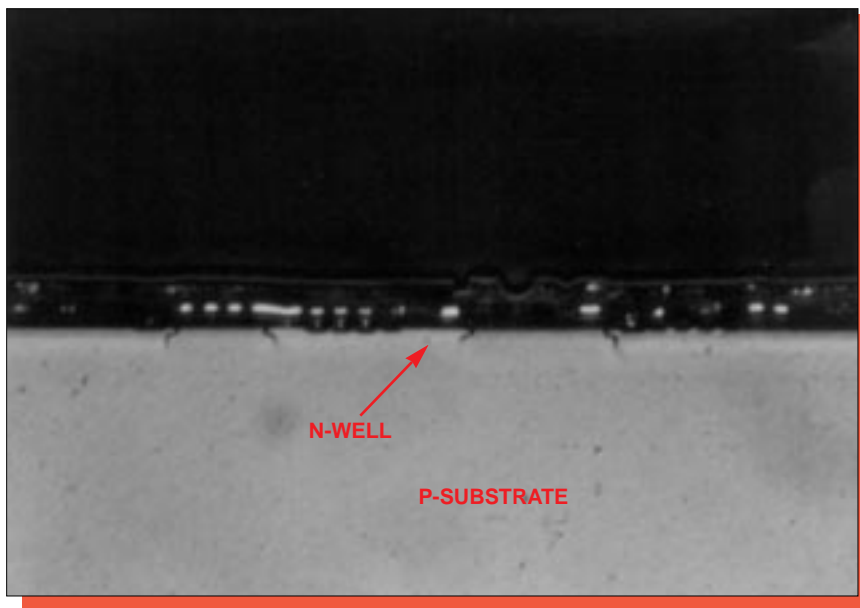
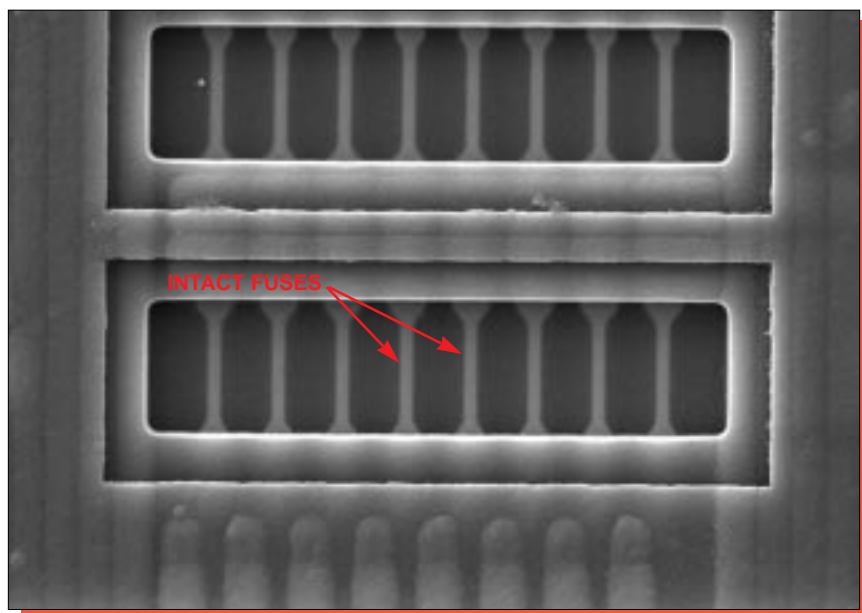
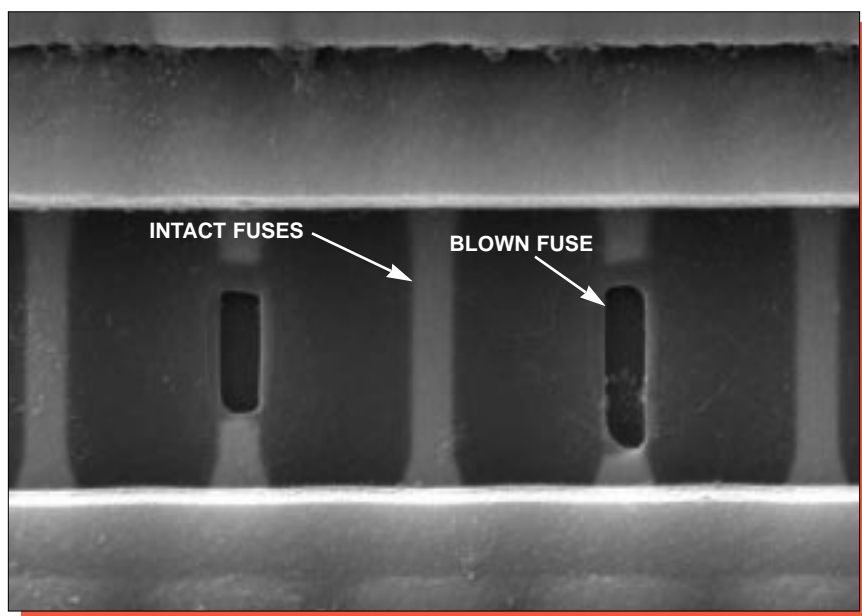


Figure 38. Optical view of the well structure. Mag. 1600x.

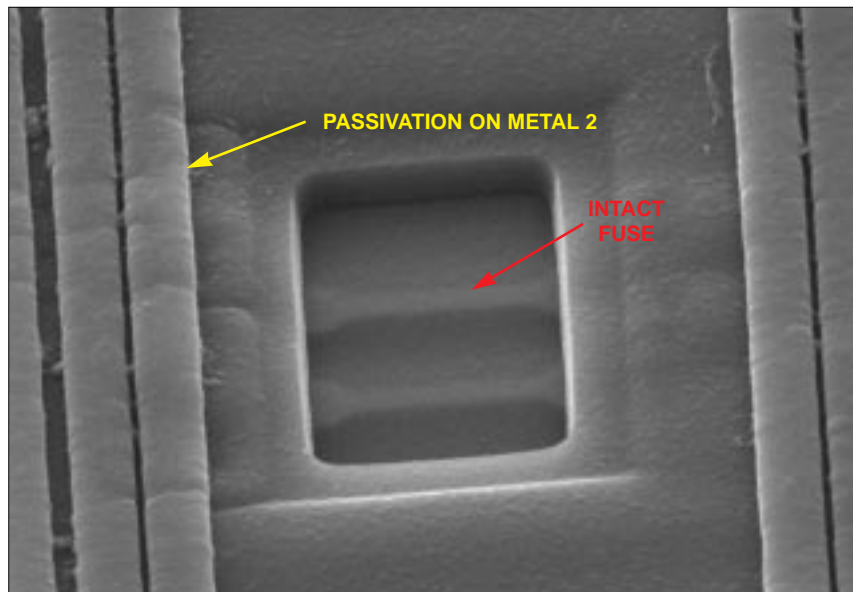


Mag. 2000x

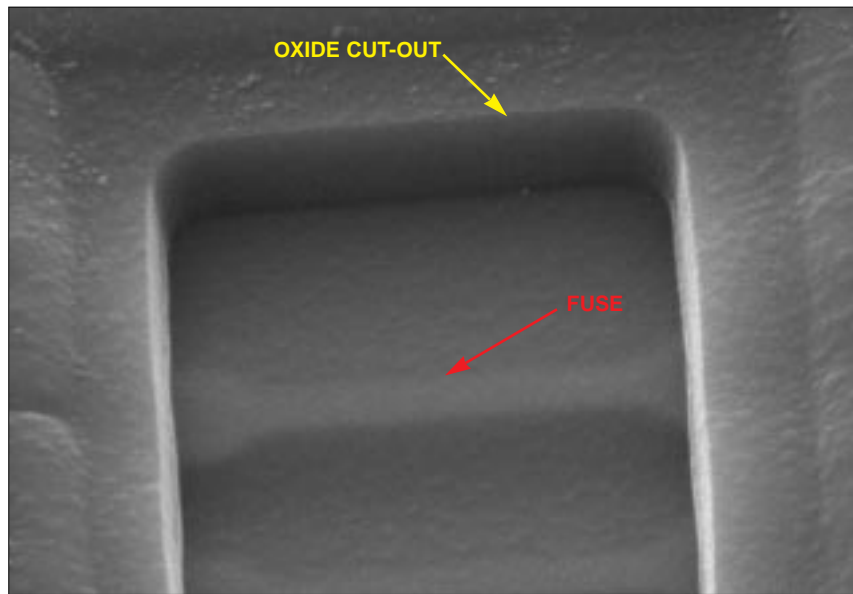


Mag. 6500x

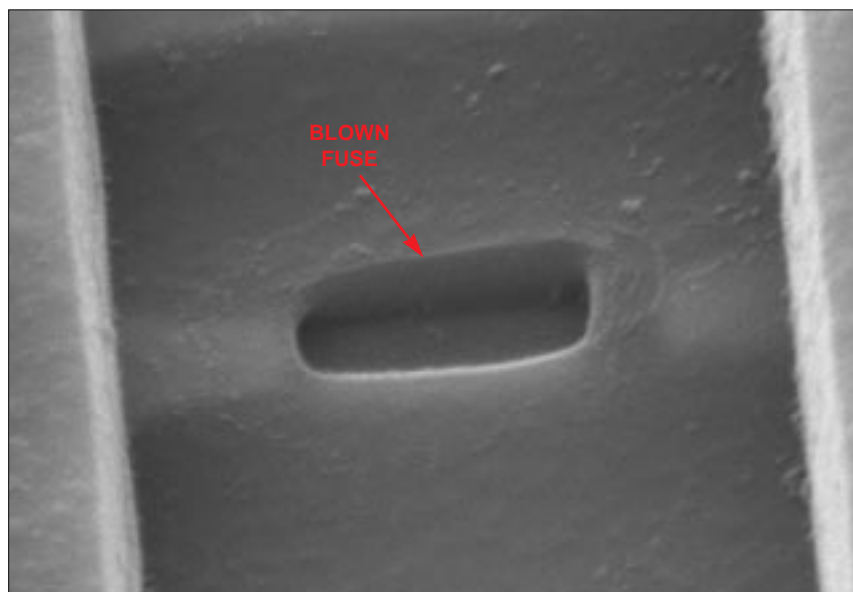
Figure 39. Topological SEM views of typical fuses. 0°.



Mag. 4000x

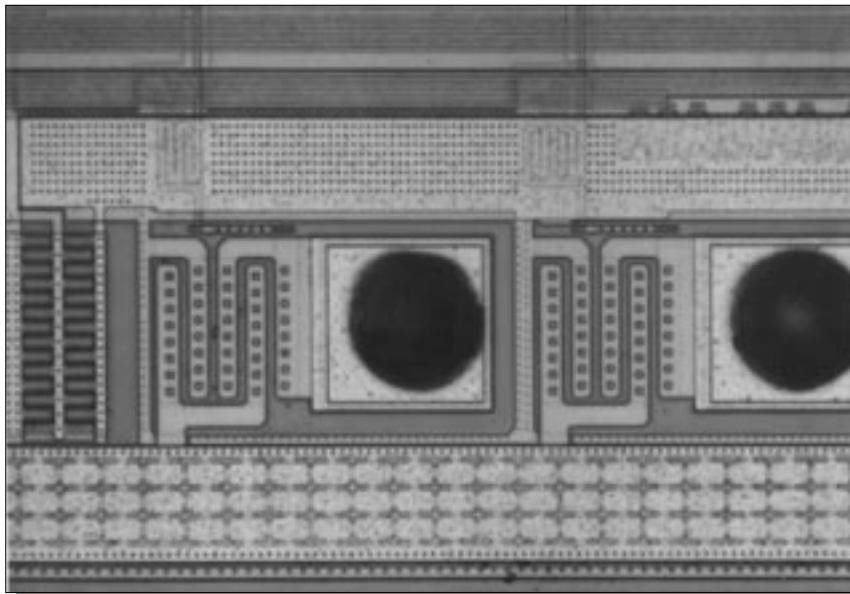


Mag. 8000x

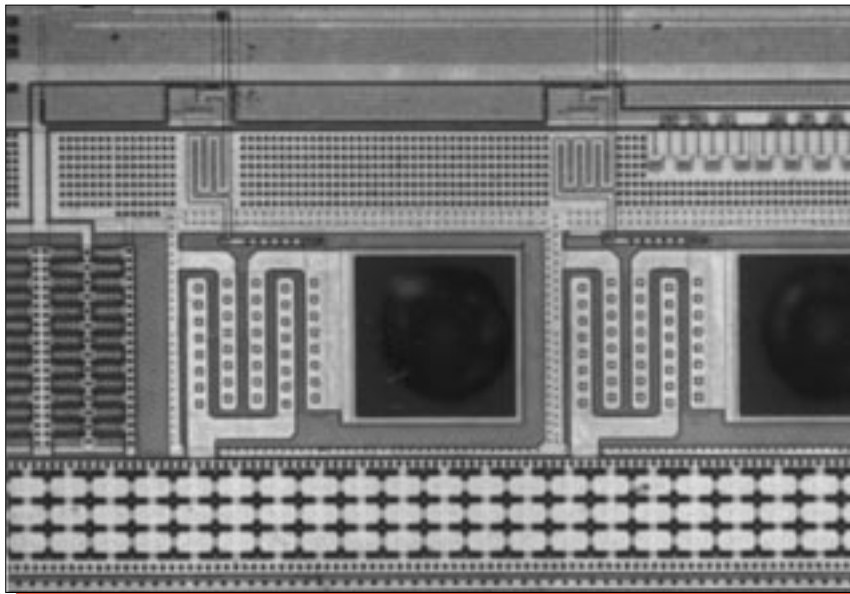


Mag. 16,000x

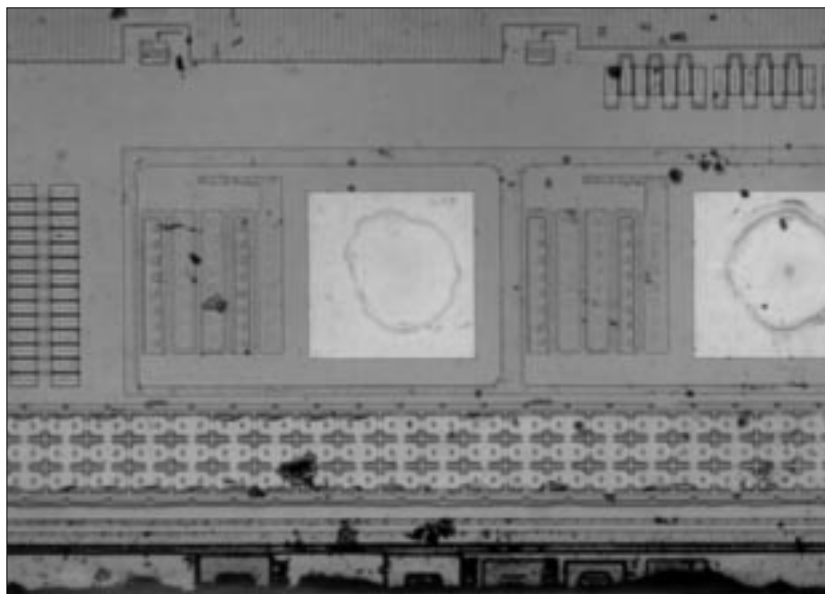
Figure 40. Perspective SEM views of typical fuses. 60°.



intact



metal 1



unlayered

Figure 41. Optical views of the input protection. Mag. 200x.

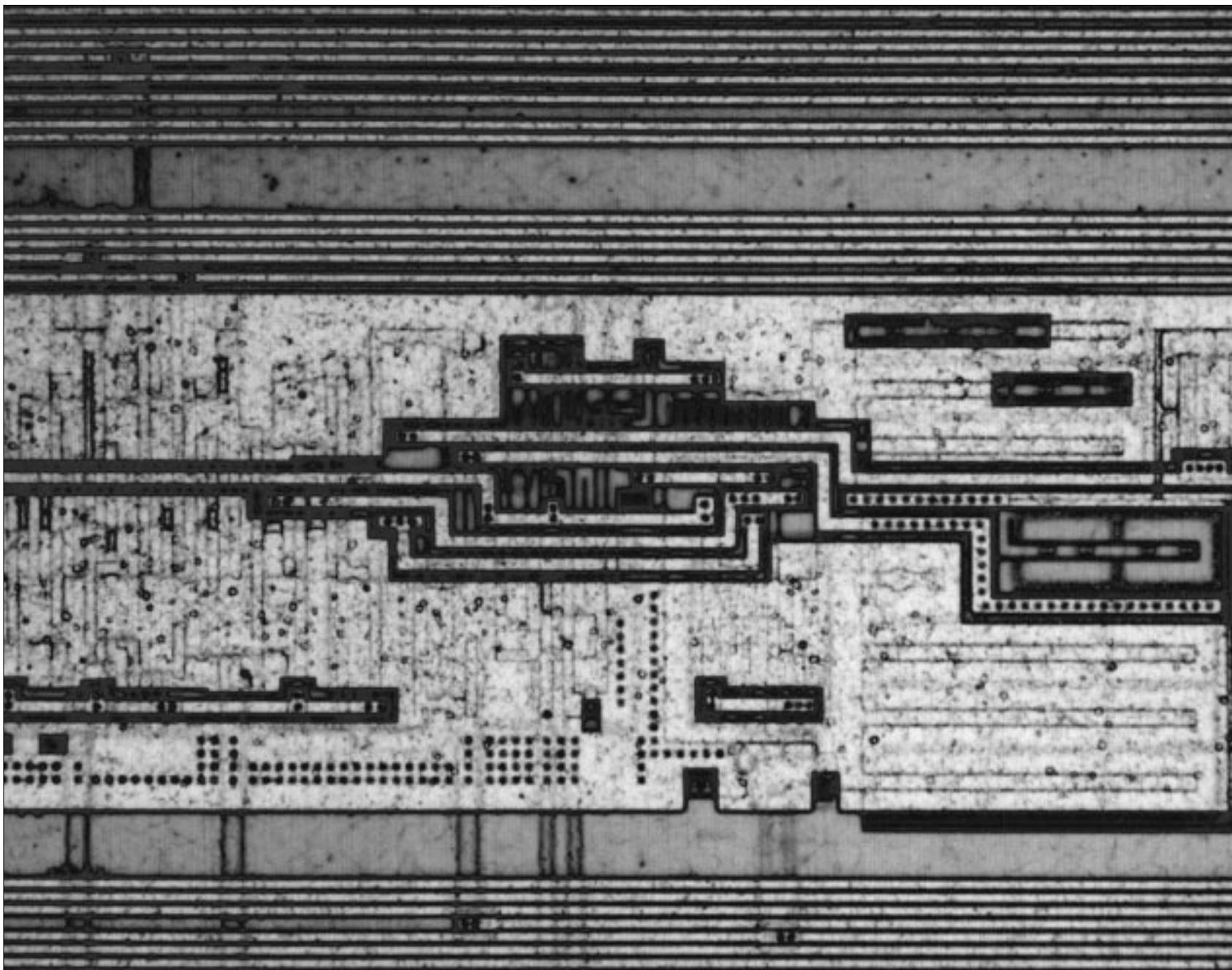


Figure 42. Optical view of circuit layout. Intact, Mag. 1000x.

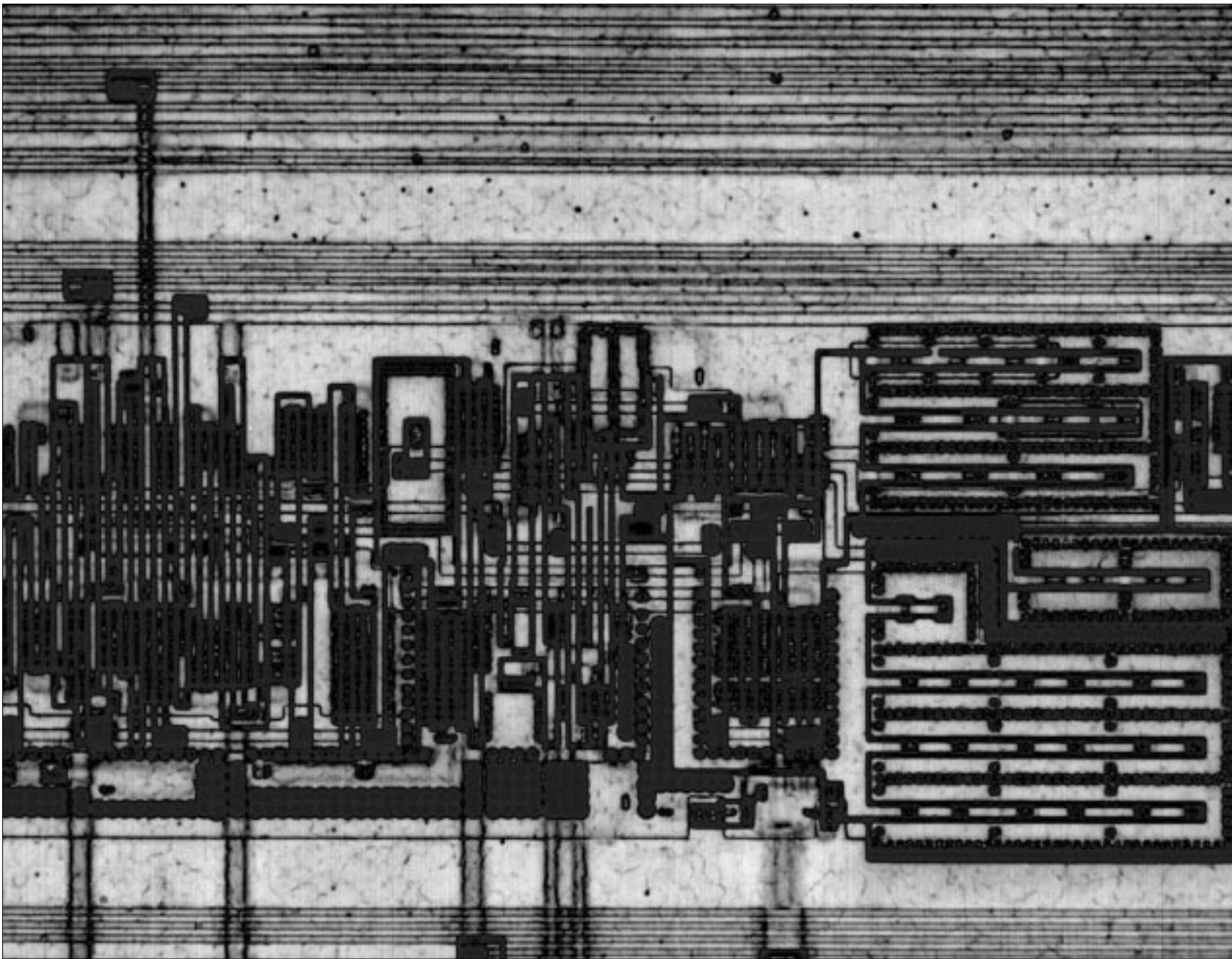


Figure 42a. Optical view of circuit layout. Metal 1, Mag. 1000x.

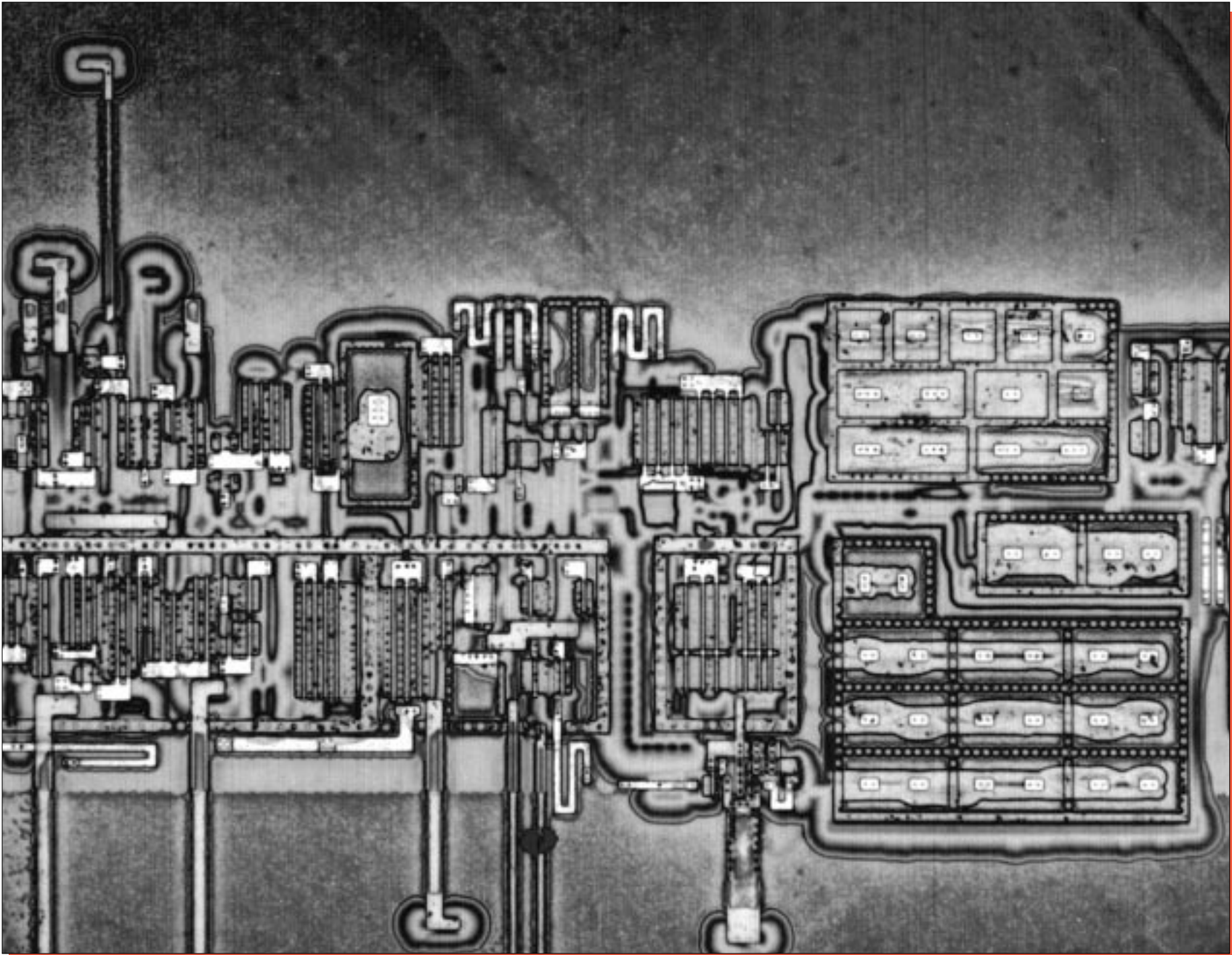
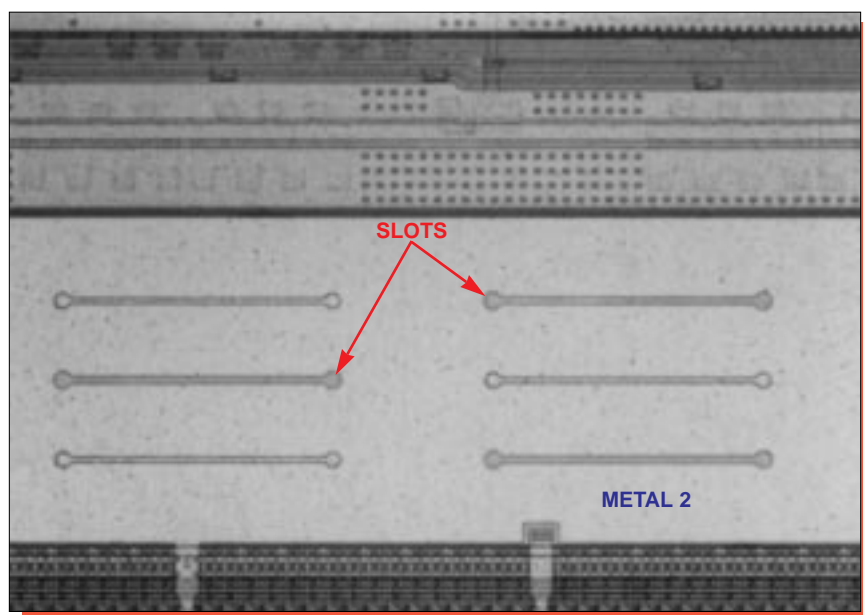
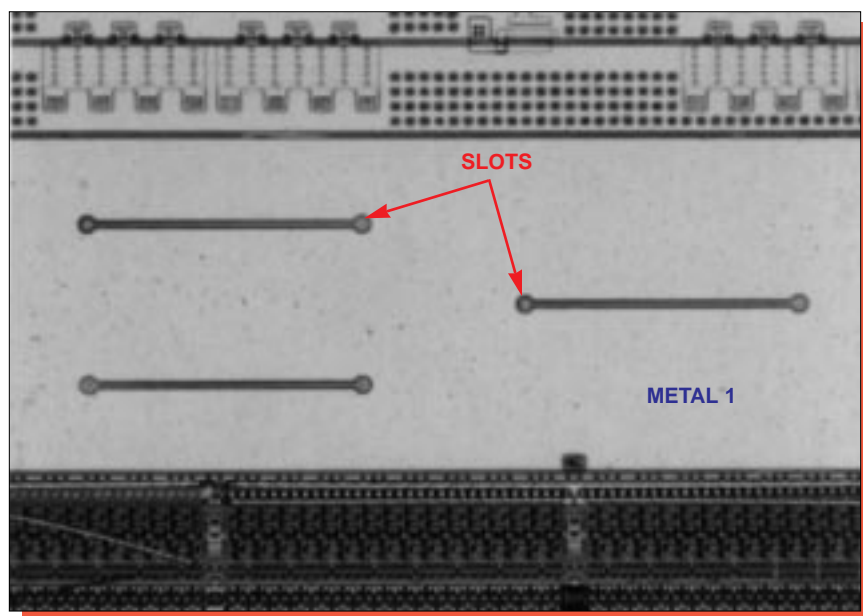


Figure 42b. Optical view of circuit layout. Unlayered, Mag. 1000x.



intact



metal 1

Figure 43. Optical views of metal slotted bus lines. Mag. 320x.

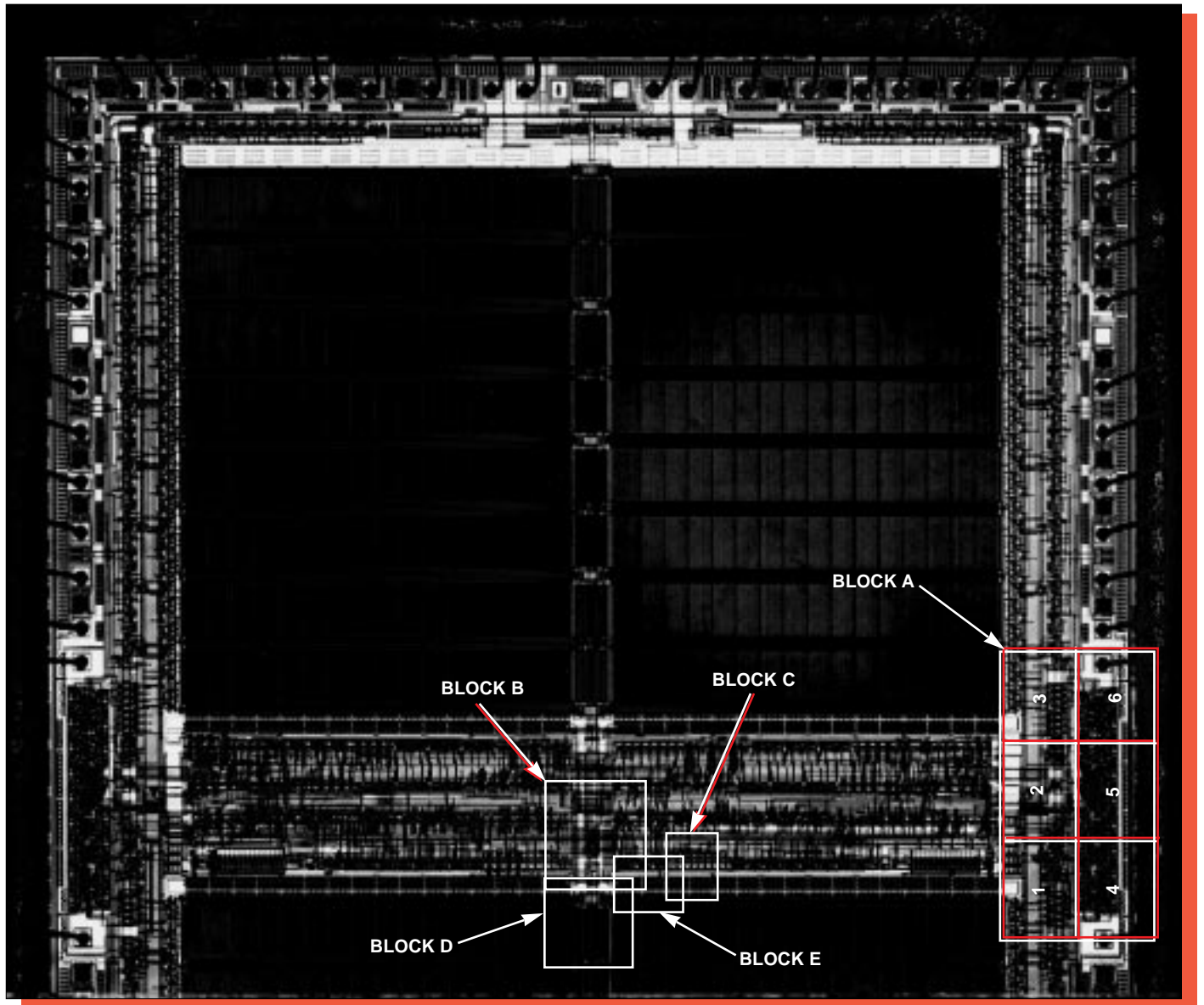


Figure 44. Portion of whole die illustrating locations of optical and SEM photos. Mag. 26x

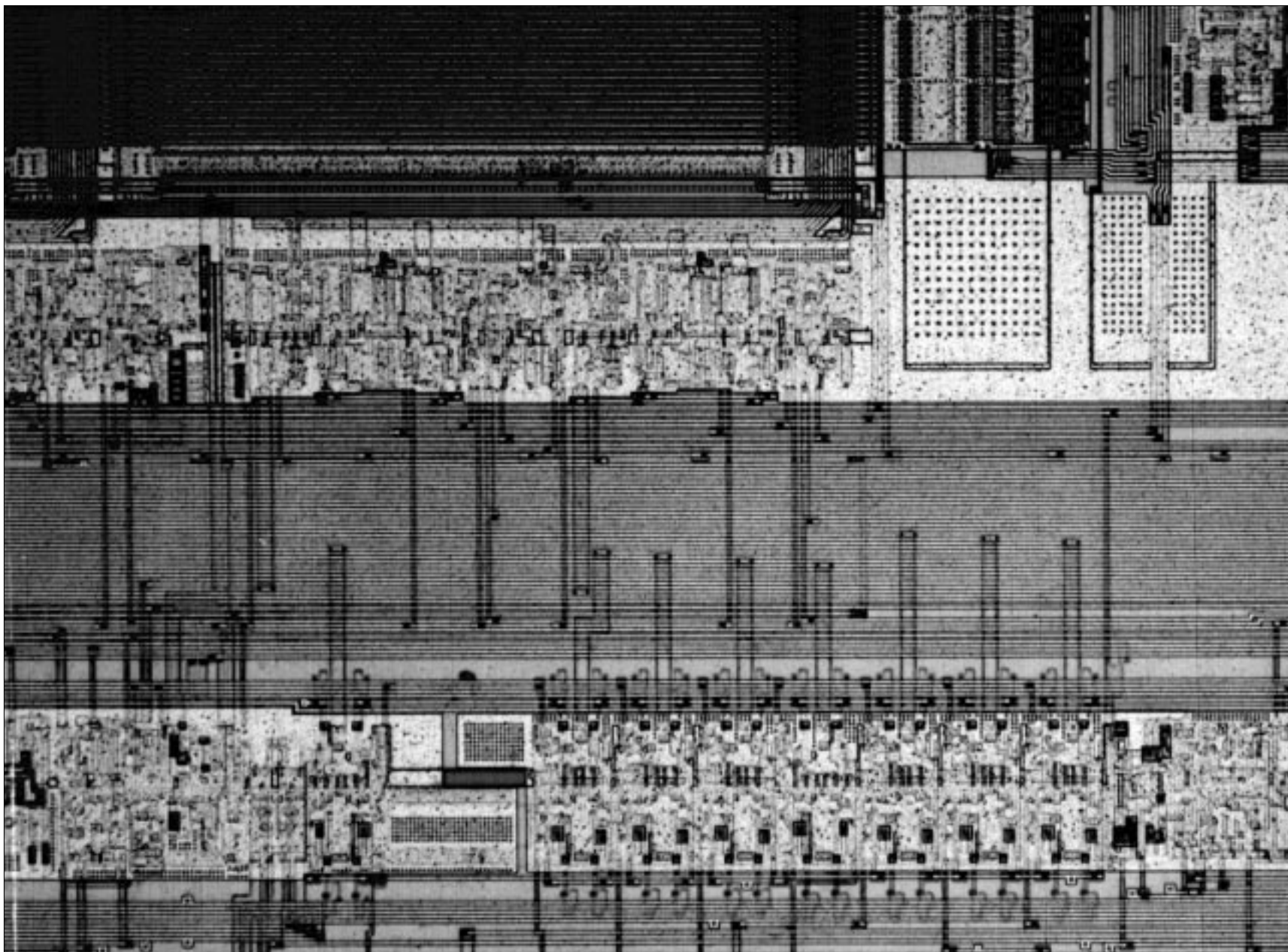


Figure 45. Optical view of circuit block A1. Intact, Mag. 320x.

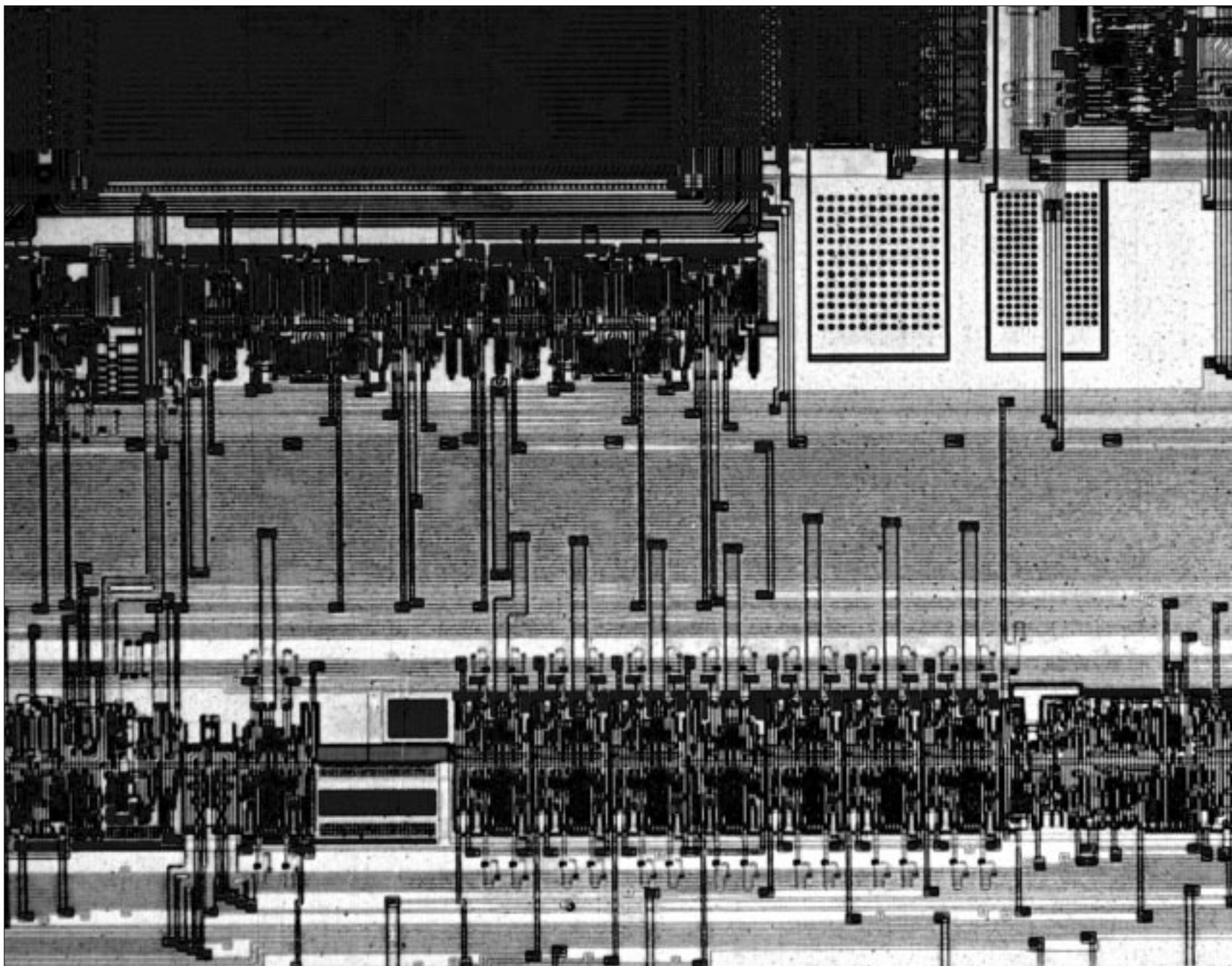


Figure 45a. Optical view of circuit block A1. Metal 1, Mag. 320x.

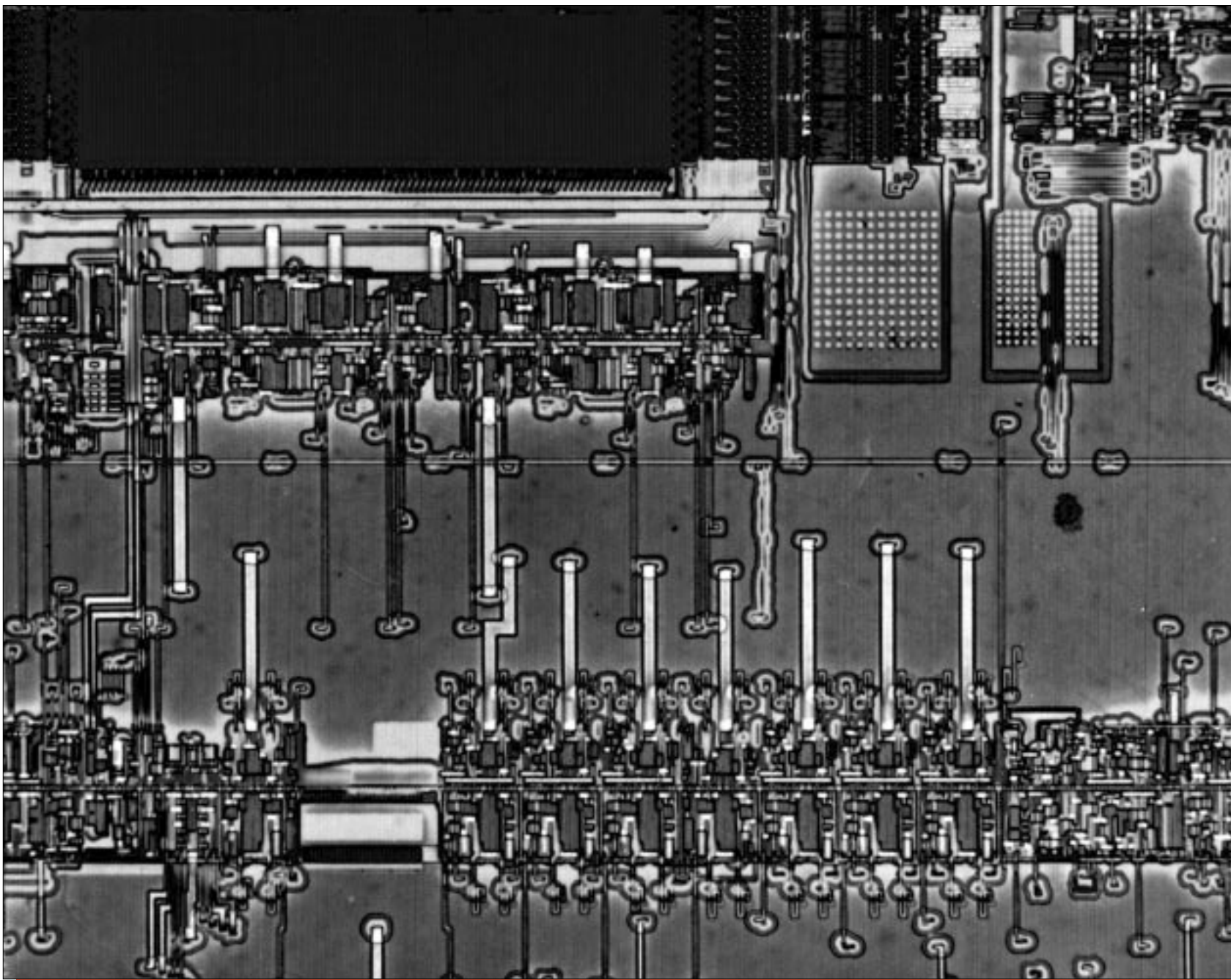


Figure 45b. Optical view of circuit block A1. Unlayered, Mag. 320x.

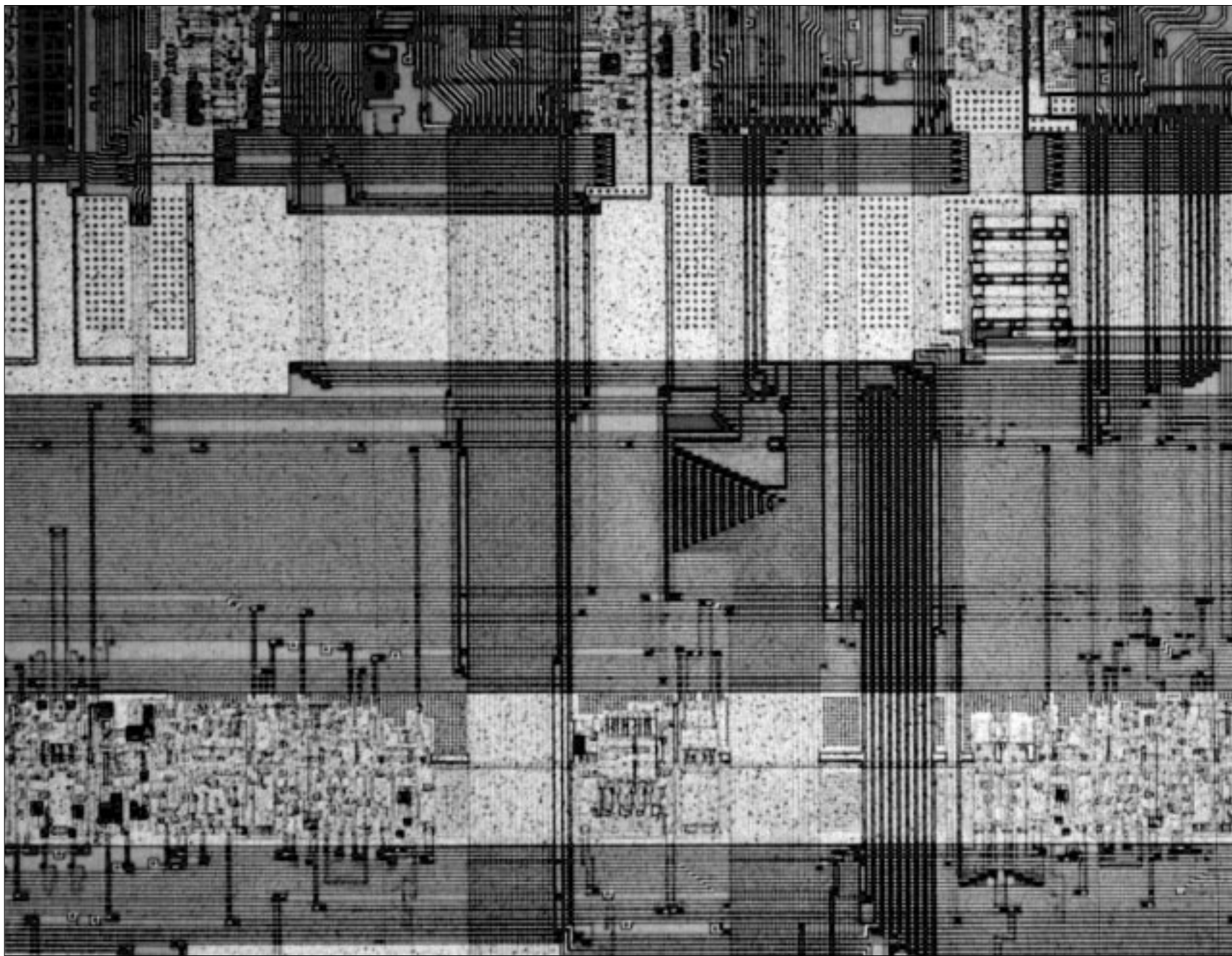


Figure 46. Optical view of circuit block A2. Intact, Mag. 320x.

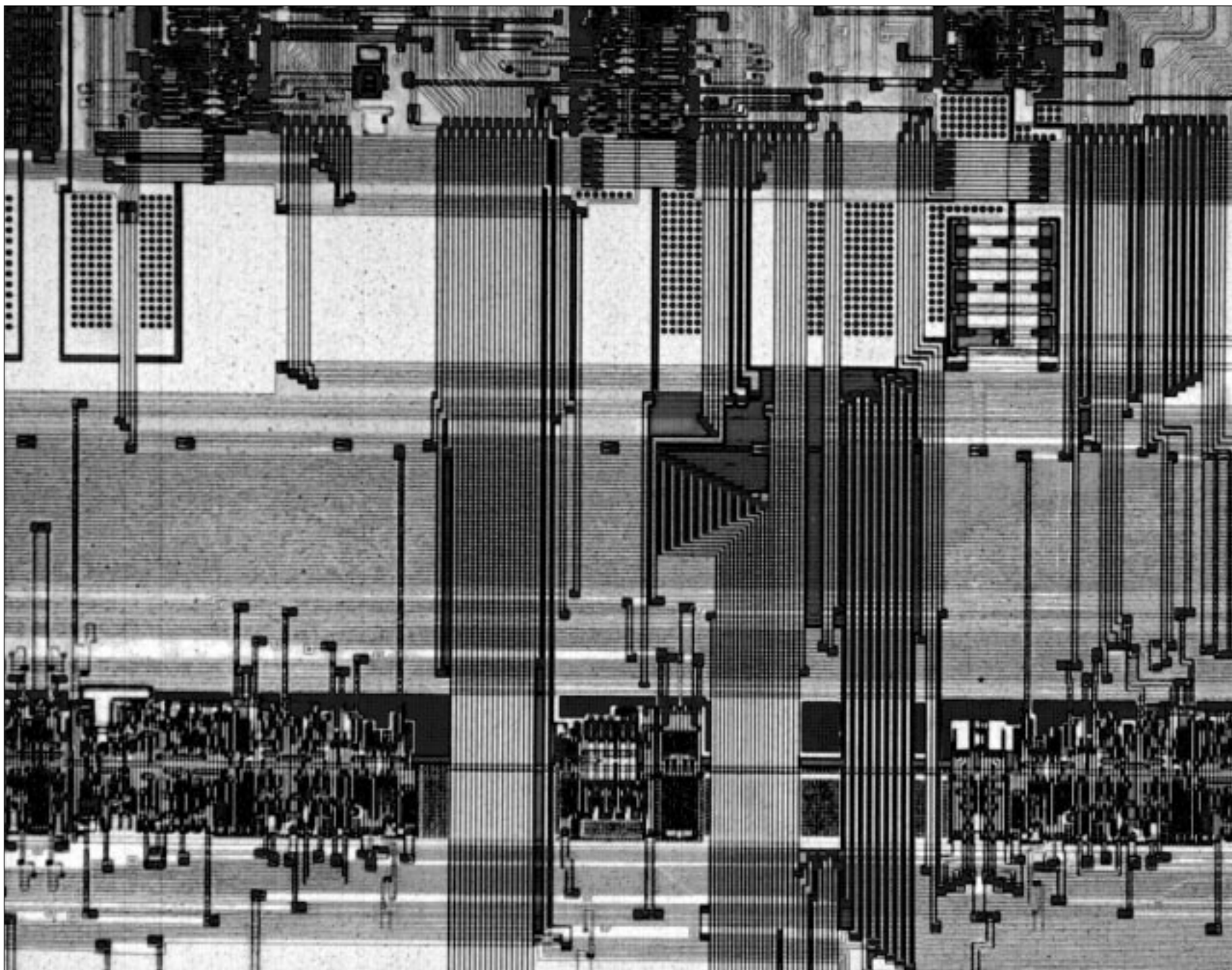


Figure 46a. Optical view of circuit block A2. Metal 1, Mag. 320x.

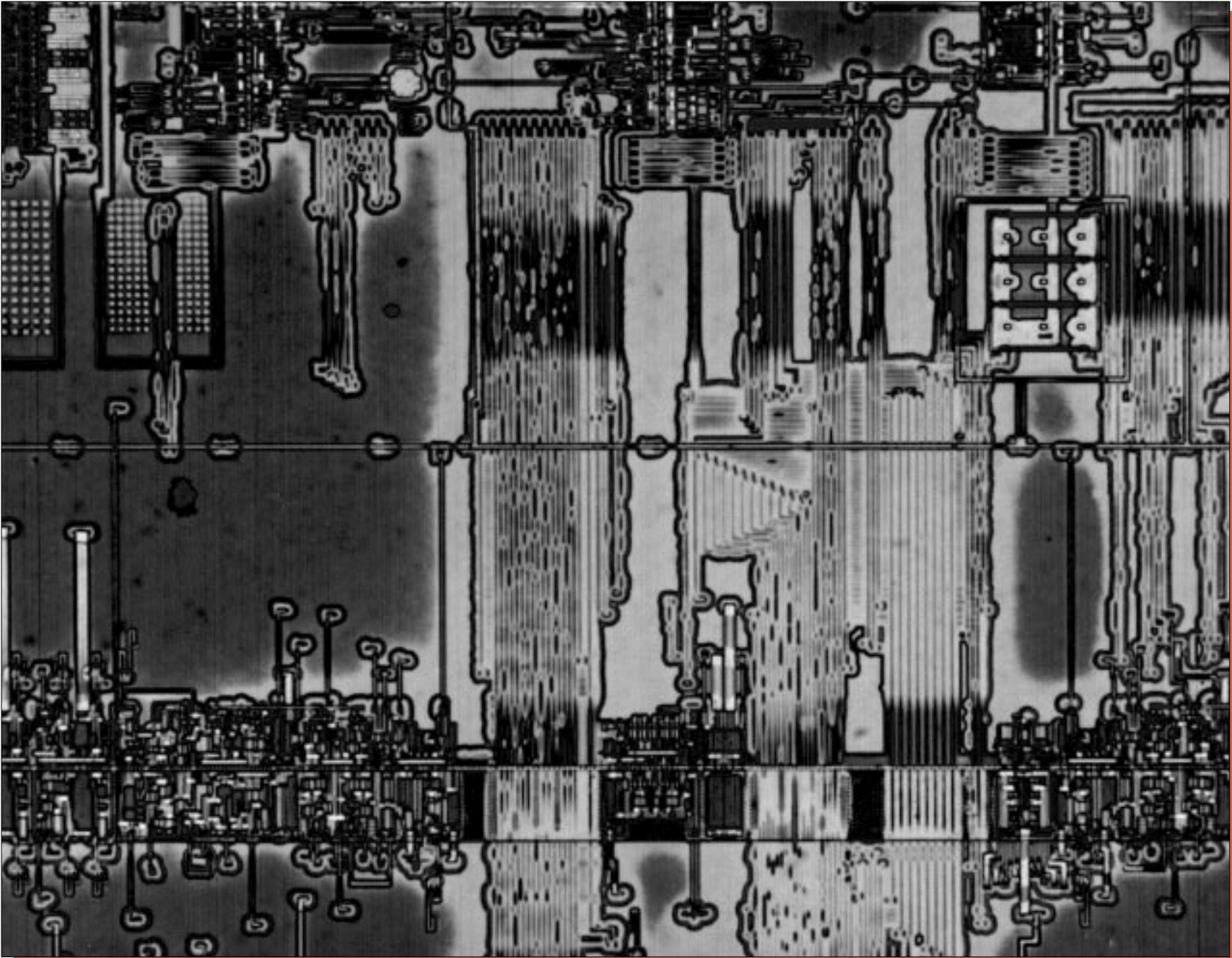


Figure 46b. Optical view of circuit block A2. Unlayered, Mag. 320x.

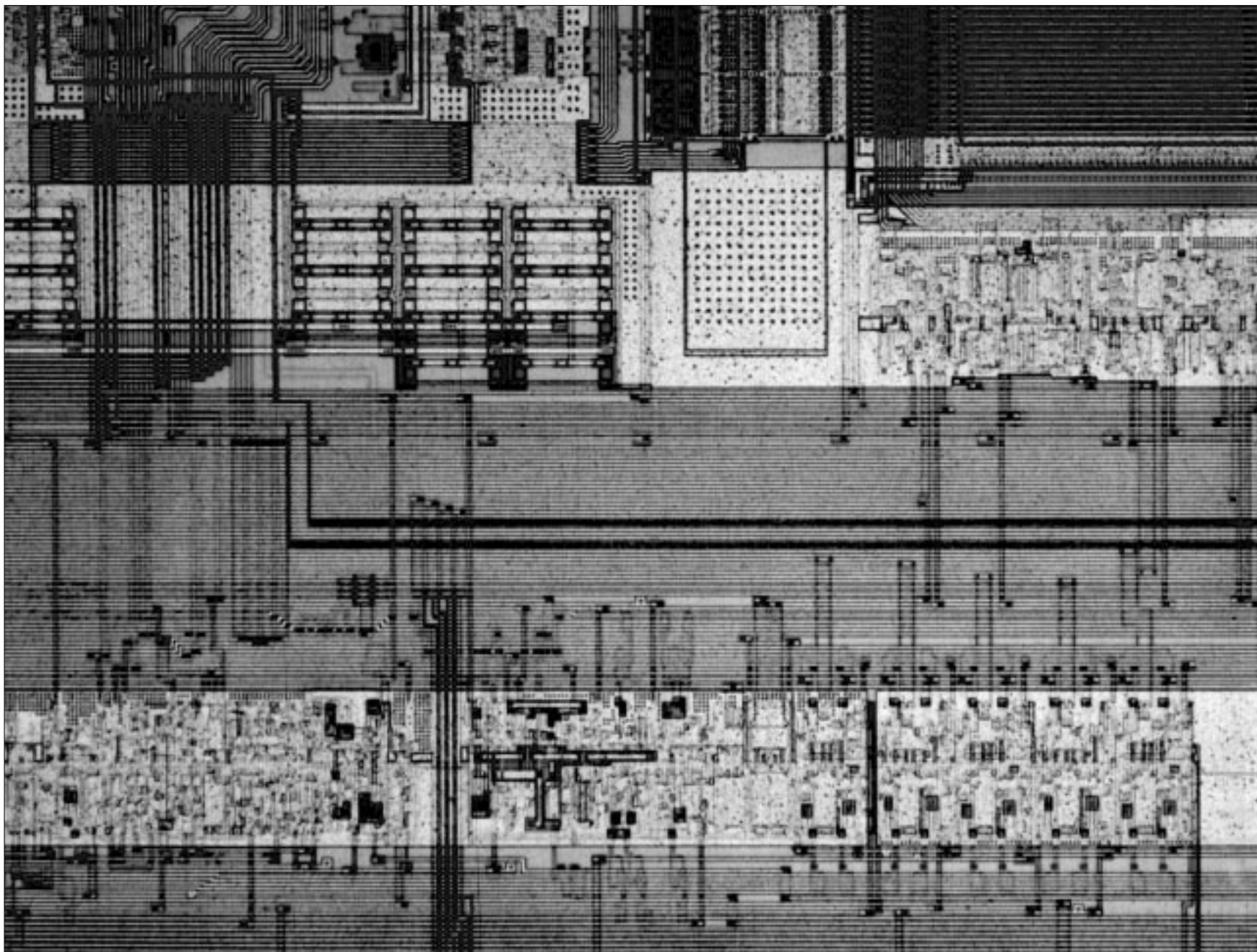


Figure 47. Optical view of circuit block A3. Intact, Mag. 320x.

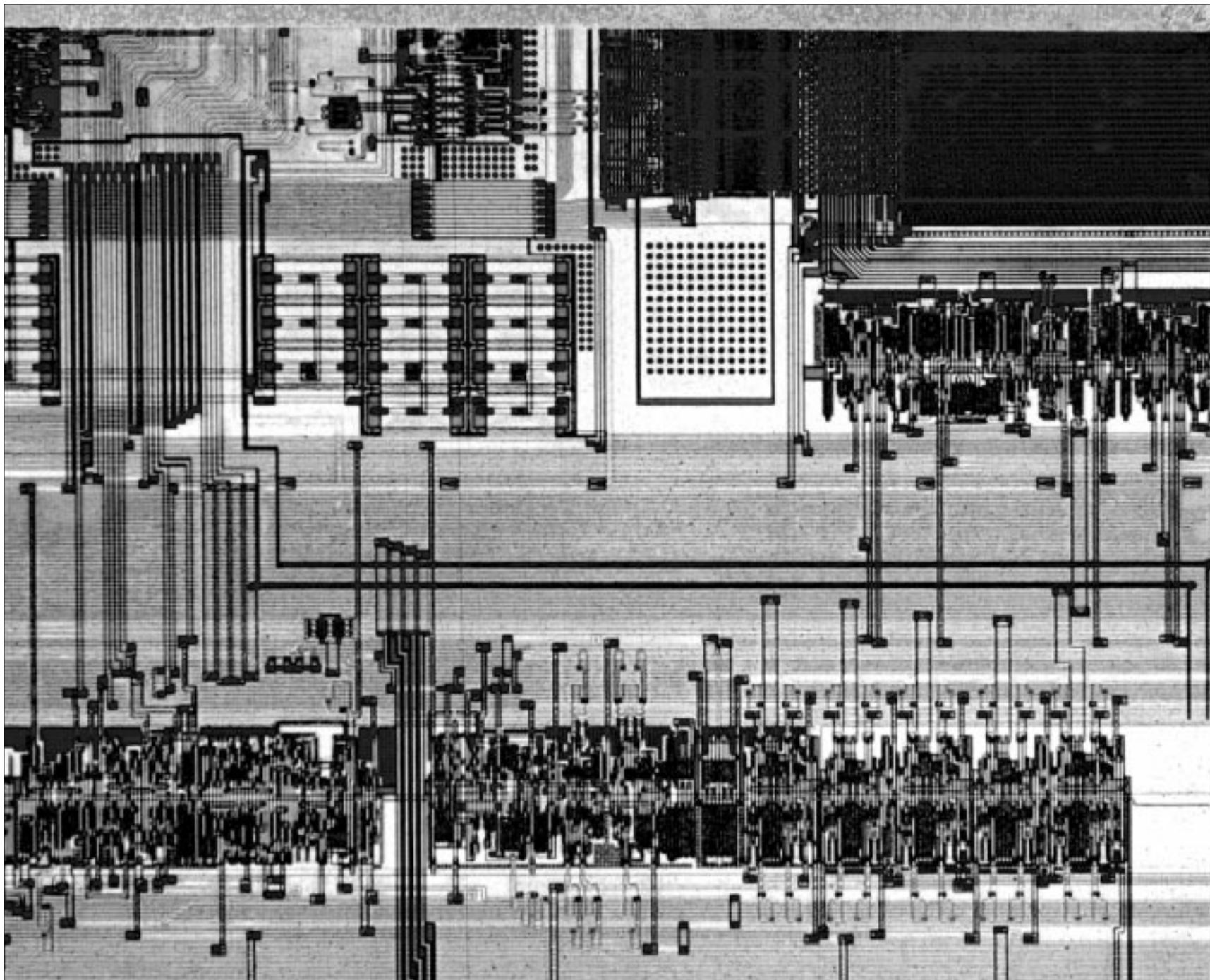


Figure 47a. Optical view of circuit block A3. Metal 1, Mag. 320x.

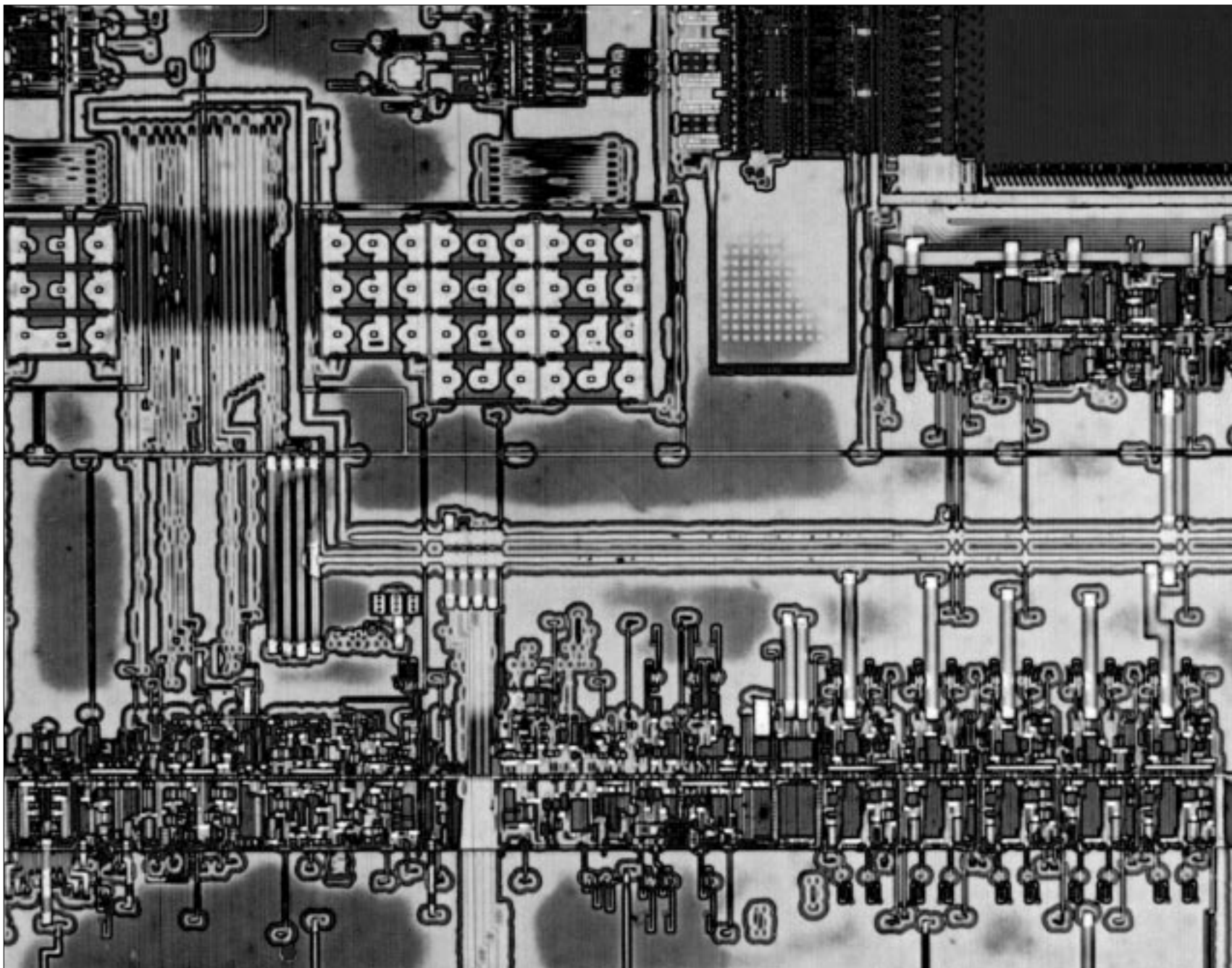


Figure 47b. Optical view of circuit block A3. Unlayered, Mag. 320x.

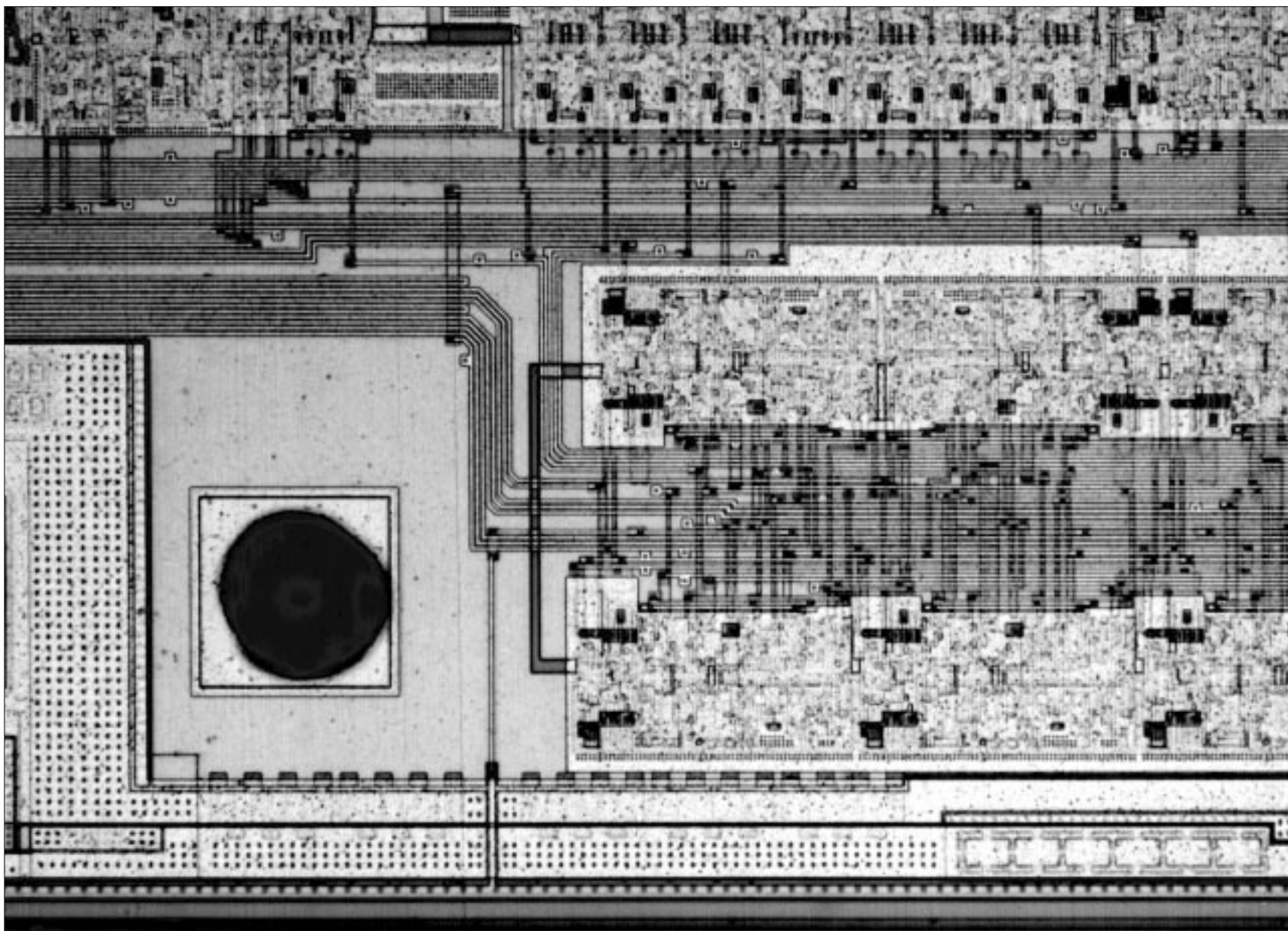


Figure 48. Optical view of circuit block A4. Intact, Mag. 320x.

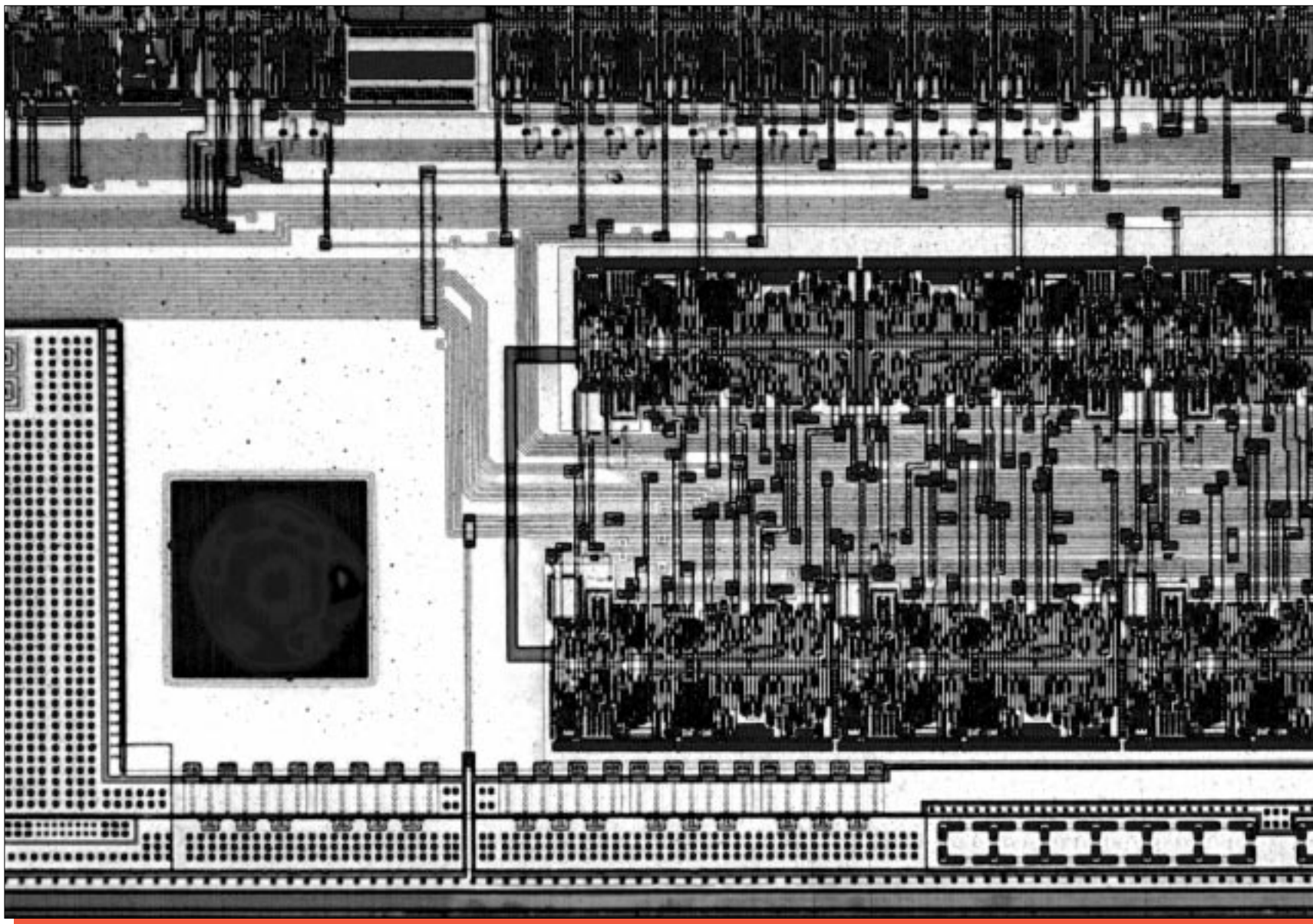


Figure 48a. Optical view of circuit block A4. Metal 1, Mag. 320x.

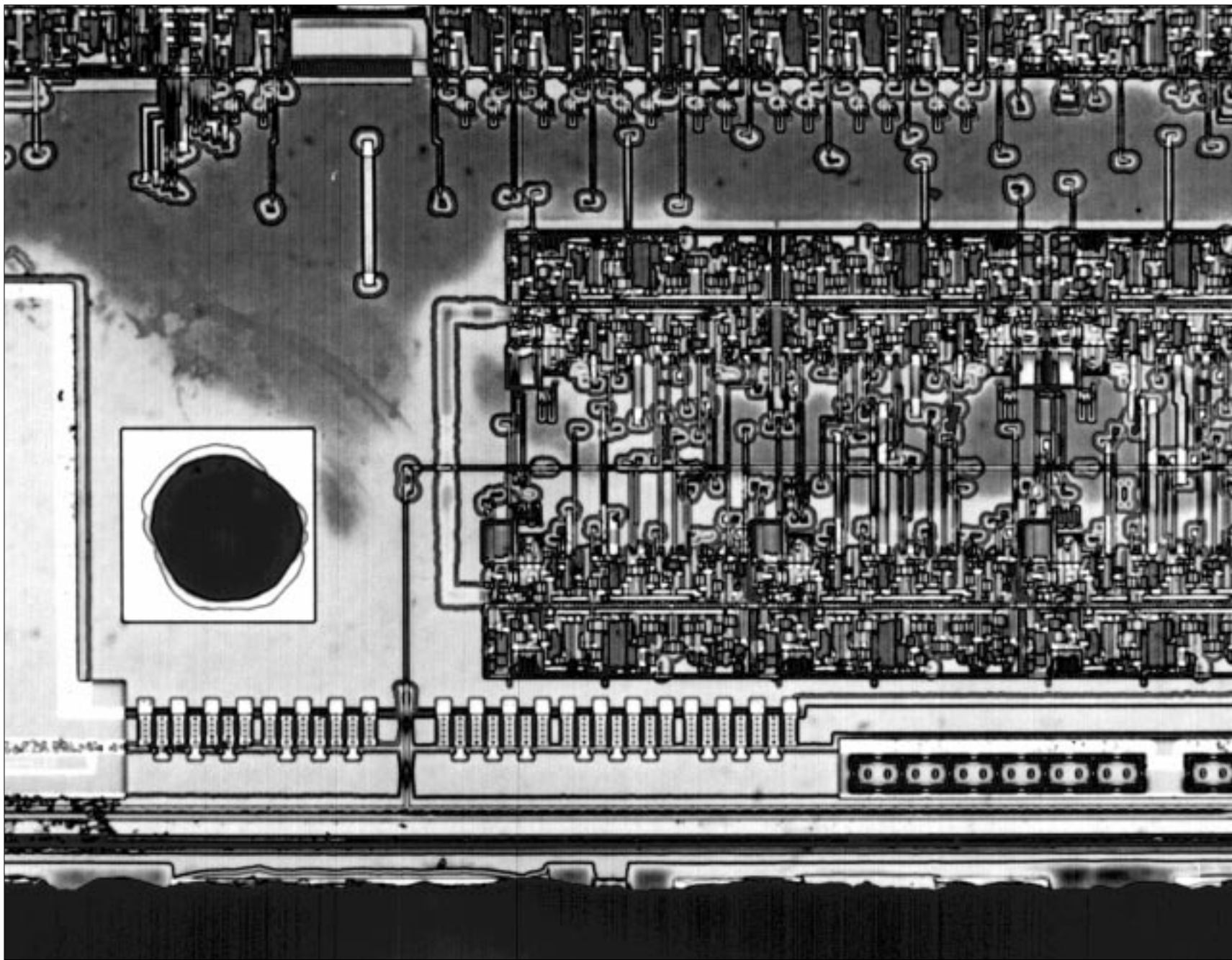


Figure 48b. Optical view of circuit block A4. Unlayered, Mag. 320x.

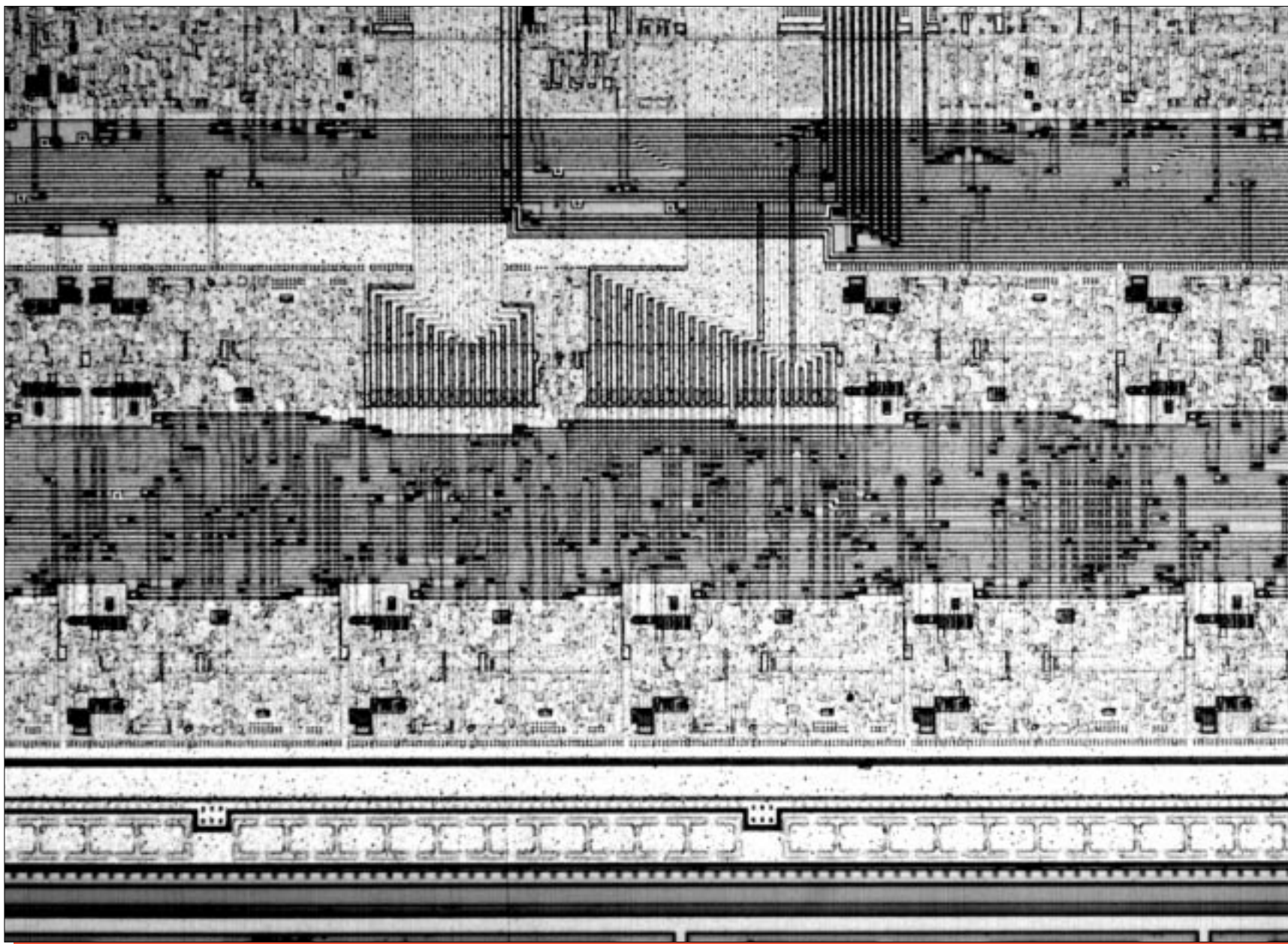


Figure 49. Optical view of circuit block A5. Intact, Mag. 320x.

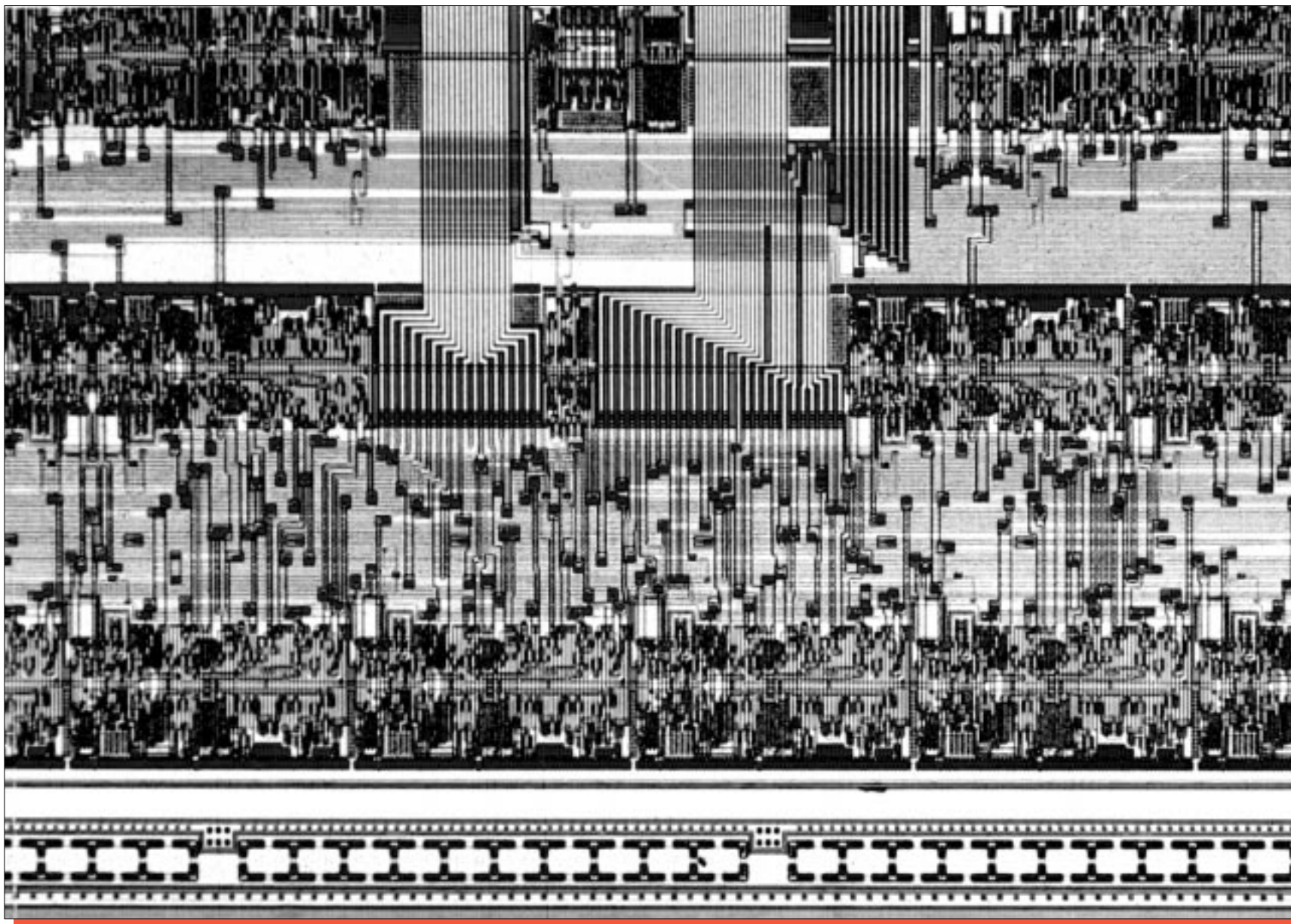


Figure 49a. Optical view of circuit block A5. Metal 1, Mag. 320x.

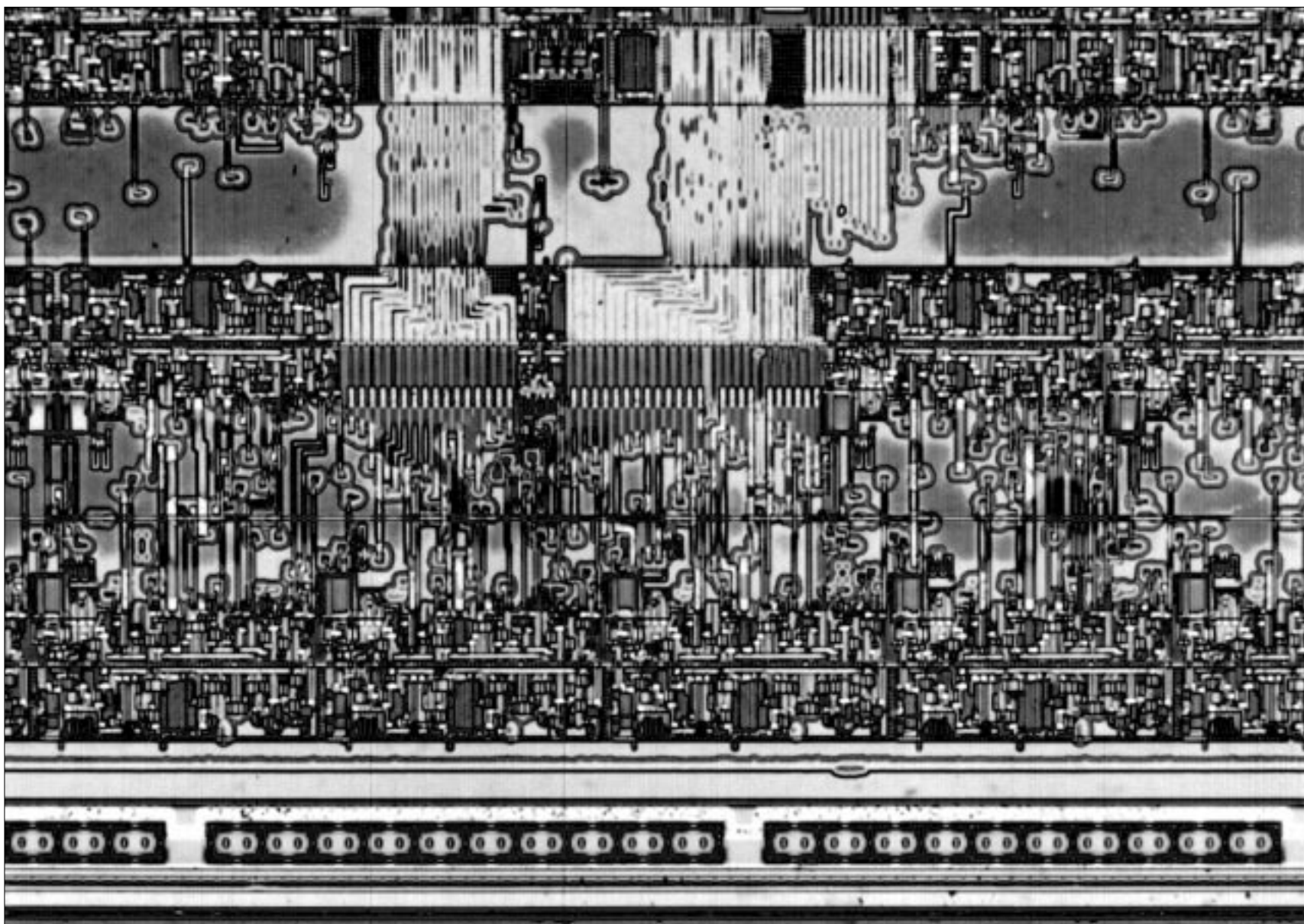


Figure 49b. Optical view of circuit block A5. Unlayered, Mag. 320x.

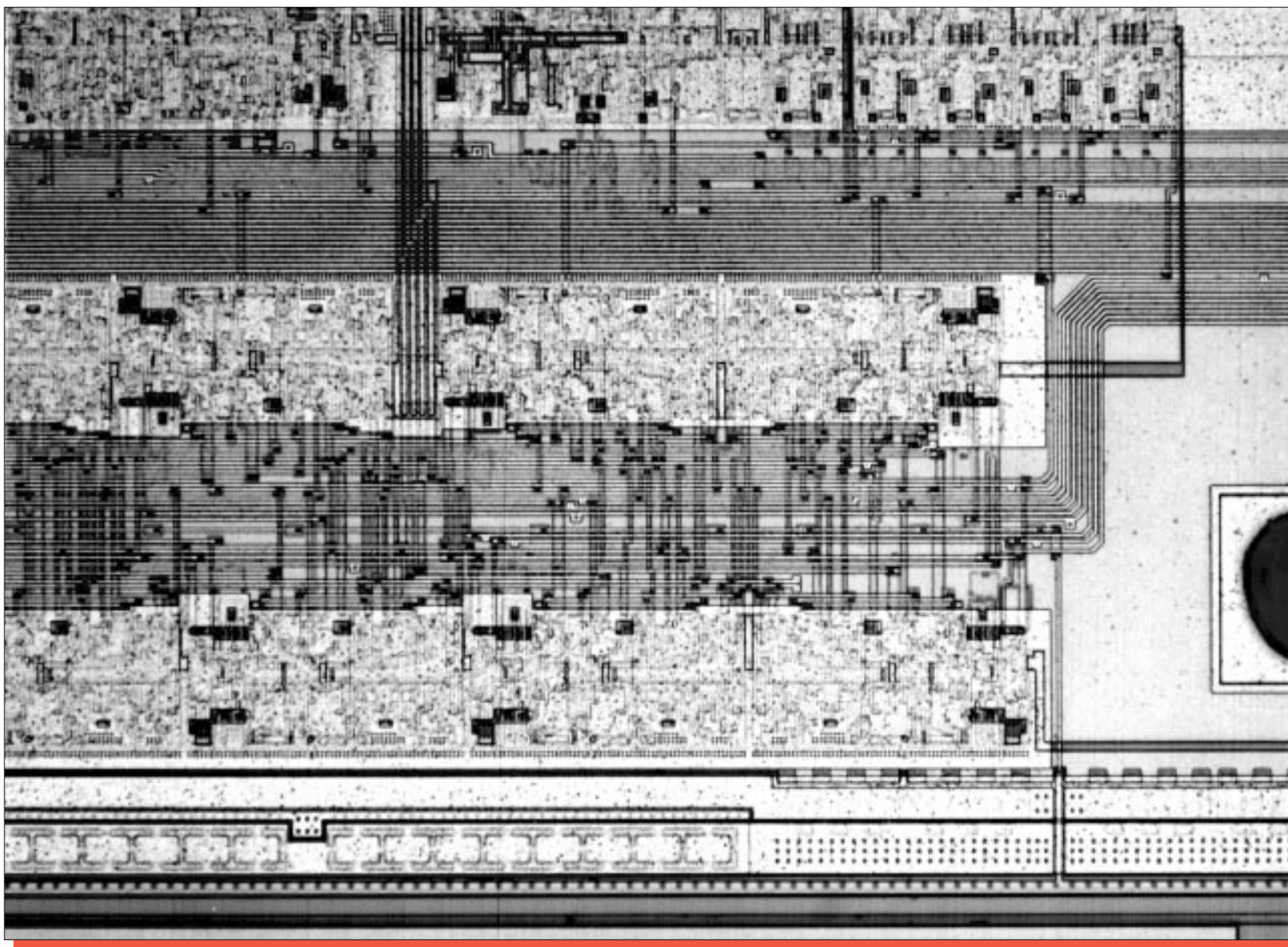


Figure 50. Optical view of circuit block A6. Intact, Mag. 320x.

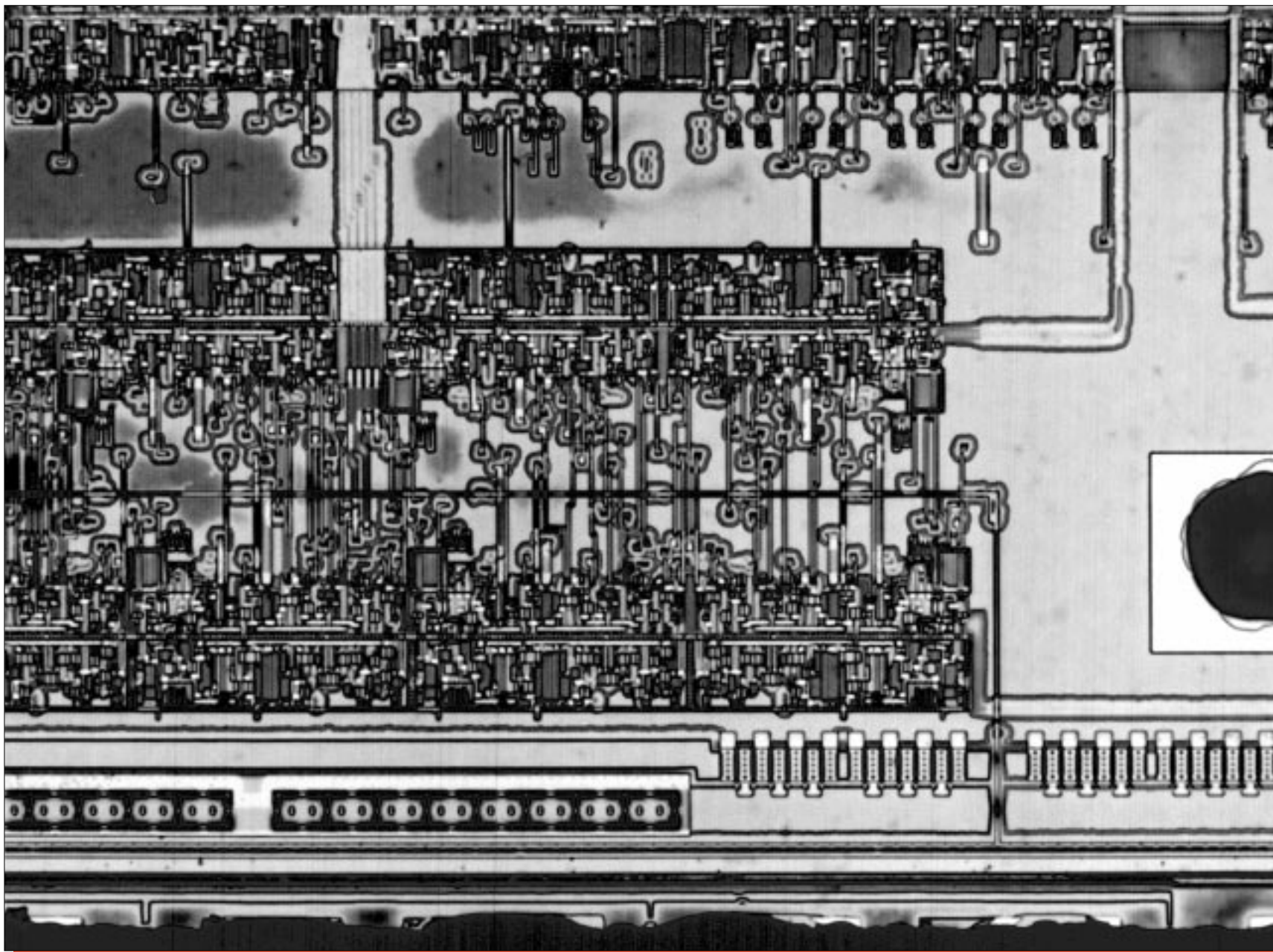


Figure 50a. Optical view of circuit block A6. Metal 1, Mag. 320x.

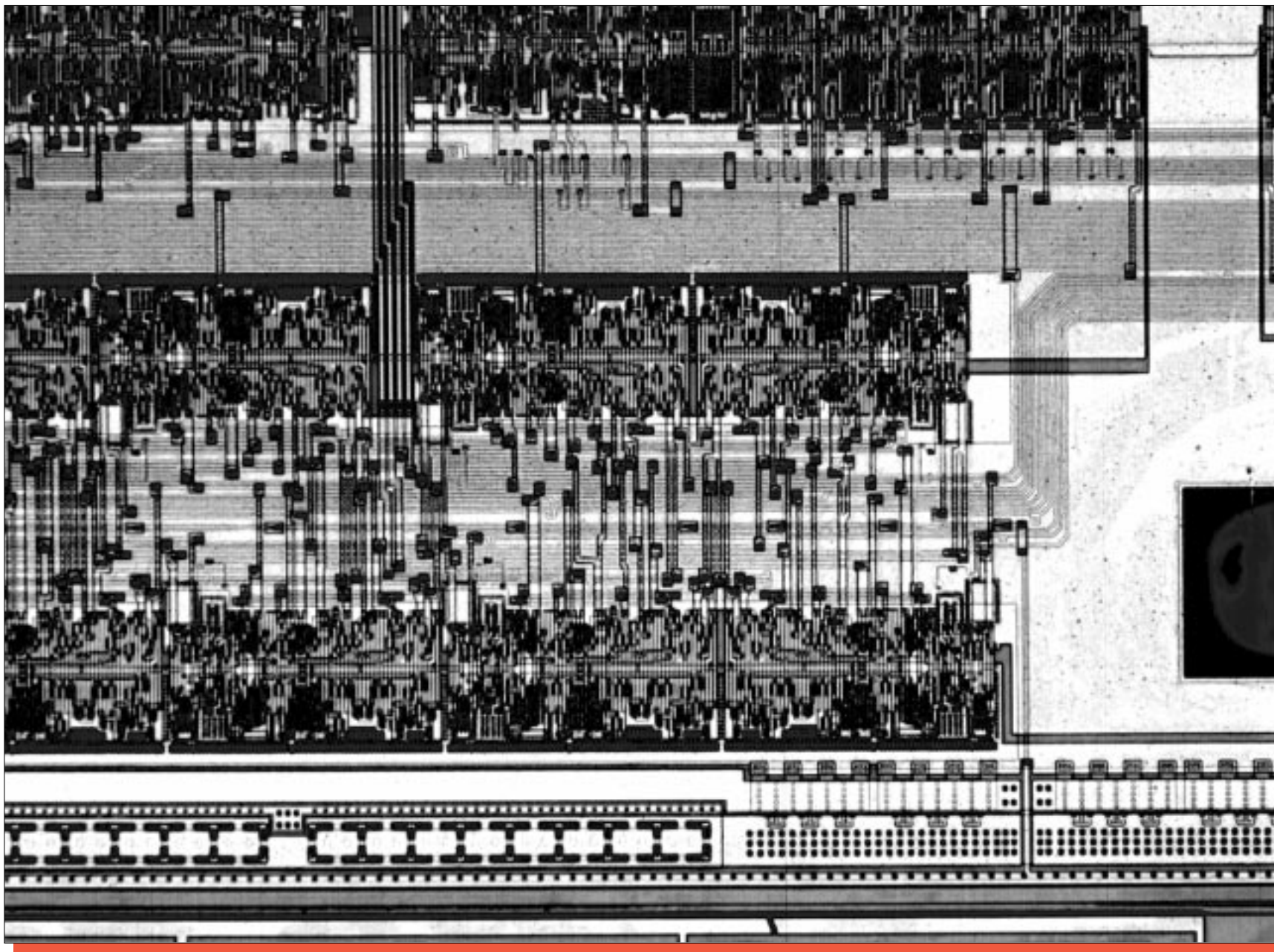


Figure 50b. Optical view of circuit block A6. Unlayered, Mag. 320x.

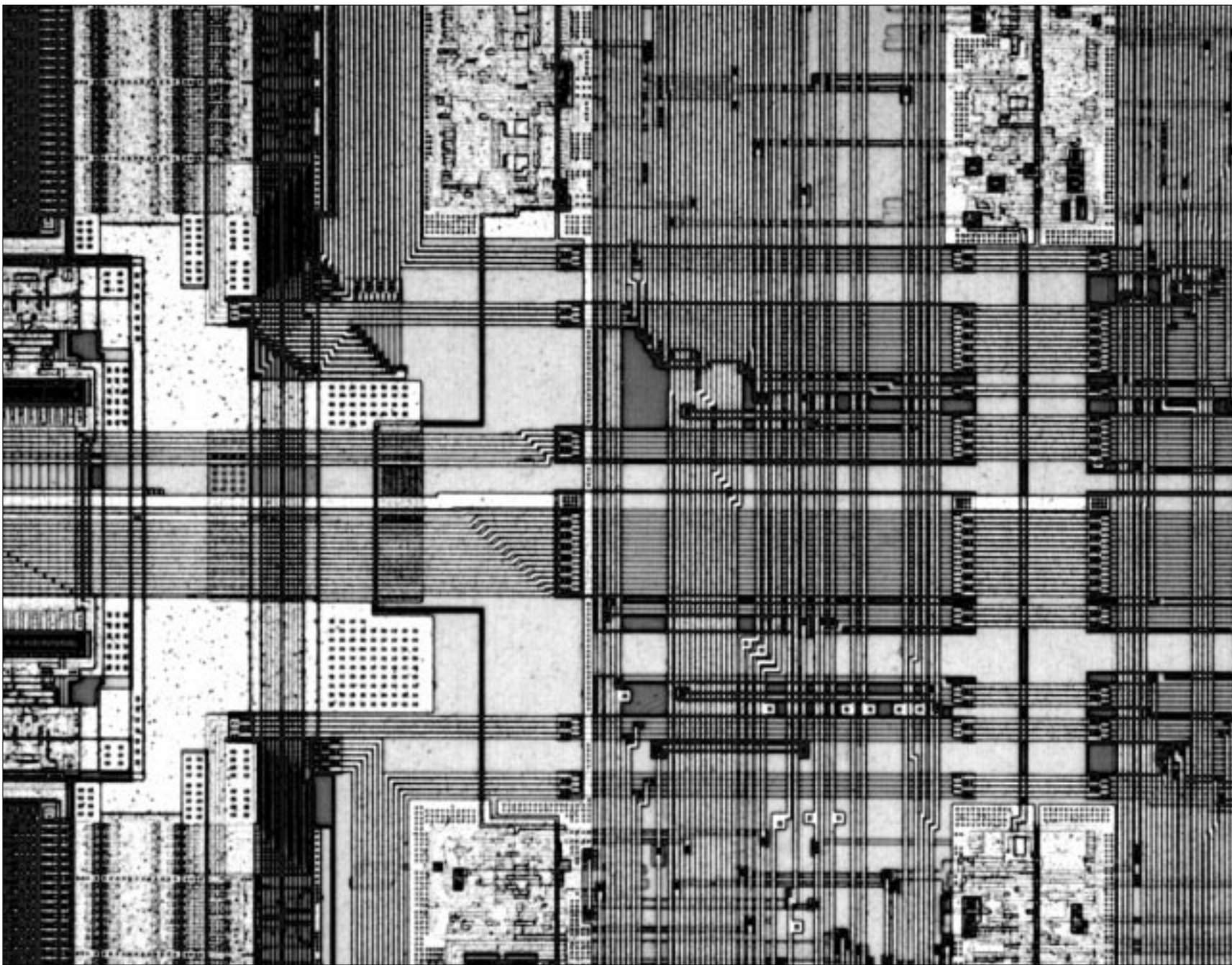


Figure 51. Optical view of circuit block B. Intact, Mag. 320x.

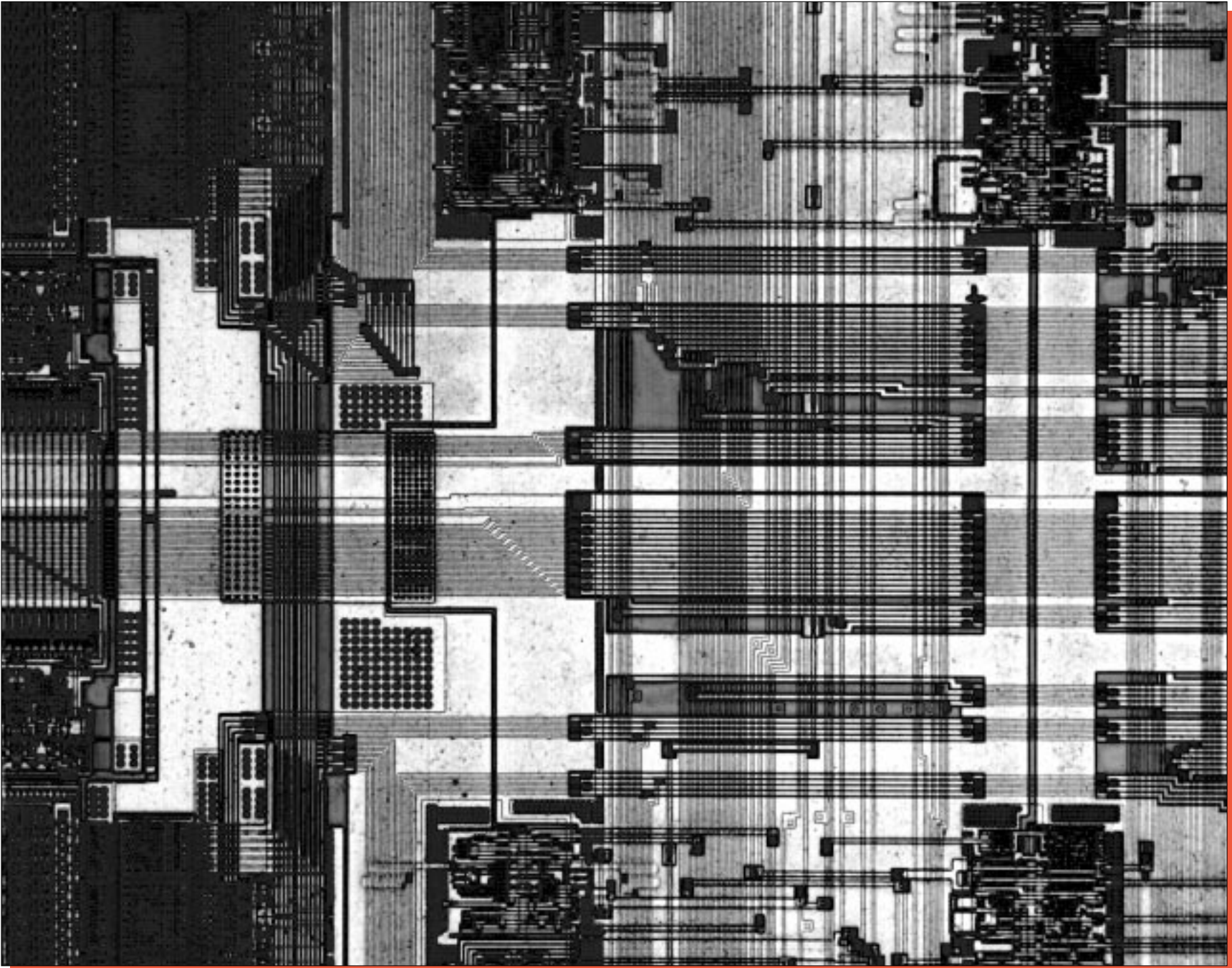


Figure 51a. Optical view of circuit block B. Metal 1, Mag. 320x.

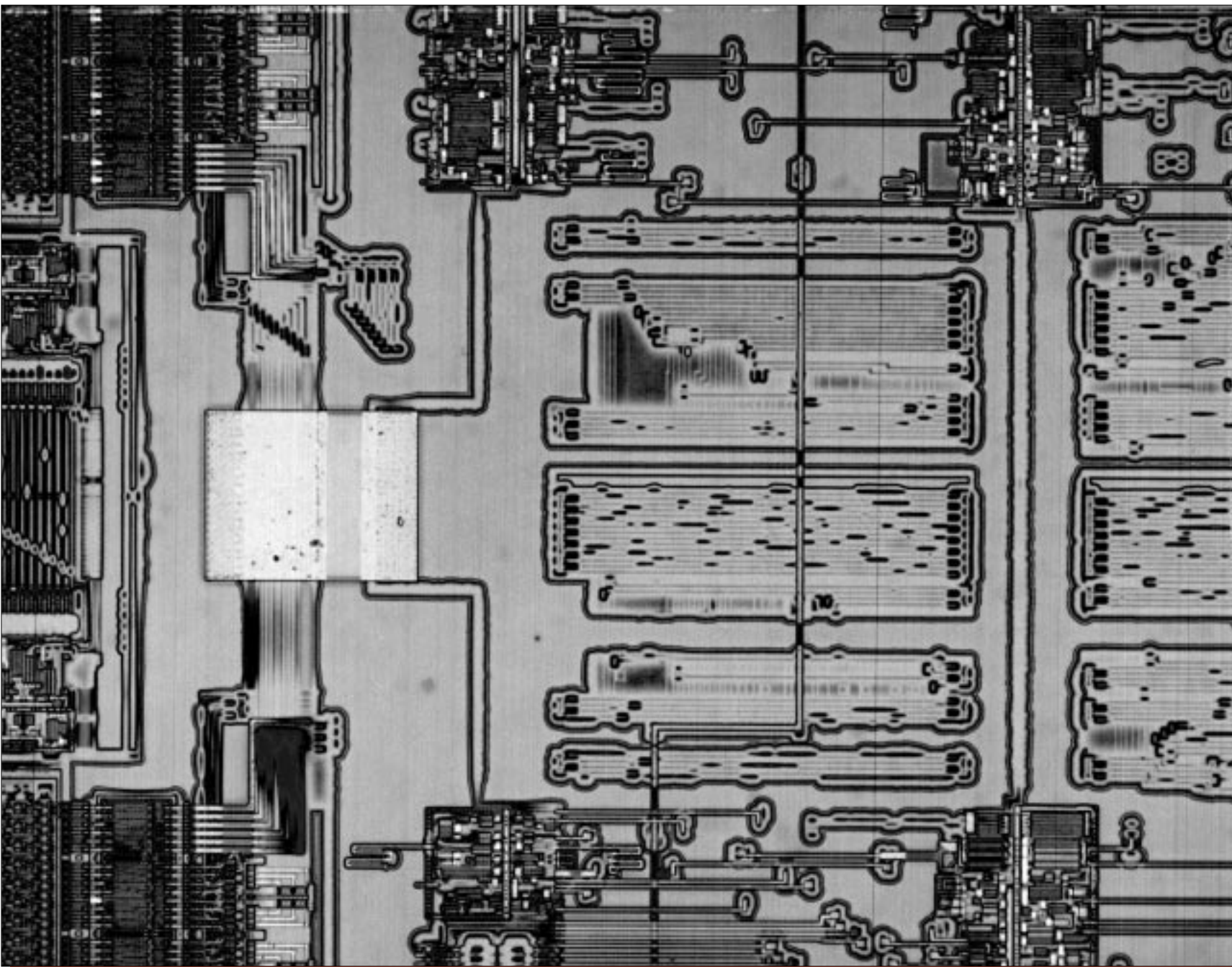


Figure 51b. Optical view of circuit block B. Unlayered, Mag. 320x.

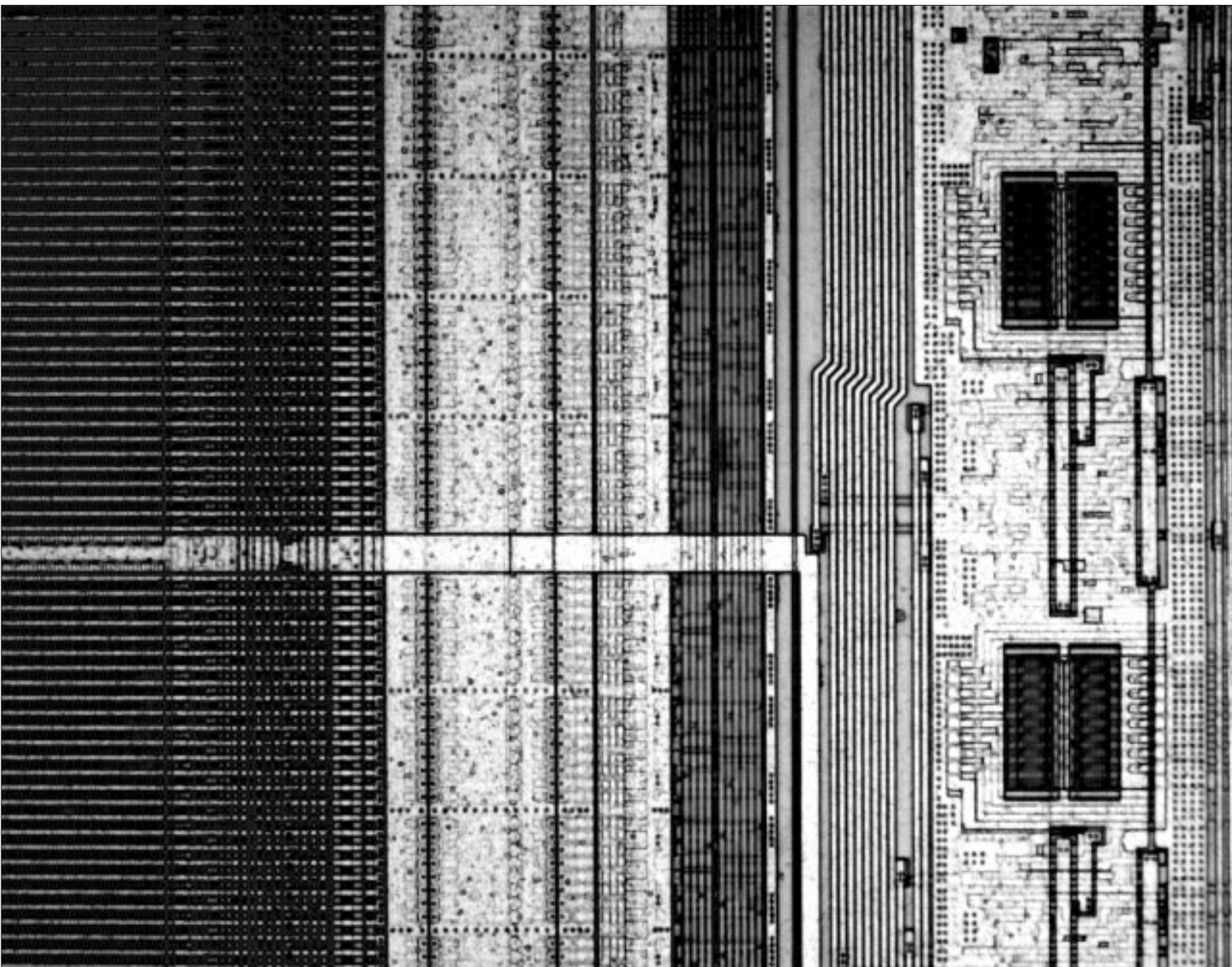


Figure 52. Optical view of circuit block C. Intact, Mag. 320x.

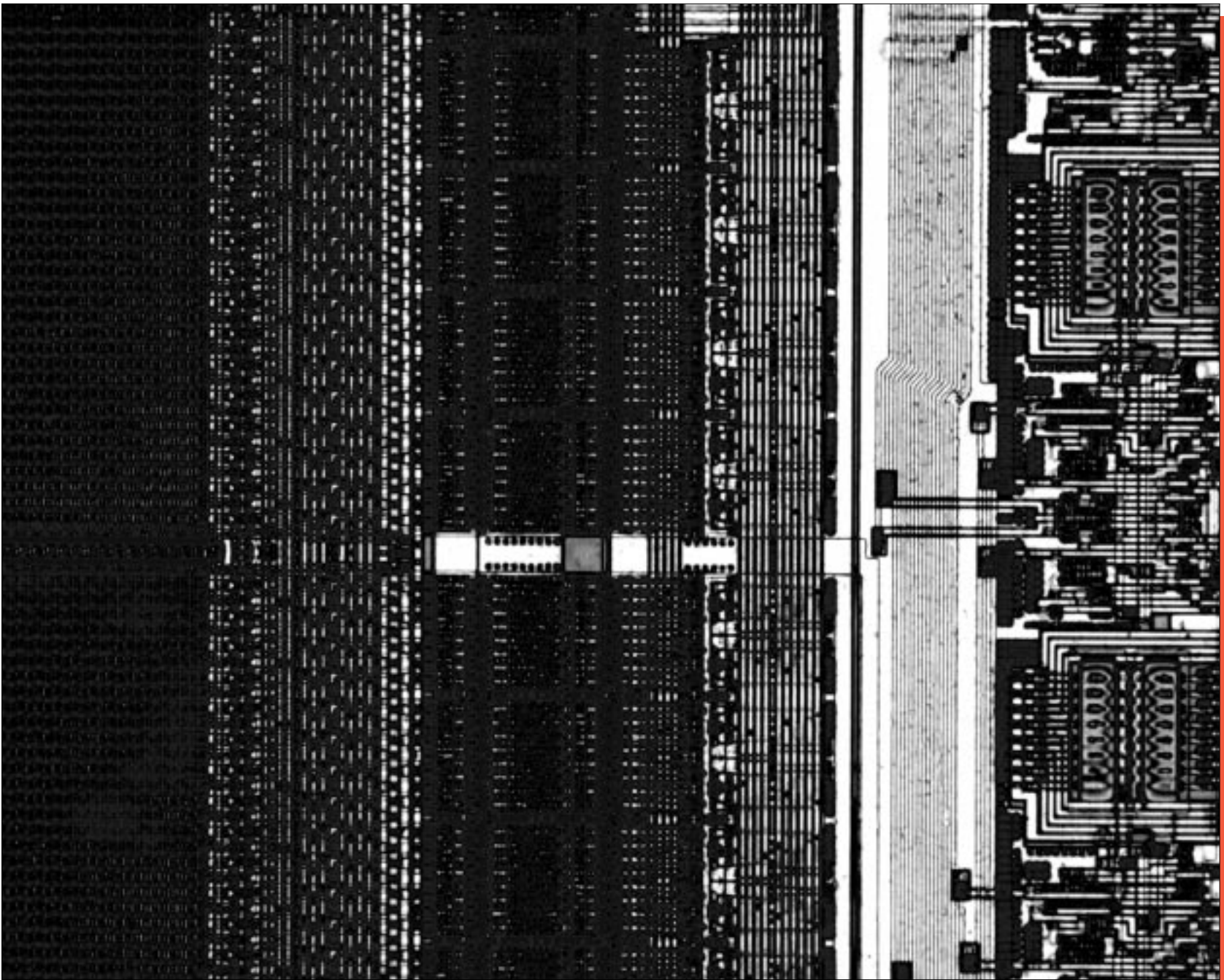


Figure 52a. Optical view of circuit block C. Metal 1, Mag. 320x.

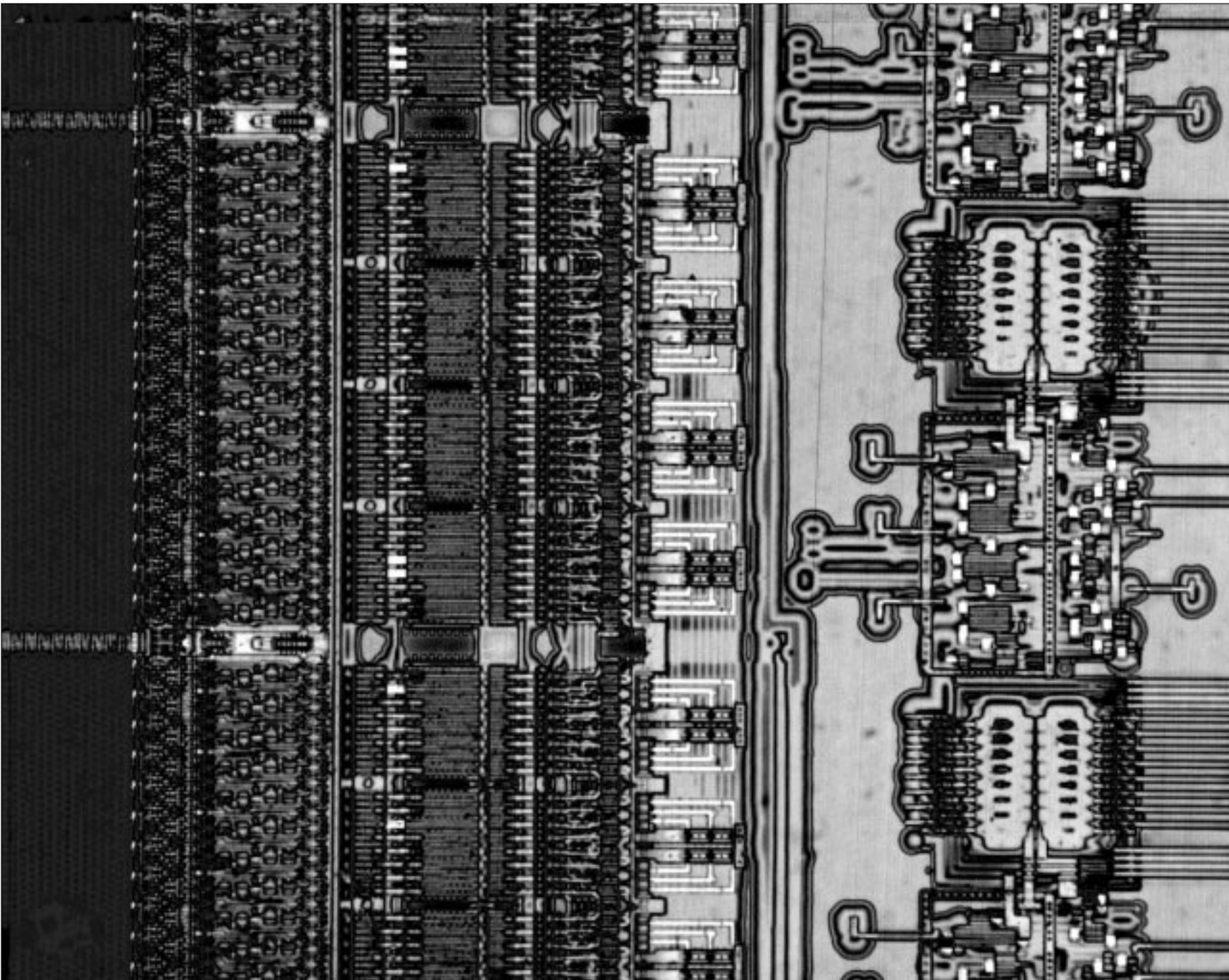


Figure 52b. Optical view of circuit block C. Unlayered, Mag. 320x.

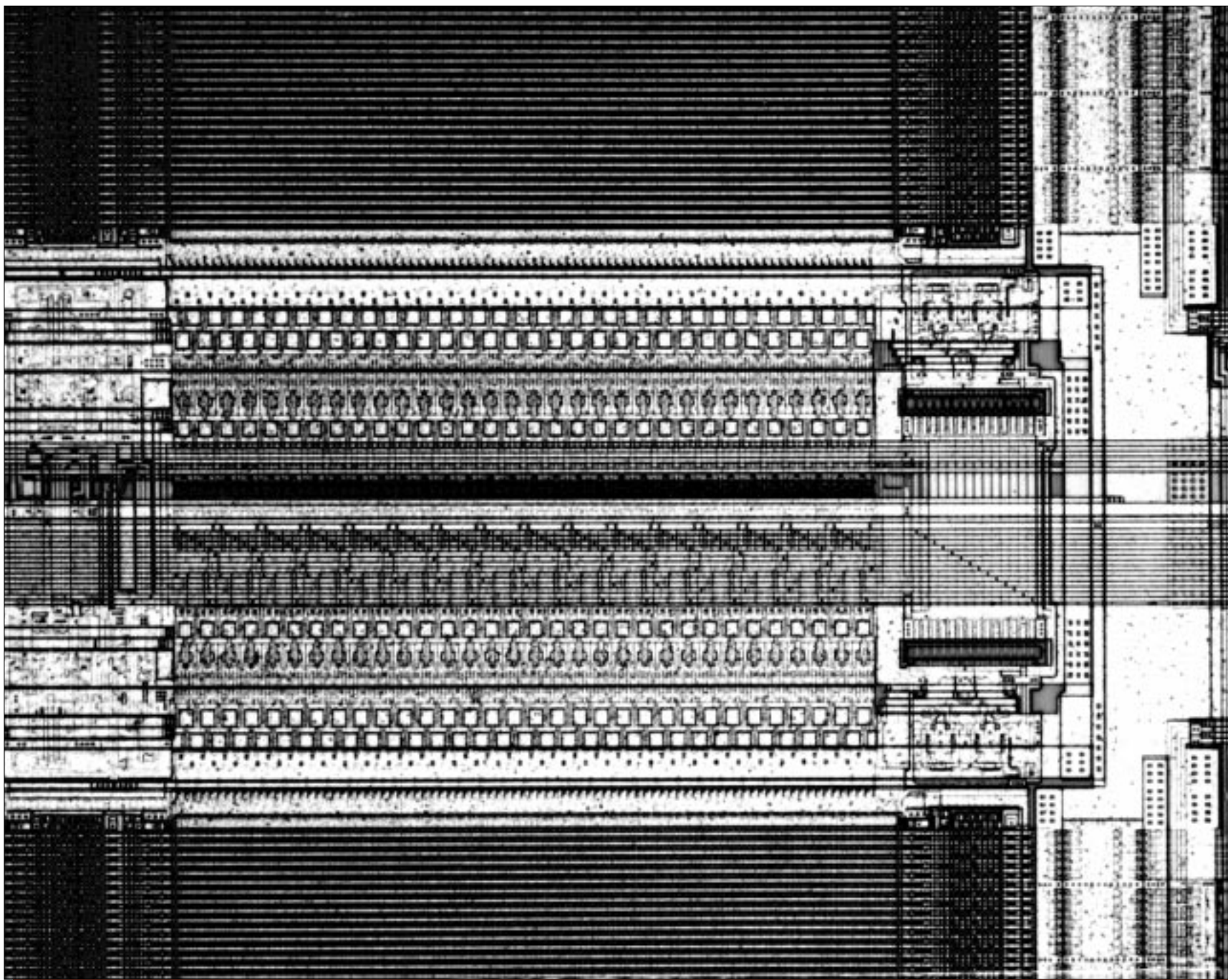


Figure 53. Optical view of circuit block D. Intact, Mag. 320x.

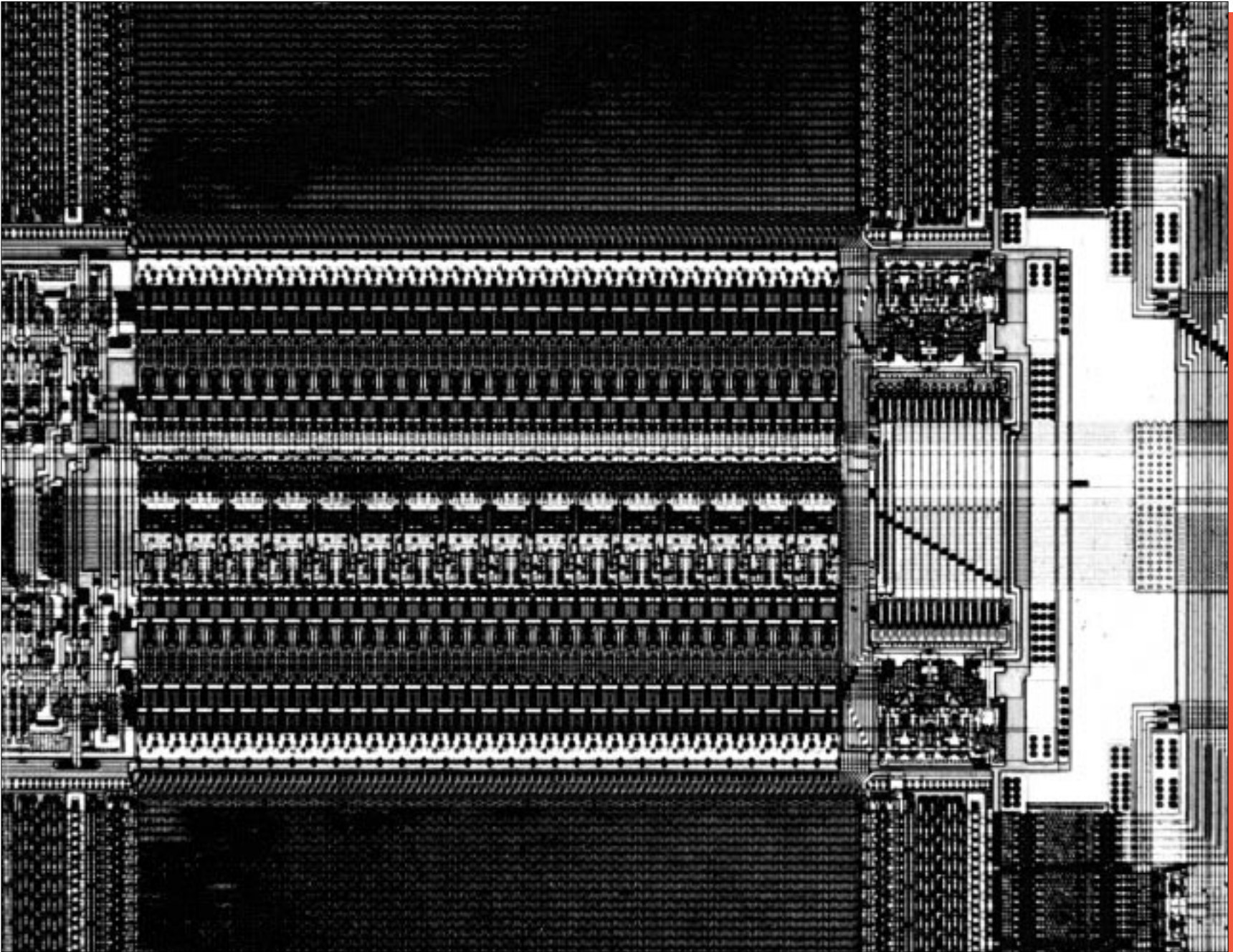


Figure 53a. Optical view of circuit block D. Metal 1, Mag. 320x.

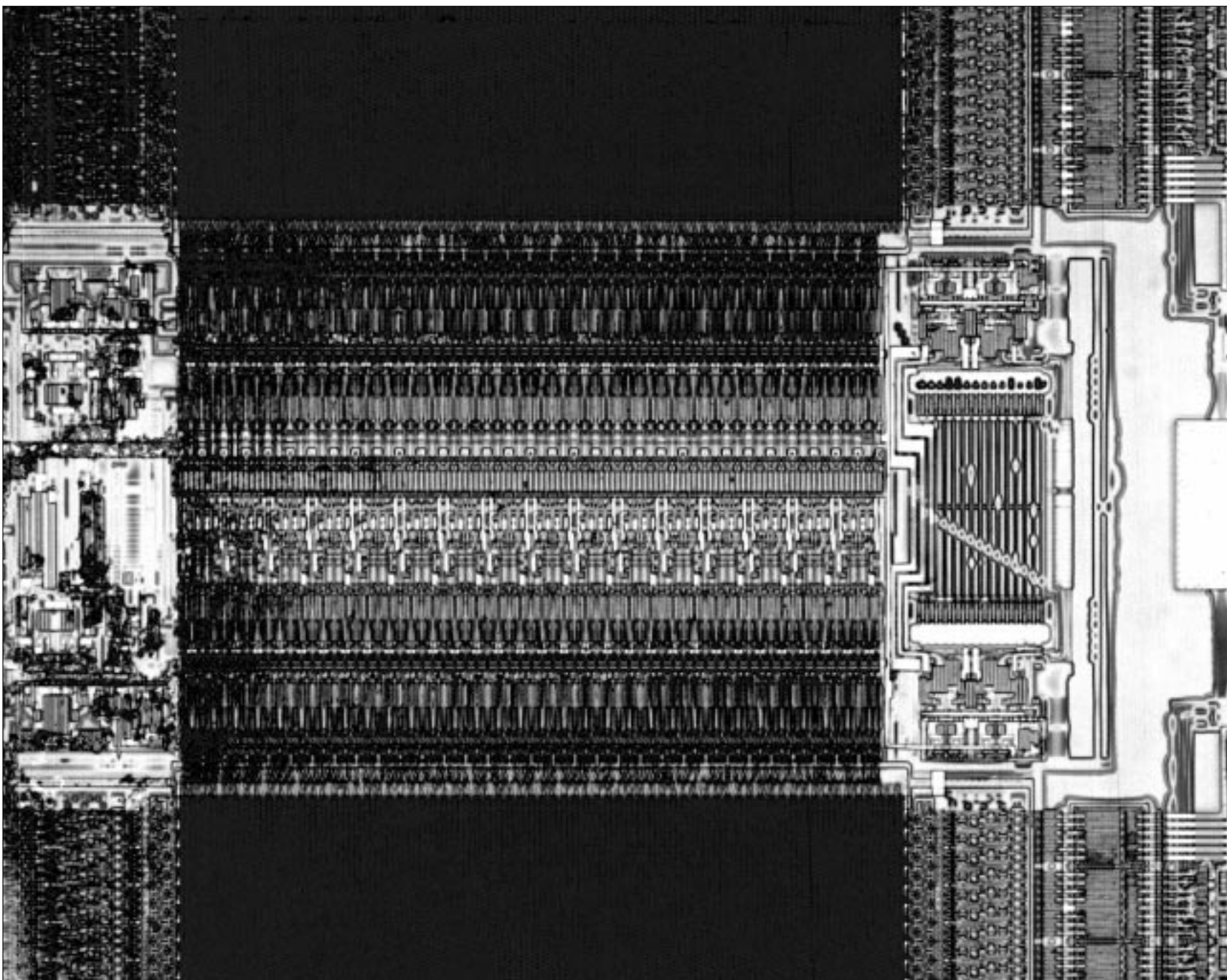


Figure 53b. Optical view of circuit block D. Unlayered, Mag. 320x.

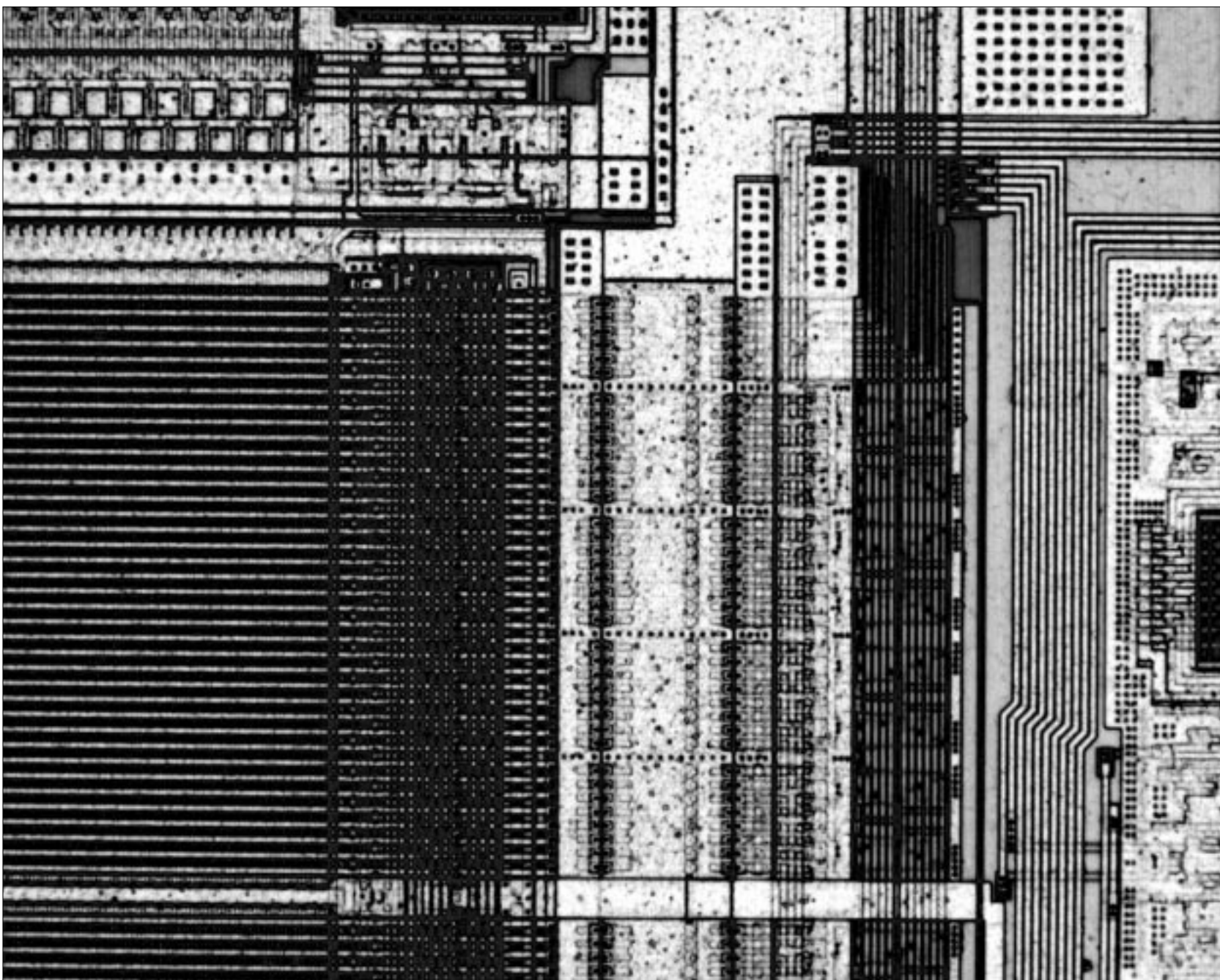


Figure 54. Optical view of circuit block E. Intact, Mag. 320x.

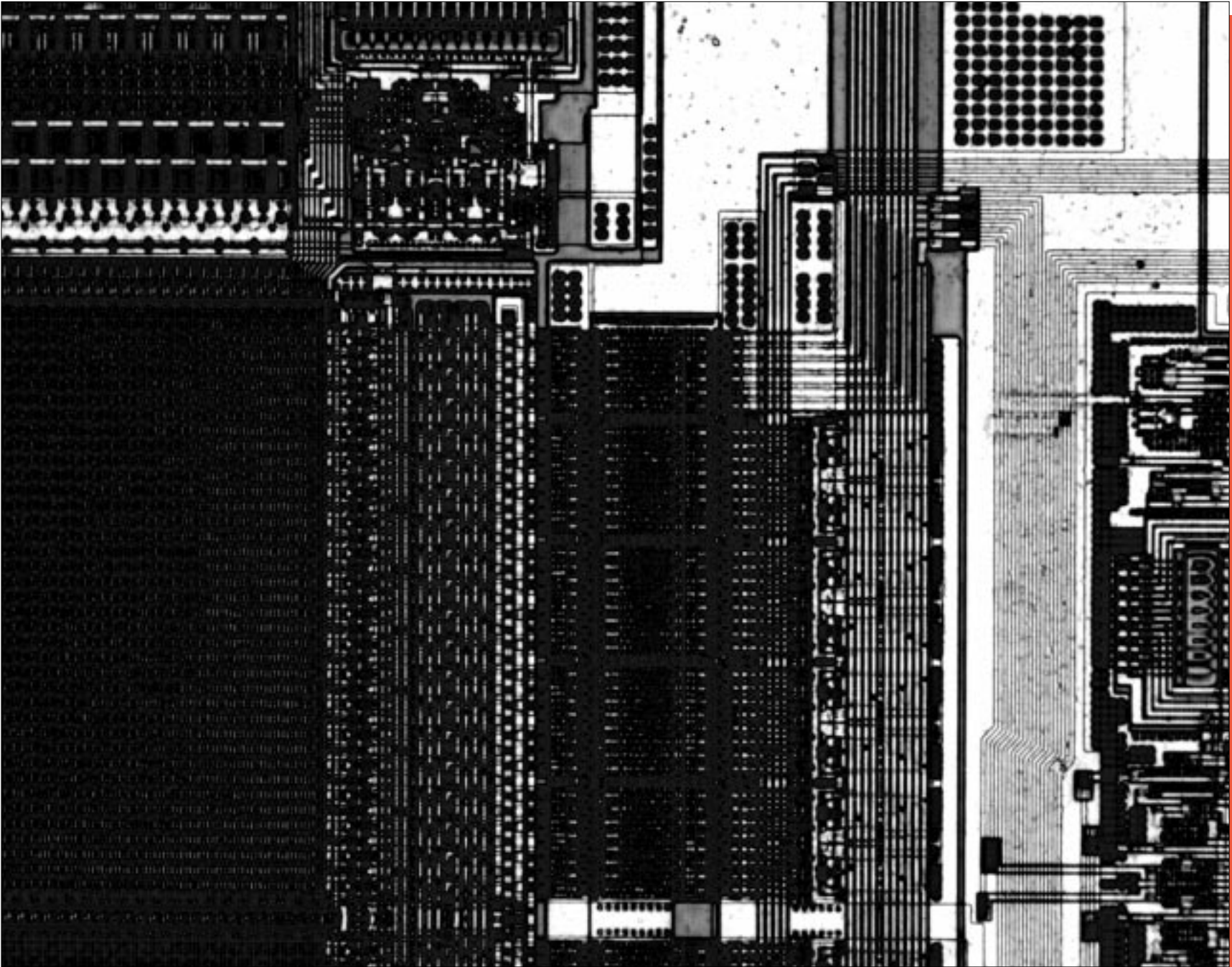


Figure 54a. Optical view of circuit block E. Metal 1, Mag. 320x.

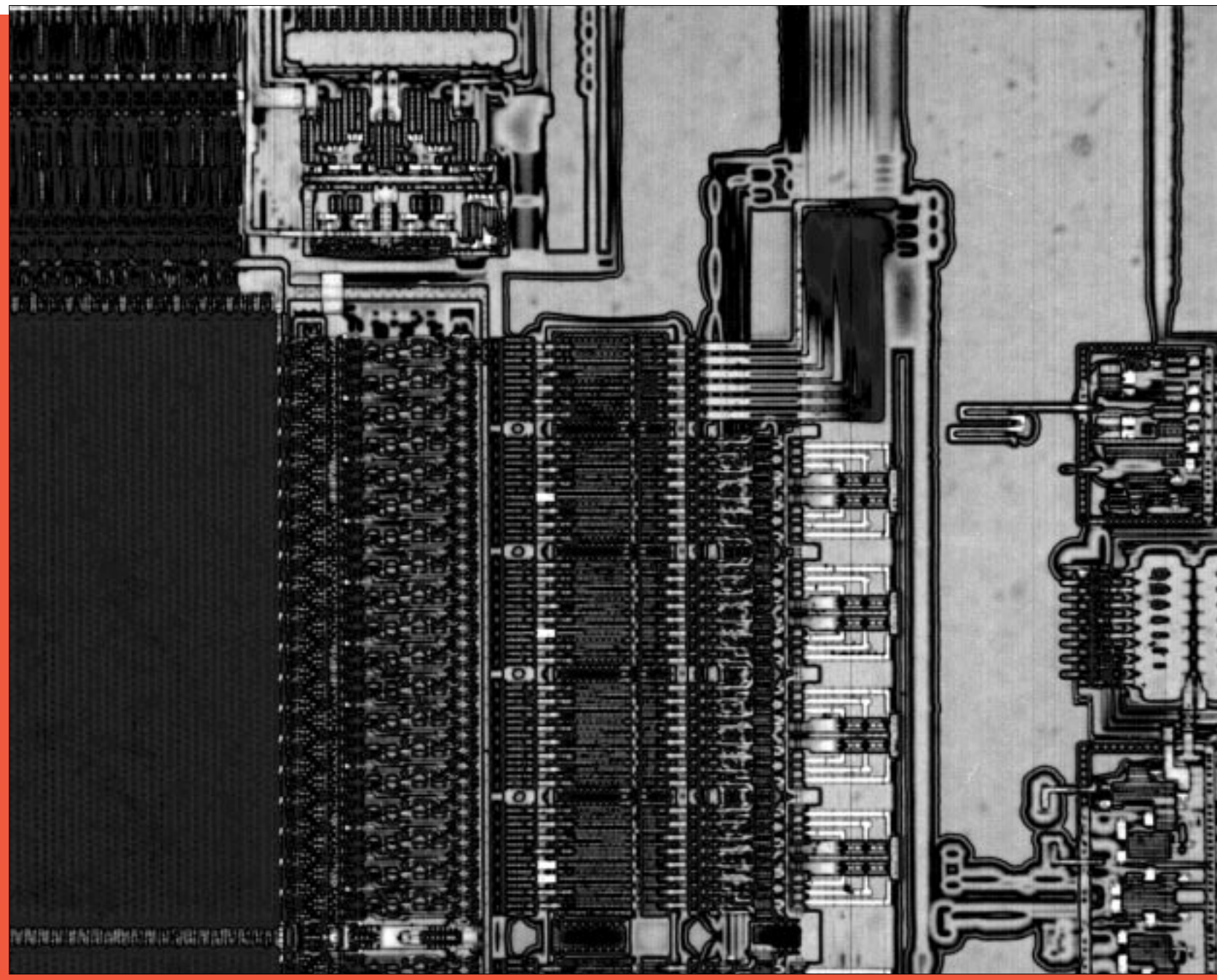


Figure 54b. Optical view of circuit block E. Unlayered, Mag. 320x.