

Construction Analysis

AMD MACH5 512 Complex Programmable Logic Device

Report Number: SCA 9702-526



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INTRODUCTION

This report describes a construction analysis of the AMD MACH5 512 Complex Programmable Logic Device (CPLD). One decapsulated device was supplied for the analysis. Mask date was 1996.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

- CMP planarization.
- Poly 2 used as a type of local interconnect.
- 0.35 micron gates.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Die Process:

- Devices were fabricated using a selective oxidation, P-well CMOS process in a P-substrate with N- epi.
- Passivation consisted of a layer of silicon-nitride over a layer of silicon-dioxide.
- Metallization employed of three layers of dry-etched metal. All metal layers consisted of aluminum with a titanium-nitride cap. No barrier materials were employed. Vias and contacts were formed using tungsten plugs.
- Intermetal dielectrics consisted of a thin layer of glass followed by a spin-on-glass (SOG) and another thick layer of glass. The SOG appeared to have been subjected to an etchback.
- Pre-metal dielectric consisted of a layer of reflow glass (probably BPSG) over various densified oxides. The glass was reflowed prior to contact cuts only.
- Two layers of poly (no silicide) were used on the die. Poly 2 was formed a type of local interconnect in the periphery and in one of the EEPROM arrays. It contacted both poly 1 and N+. Poly 1 was used to form all gates on the die and the select/word lines in the EEPROM cell arrays. Definition of the poly was by a dry etch.
- Buried contacts were employed using poly 2 to N+ diffusions.
- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

TECHNOLOGY DESCRIPTION (continued)

- Local oxide (LOCOS) isolation. No step was present in the oxide at the edge of the well boundaries indicating that probably only single polarity wells were used along with the epi.
- Two similar EEPROM layout designs were employed on the device.
- Memory cell “A” consisted of a 3T, single capacitor, EEPROM design. Metal 1 was used to form the select line, program line, output connections and to distribute GND. Poly 1 was used to form the transistors, one plate of the capacitor and the tunnel-oxide device. Memory cell “B” also consisted of a 3T, single capacitor, EEPROM design. Metal 1 was used to form the select line, program line, output and enable lines and poly 1 formed the transistors, one plate of the capacitor and the tunnel oxide device. Programming of both cell types was achieved through the thin tunnel oxide.
- Redundancy fuses were not present.

ANALYSIS RESULTS

Die Process:

Figures 1 - 41

Questionable Items:¹ None.

Special Features:

- CMP planarization.
- Poly 2 used as a type of local interconnect.
- 0.35 micron gates.

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, P-well CMOS process in a P substrate with N-epi.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Overlay passivation: A layer of silicon-nitride over a layer of silicon-dioxide. Overlay integrity was good (no defects noted). Edge seal was good as it extended into the scribe lane to seal the metallization.
- Metallization: Three layers of dry-etched metal. All metal layers consisted of aluminum with a titanium-nitride cap. No barrier materials were employed. Vias and contacts were formed using tungsten plugs. Metal 3 and metal 2 bus lines were slotted for stress relief.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS (continued)

- Metal patterning: All metal layers were patterned by a dry etch of normal quality.
- Metal defects: No voiding, notching, or neckdown was noted in the metal layers. No silicon nodules were found following the removal of the aluminum layer.
- Vias and contacts: Vias and contacts were formed using tungsten on a titanium adhesion layer.
- Metal step coverage: Metal thinning was not present due to the use of tungsten plugs at vias and contacts and chemical-mechanical planarization (CMP) was employed after plug formation and at all three levels.
- Intermetal dielectrics consisted of a thin layer of glass followed by a spin-on-glass (SOG) and another thick layer of glass. The SOG appeared to have been subjected to an etchback, and as stated above CMP was used under each layer of metallization.
- Pre-metal dielectric: A layer of CVD glass over various densified oxides was used under the metal 1. It was planarized by CMP. No problems were found.
- Contact defects: Via and contact cuts were defined by a dry-etch. No over-etching of the vias or contacts was noted. They were filled with tungsten plugs on a thin layer of titanium and had been planarized by the CMP process.
- Polysilicon: Two layers of poly (no silicide) were used on the die. Poly 2 was used to form a type of local interconnect in the periphery and in EEPROM cell type "B." Poly 1 was used to form all gates on the die and the select/word lines in the EEPROM cell arrays. Definition was by a dry etch of good quality.
- Buried contacts were employed using poly 2 to N+ diffusions. Poly 2 also contacted poly 1 in many locations.

ANALYSIS RESULTS (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No silicide was present on the diffusions, and no problems were found.
- Local oxide (LOCOS) isolation was used. No problems were noted. No step was noted in the oxide at the well boundaries.
- Two similar EEPROM designs were employed on the device.
- Memory cell “A” consisted of a 3T, single capacitor, EEPROM design. Metal 1 was used to form the select lines, program lines, output connections and to distribute GND. Poly 1 was used to form the transistors, one plate of the capacitor and the tunnel-oxide device. Memory cell “B” also used a 3T, single capacitor, EEPROM design. Metal 1 was used to form the select lines, program lines, output lines and enable lines and poly 1 formed the transistors, one plate of the capacitor and the tunnel oxide device. Programming of both cell types was achieved through the thin tunnel oxide windows. Poly 2 provided some local interconnect in the type “B” cells only.
- Redundancy fuses were not used on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

- Optical inspection
- Passivation integrity test
- Passivation removal
- SEM inspection of metal 3
- Delayer to metal 2 and inspect
- SEM inspection of metal 2
- Delayer to metal 1 and inspect
- Metal 1 removal and inspect
- Delayer to silicon and inspect poly/die surface
- Remove poly and inspect substrate
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	G
Contact coverage	G
Contact registration	G

DIE MATERIAL ANALYSIS

Overlay passivation: A layer of silicon-nitride over a layer of silicon dioxide.

Metallization (M1, M2 and M3): Aluminum (Al) with a titanium-nitride (TiN) cap.

Vias and contacts: Tungsten (W) with a (Ti) adhesion layer.

Intermetal dielectric: A thin layer of glass followed by an SOG and a thick layer of glass.

Pre-metal dielectric: A layer of CVD glass over various densified oxides

No polycides or silicides were present.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

HORIZONTAL DIMENSIONS

Die size:	13.0 x 13.1 mm (331 x 335 mils)
Die area:	170 mm ² (110,885 mils ²)
Min metal 3 width:	1.0 micron
Min metal 3 space:	0.3 micron
Min metal 3 pitch (w/o contact):	1.3 micron
Min via 2:	0.4 micron
Min via 2 space:	0.6 micron
Min metal 2 width:	1.0 micron
Min metal 2 space:	0.4 micron
Min metal 2 pitch (w/o contact):	1.4 micron
Min via 1:	0.45 micron
Min via 1 space:	0.6 micron
Min metal 1 width:	0.8 micron
Min metal 1 space:	0.4 micron
Min metal 1 pitch (w/o contact):	1.3 micron
Min contact:	0.6 micron
Min contact space:	0.6 micron
Min poly 2 width:	0.5 micron
Min poly 2 space:	0.7 micron
Min poly 1 width:	0.35 micron
Min poly 1 space:	0.7 micron
Min gate poly to contact space:	0.5 micron
Min gate length* - (N-channel):	0.35 micron
- (P-channel):	0.35 micron
Tunnel oxide window:	0.6 x 1.2 micron (oval)
EEPROM cell array size (both):	5.2 x 10.7 microns
EEPROM cell array area (both):	55.6 microns

*Physical gate length.

VERTICAL DIMENSIONS

Layers:

Passivation 2:	1.0 micron
Passivation 1:	0.8 micron
Metal 3 - cap:	0.08 micron (approx.)
- aluminum:	0.8 micron
Intermetal dielectric:	2.0 microns
Metal 2 - cap:	0.1 micron
- aluminum:	0.8 micron
Intermetal dielectric:	2.0 microns
Metal 1 - cap:	0.1 micron
- aluminum:	0.5 micron
Pre-metal dielectric:	1.0 micron
Poly 2:	0.05 micron (approx.)
Poly 1:	0.2 micron
Local oxide:	0.35 micron
N+ S/D:	0.25 micron
P + S/D:	0.2 micron
N-well:	2.5 microns
P- epi:	6.5 microns

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MEMORY CELLS (EEPROM, Array A)	Figures 26 - 35
(EEPROM, Array B)	Figures 36 - 39
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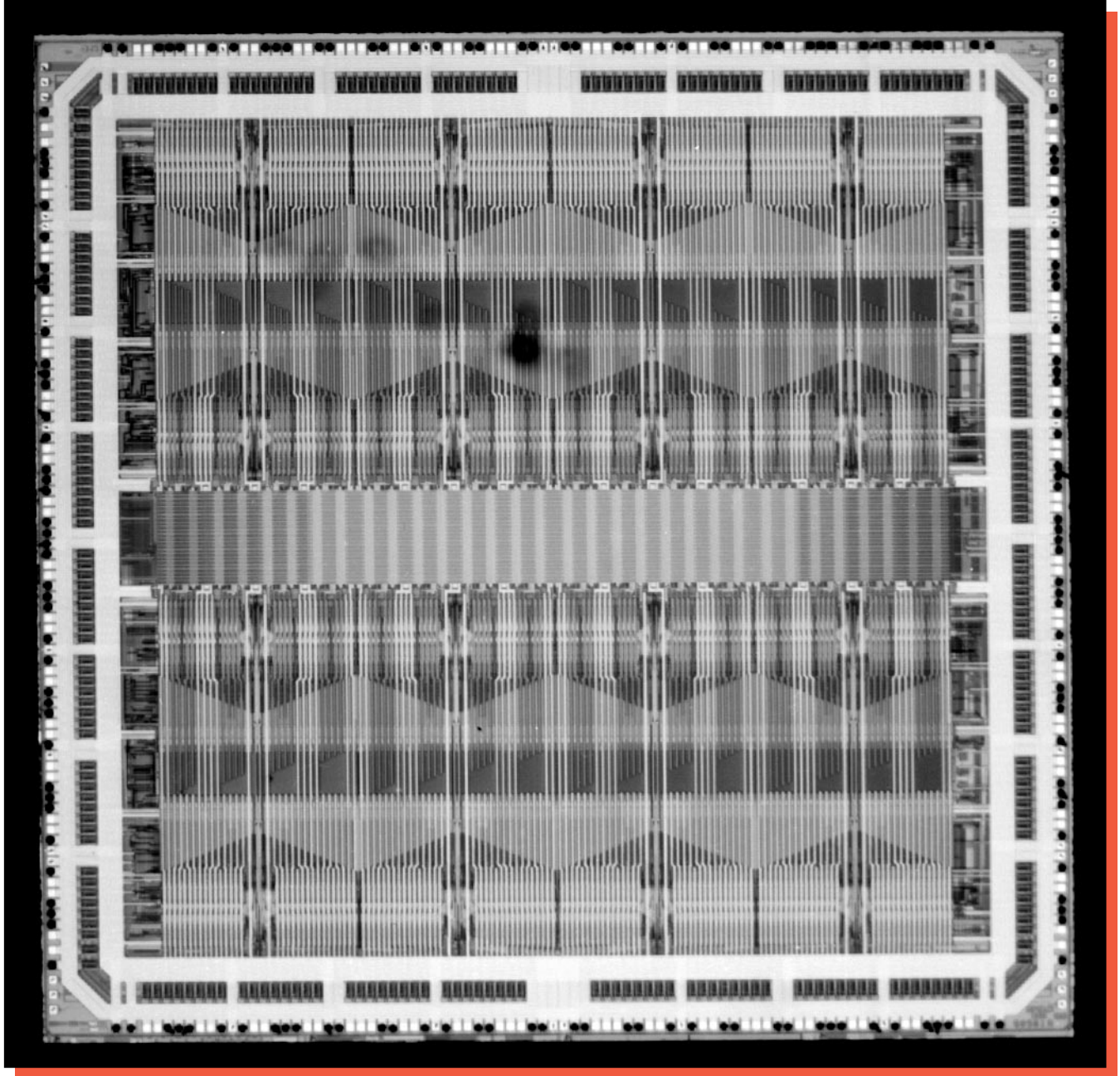


Figure 1. Whole die photograph of the AMD Mach 5 512. Mag. 20x.

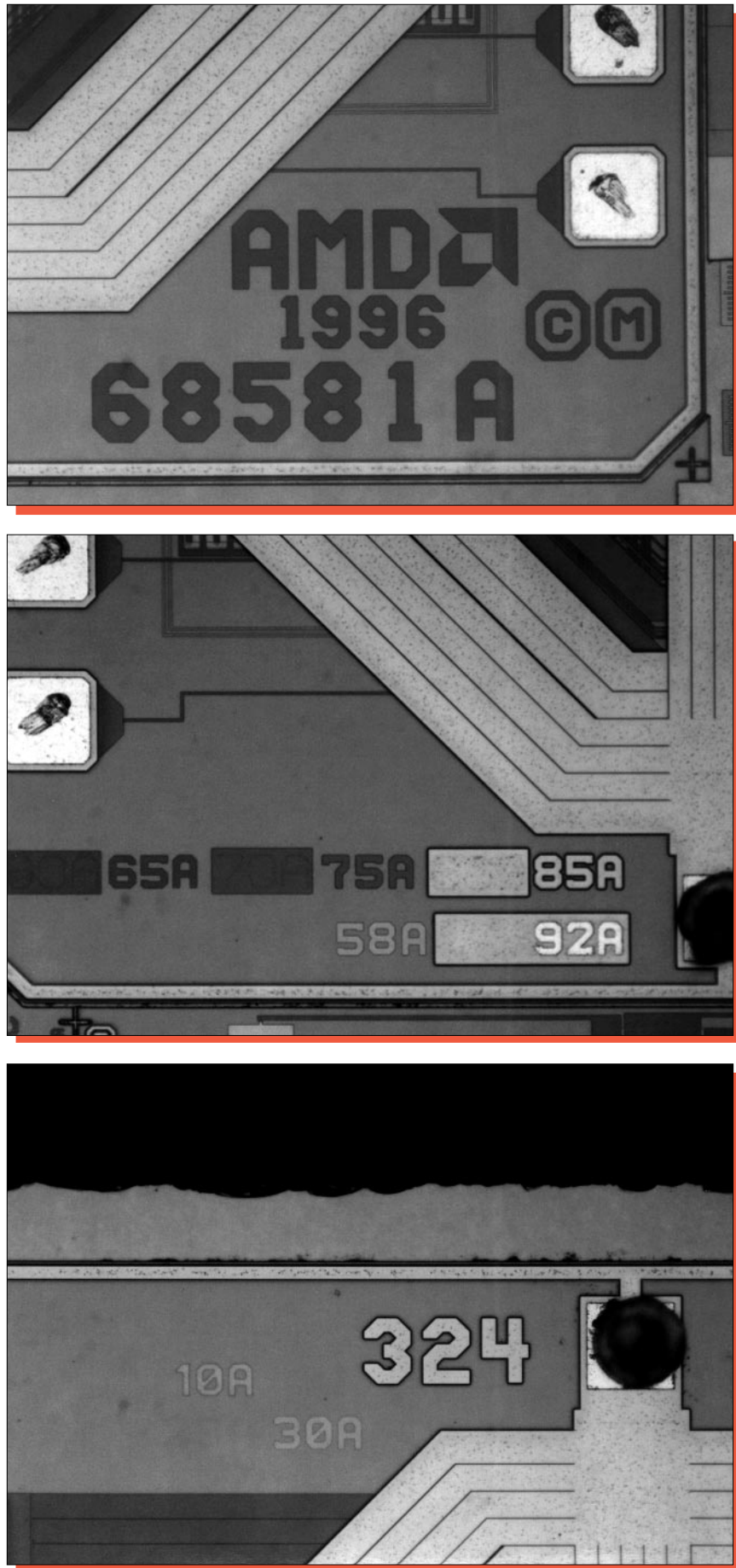
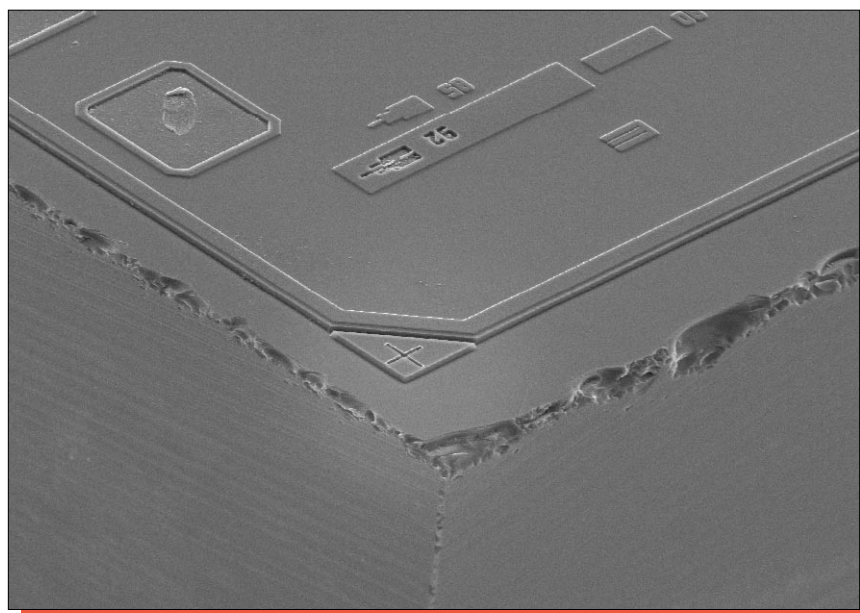
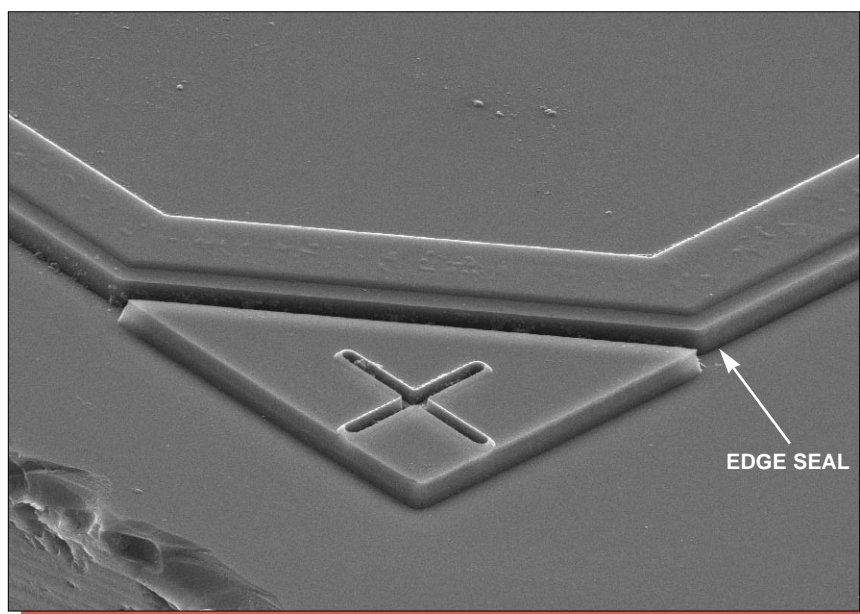


Figure 2. Optical views of die identification markings. Mag. 200x.

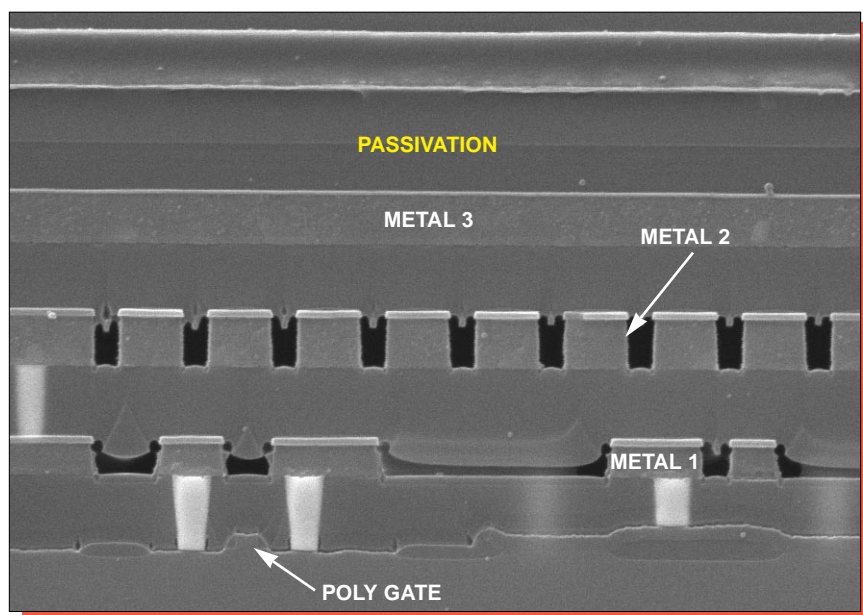


Mag. 275x

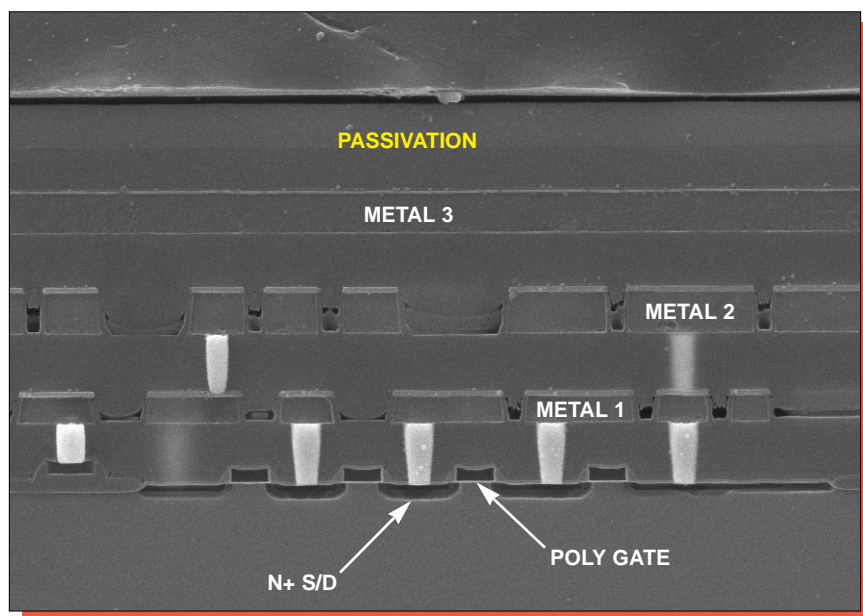


Mag. 1100x

Figure 3. SEM views illustrating a die corner and edge seal. 60°.

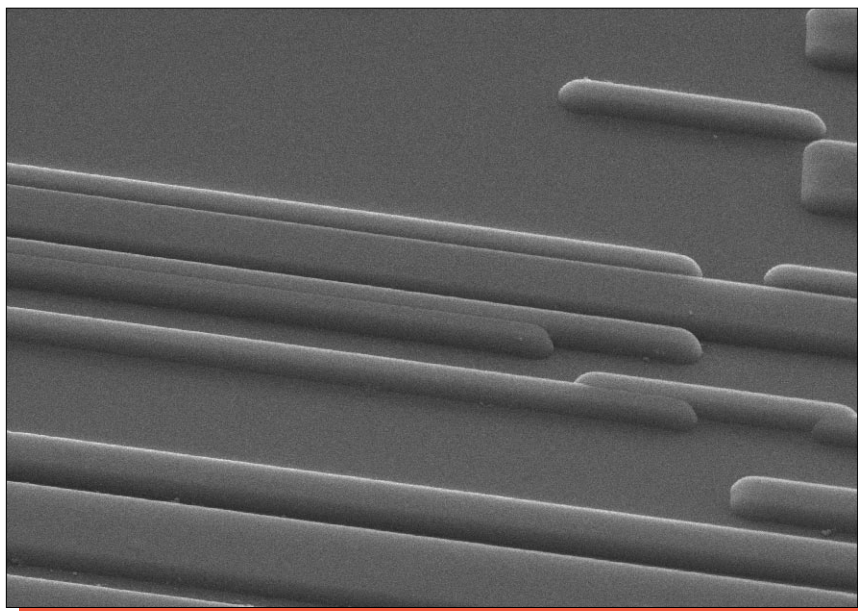


glass etch, Mag. 8000x

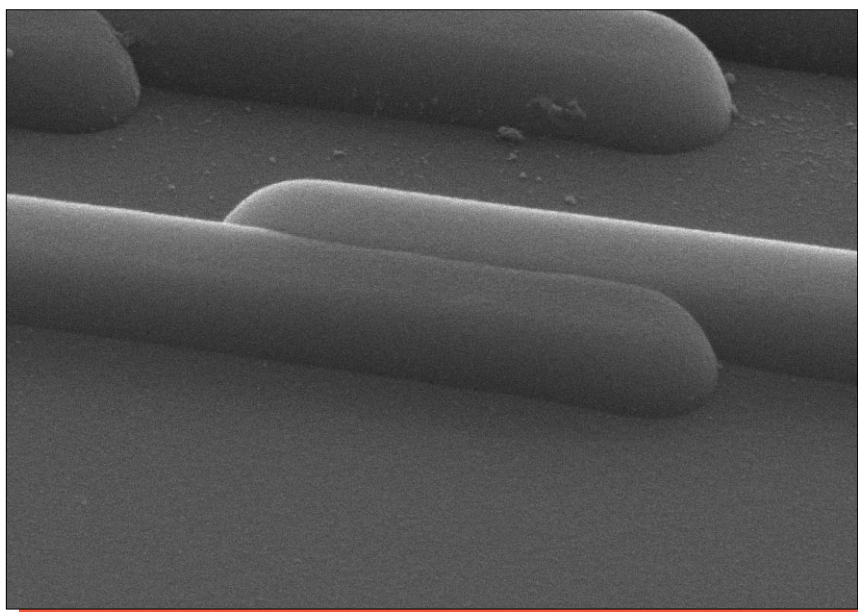


Mag. 6500x

Figure 4. SEM section views illustrating general device structure.

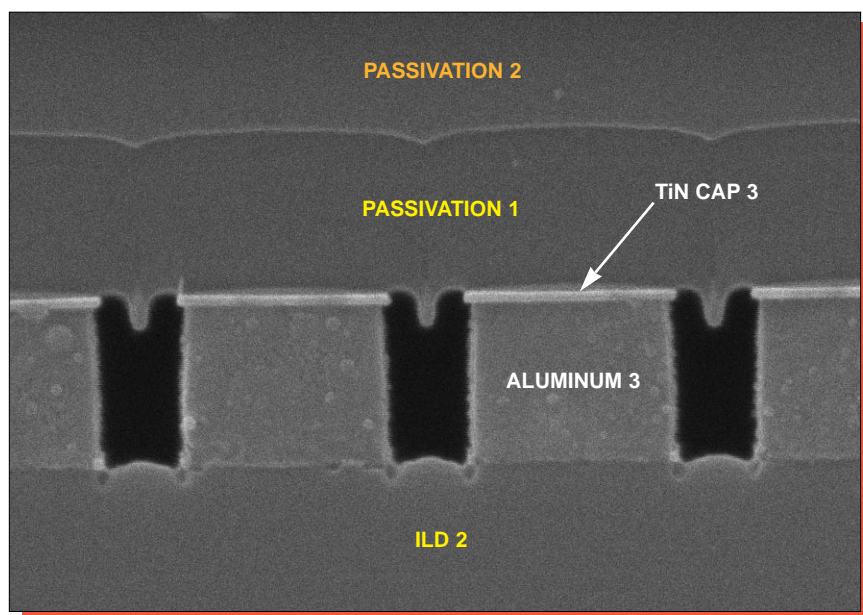


Mag. 2200x

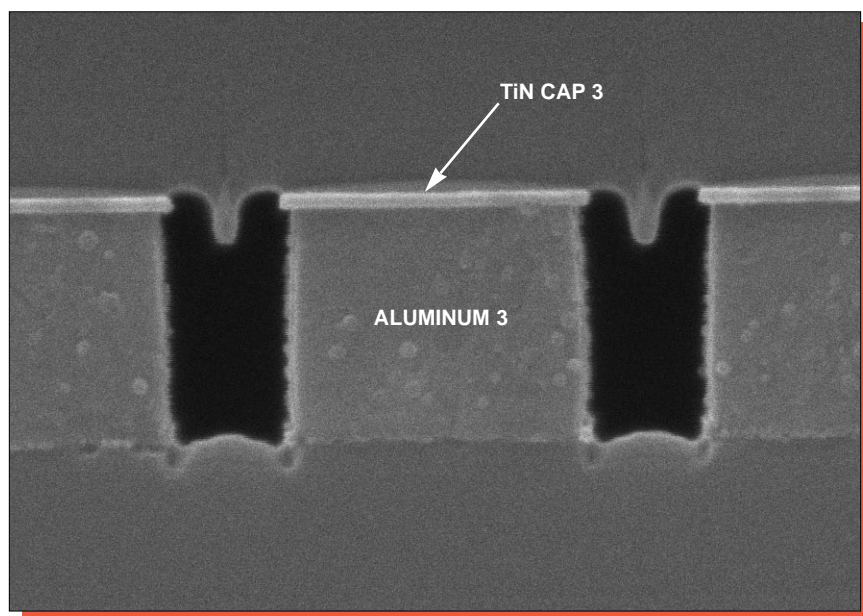


Mag. 8800x

Figure 5. SEM views illustrating passivation coverage. 60°.

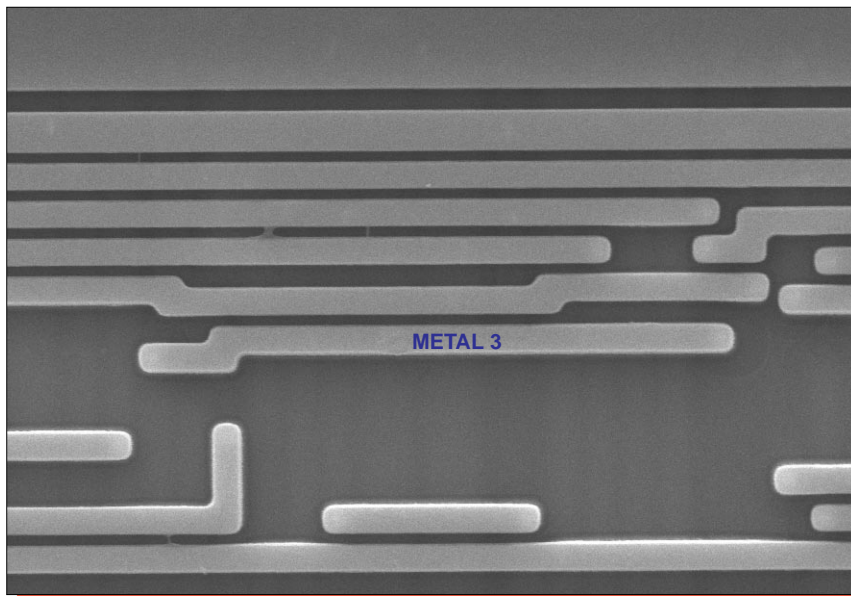


Mag. 26,000x

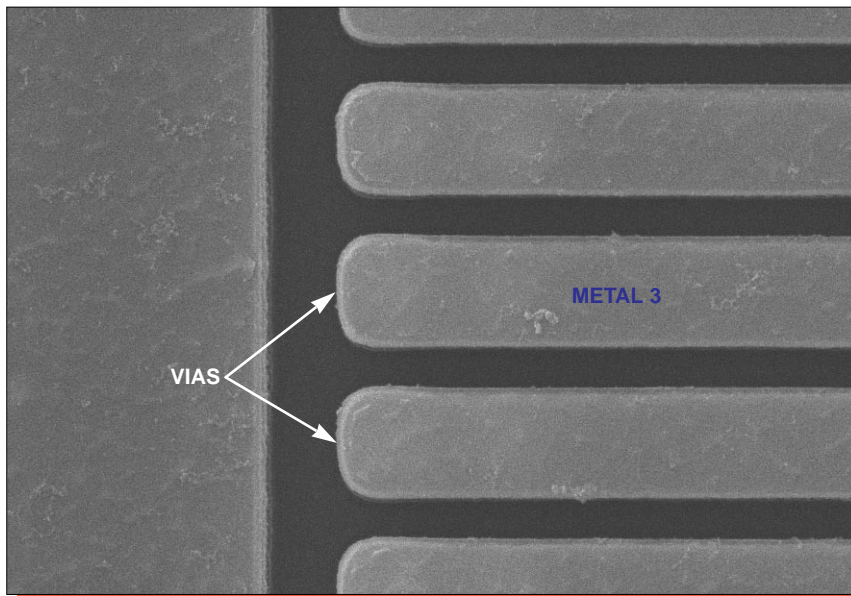


Mag. 40,000x

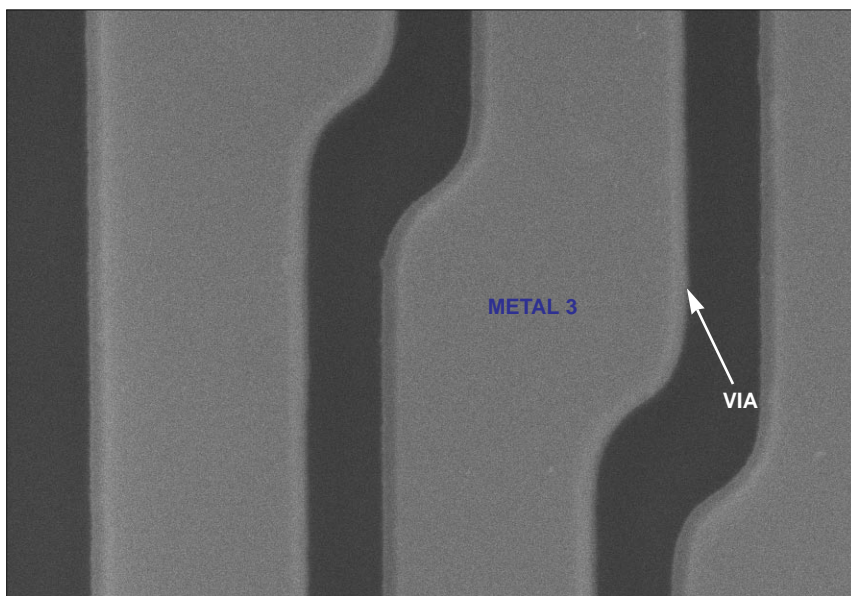
Figure 6. SEM section views illustrating metal 3 line profiles.



Mag. 3250x

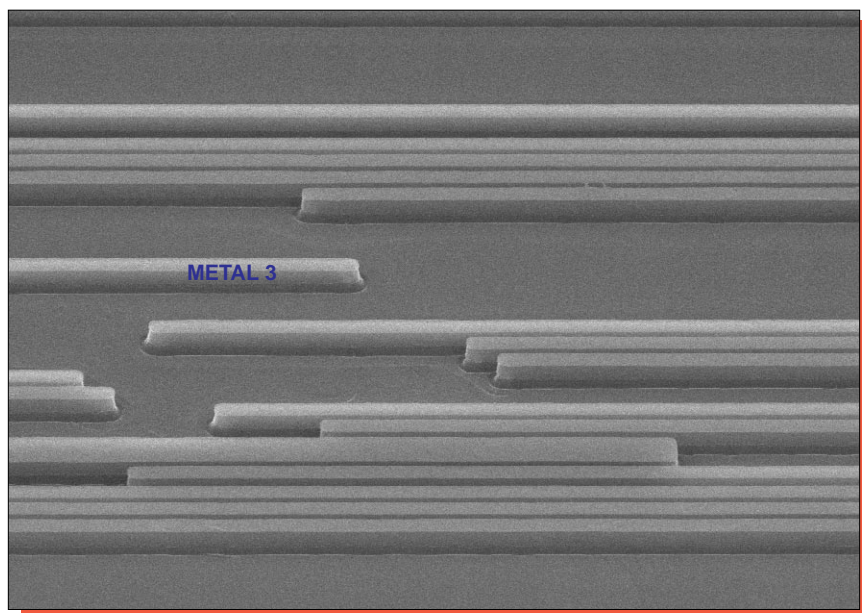


Mag. 13,000x

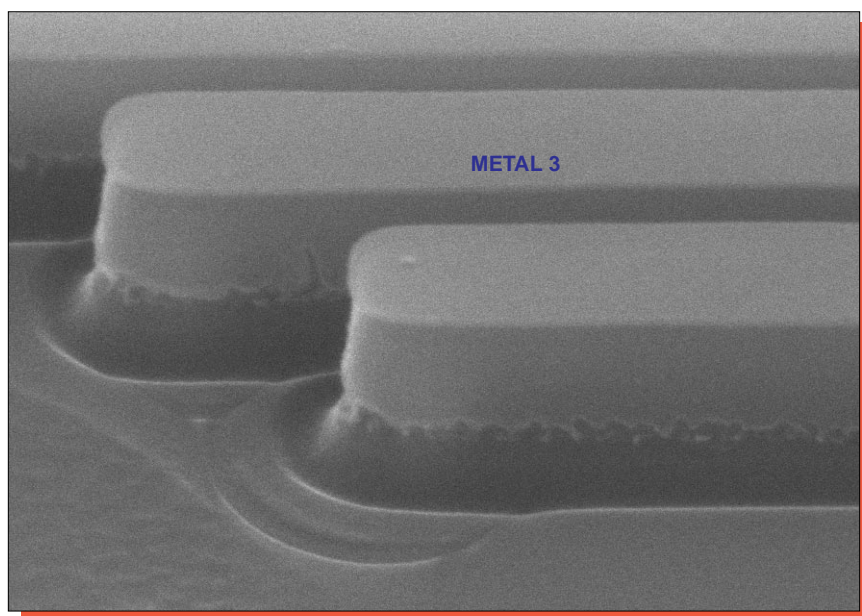


Mag. 26,000x

Figure 7. Topological SEM views illustrating metal 3 patterning. 0°.

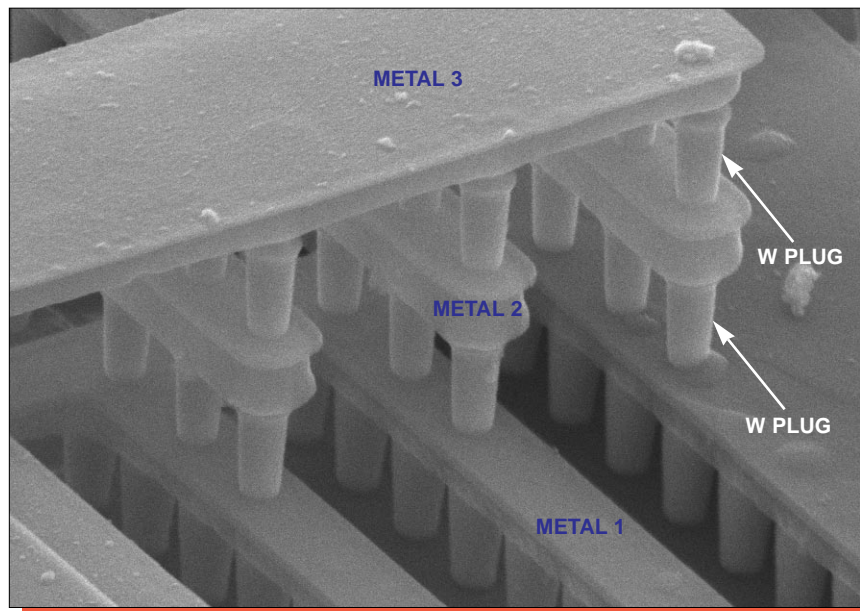


Mag. 2700x

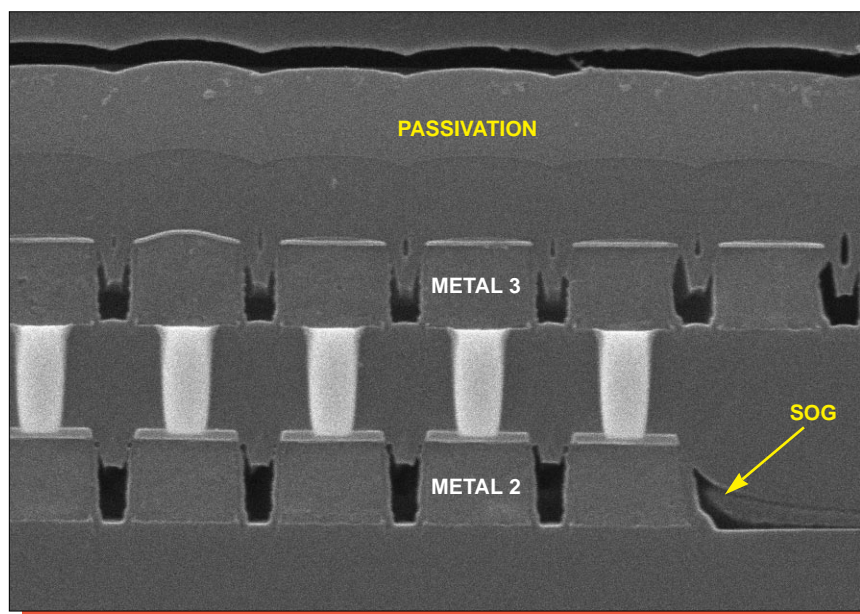


Mag. 22,000x

Figure 8. SEM views illustrating metal 3 coverage. 60°.

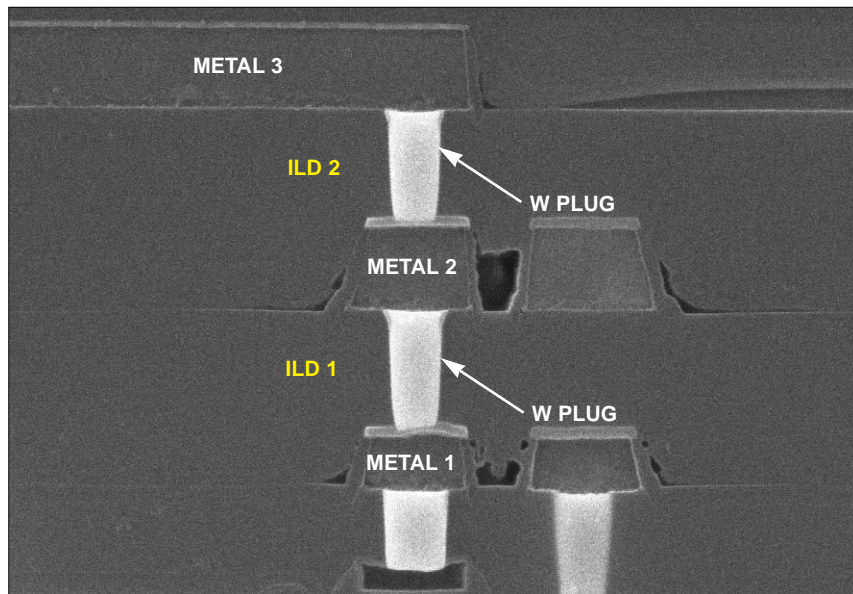


Mag. 12,400x, 60°

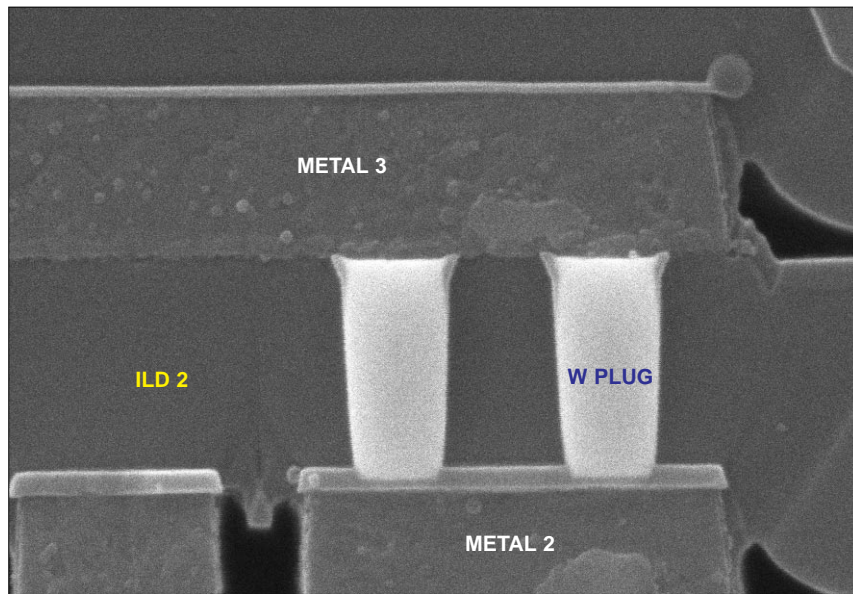


Mag. 13,000x

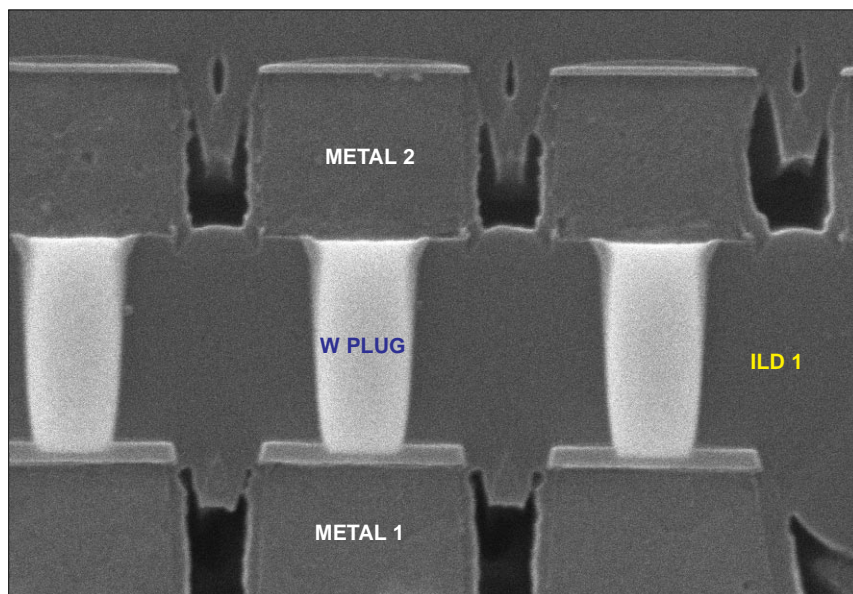
Figure 9. SEM views illustrating metal line structures.



Mag. 13,000x

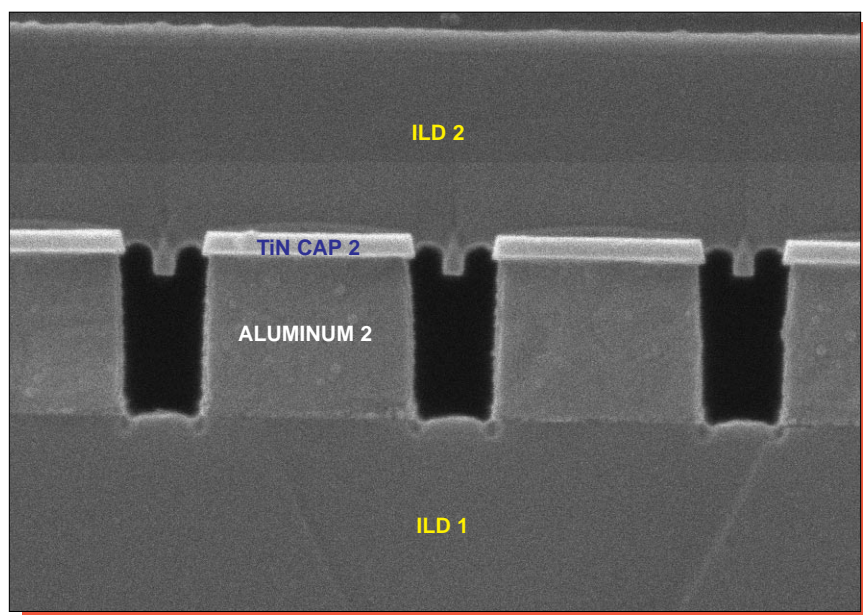


Mag. 26,000x

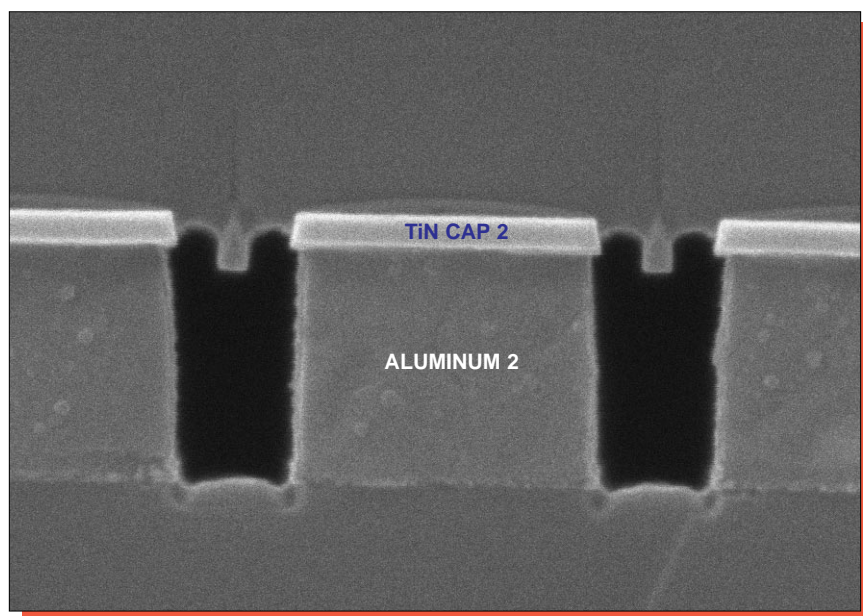


Mag. 26,000x

Figure 9a. SEM section views illustrating metal 3-to-metal 2 vias.

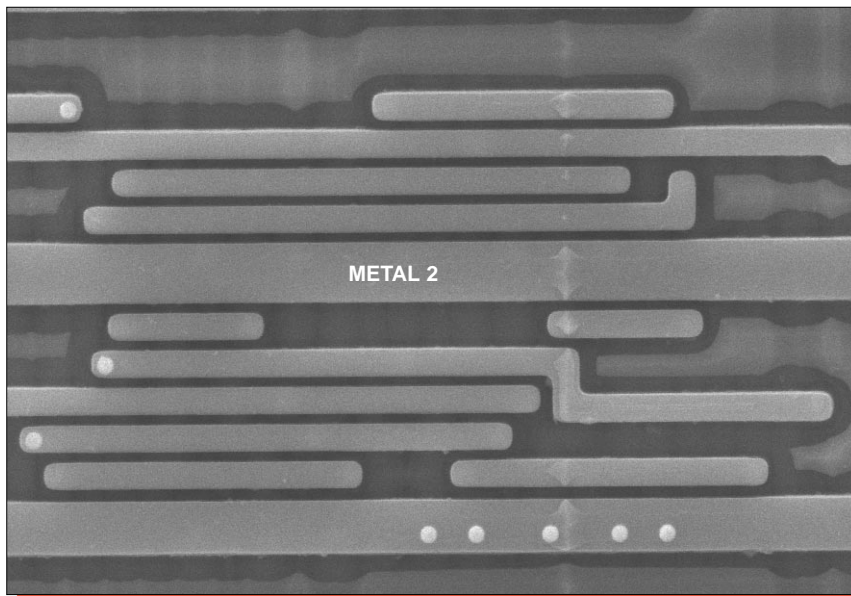


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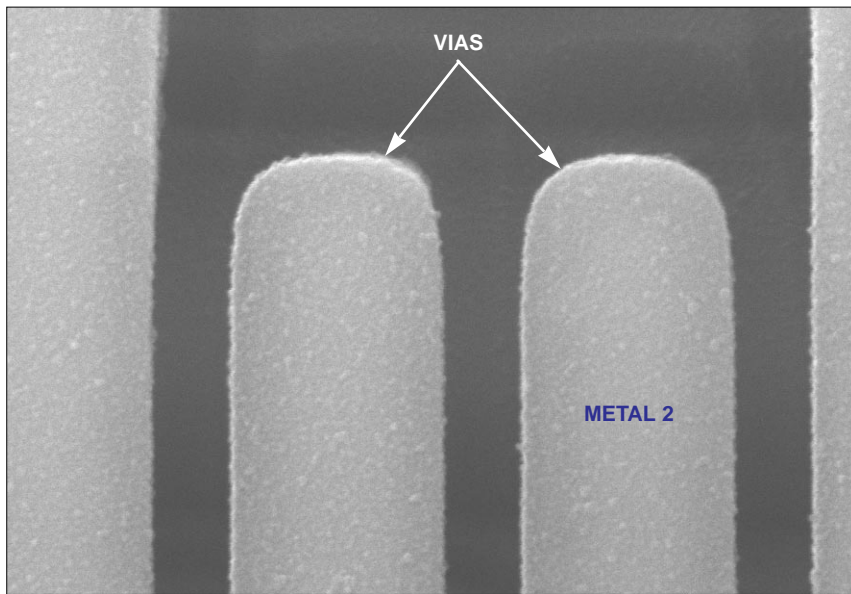


Mag. 40,000x

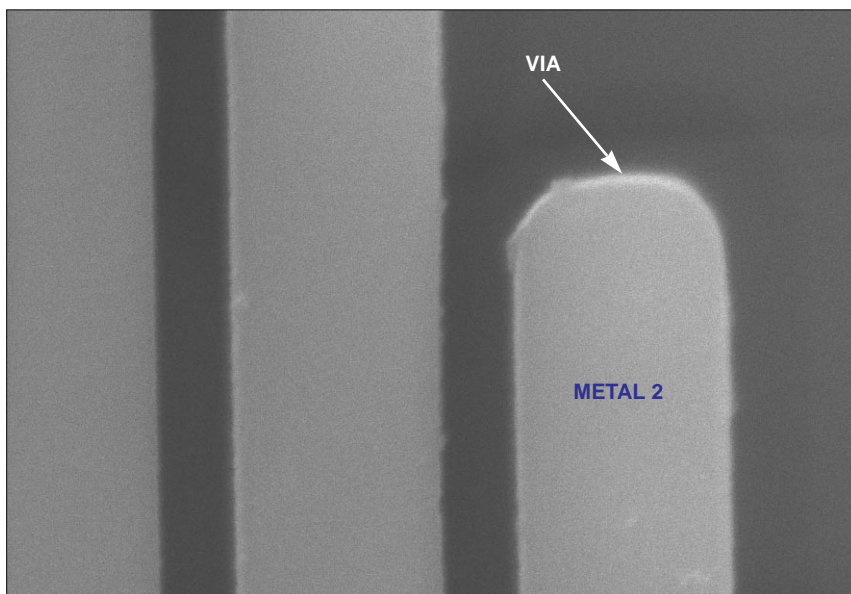
Figure 10. SEM section views illustrating metal 2 line profiles.



Mag. 3250x

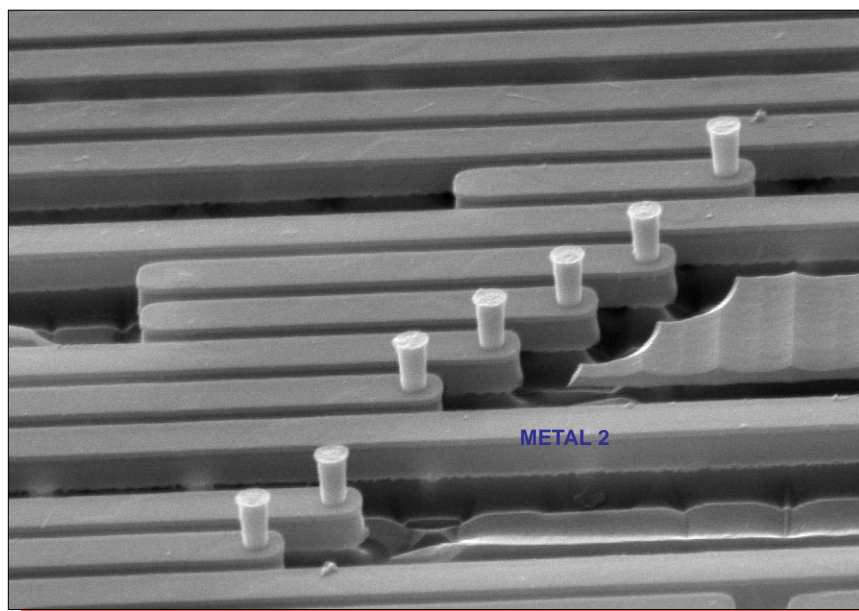


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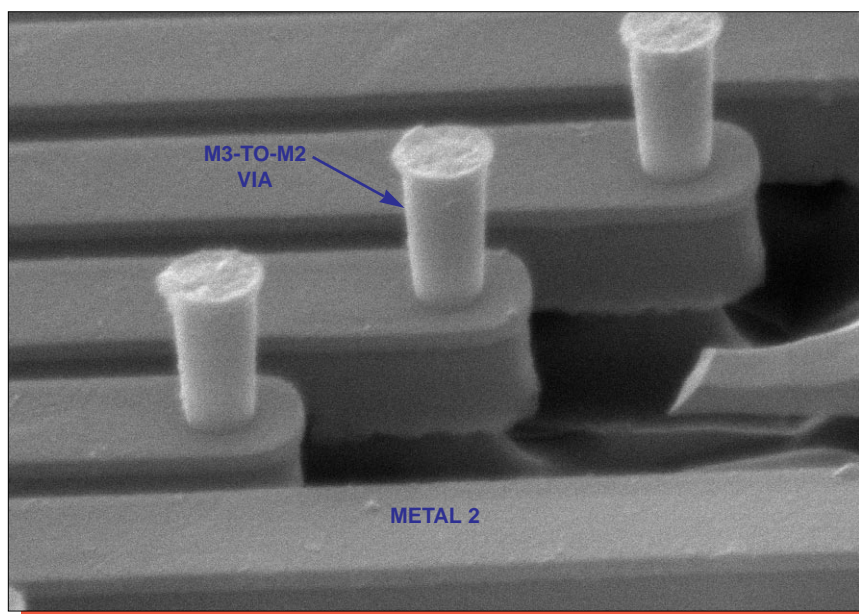


Mag. 26,000x

Figure 11. Topological SEM views illustrating metal 2 patterning. 0°.

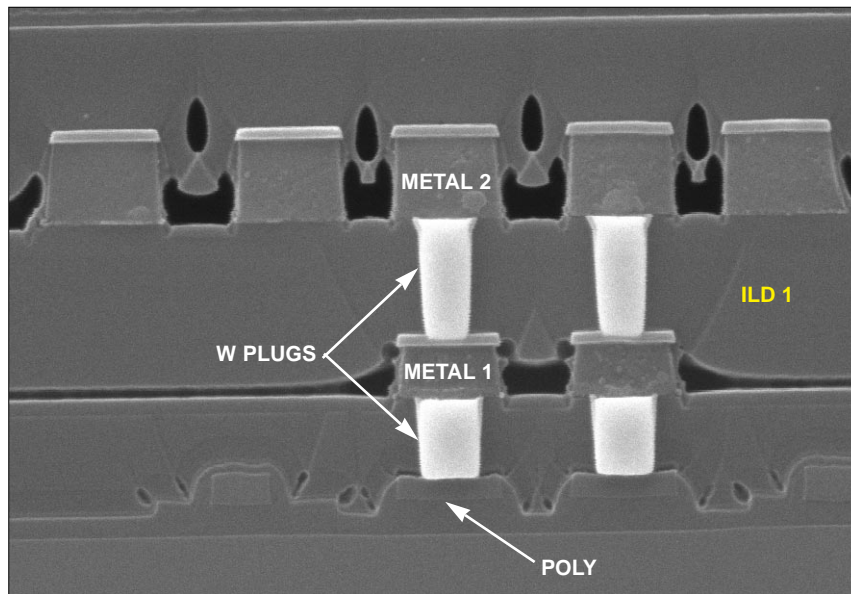


Mag. 6750x

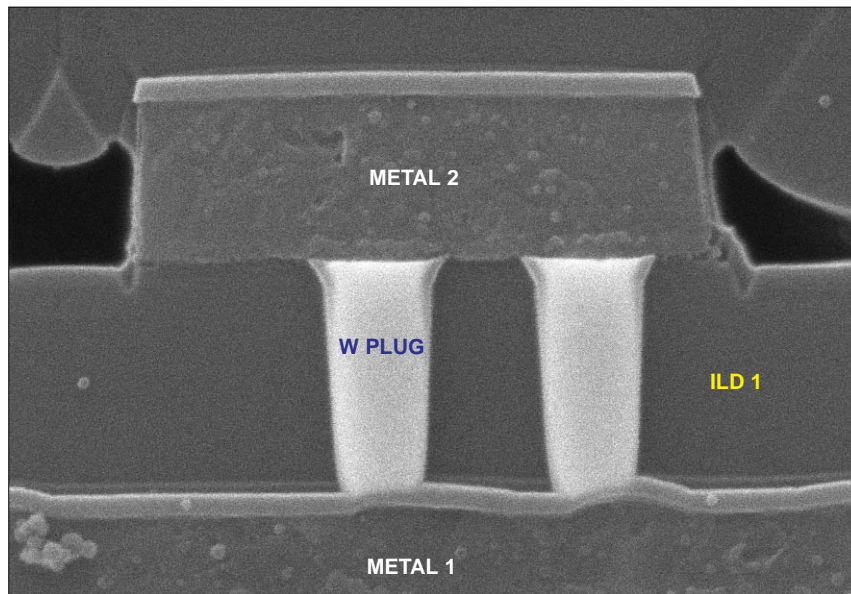


Mag. 20,000x

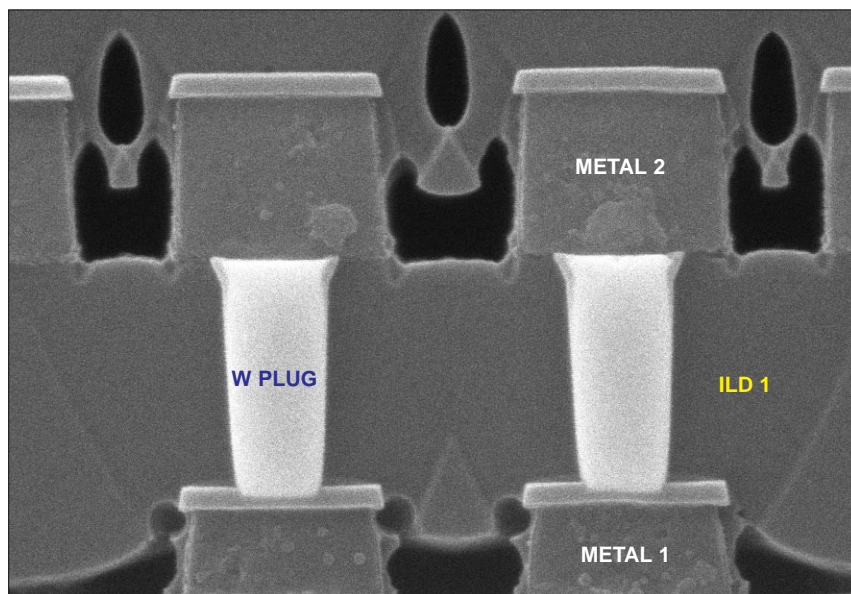
Figure 12. SEM views illustrating metal 2 coverage. 60°.



glass etch,
Mag. 13,000x

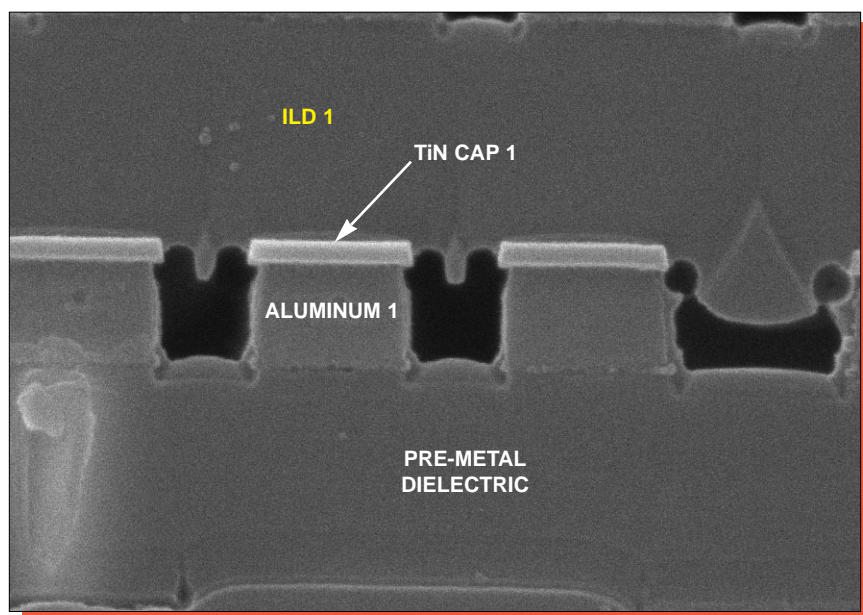


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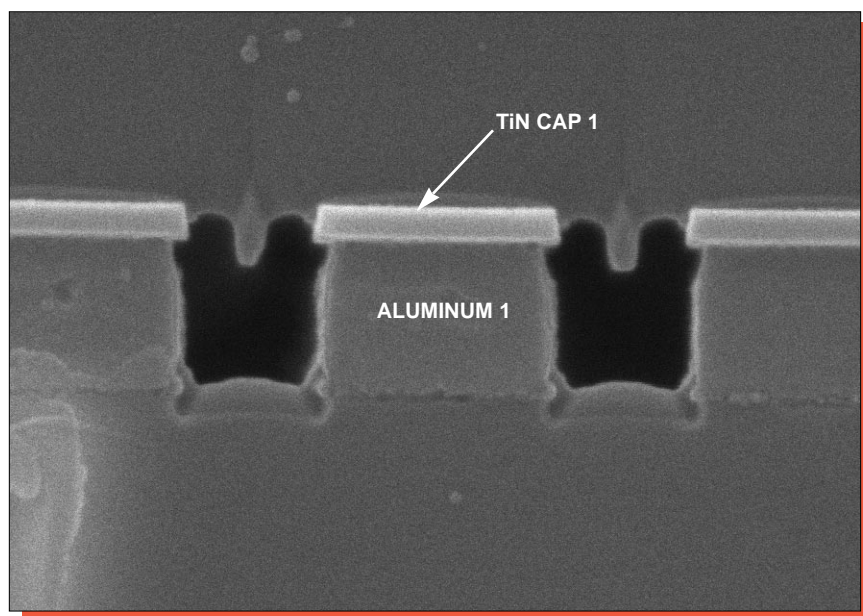


Mag. 26,000x

Figure 13. SEM section views illustrating metal 2-to-metal 1 vias.

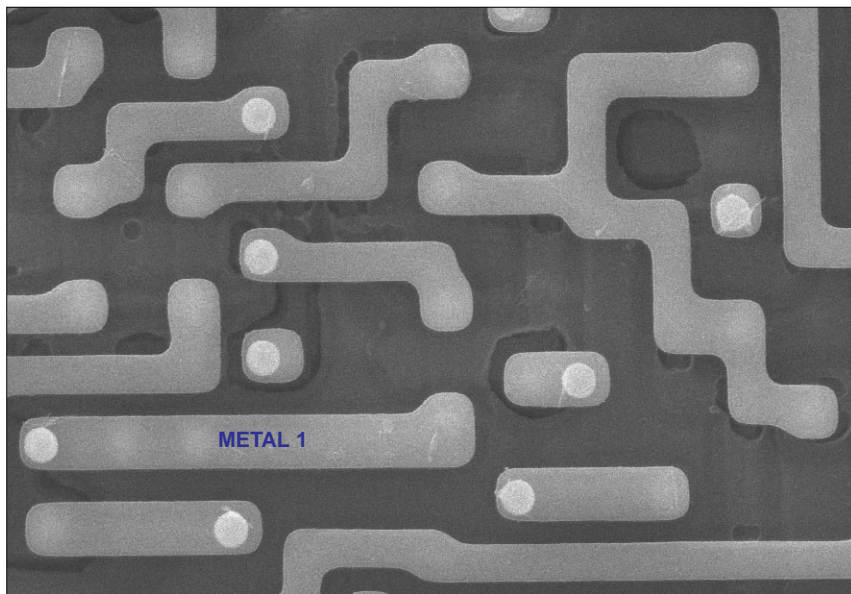


Mag. 26,000x

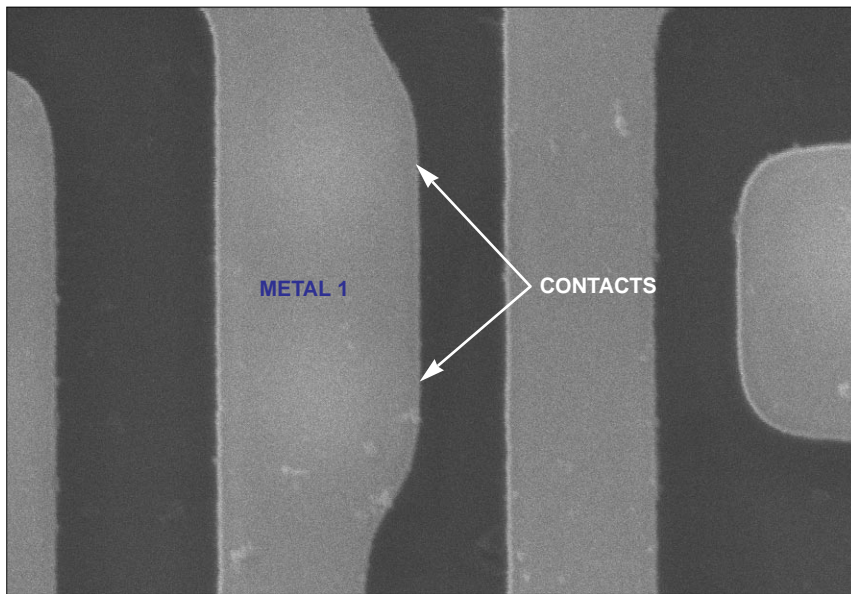


Mag. 40,000x

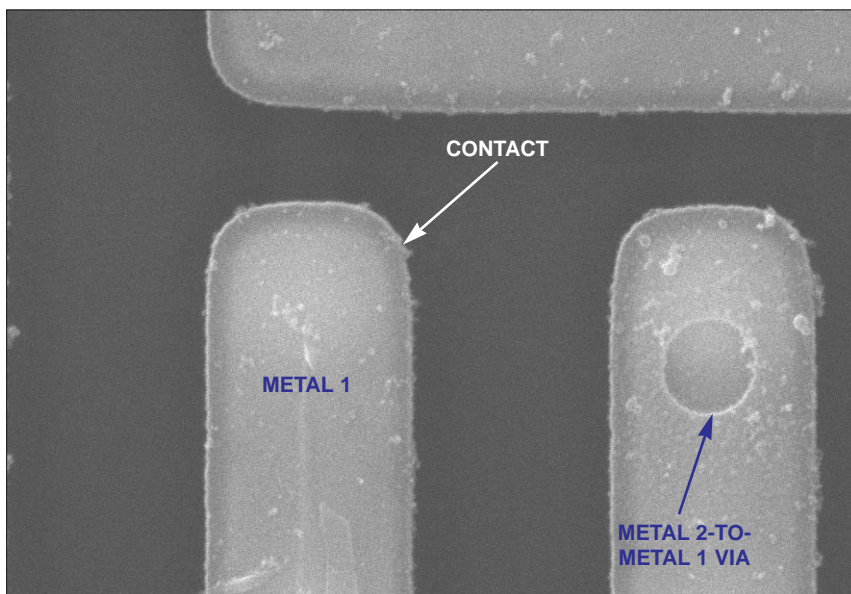
Figure 14. SEM section views illustrating metal 1 line profiles.



Mag. 6500x

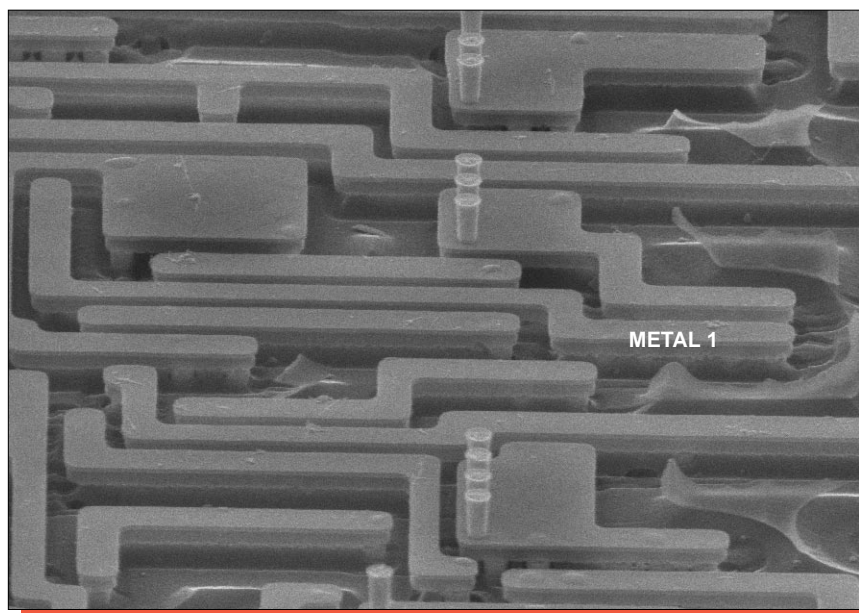


Mag. 26,000x

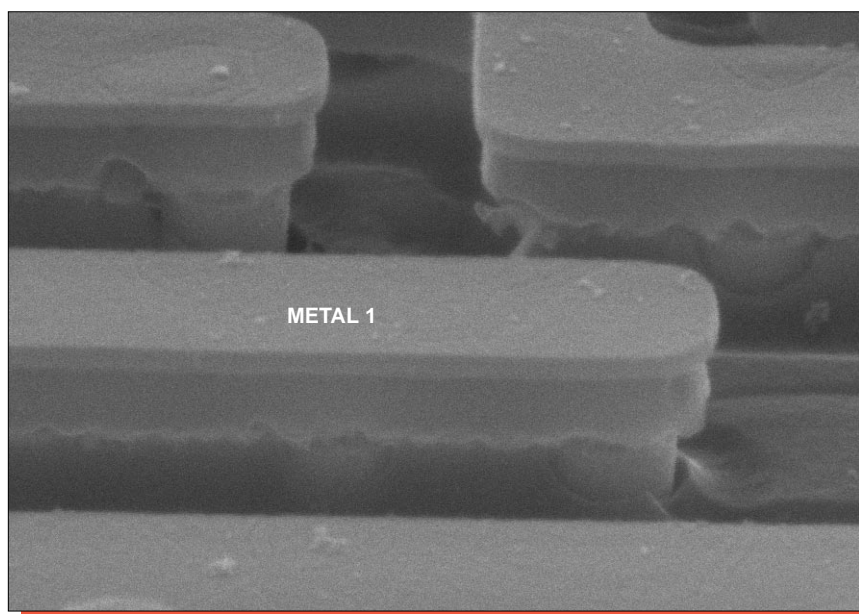


Mag. 26,000x

Figure 15. Topological SEM views illustrating metal 1 patterning. 0°.

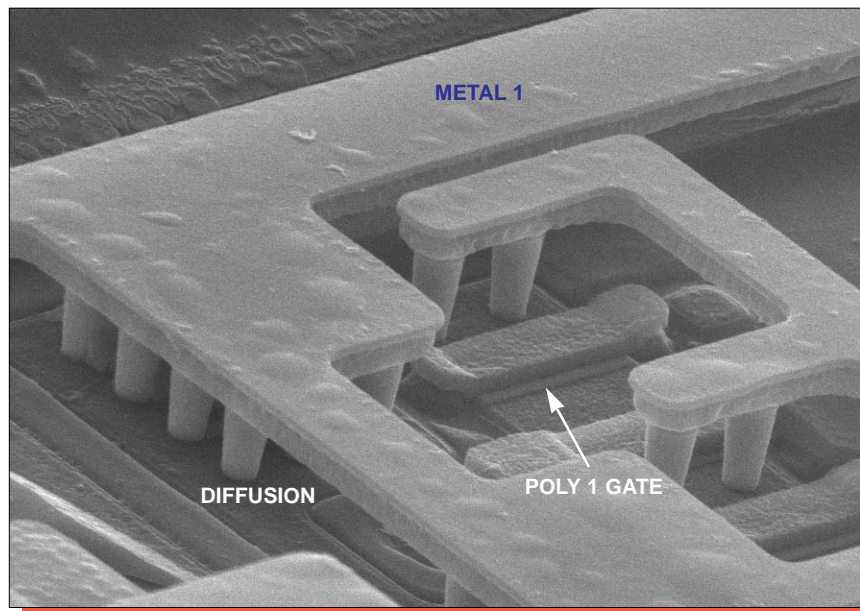


Mag. 5200x

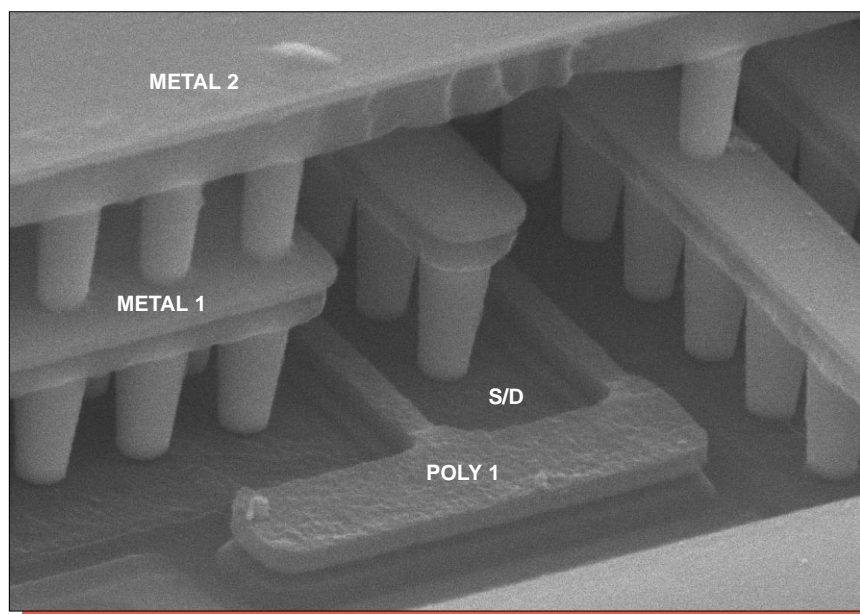


Mag. 27,000x

Figure 16. SEM views illustrating metal 1 coverage. 60°.



Mag. 10,000x



Mag. 15,000x

Figure 16a. Additional views illustrating metal 1 structures. 60°.

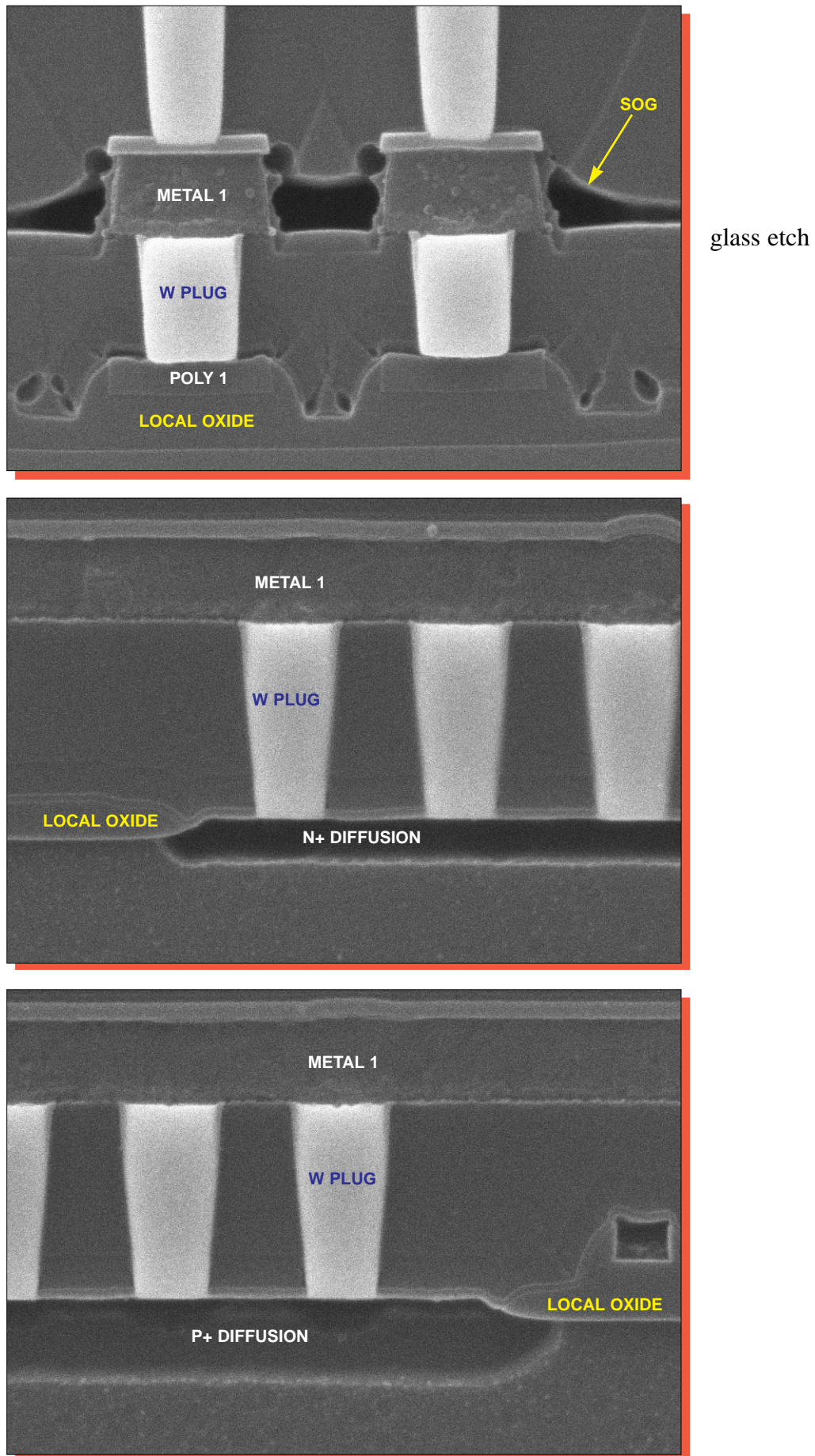


Figure 17. SEM section views illustrating metal 1 contacts. Mag. 26,000x.

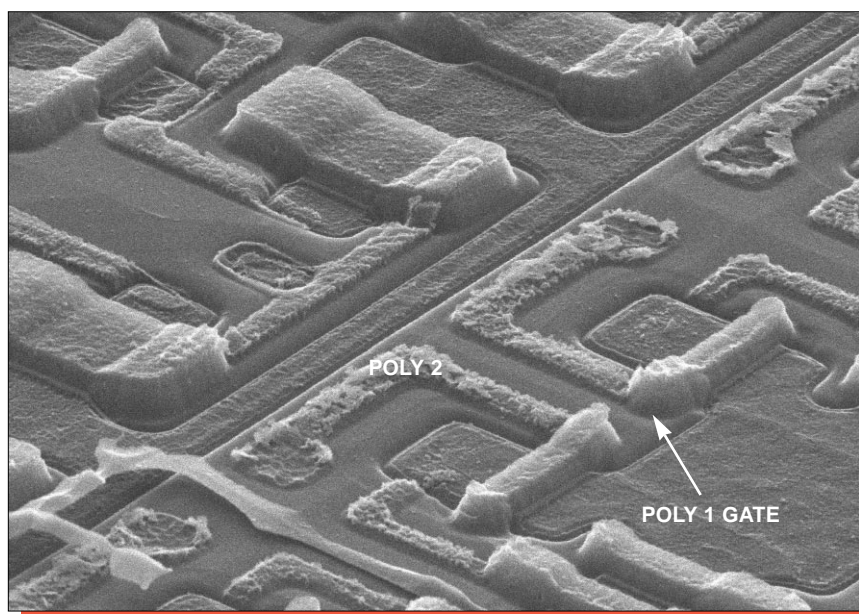
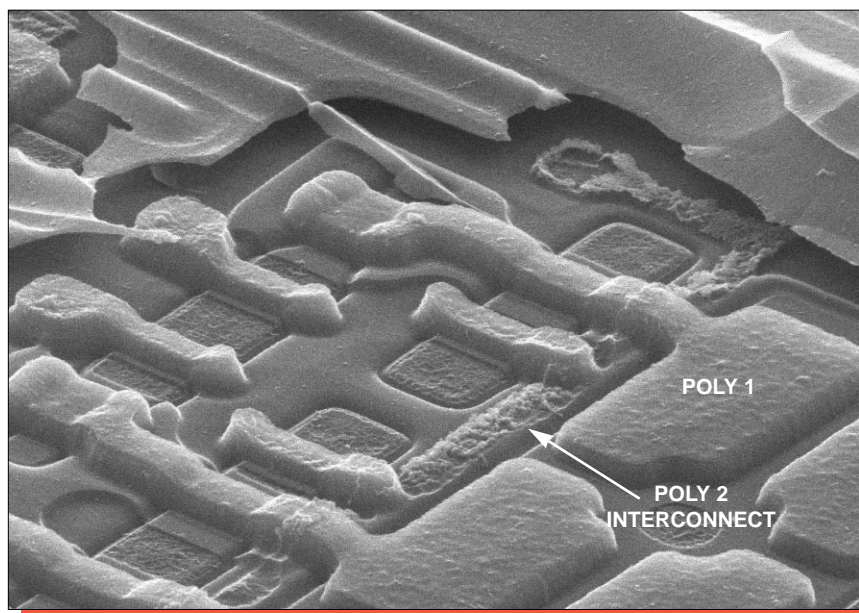
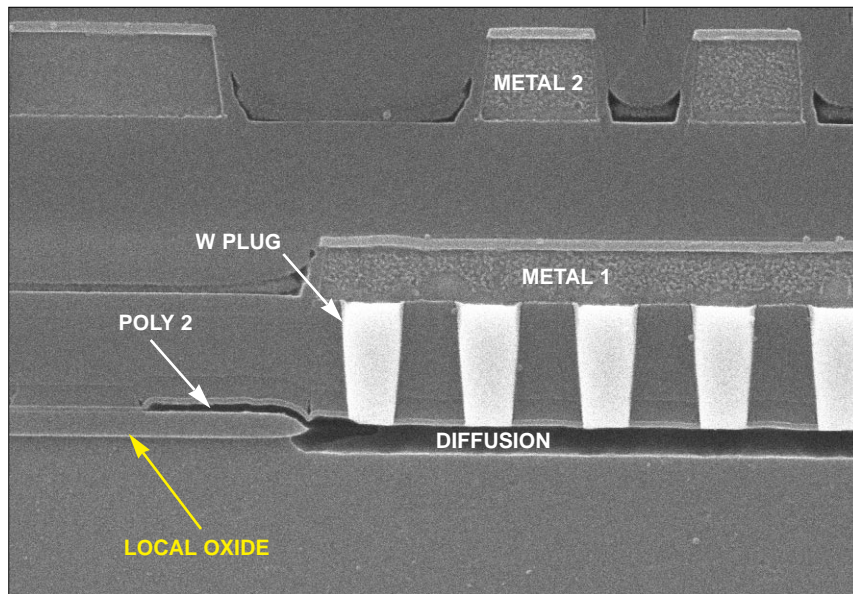
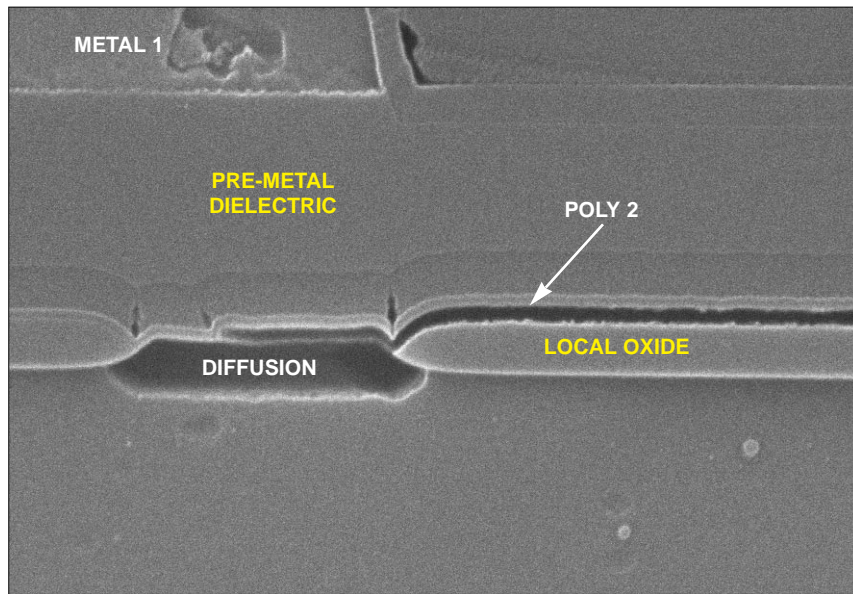


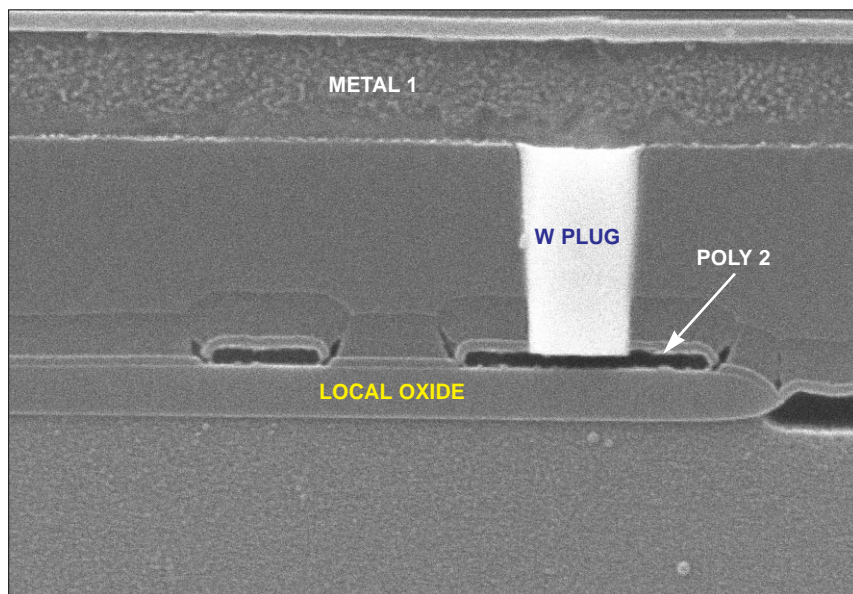
Figure 18. SEM views illustrating poly structures. Mag. 10,000x, 60°.



Mag. 13,000x

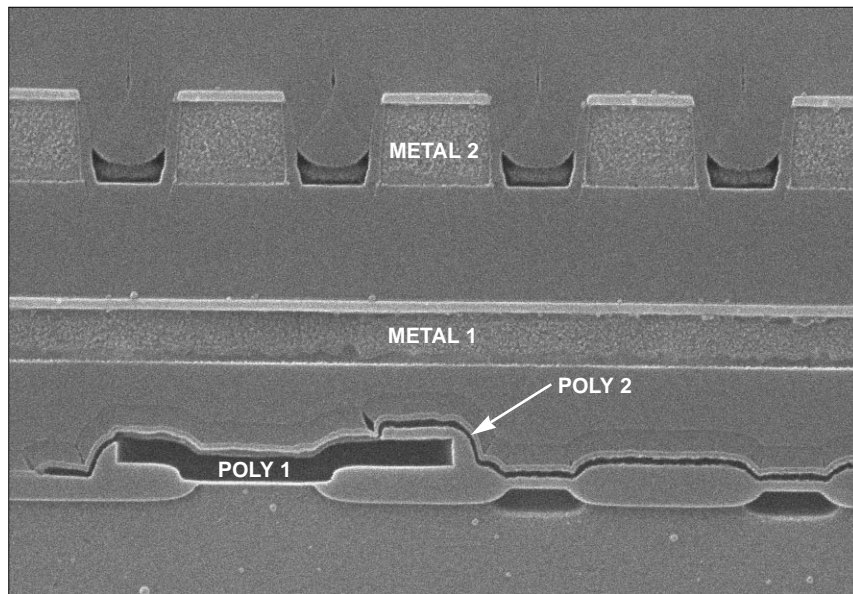


Mag. 26,000x

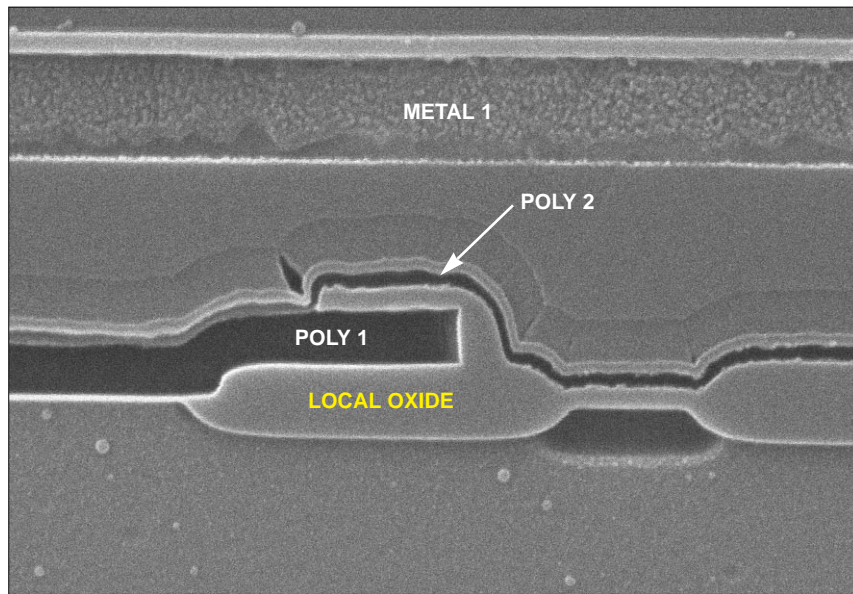


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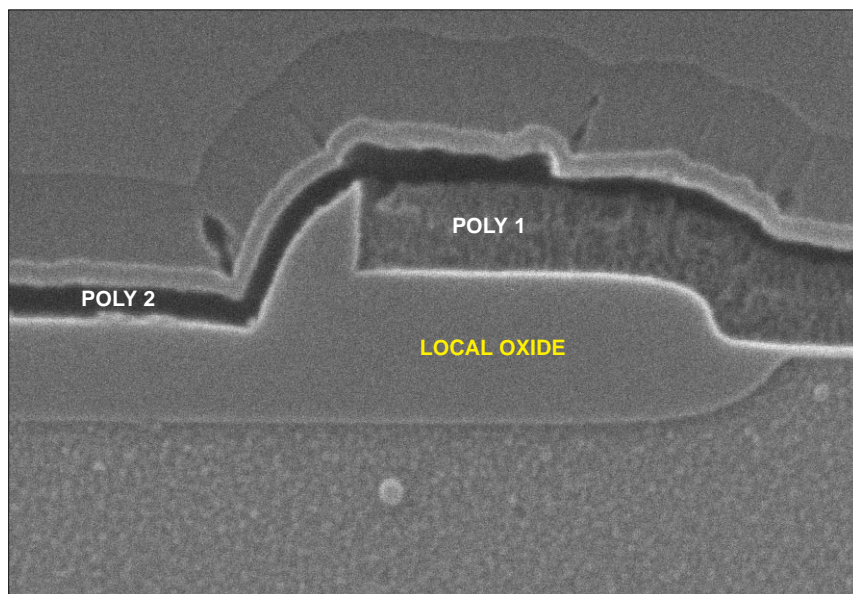
Figure 18a. SEM section views illustrating poly 2.



Mag. 13,000x

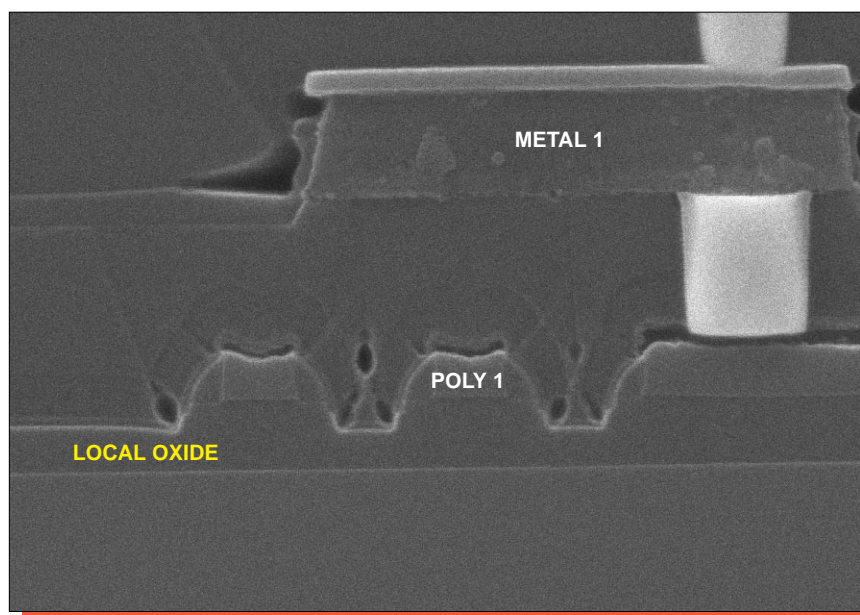


Mag. 26,000x

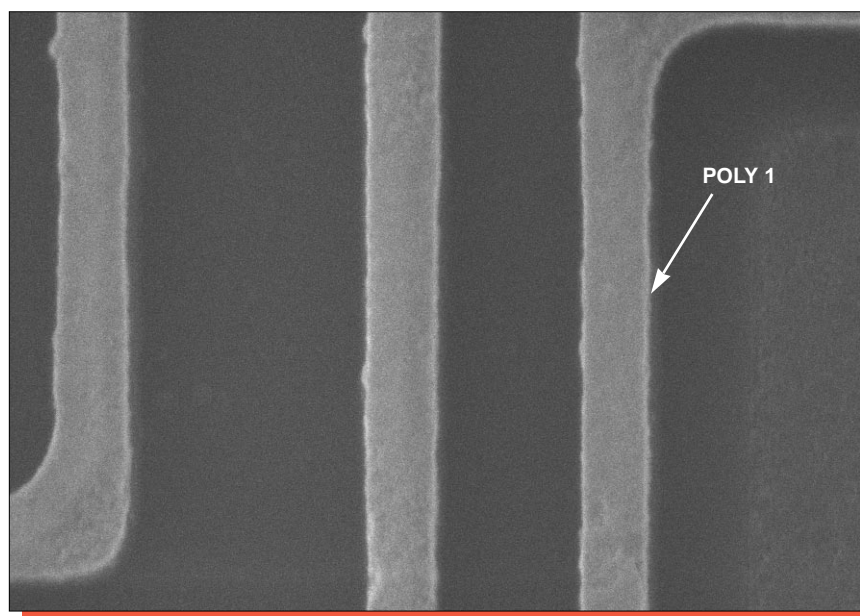


Mag. 52,000x

Figure 18b. Additional SEM section views illustrating poly 2.

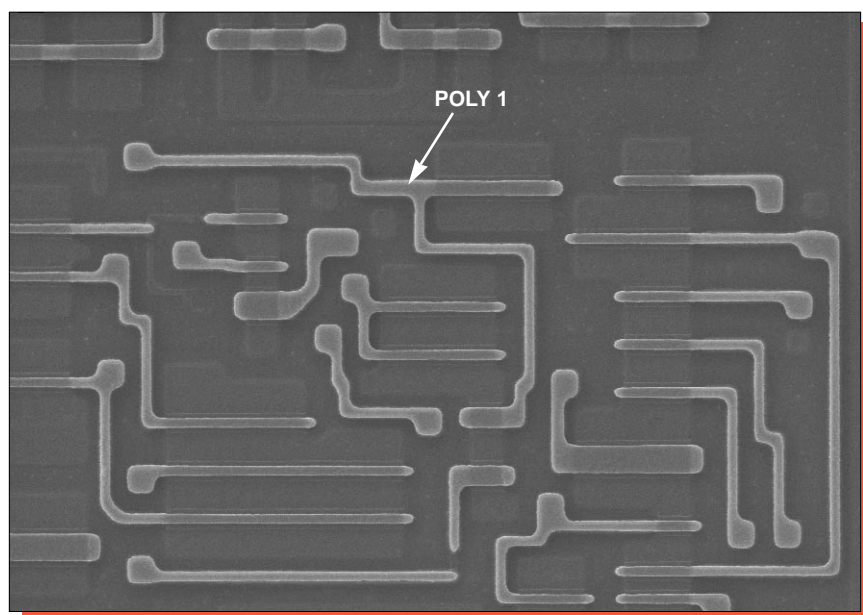


glass etch

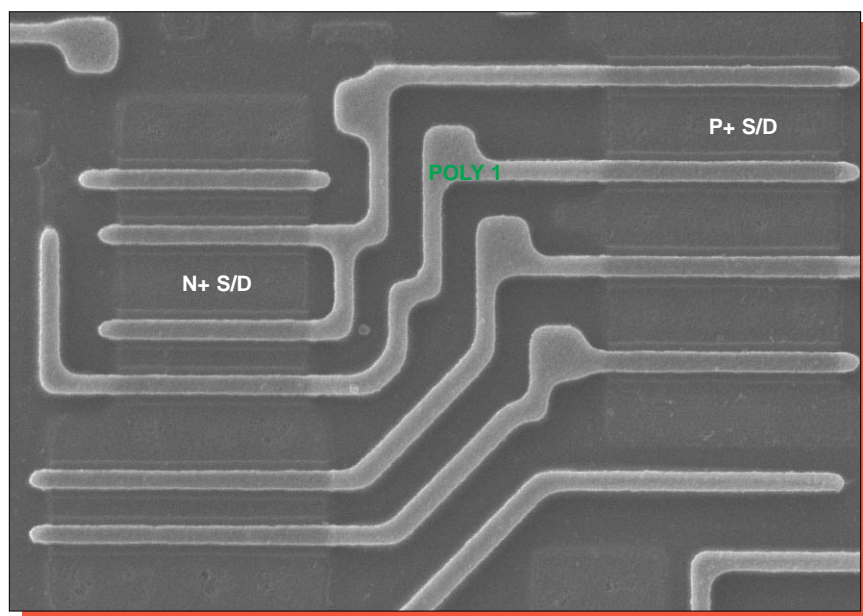


0°

Figure 19. SEM views illustrating poly 1 profiles. Mag. 26,000x.

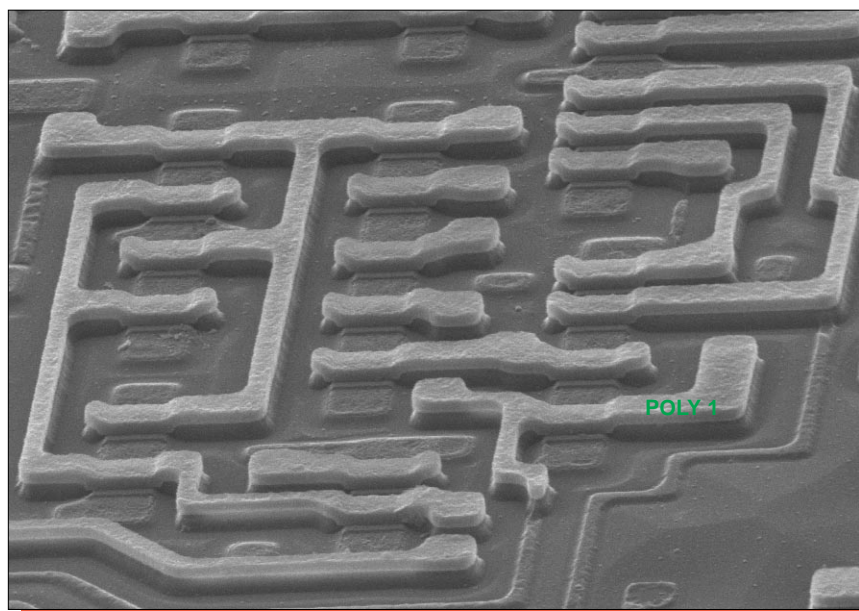


Mag. 3250x

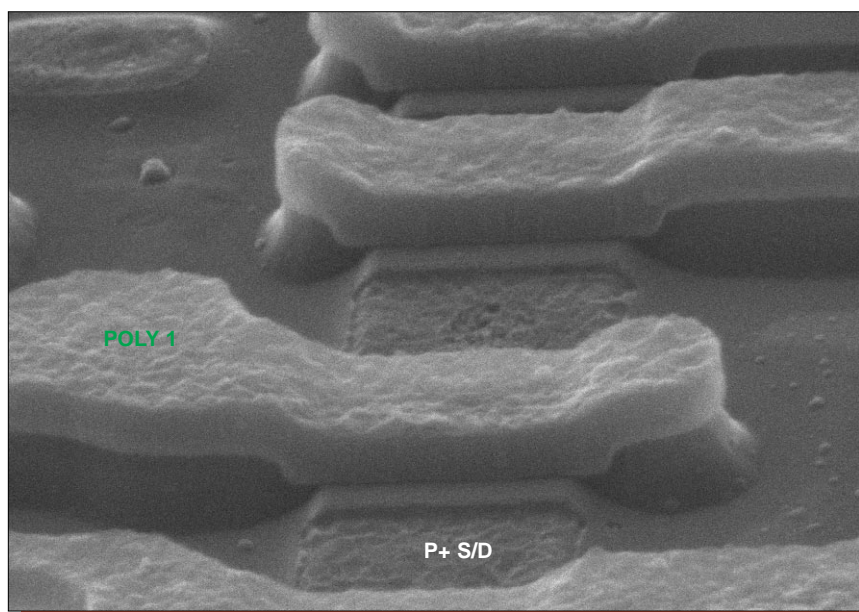


Mag. 6500x

Figure 20. Topological SEM views illustrating poly 1 patterning. 0°.

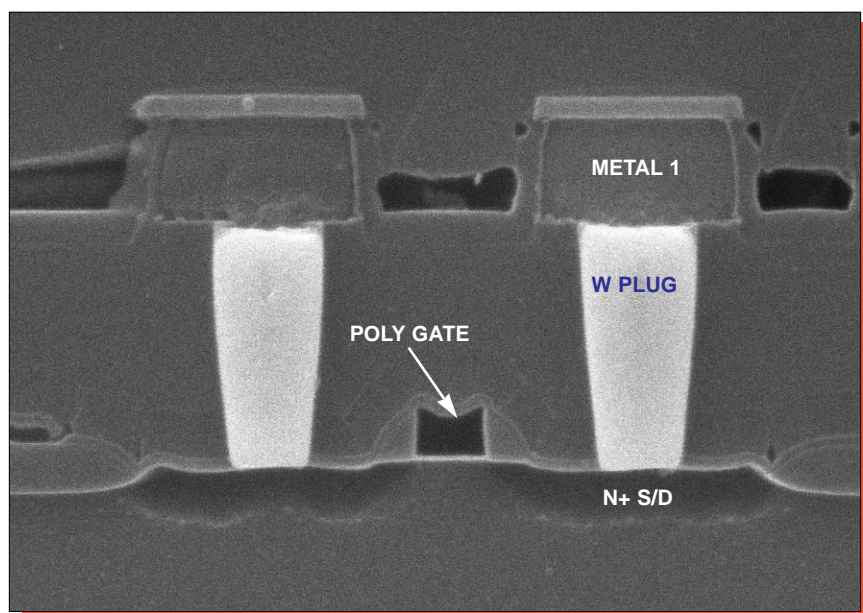


Mag. 6200x

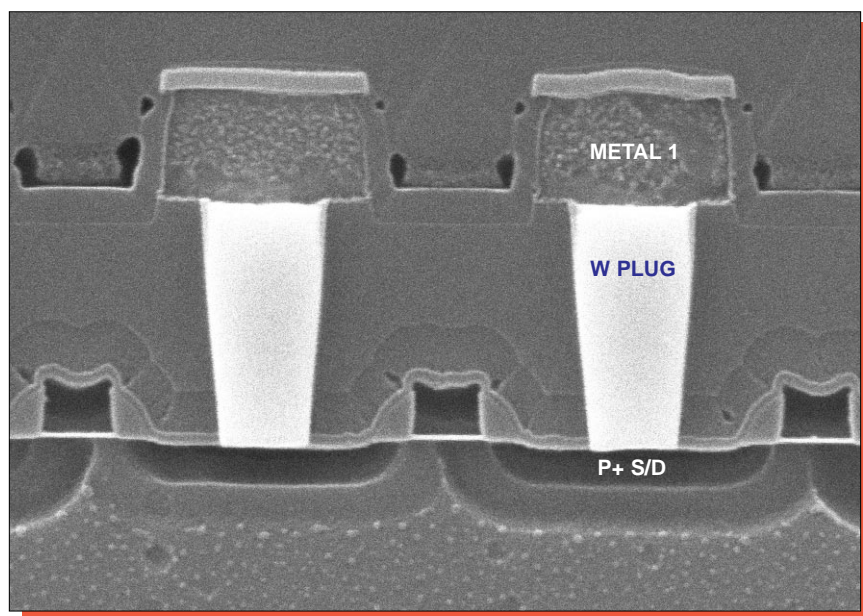


Mag. 27,000x

Figure 21. SEM views illustrating poly 1 coverage. 60°.



N-channel



P-channel

Figure 22. SEM section views illustrating typical gate structure. Mag. 26,000x.

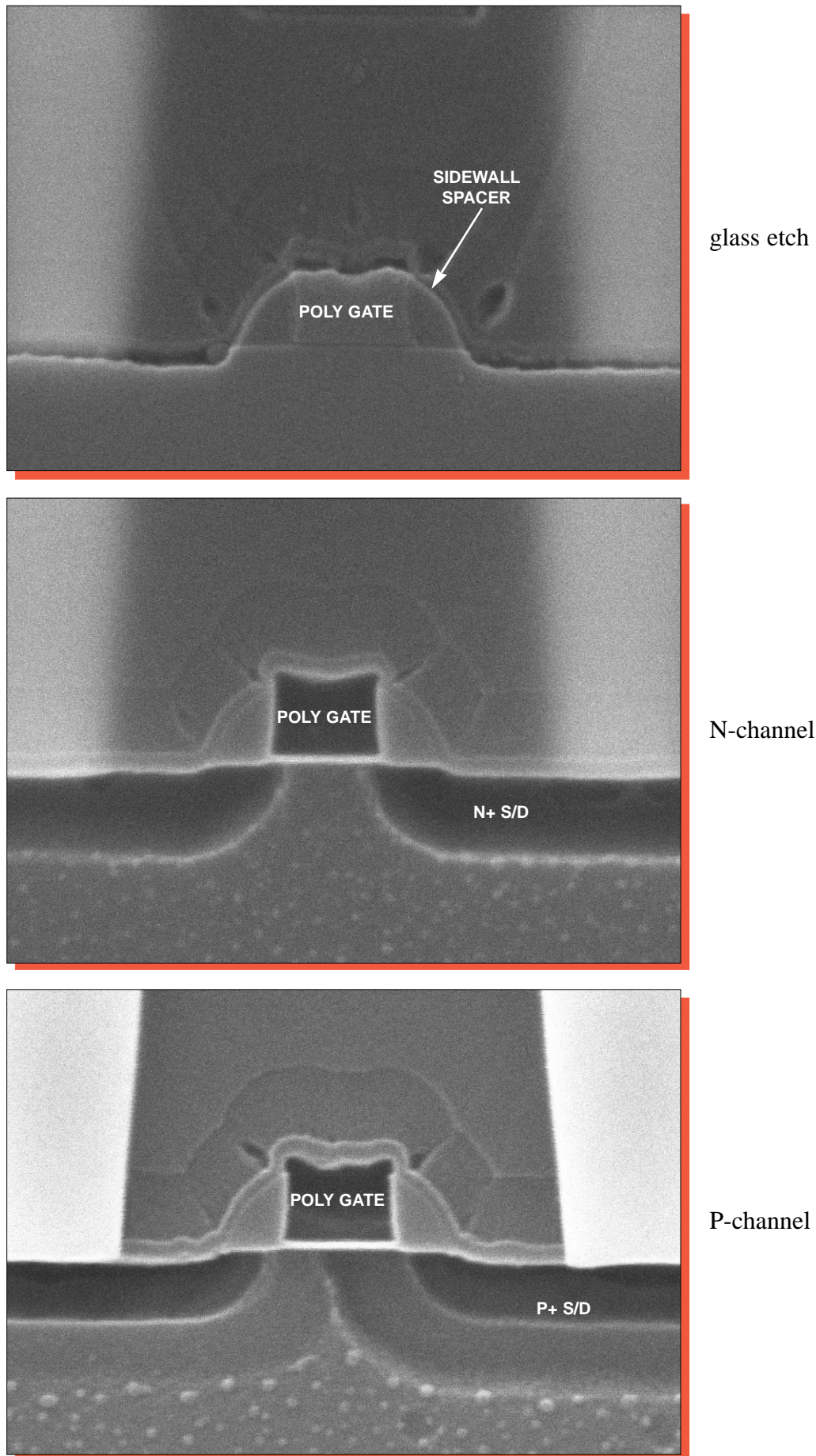
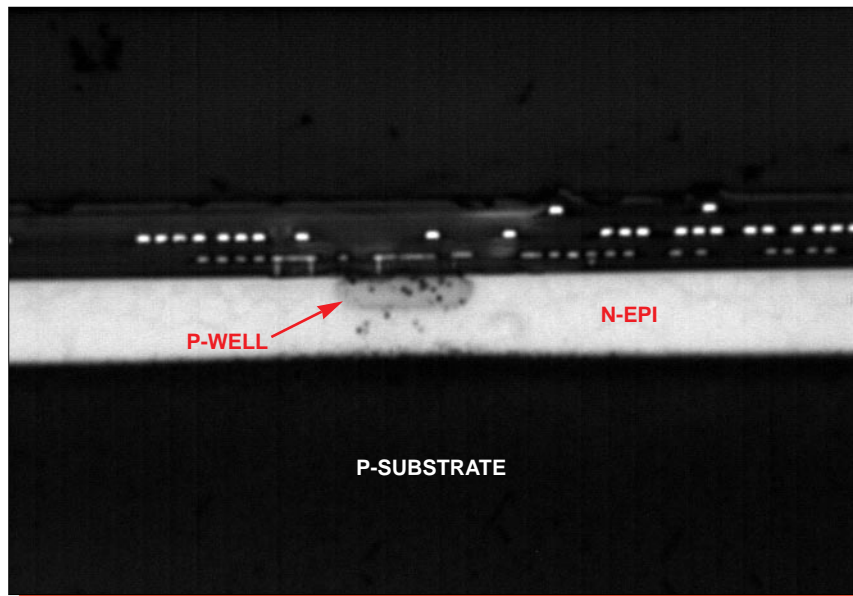
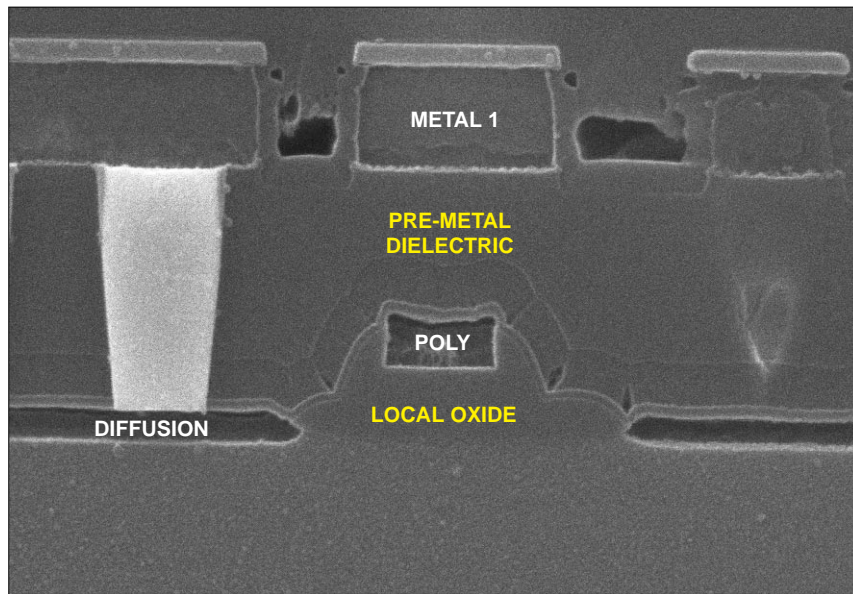


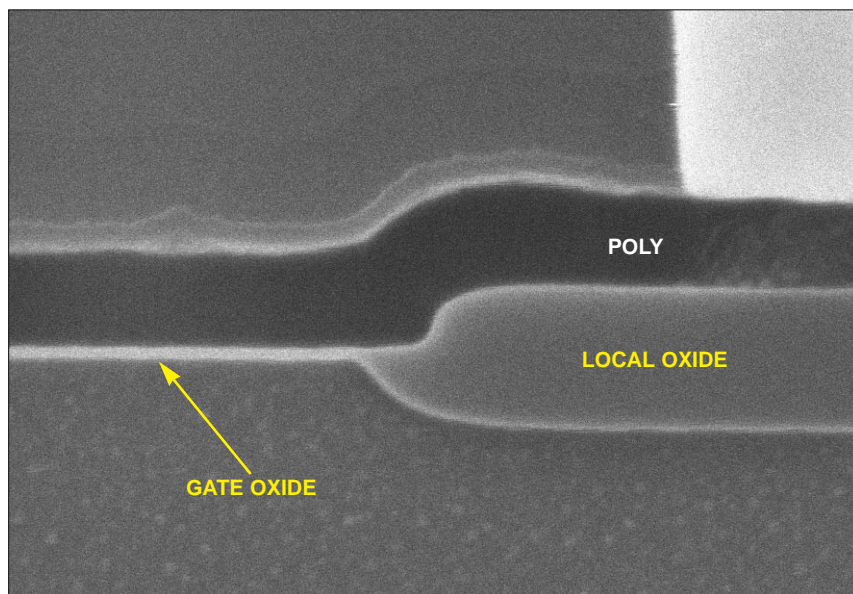
Figure 23. Detailed SEM views illustrating typical gates. Mag. 52,000x.



Mag. 1535x

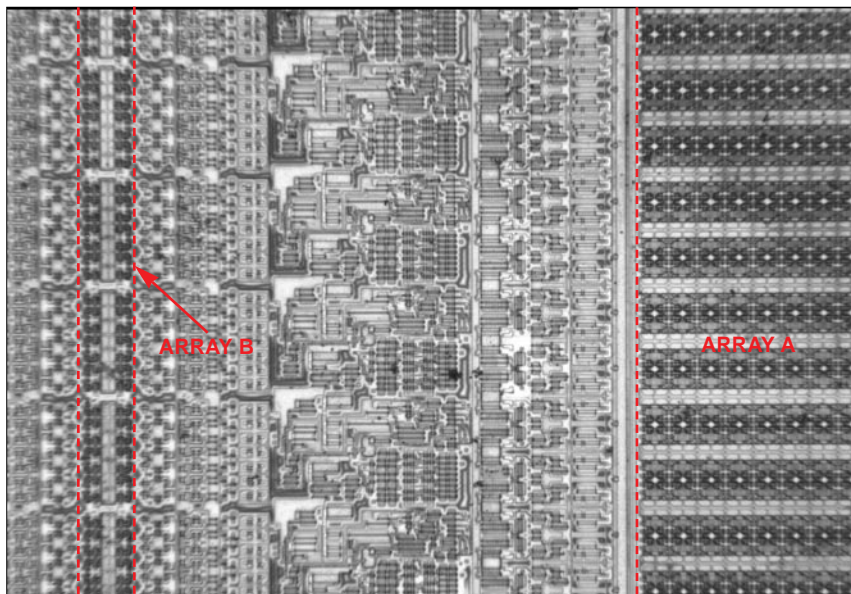


Mag. 26,000x

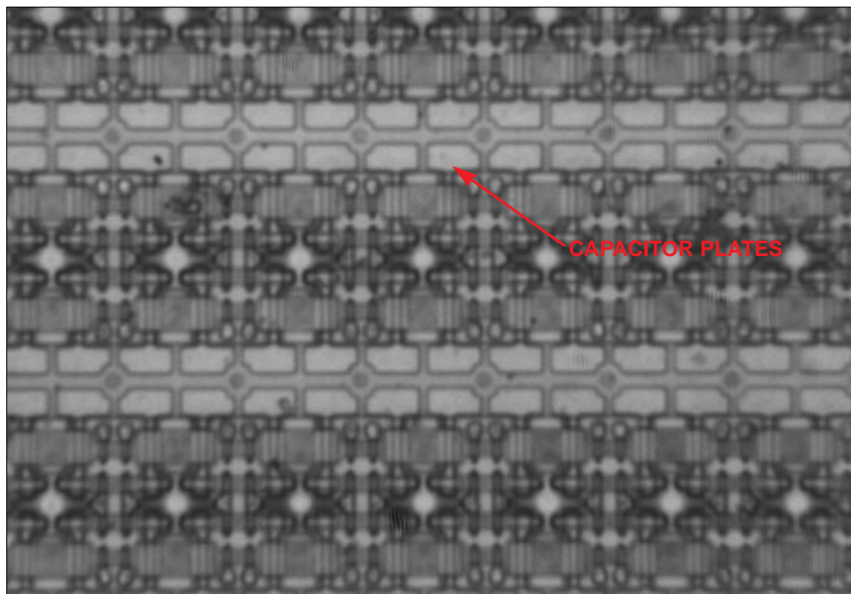


Mag. 52,000x

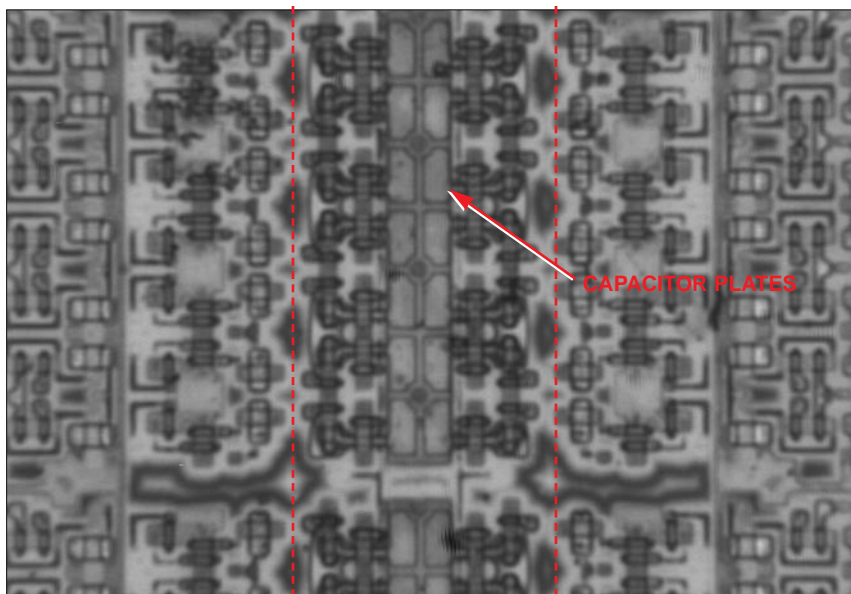
Figure 24. Section views illustrating well structure, local oxide, and typical birdsbeak.



Mag. 350x

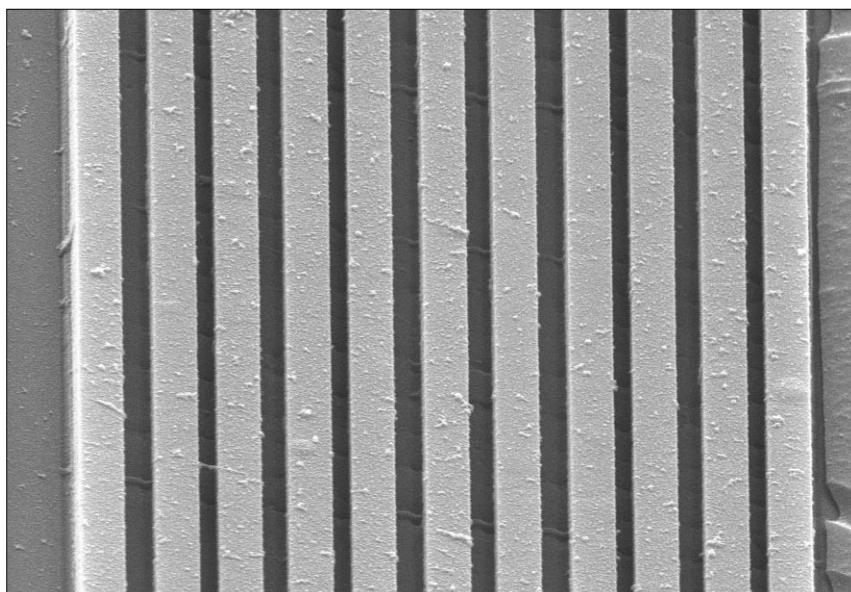


array A,
Mag. 1535x

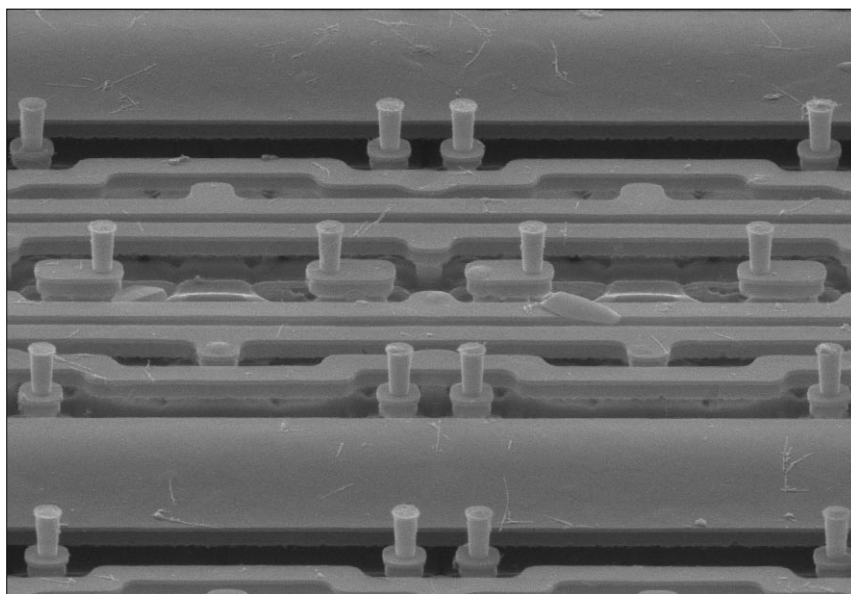


array B,
Mag. 1535x

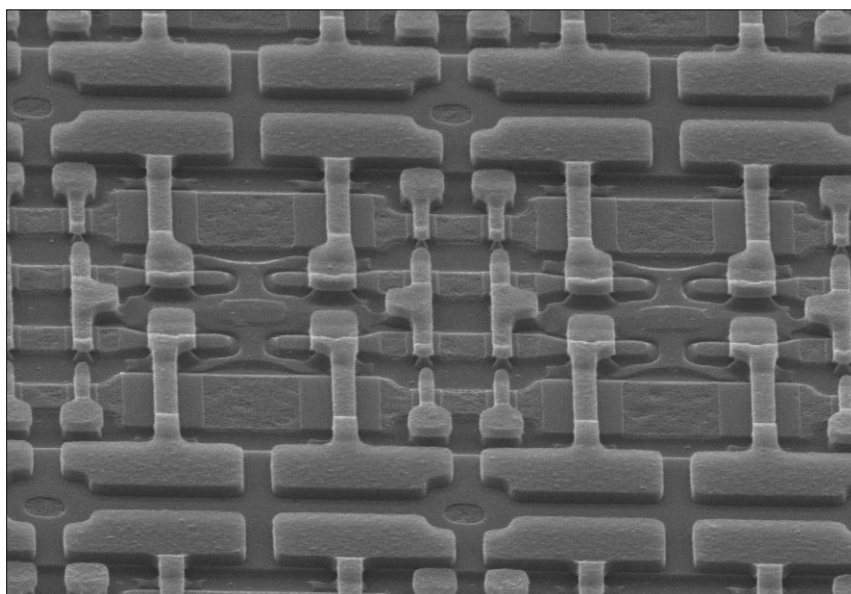
Figure 25. Optical views of EEPROM cell arrays.



metal 2

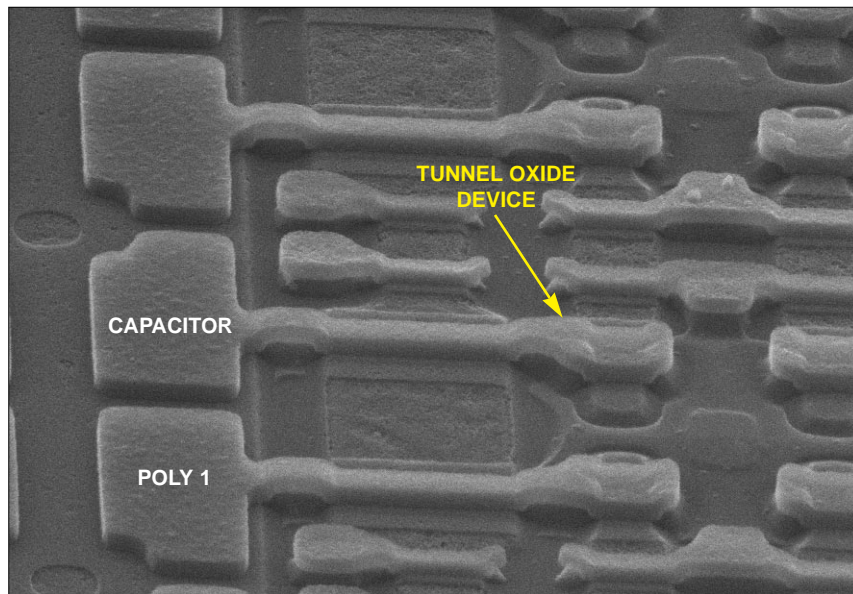


metal 1

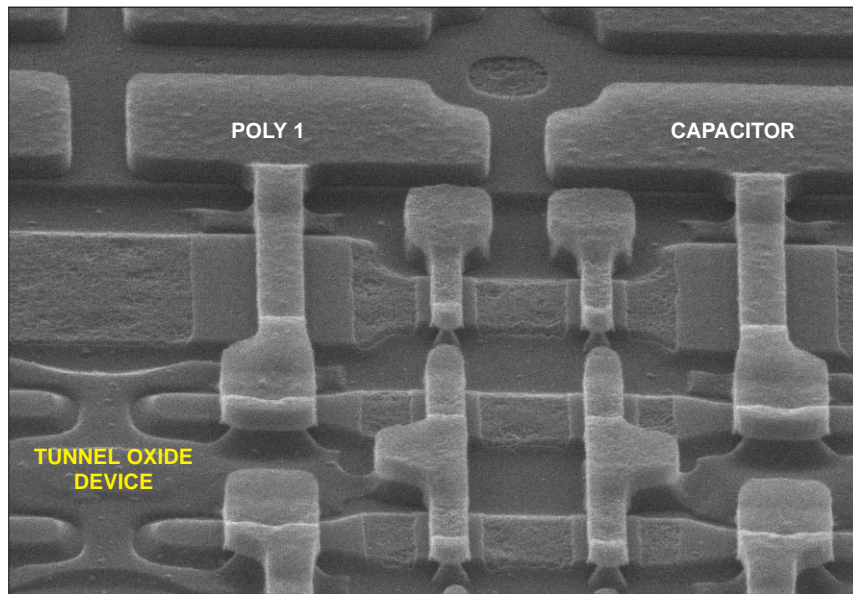


poly

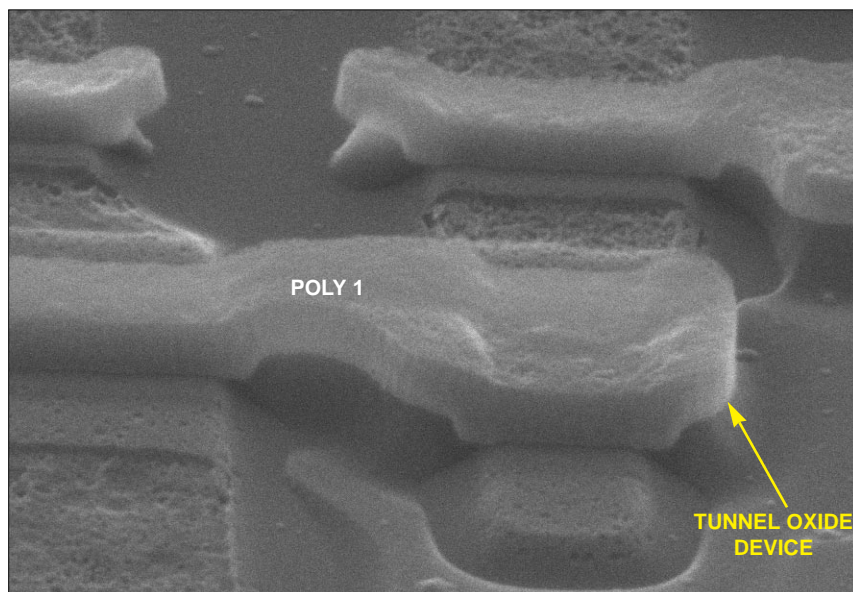
Figure 26. SEM views illustrating EEPROM array A. Mag. 5450x, 60°.



Mag. 8800x

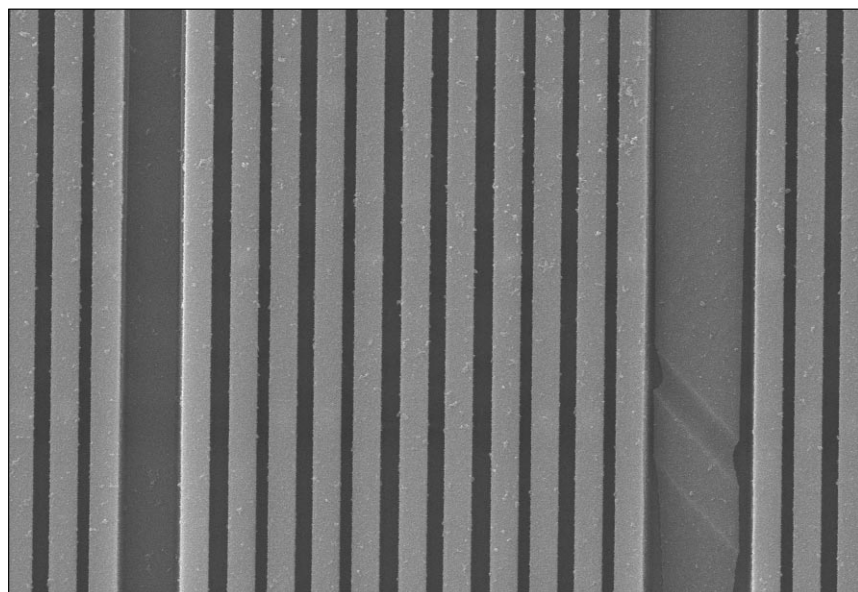


Mag. 10,000x

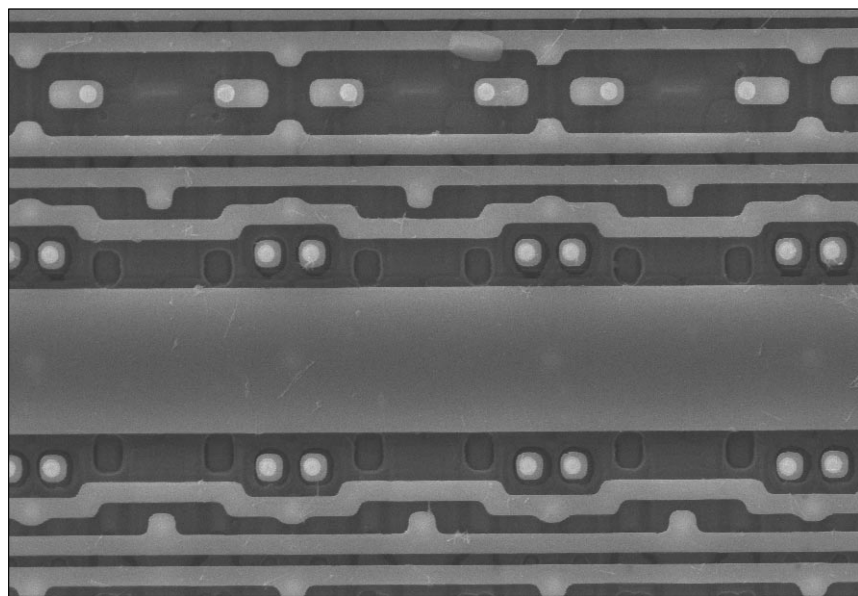


Mag. 27,000x

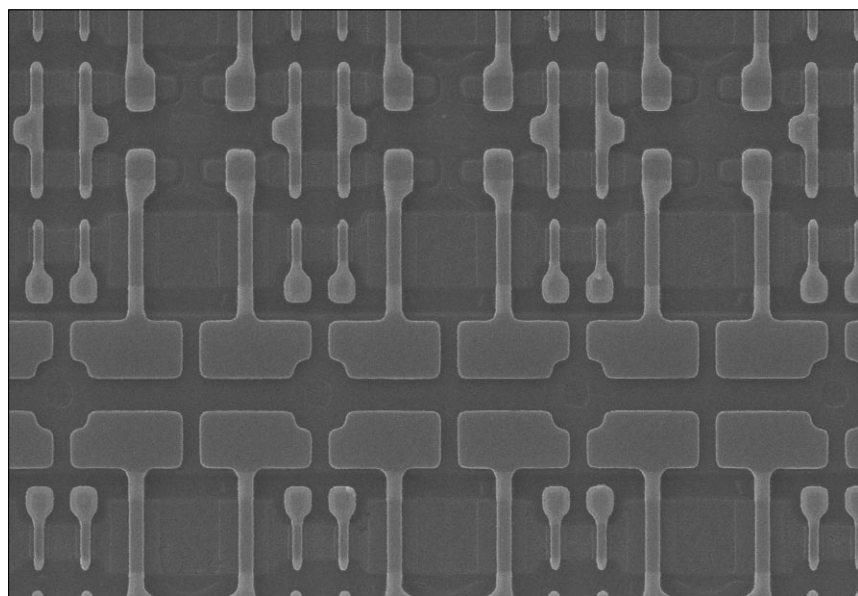
Figure 27. Detailed SEM views illustrating EEPROM array A. 60°.



metal 2

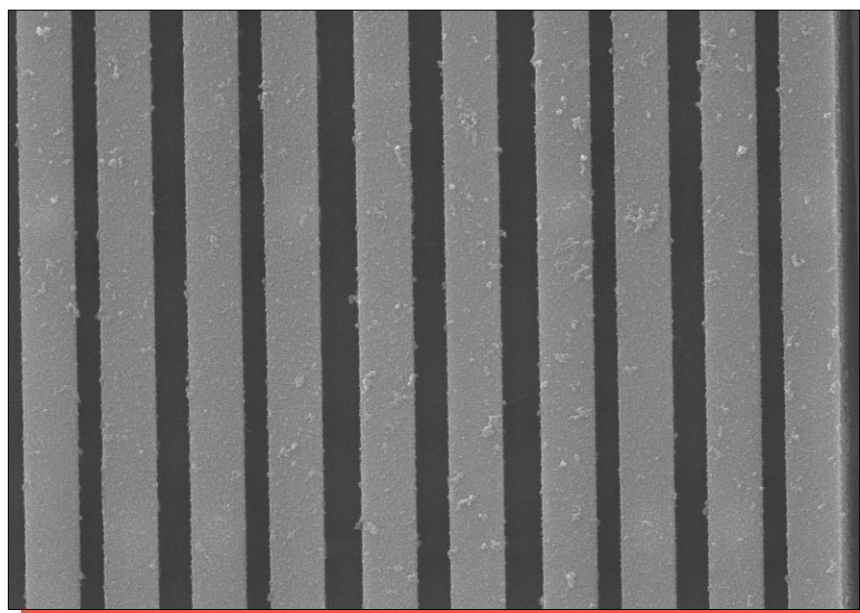


metal 1

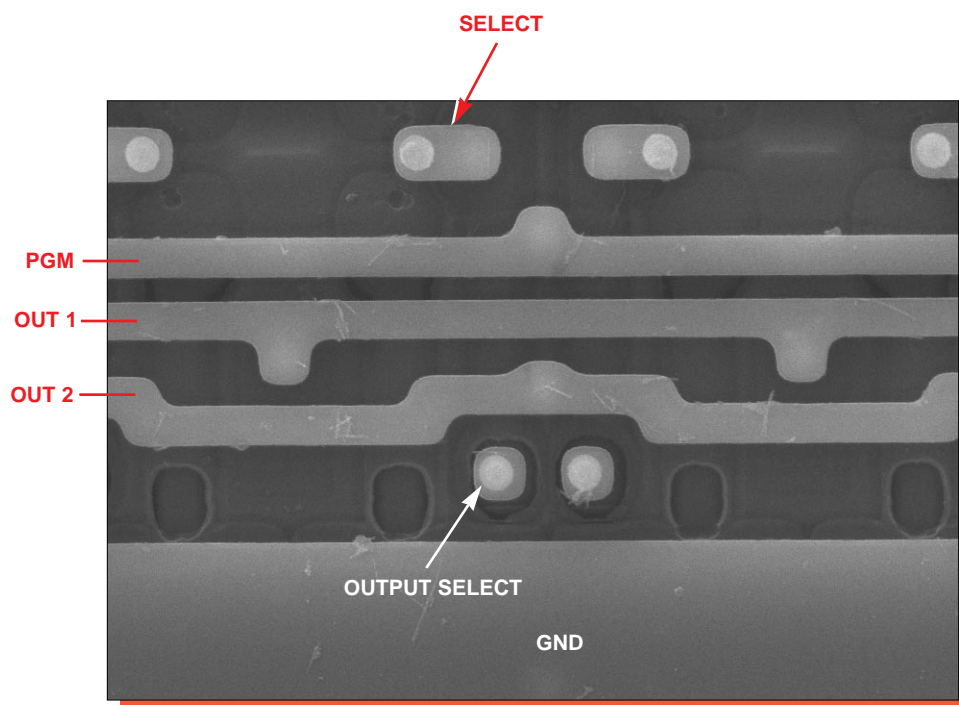


unlayered

Figure 28. SEM views illustrating EEPROM cells in array A. Mag. 3250x, 0°.

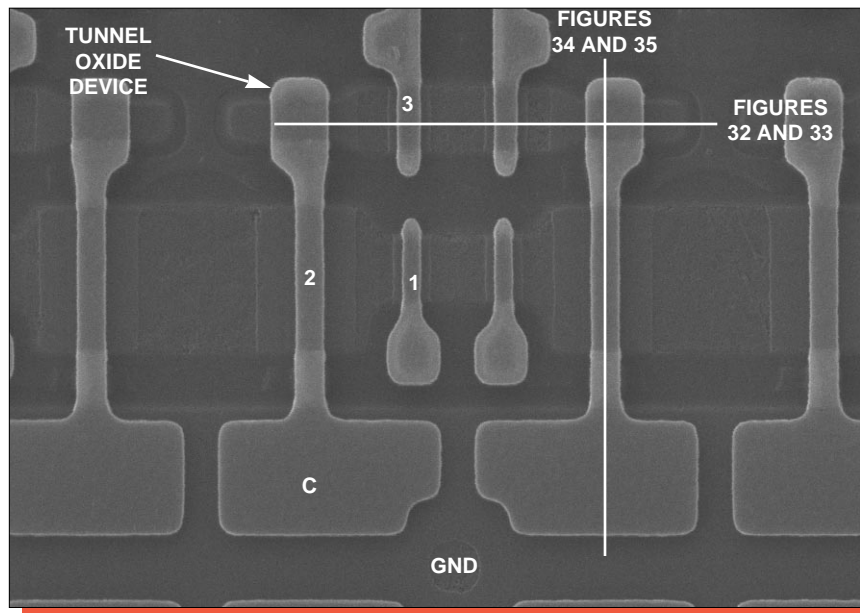


metal 2



metal 1

Figure 29. Detailed SEM views illustrating EEPROM cells in array A. Mag. 6500x, 0°.



unlayered

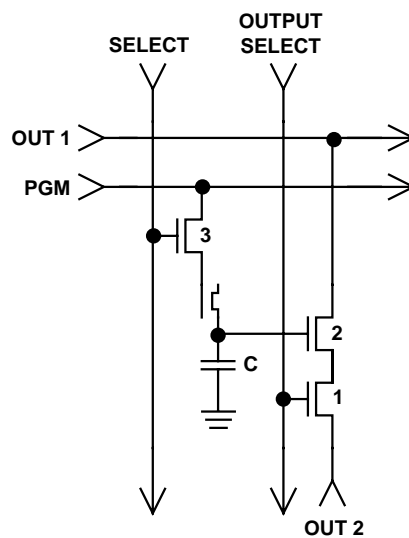
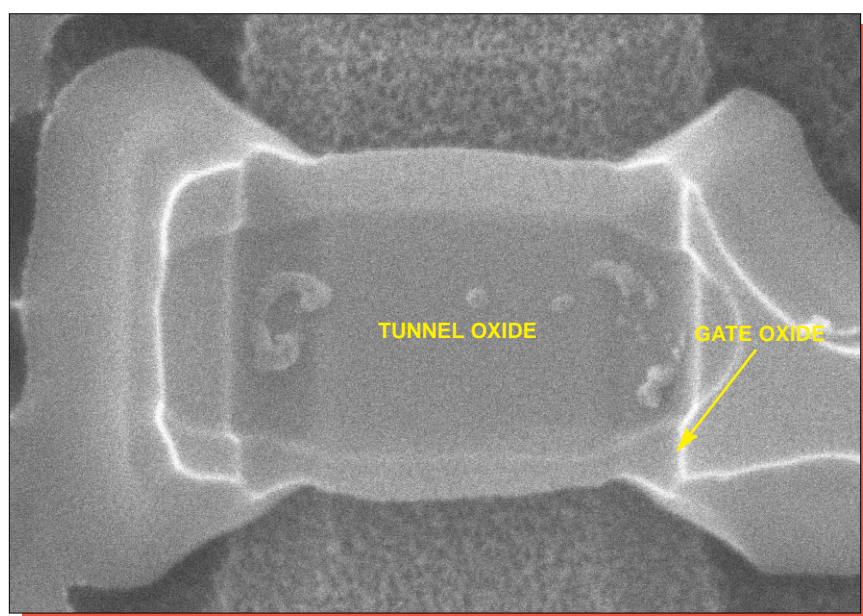
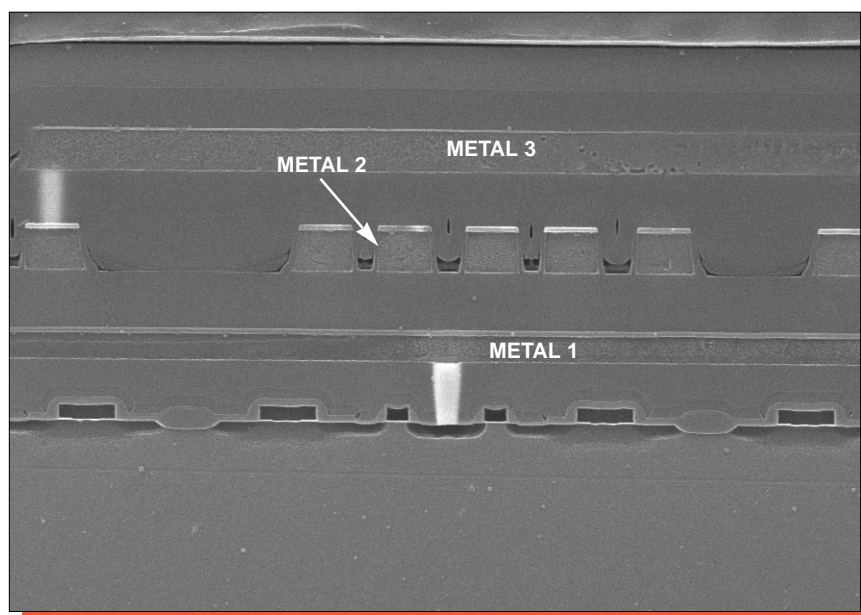


Figure 30. Detailed SEM view illustrating EEPROM cell in array A and schematic.
Mag. 6500x, 0°.

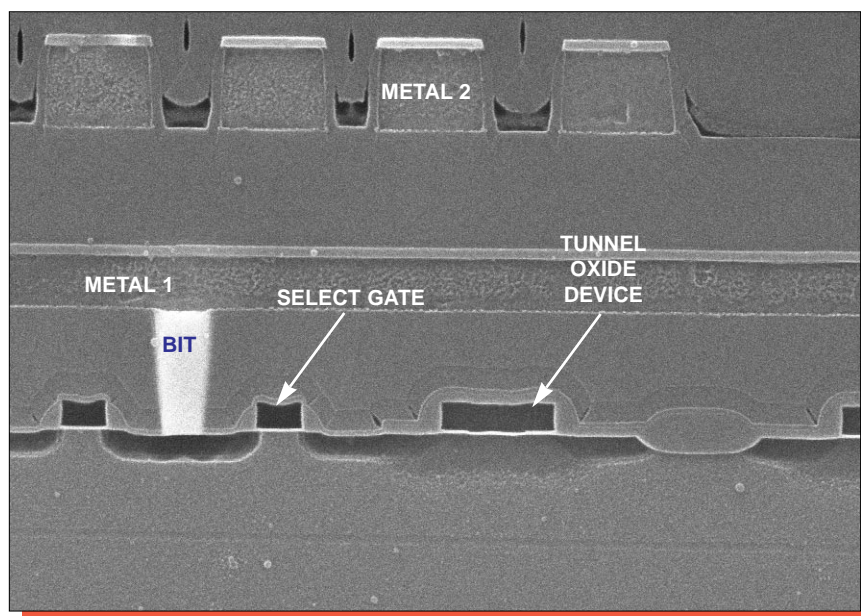


poly removed

Figure 31. Topological view of the tunnel oxide window. Mag. 52,000x, 0°.



Mag. 6500x



Mag. 13,000x

Figure 32. SEM section views illustrating an EEPROM cell in array A.

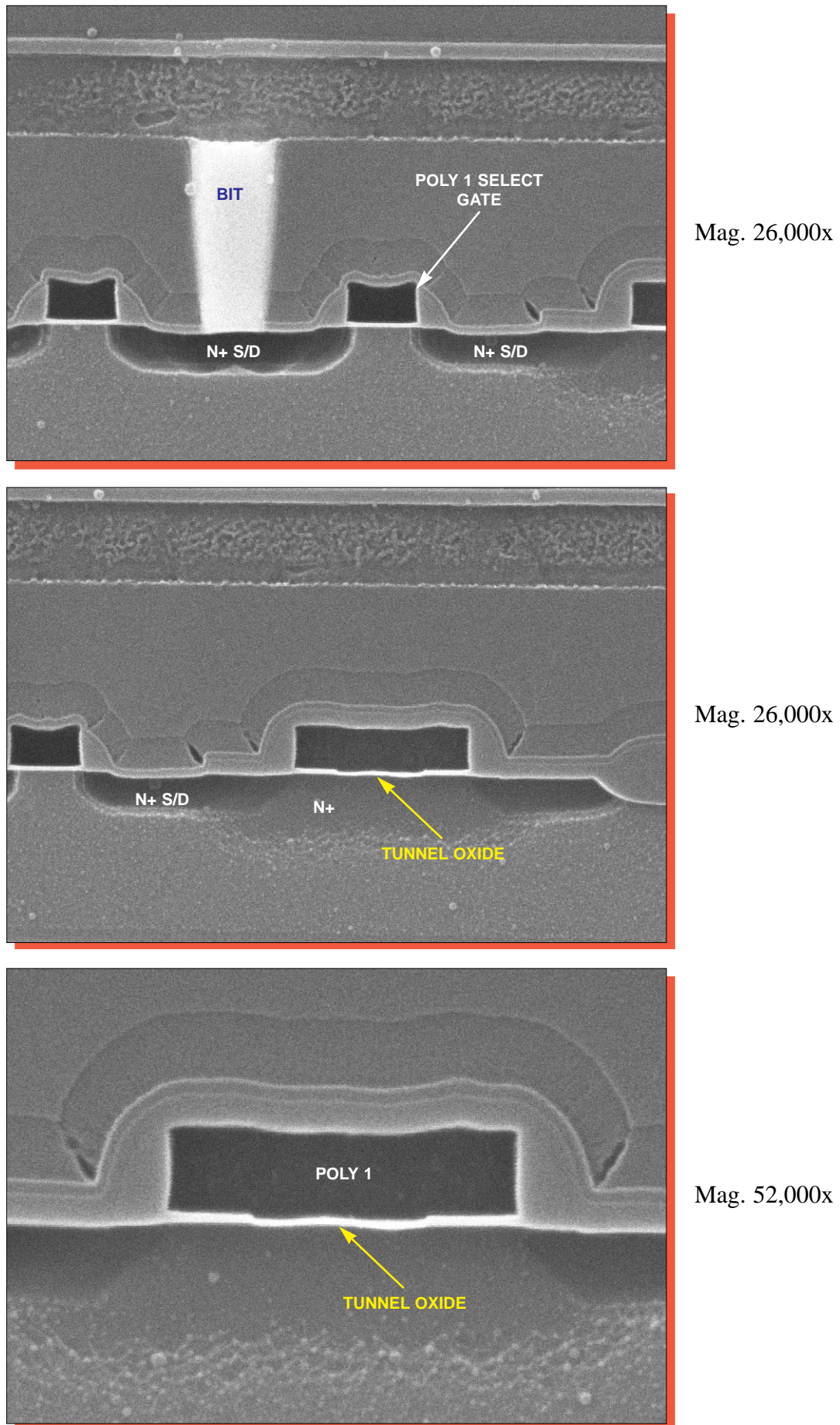
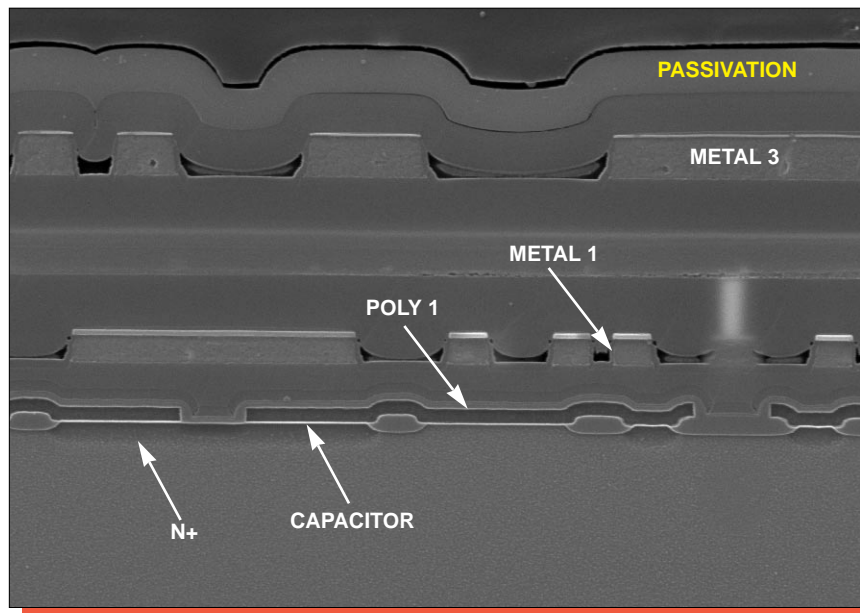
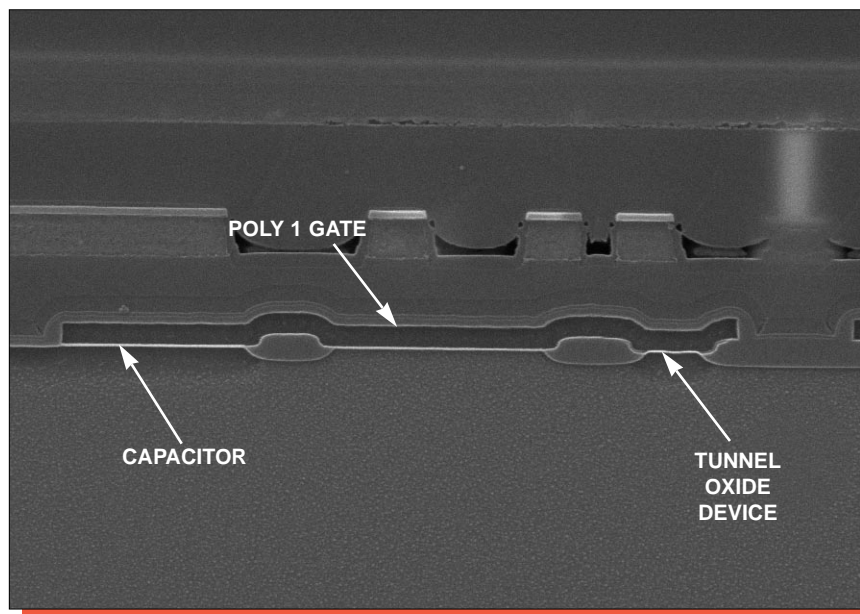


Figure 33. Detailed SEM views illustrating an EEPROM cell in array A.



Mag. 6500x



Mag. 10,000x

Figure 34. SEM views illustrating an EEPROM cell in array A.

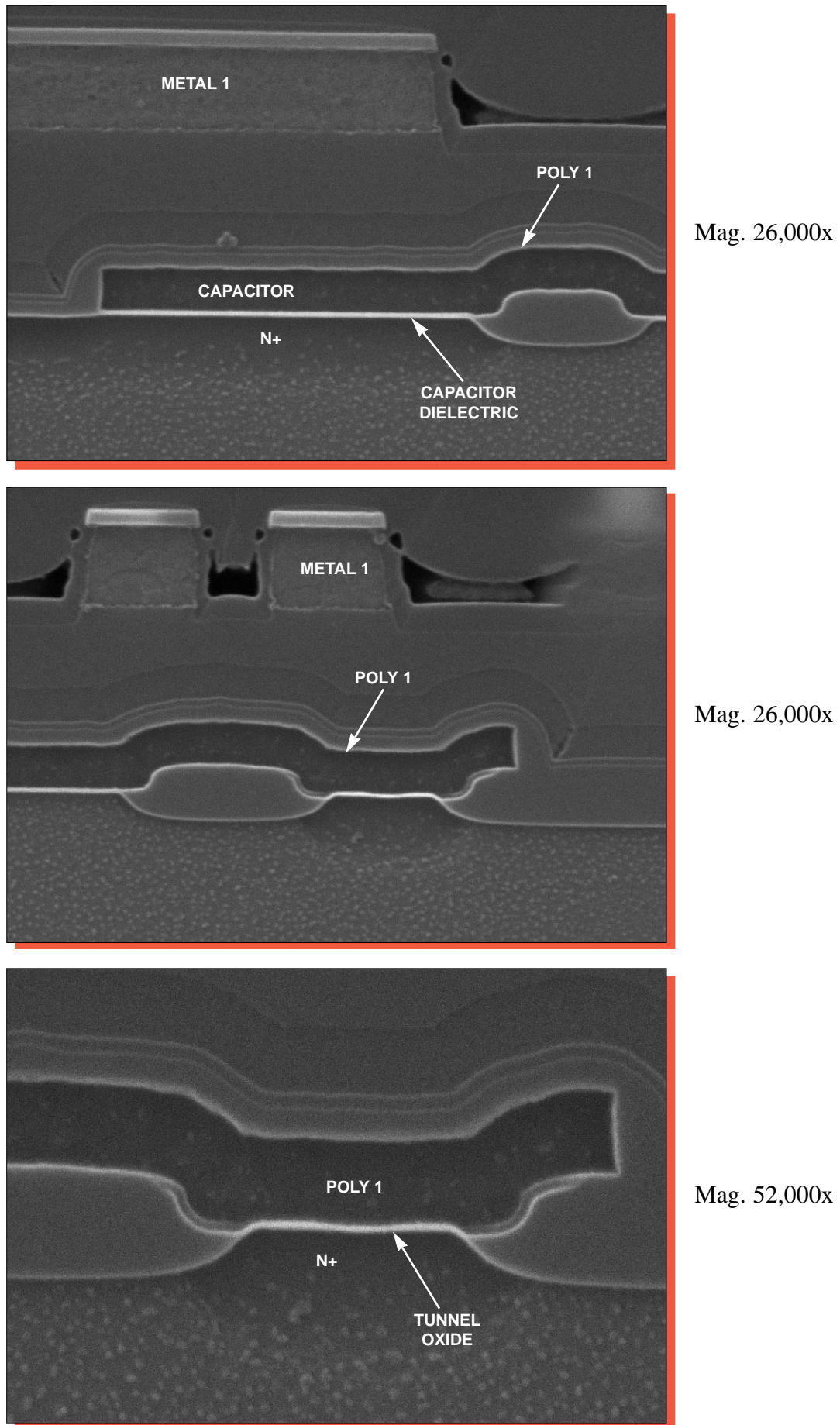


Figure 35. Detailed SEM views illustrating an EEPROM cell in array A.

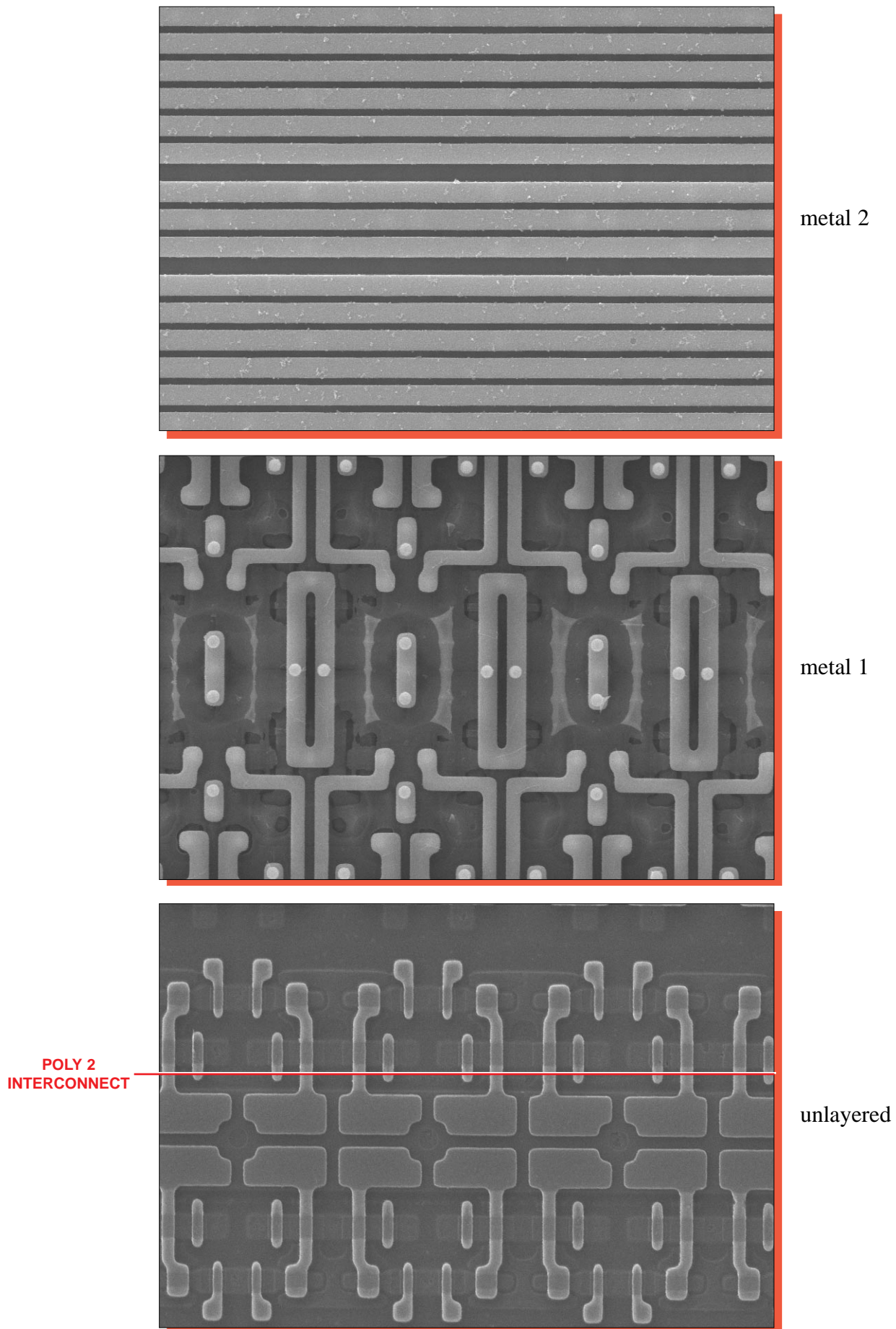
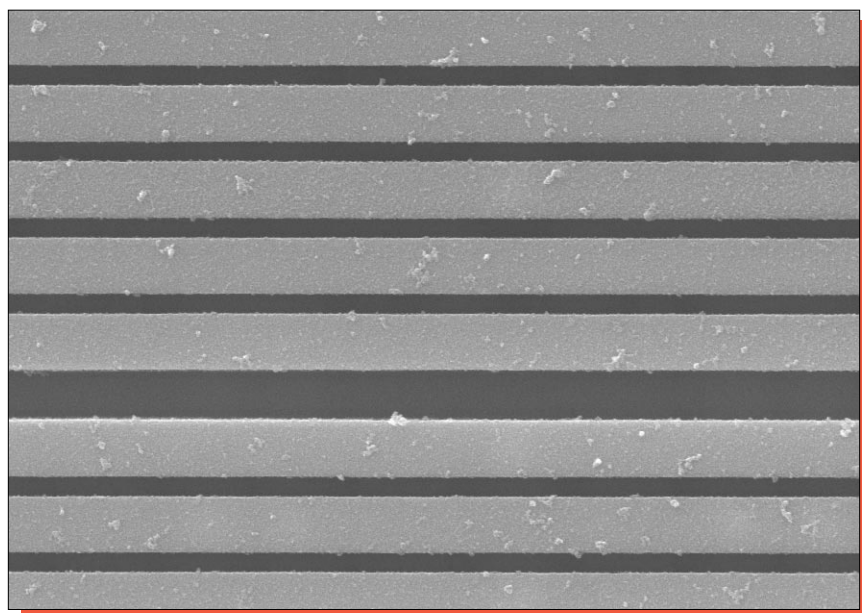
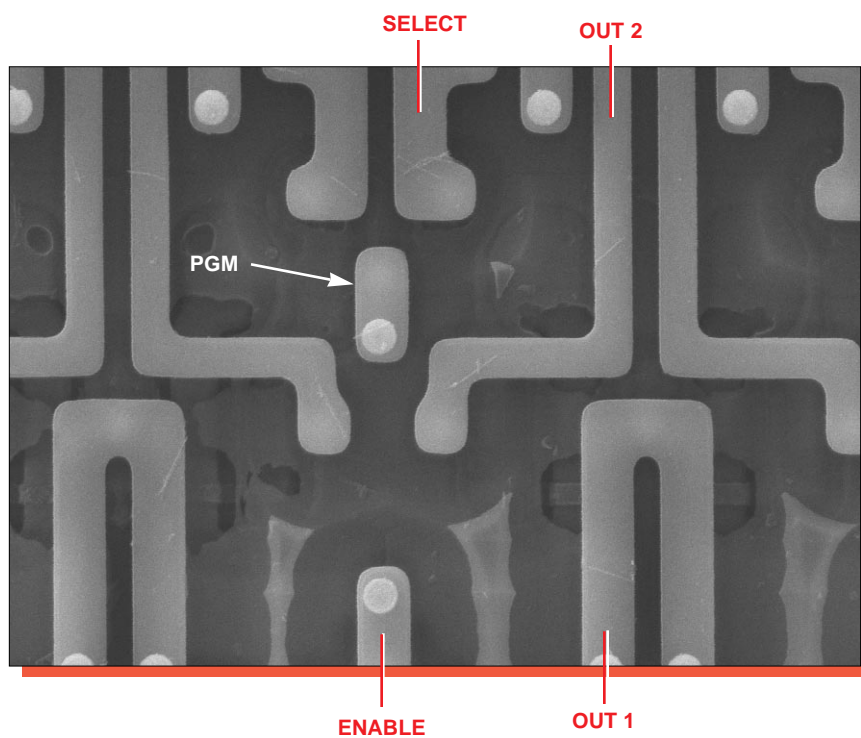


Figure 36. SEM views illustrating the EEPROM cells in array B. Mag. 3250x.



metal 2



metal 1

Figure 37. SEM views illustrating the EEPROM cell in array B. Mag. 6500x.

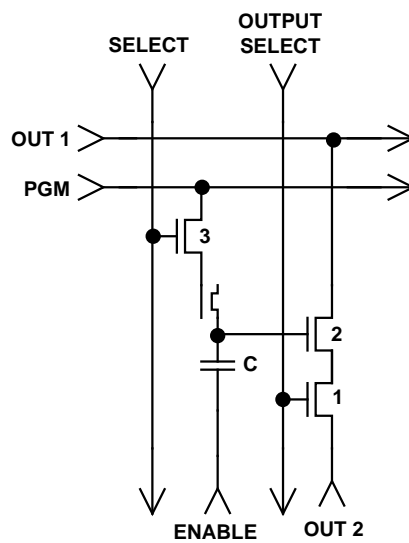
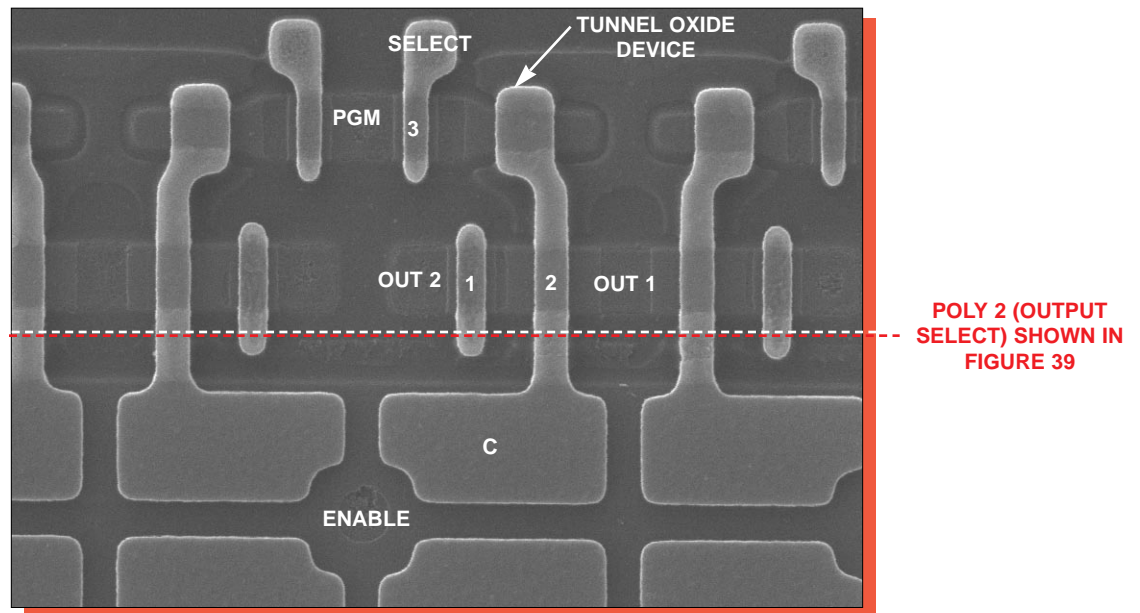


Figure 38. SEM views illustrating the EEPROM cell in array B and schematic.
Mag. 6500x.

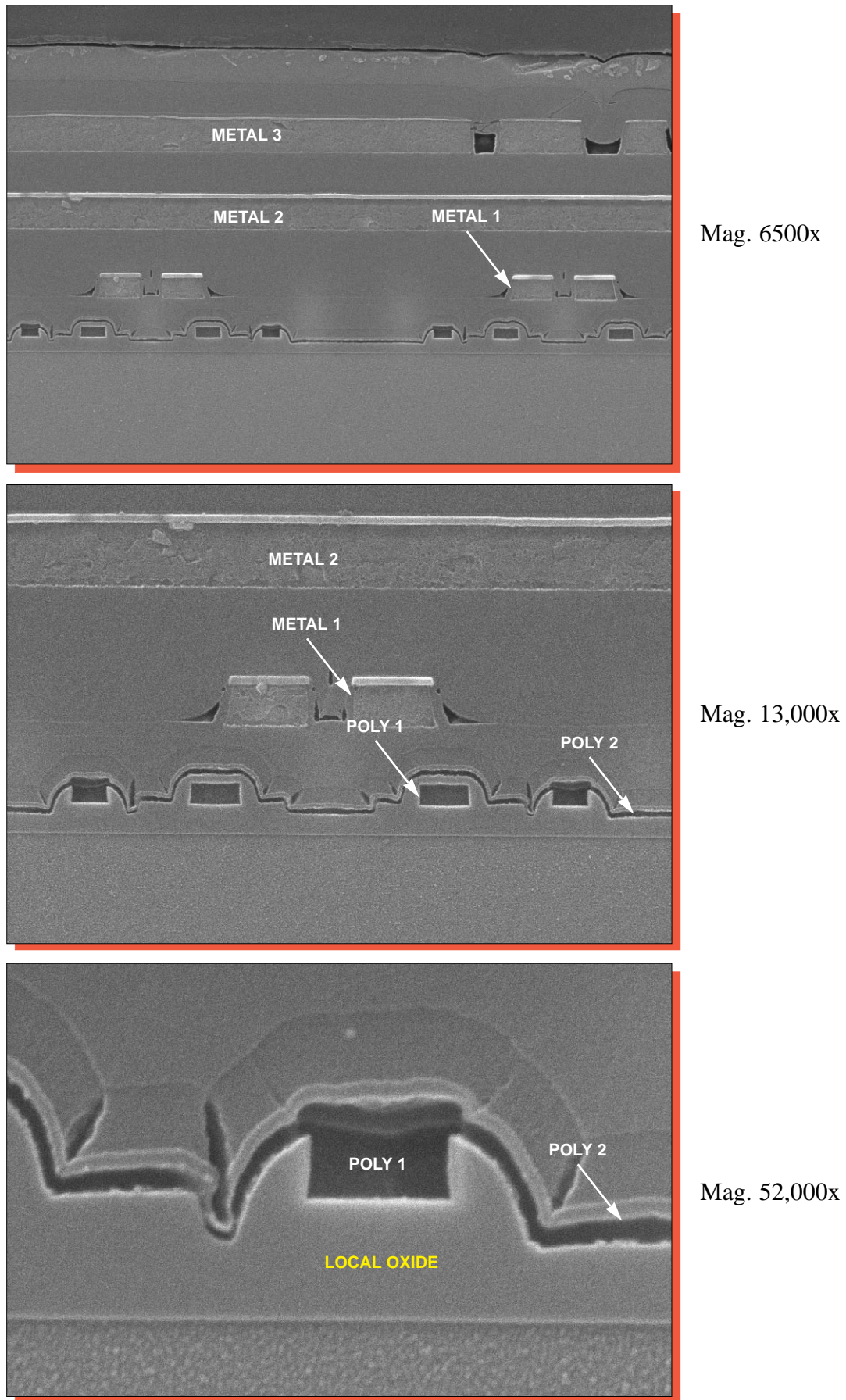
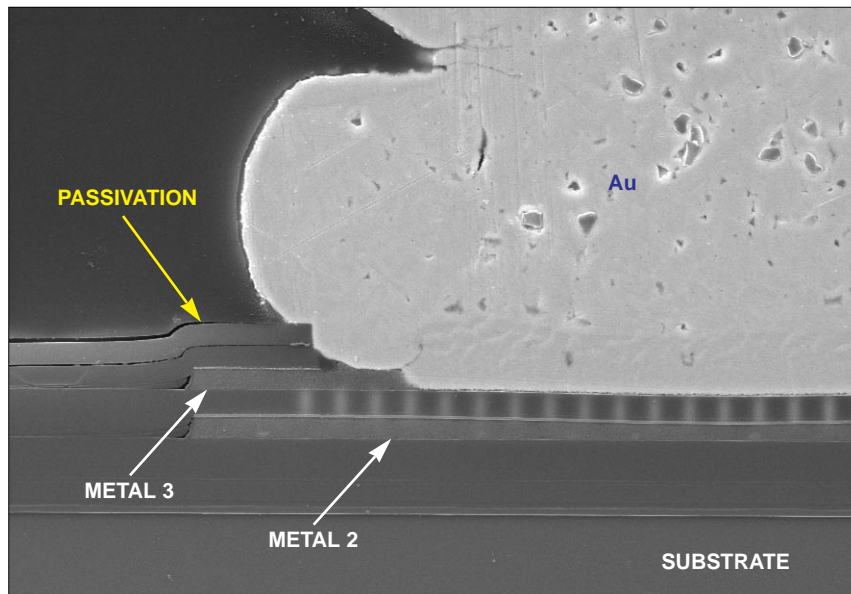


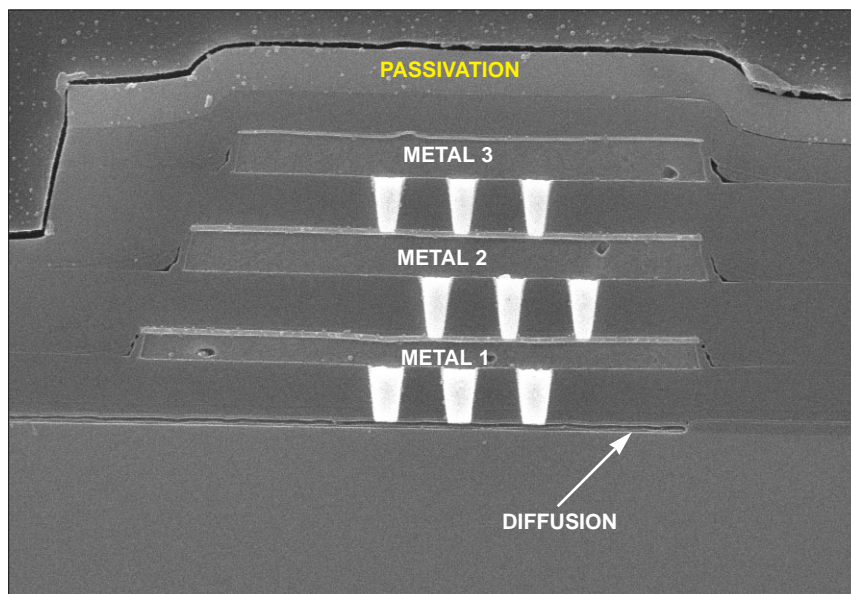
Figure 39. SEM section views illustrating poly 2 interconnect in EEPROM cell array B.



Mag. 3250x

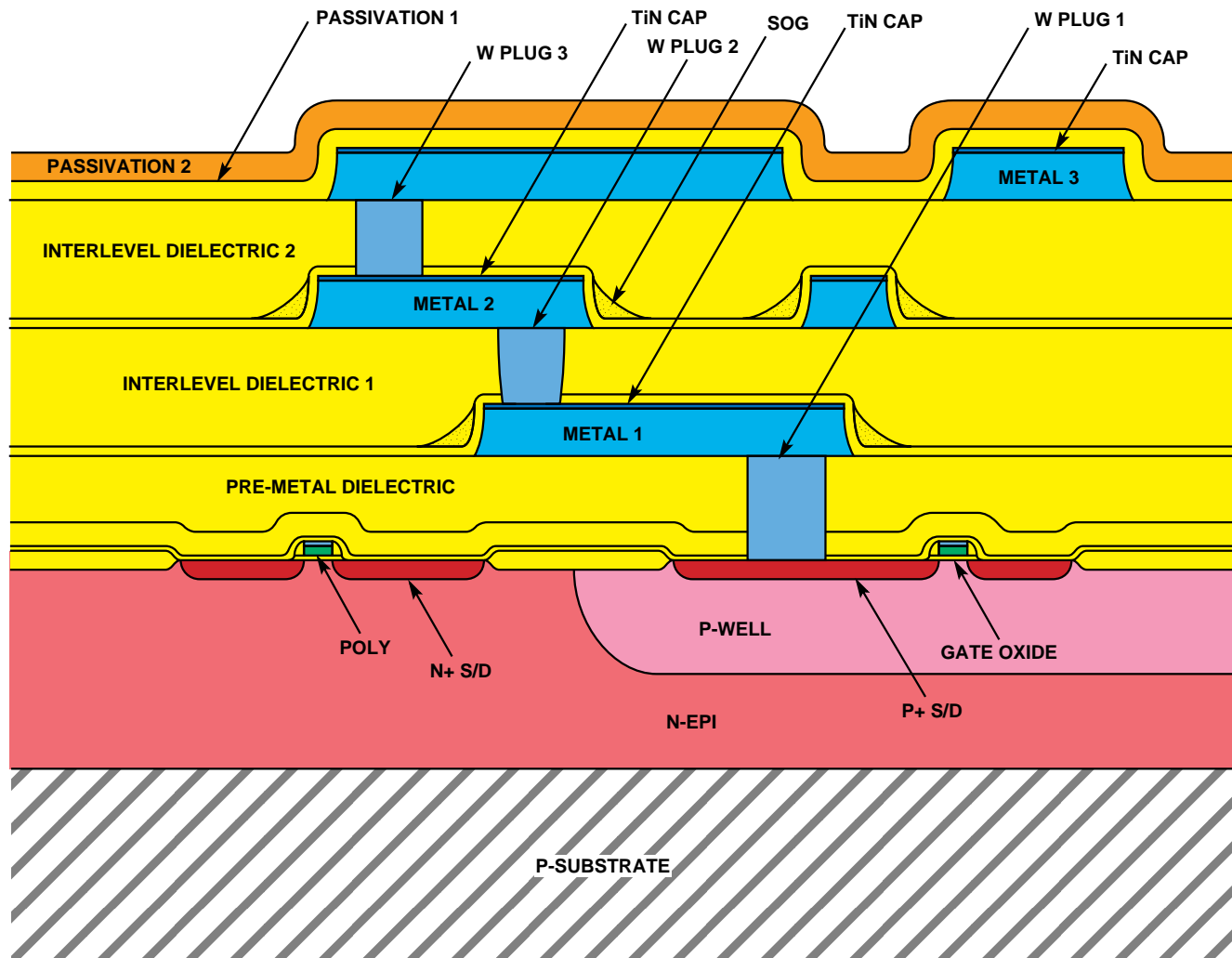


Mag. 1600x



Mag. 6500x

Figure 40. SEM section views illustrating a bond pad and edge seal.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

Figure 41. Color cross section drawing illustrating device structure.