

## Construction Analysis

# Toshiba TC5165165AFT-50 64 Mbit DRAM

Report Number: SCA 9702-524



**INTEGRATED CIRCUIT ENGINEERING**

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## **INTRODUCTION**

This report describes a construction analysis of the Toshiba TC5165165AFT-50, 64 Mbit DRAM. Three devices packaged in 50-pin TSOP plastic packages using an LOCCB design were received for the analysis. Parts were date coded 9651.

## **MAJOR FINDINGS**

### **Questionable Items:<sup>1</sup>**

- Metal 3 aluminum thinned up to 95 percent<sup>2</sup> at some via edges (Figure 14). We suspect that this is not really a problem but the manufacturer should be consulted.

### **Special Features:**

- LOCCB (Lead on chip, center bonded) package design.
- Tight metal pitch (0.8 micron M2 and 0.7 micron M1). Metal 1 was composed of damascene tungsten on a titanium-nitride barrier.
- Deep (7 microns) poly-filled trench capacitors. Cell size 1.1 micron<sup>2</sup>.
- Shallow trench oxide isolation.
- Extremely close contact-to-edge of gate spacing in array (approximately 500Å), made possible by densified oxide sidewall etch stops with a thin nitride.

<sup>1</sup>*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

<sup>2</sup>*Seriousness depends on design margins.*

## **TECHNOLOGY DESCRIPTION**

### **Assembly:**

- The devices were packaged in 50-pin, plastic, Thin Small Outline Packages (TSOP) with gull-wing leads for surface mount applications.
- The leadframe design was LOCCB (lead-on-chip, center bond). Multiple internal leadframe “fingers” were employed at power pins as well as some other pins. The die surface was connected to the bottom of the leadframe using a double backed Kapton-type tape. A thin, patterned polyimide die coat was used.
- Lead-locking design was present at all pins. No header/paddle was employed.
- Die separation by sawn dicing (full depth).
- Wirebonding by the thermosonic ball bond method using 1.1 mil gold wire.
- Numerous pins were not connected.

### **Die Process**

- Layout design: The 166 mm<sup>2</sup> (8.8 x 18.8 mm) die used a design employing eight blocks of cell arrays, with the peripheral circuitry forming a cross in the middle of the die, facilitating the center bond assembly.
- Fabrication process: Oxide filled shallow trench CMOS process employing multiple-wells in a N-epi on a P substrate.
- Final passivation: A layer of silicon-nitride over a layer of silicon-dioxide.
- Metallization: Three levels of metal were employed on the die. Metals 2 and 3 consisted of a layer of dry-etched aluminum with titanium-nitride caps and barriers.



## **TECHNOLOGY DESCRIPTION (continued)**

Metal pitch for M2 was 0.8 micron, while M1 had a 0.7 micron pitch. Standard vias were used with Metal 3, while Metal 2 employed tungsten plugs at vias. Metal 1 consisted of a damascene tungsten with a titanium-nitride barrier. Tungsten plugs were used at Metal 1 contacts.

- **Intermetal dielectrics:** Intermetal dielectric layers (IMD1 and IMD2) each consisted of a thick layer of deposited glass followed by a thin glass. Both intermetal dielectrics had been planarized by CMP (chemical mechanical planarization).
- **Pre-metal dielectric:** Dielectric under M1 consisted of a thin layer of glass over a thick layer of silicon-dioxide and densified oxides. A thin nitride layer was apparent over the densified oxide. This structure appears to have been planarized by CMP.
- **Polysilicon:** Three layers of polysilicon were employed. The first layer was used to fill the trenches (probably deposited in two steps as reported by IBM), forming the individual trench capacitor plates in the array (i.e. not really a “layer”). The second layer consisted of a polycide (tungsten silicide) which formed all gates on the die. The third layer was used exclusively in the cell array to form small connecting links (“straps”) between the drains of the select gates and the trench capacitors.
- **Diffusions:** Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Sidewall spacers had been used to provide the LDD spacing. As mentioned, a thin nitride layer was deposited over the densified oxide. It provides both an etch stop to insulate gates from the tungsten plugs making contact to the source/drain diffusions, facilitating what IBM calls “borderless contacts”, and also provides a sealing layer to stop contaminants from the CMP process.
- **Wells:** A complex well structure is present. The substrate is P type with a thin apparent N-epi. A P-well is diffused into the epi for the N-channel select transistors in the array. The P substrate appears to act as the common plate for the trench capacitors.

## **TECHNOLOGY DESCRIPTION (continued)**

Standard wells and possible retrograde wells are used in peripheral circuit areas. No step was noted in the oxide at well boundaries.

- Fuses: Poly 2 (polycide) redundancy fuses were used on the devices. Some laser blown fuses were found. Cutouts in the passivation and dielectrics were present over all fuses. There was an “undercut” at the base of the cutout over the fuses. It appears that Metal 1 tungsten was deposited over the fuses and was used as an etch stop for the cutout. The tungsten layer was subsequently removed by a wet etch leaving the void (“undercut”).
- Memory cells: The memory cells consisted of a “trench capacitor” DRAM design referred to by IBM as a “Buried Plate Trench” (BPT) cell. Metal 3 was not used directly in the individual cell arrays. Metal 2 formed “piggyback” word lines. Metal 1 formed the bit lines, poly 2 (polycide) formed the word lines and select gates. The individual capacitor plates were formed by poly 1 filled trenches. The common capacitor plate was the P-substrate. IBM has reported that an N-well forms the common plate of the trench capacitors by out diffusion from the cell trenches. It does not appear that this process feature is present on this device, since no evidence of the N-well region could be revealed in cross-section. A thin oxide-nitride-oxide sandwich was apparently used for the capacitor dielectric. Trenches were offset from the select gates so a small poly 3 link (“strap”) was used to connect the drains of the select gates to the trench capacitor poly. Trenches were 7.0 microns deep, but only had a 0.2 micron x 1 micron surface area. Select gates were formed in the shallow P-wells and bit contacts were of the “borderless” type. Cell size was 0.75 x 1.45 micron (1.1 micron<sup>2</sup>).

## **ANALYSIS RESULTS I**

### **Assembly:**

### **Figures 1 - 4**

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- LOCCB leadframe design.

### **General Items:**

- Overall package quality: Good. No defects were found on the external portions of the packages. External (gull-wing) pins were well formed and tinning of the leads was complete. No voids or cracks were noted anywhere.
- Wirebonding: Thermosonic ball bond method using 1.1 mil gold wire. Bonds were well formed and placement was good.
- Die attach: The die was attached to the underside of the leadframe with a double side Kapton-type tape. No problems were found.
- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges.
- A thin, patterned, polyimide die coat was apparently employed over the die surface. No problems were noted.
- Metal bus lines were beveled slightly at die corners (no slots noted) to relieve stresses. A poly 2 “waffle pattern” was present in the inactive circuit areas of the die. This pattern is apparently employed to aid the CMP planarization purposes.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **ANALYSIS RESULTS II**

### **Die Process and Design:**

**Figures 5 - 46**

#### **Questionable Items:<sup>1</sup>**

- Metal 3 aluminum thinned up to 95 percent<sup>2</sup> at some via edges (Figure 14).

#### **Special Features:**

- Tight metal pitch and damascene Metal 1 (tungsten).
- Deep trench cell capacitors. Cell size 1.1 micron<sup>2</sup>.
- Oxide filled shallow trench isolation.

#### **General Items:**

- Fabrication process: Oxide filled shallow trench isolation CMOS process employing multiple-wells in a P substrate with shallow N-epi. No significant problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A thin patterned polyimide die-coat covered a layer of silicon-nitride over a layer of silicon-dioxide. The passivation integrity test indicated defect-free passivation. Edge seal was also good, as the passivation extended into the

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

*<sup>2</sup>Seriousness depends on design margins.*

## **ANALYSIS RESULTS II (continued)**

scribe lane to seal the metallization.

- Metallization: Three levels of metallization were used. Metal 2 and 3 consisted of aluminum with a titanium-nitride cap and barrier. Metal 1 consisted of damascene tungsten on a titanium-nitride barrier. Standard vias were used between M3 and M2. Metals 2 and 1 used tungsten plugs.
- Metal patterning: Metals 2 and 3 were patterned by a normal dry etch. The observed feature that indicates the use of the damascene technique is the fold observed in the center of the metal 1 lines - shown in Figures 20, 24, 39, 41 and 44.
- Metal defects: None. No notching or voiding of the metal layers was found. No silicon nodules were noted following the removal of the aluminum.
- Metal step coverage: Metal 3 aluminum thinned up to 95 percent at some via edges; however, the cap and barrier reduced total metal thinning to approximately 85 percent. MIL-STD allows up to 70 percent thinning for contacts of this size. No metal 2 or 1 thinning was noted due to the use of tungsten plugs.
- Contacts: Via cuts under M3 were slope-etched through the interlevel dielectric. No overetching of the vias was noted. Plugs under M2 and M1 had straight walls. Spacing to gate edges is only approximately 500Å where needed (e.g., in the cell array). No problems were found at any contacts or vias.
- Intermetal dielectric: Intermetal dielectric layers (IMD1 and IMD2) consisted of a thick layer of deposited glass followed by a thin glass. They were planarized by CMP. No problems were found with these layers. No SOG was used.

## **ANALYSIS RESULTS II (continued)**

- **Pre-metal dielectric:** This dielectric consisted of a thin layer of glass over a thick layer of silicon-dioxide followed by a thin nitride layer and densified oxides, on top of the polycide and diffusions. It appeared to be planarized by CMP and showed no evidence of any problems.
- **Polysilicon:** A total of three different layers of polysilicon were employed in this process. The first poly layer (poly 1) was used to fill the trenches of the memory cells and thus formed one side of the cell capacitor. Poly trenches were probably filled in two poly depositions. No problem areas were found in this layer. Poly 2 was a polycide (polysilicon with a tungsten-silicide on top) used throughout for transistor gates and for redundancy fuses. No problems were identified in this layer either. The third poly layer (poly 3) was a highly doped layer that was used exclusively to form very small connecting links (“straps”) between the drains of the select gates and the poly 1 capacitor plates in the cell array.
- **Isolation:** Oxide filled shallow trench isolation was used and was very well implemented. No steps were visible in this field oxide at the well boundaries.
- **Source/drain:** Implanted N<sup>+</sup> and P<sup>+</sup> diffusions were used for sources and drains. An LDD process was used and employed oxide sidewall spacers that appeared to be partially removed. A thin layer of nitride was deposited over the densified oxide. It provided an etch stop for protection against shorting the gates to the extremely closely spaced tungsten plugs contacting sources and drains. It is also useful as a sealing layer when using CMP. Diffusions were not silicided. No problems were found in any of these areas.
- **Wells:** Multiple-wells were used in a P substrate with a thin N-epi layer. Only some P-wells could be delineated well enough to obtain a depth measurement.

## **ANALYSIS RESULTS II (continued)**

- Fuses: Poly 2 redundancy fuses were present on the die. Some laser blown fuses were noted. Cutouts (passivation and intermetal dielectric) were present over all fuses. There was an “undercut” at the base of the cutout over the fuses. It appears that Metal 1 tungsten was deposited over the fuses and was used as an etch stop for the cutout. The tungsten layer was subsequently removed by a wet etch leaving the void (“undercut”).
- Memory cells: As mentioned, these parts used a trench cell design which is essentially the same as that used by IBM and Siemens. Whereas in trench cell designs from other manufacturers, the poly fill is always the passive common plate connected to a DC voltage or memory-enable, and the drains of the select gates connect via diffusion to the implant in the substrate around the trench, in this case, the P substrate around the trench is the common plate. This requires that this substrate region needs to be fairly low resistance and thus can not be the same as the body terminal of the select gates. Also, as described by IBM,\* isolation of this “substrate” (well) is desirable for operating characteristics. This is accomplished by forming an N-well around the trenches by out diffusing N+ through the trench walls. It does not appear that this last process feature was employed on this device, since no evidence of the N-well region could be revealed in cross-section. Select gates are N- type formed in the P-well so that the total vertical diffusion structure in the array is as follows. From the surface there are: N+ source/drains in the P-well which is within the N-epi on a P substrate. Since the poly filled trenches form the individual cell capacitor plates, a poly link (“strap”) is used to connect select gate drains to the trench poly. In addition to the above, the aspect ratio of the cell trenches was high (approximately 14:1 ), and the tungsten contact plugs were placed directly against the densified oxide/thin nitride layer that protected the edges of the select gates. Since the layout uses an offset between the various cell elements it is impossible to illustrate the entire cell structure in one cross section plane. Due to the

## **ANALYSIS RESULTS II (continued)**

high aspect ratio we were unsuccessful in showing any complete poly trench depth from the top to the bottom in one direction (see Figure 45); however, the full trench depth is clearly illustrated in Figures 42 and 43. With the tight structures present correct interpretation is difficult, however, an excellent and detailed explanation of the IBM 64M DRAM cell was published by E. Adler et. al. in the *IBM Journal of Research and Development*, Volume 39, No 1/2, January/March 1995. No problems were found in any of the structures, and cell size was measured to be 0.75 x 1.45 micron (1.1 micron<sup>2</sup>).

\**IBM Journal of Research and Development*, Volume 39, No 1/2, January/March 1995.



## **PROCEDURE**

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM inspection of assembly features and passivation

Delayer to metal 3 and inspect

Metal 3 removal and inspect barrier

Delayer to metal 2 and inspect

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal

Delayer to poly/substrate and inspect poly layers and substrate.

Die sectioning (90° for SEM)\*

Measure horizontal dimensions

Measure vertical dimensions

Material analysis

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal/Good

**DETAIL OF EVALUATION**

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Double backed tape.
Dicing method:	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	NP*
Metal registration	N
Contact coverage	G
Contact registration	G

*\*Metal 3 aluminum thinned up to 95 percent.*

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

## **PACKAGE MARKINGS**

### **TOP**

TOSHIBA T82253

9651KBD

JAPAN

TC5165165AFT-50

## **DIE MATERIALS**

Overlay passivation:	Silicon-nitride over silicon-dioxide.
Metal 3:	Aluminum with a titanium-nitride cap and barrier.
Intermetal dielectric 2:	Silicon-dioxide.
Metal 2:	Aluminum with a titanium-nitride cap and barrier. Tungsten plugs at vias.
Intermetal dielectric 1:	Silicon-dioxide.
Metal 1:	Tungsten with a titanium-nitride barrier and tungsten plugs.
Pre-metal dielectric:	Silicon-dioxide over a thin nitride on densified oxide.
Polycide:	Tungsten silicide on poly 2.

**Note:** Diffusion did not use a salicide process.

## **HORIZONTAL DIMENSIONS**

Die size:	8.8 x 18.8 mm (348 x 742 mils)
Die area:	166 mm <sup>2</sup> (258,216 mils <sup>2</sup> )
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.1 x 0.1 mm (4 x 4 mils)
Min pad space:	0.1 mm (3.8 mils)
Min metal 3 width:	1.4 micron
Min metal 3 space:	1.5 micron
Min metal 3 pitch:	2.9 microns
Min metal 2 width:	0.4 micron
Min metal 2 space:	0.4 micron
Min metal 2 pitch:	0.8 micron
Min metal 1 width:	0.4 micron
Min metal 1 space:	0.3 micron
Min metal 1 pitch:	0.7 micron
Min via (M3 - M2):	0.65 micron
Min via (M2 - M1):	0.4 micron
Min contact:	0.45 micron
Min poly 2 width:	0.35 micron
Min poly 2 space:	0.35 micron
Poly 1 width (trench):	0.25 micron
Min gate length* - (N-channel):	0.4 micron
- (P-channel):	0.45 micron
Cell size:	1.1 micron <sup>2</sup>
Cell pitch:	0.75 x 1.45 micron

*\*Physical gate length.*

## **VERTICAL DIMENSIONS**

### **Layers**

Passivation 2:	0.5 micron
Passivation 1:	0.45 micron
Metal 3 - cap:	0.07 micron (approx.)
- aluminum:	1.0 micron
- barrier:	0.07 micron (approx.)
Intermetal dielectric 2:	0.7 micron
Metal 2 - cap:	0.07 micron (approx.)
- aluminum:	0.35 micron
- barrier:	0.04 micron (approx.)
- plugs:	0.45 micron
Intermetal dielectric 1:	0.5 micron
Metal 1 - tungsten:	0.2 micron
- barrier:	0.04 micron (approx.)
- plugs:	0.7 - 0.9 micron
Pre-metal dielectric:	0.4 - 0.85 micron
Poly 3:	0.4 micron
Oxide on poly 2:	0.25 micron
Poly 2 - silicide:	0.06 micron (approx.)
- poly:	0.1 micron
Poly 1 - (trench):	6.8 microns
Shallow trench oxide (isolation):	0.4 micron
N+ S/D diffusion:	0.15 micron
P+ S/D diffusion:	0.15 micron
P- well:	1.5 micron
N- epi:	2 microns

## **INDEX TO FIGURES**

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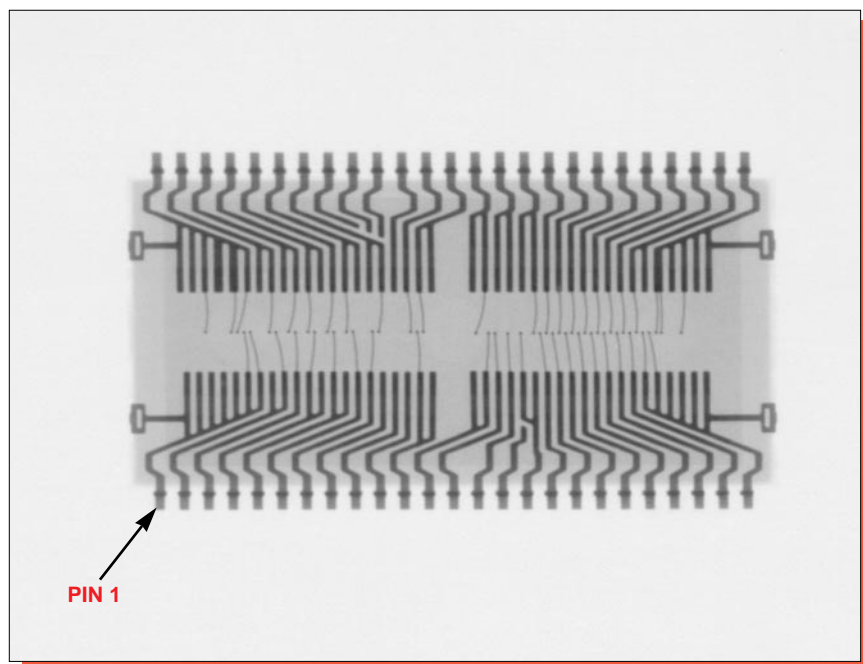
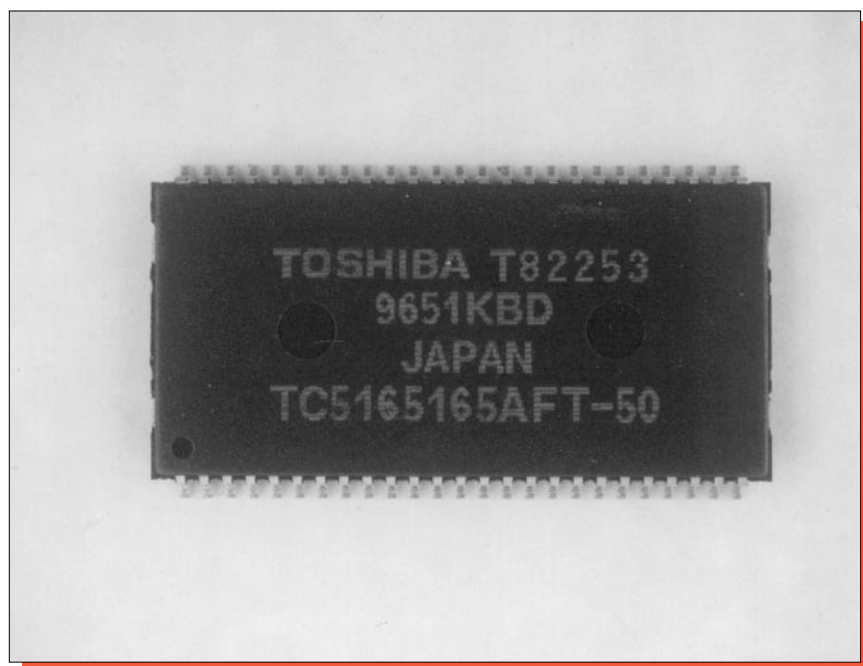
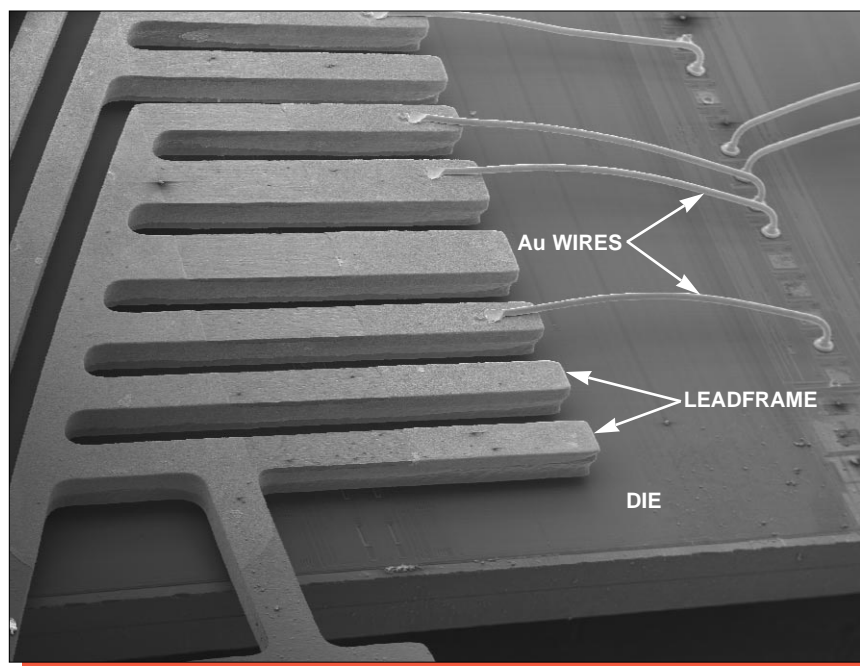
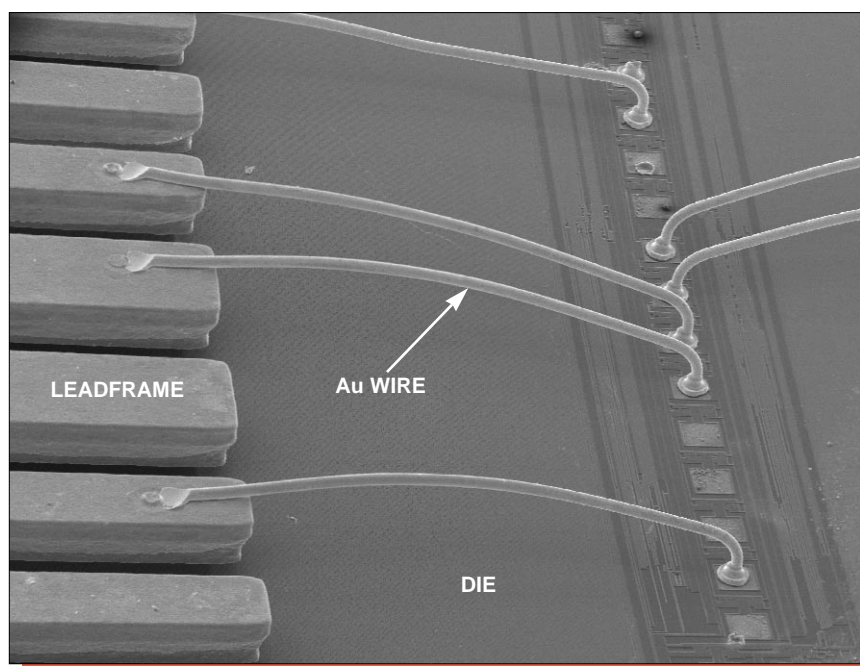


Figure 1. Package photograph and x-ray view of the Toshiba TC5165165AFT-50 64M DRAM. Mag 4x.



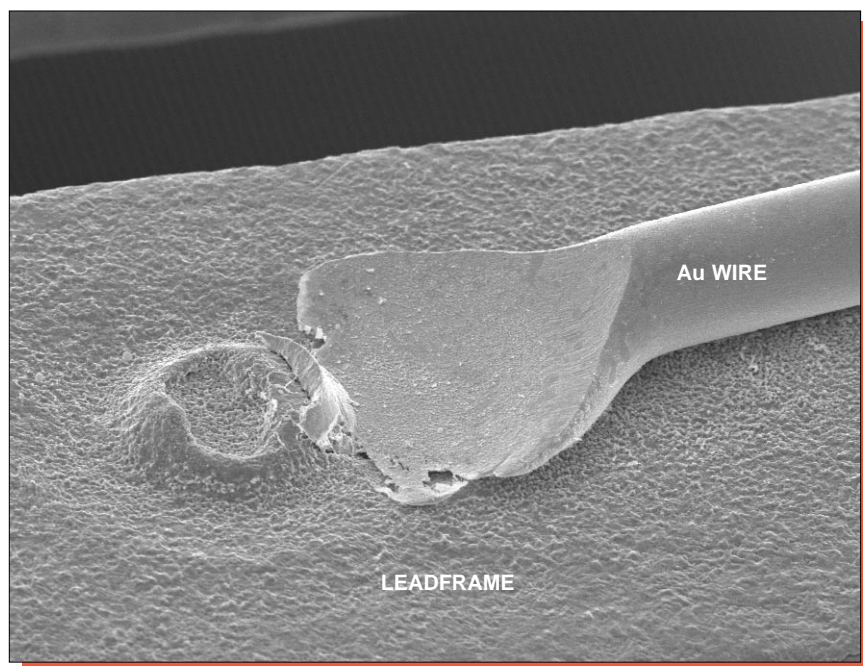
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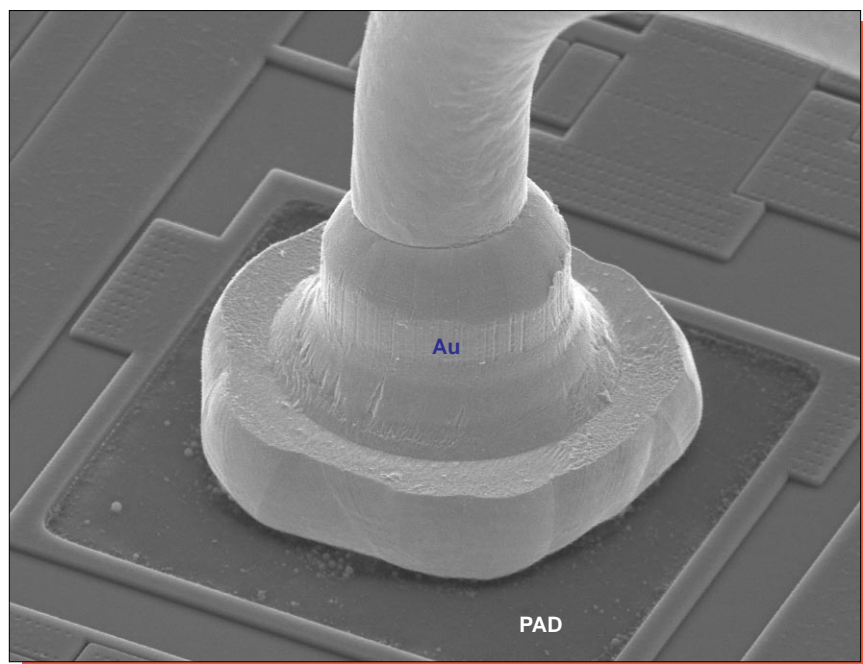
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Figure 2. Perspective SEM views illustrating assembly structure. 60°.



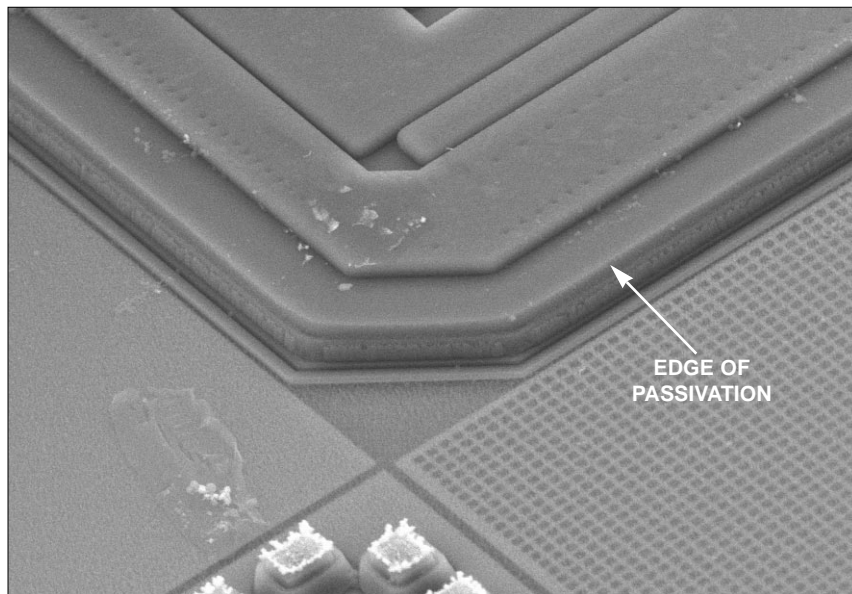


Mag. 600x

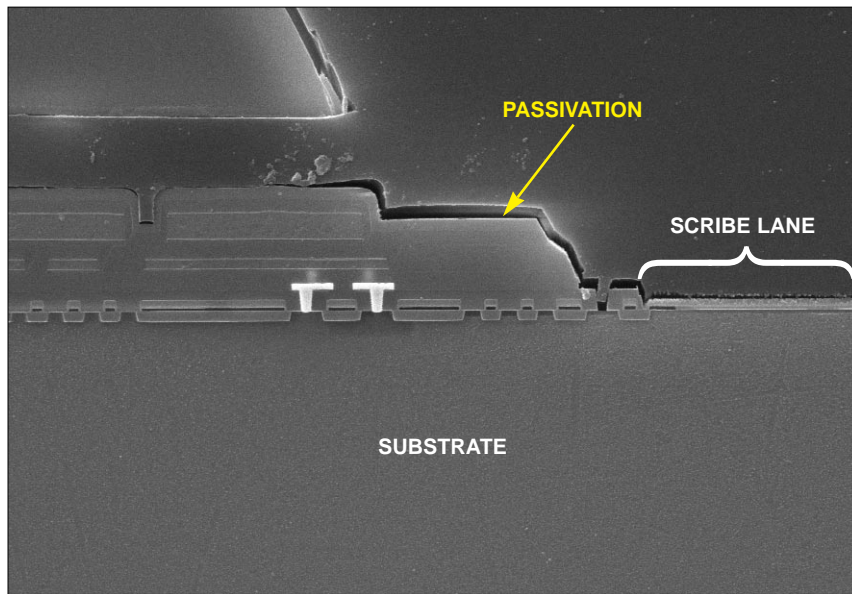


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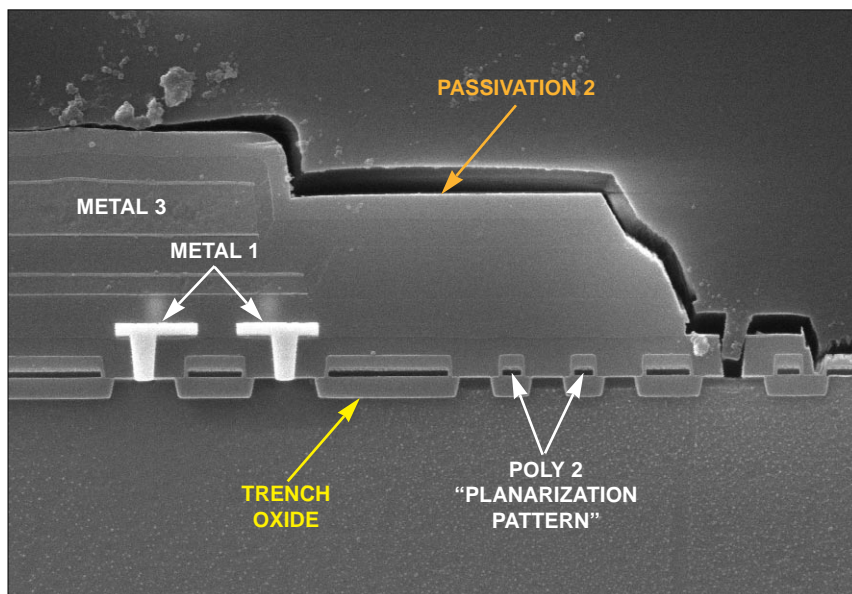
Figure 3. SEM views of typical wirebonds. 60°.



Mag. 1400x, 60°



Mag. 3200x



Mag. 6500x

Figure 4. SEM views of the edge seal structure.

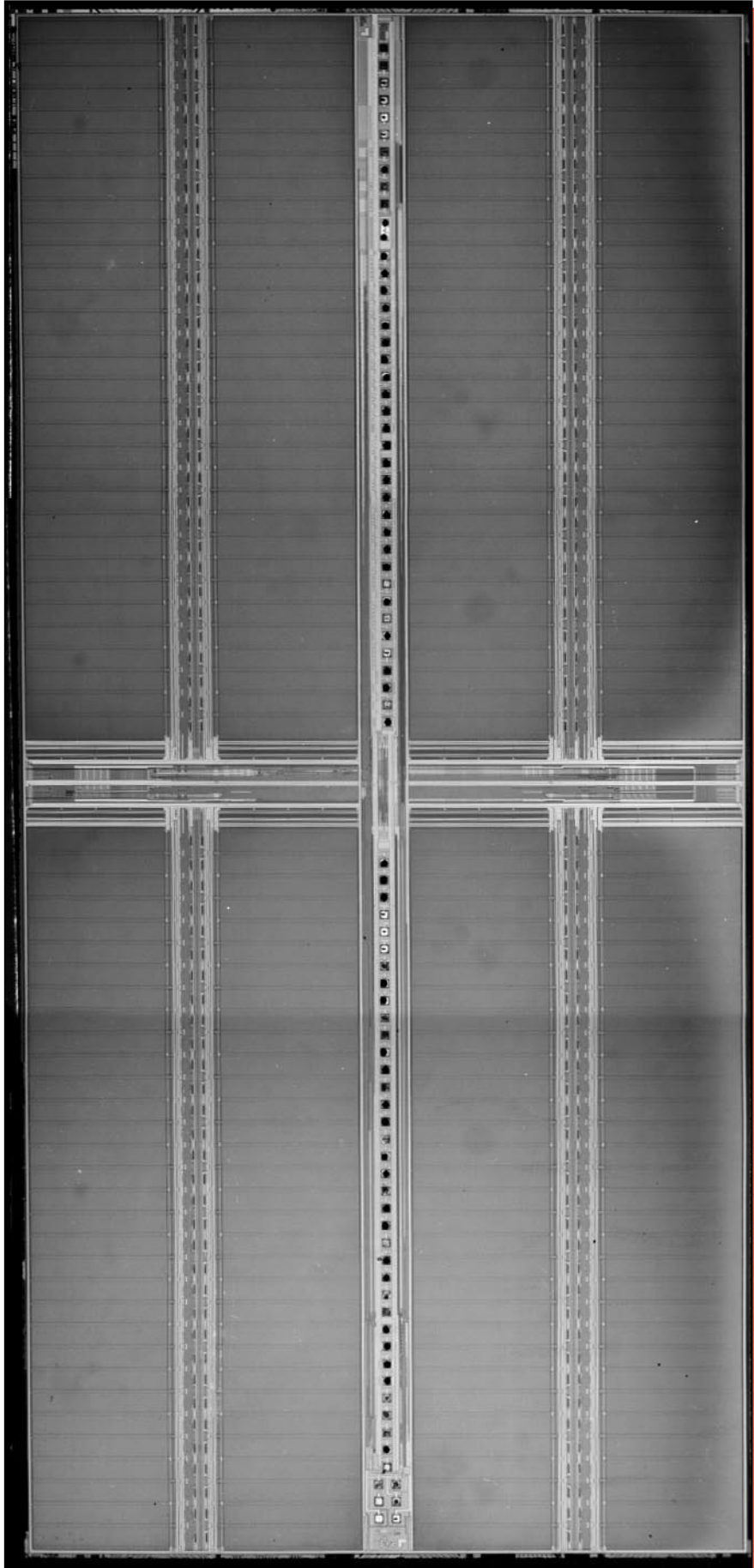
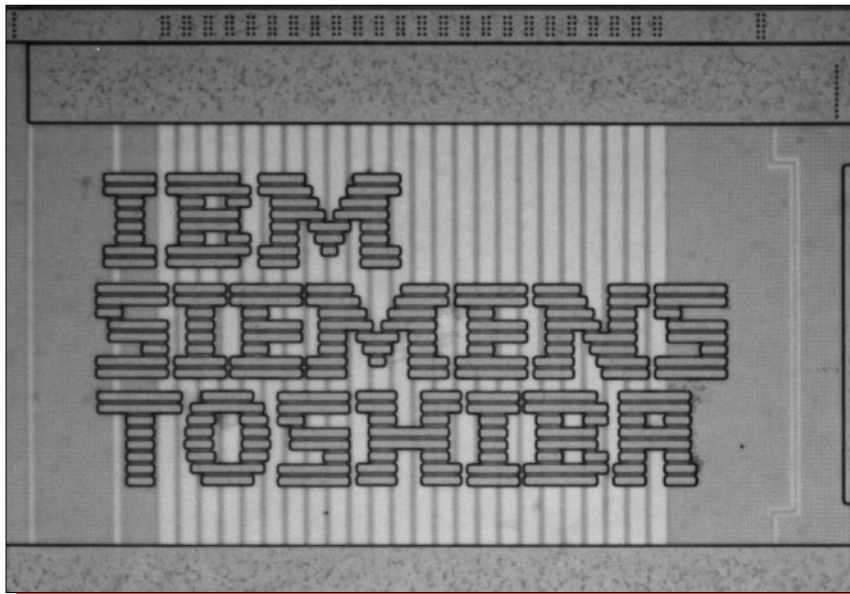
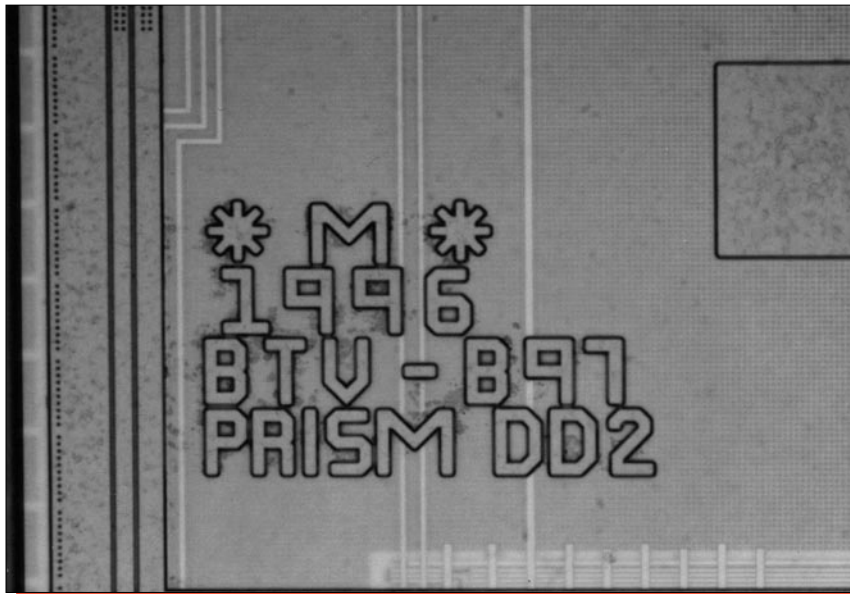


Figure 5. Whole die photograph of the Toshiba TC5165165AFT-50 64M DRAM. Mag. 13x.

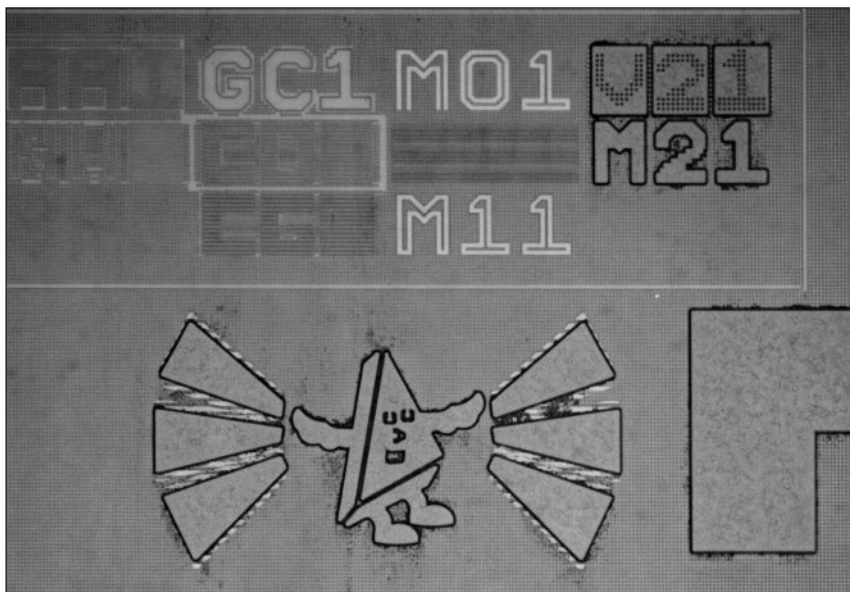




Mag. 500x

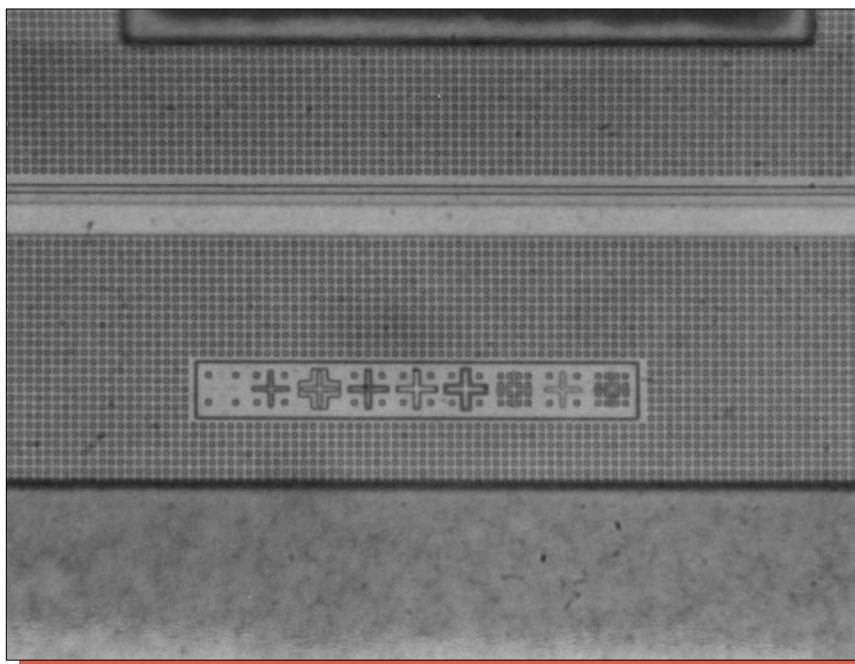


Mag. 400x

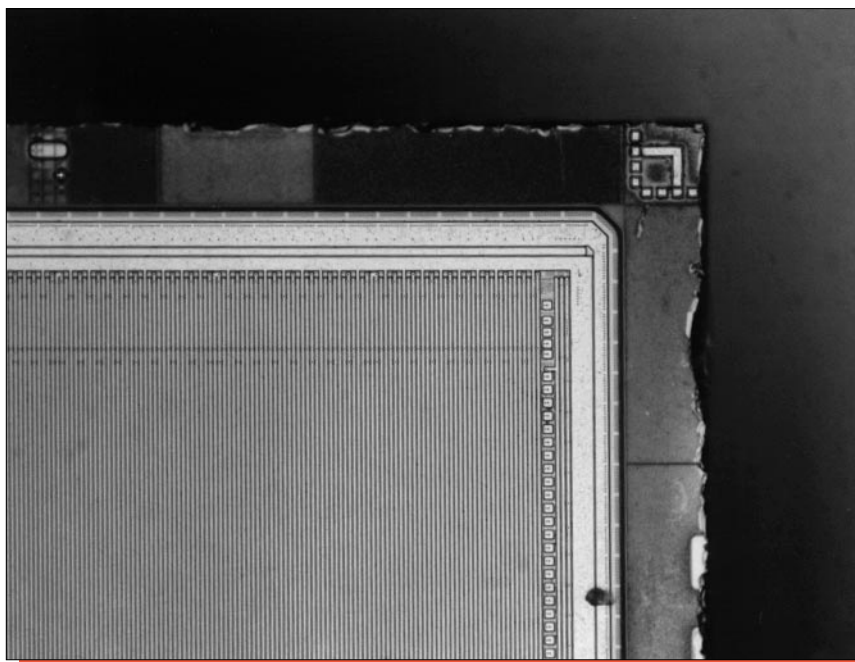


Mag. 320x

Figure 6. Die identification markings.

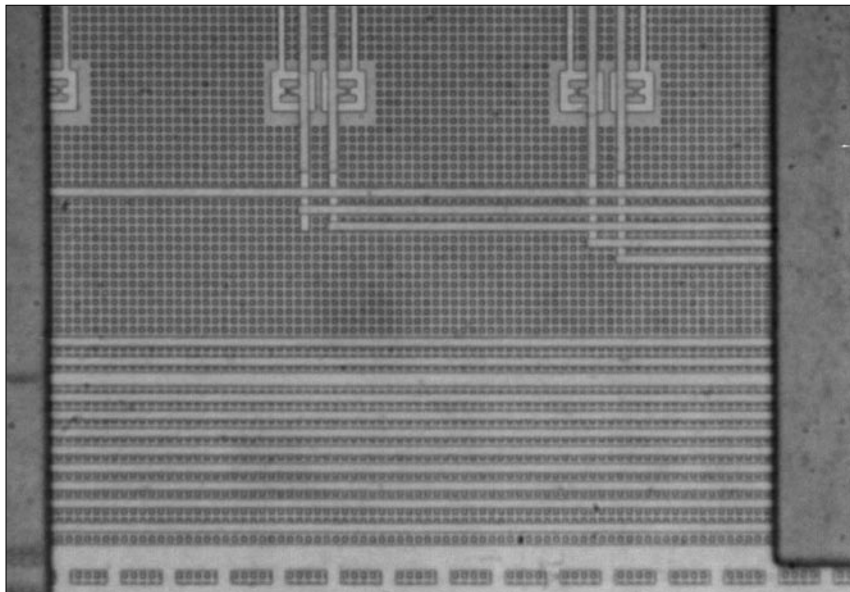


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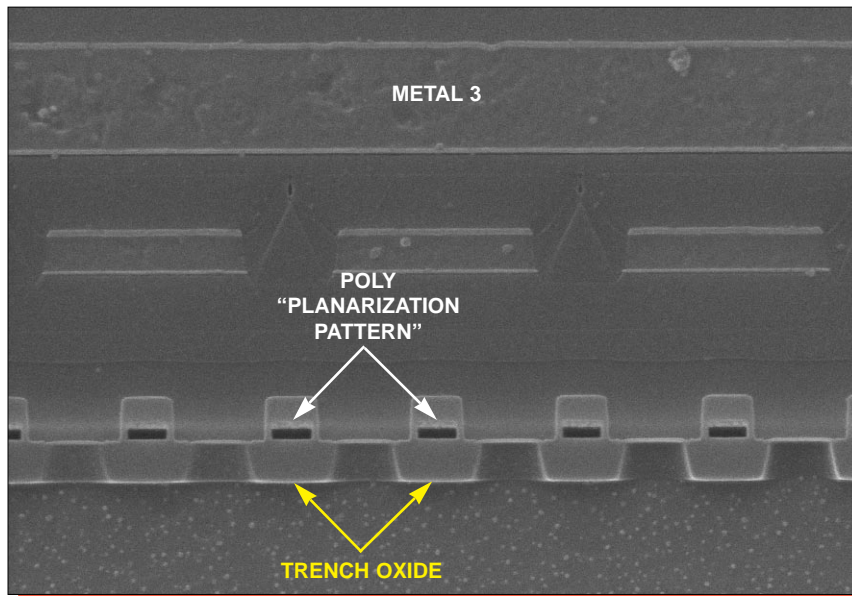


Mag. 200x

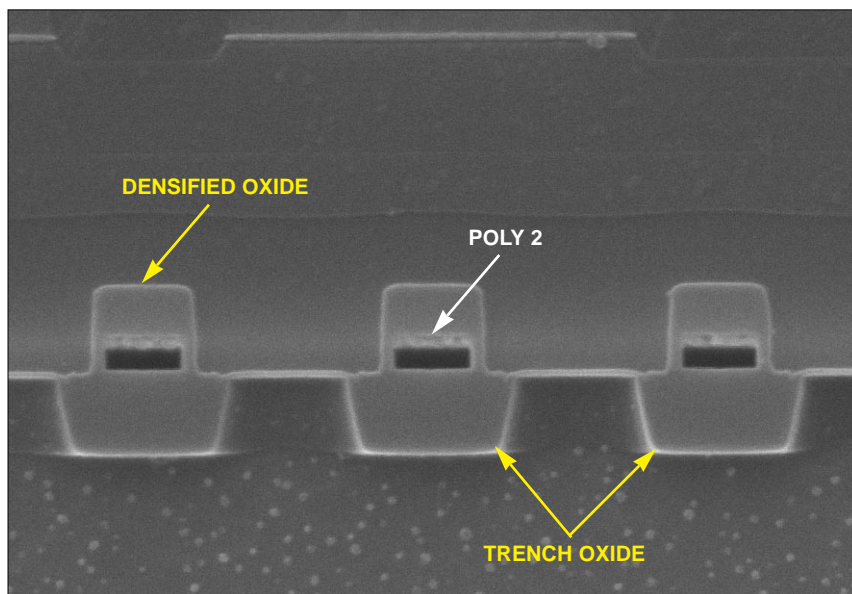
Figure 6a. Alignment keys from the die surface and typical die corner structure.



Mag. 800x



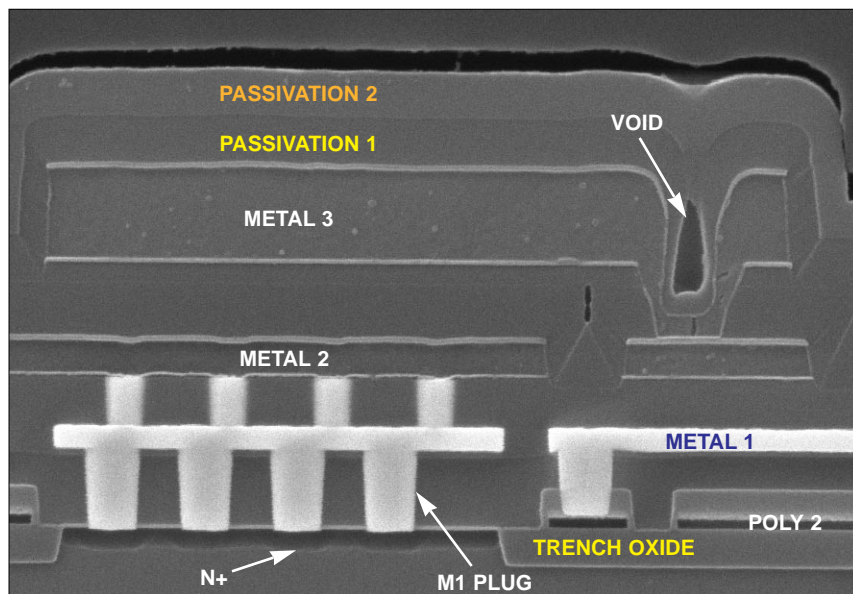
Mag. 13,000x



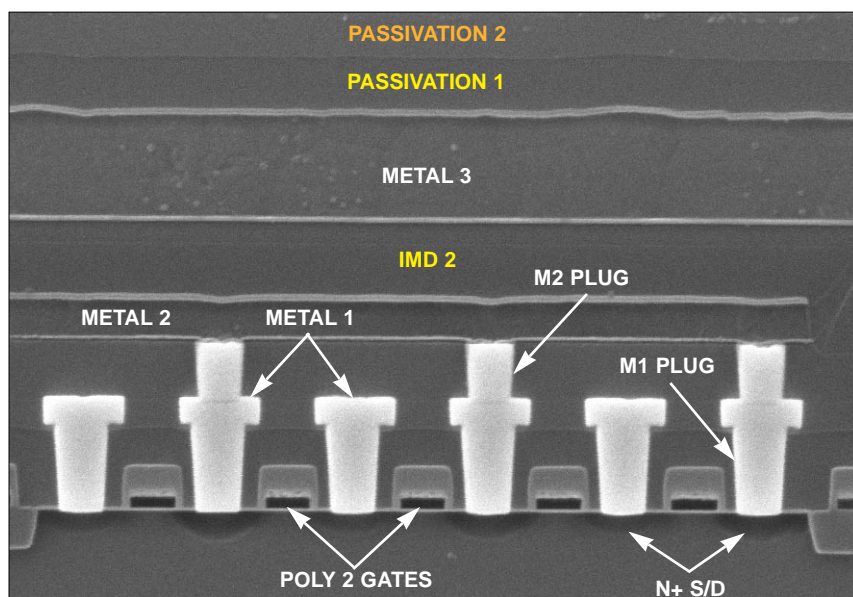
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Figure 7. Optical and SEM section views illustrating planarization pattern.

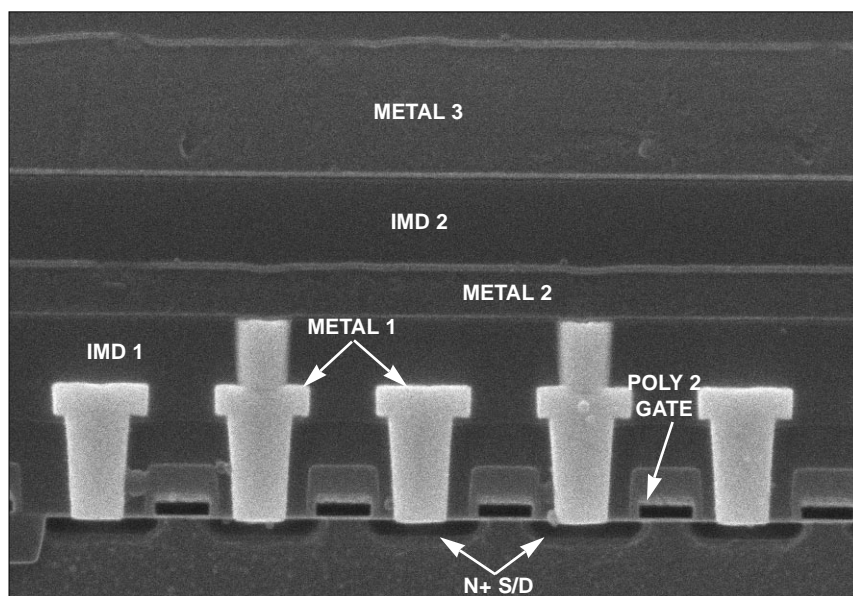




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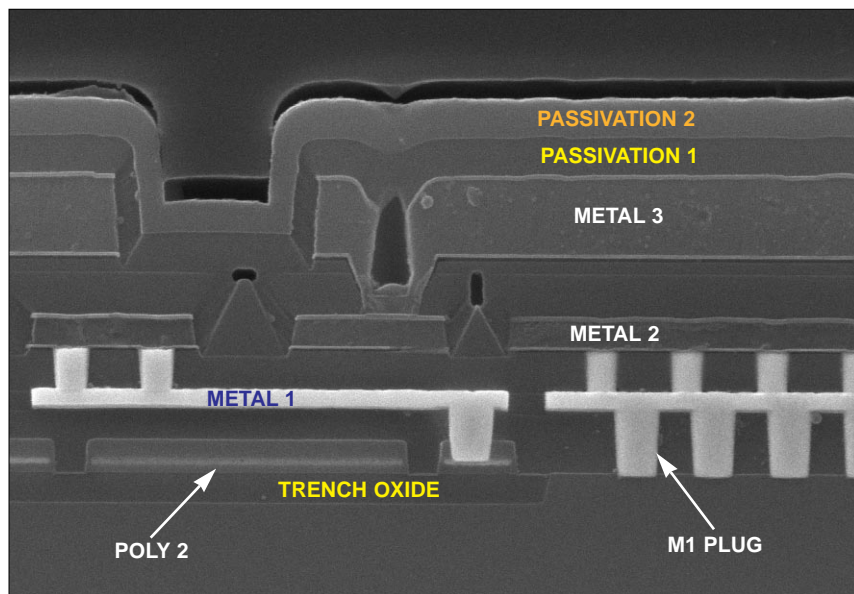


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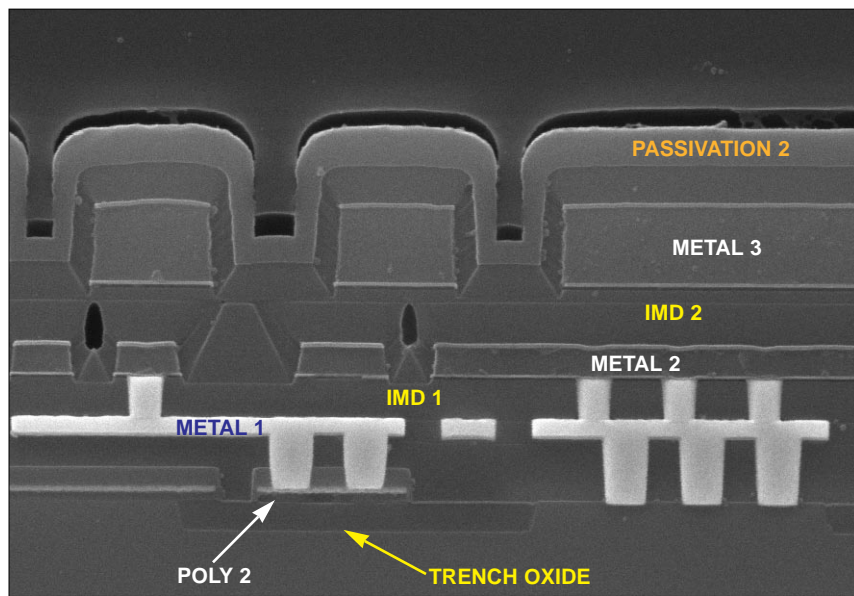


Mag. 16,000x

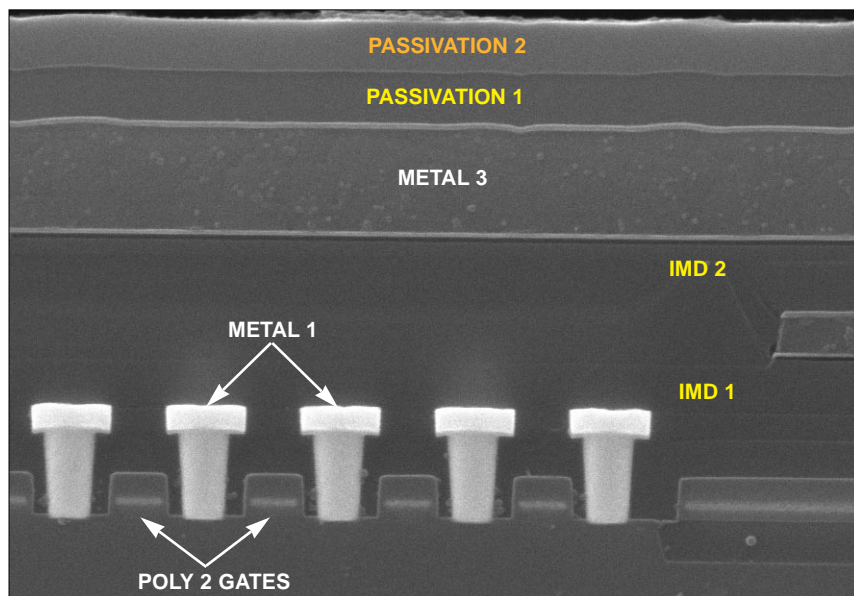
Figure 8. Silicon etch section views illustrating general device structure.



Mag. 10,000x



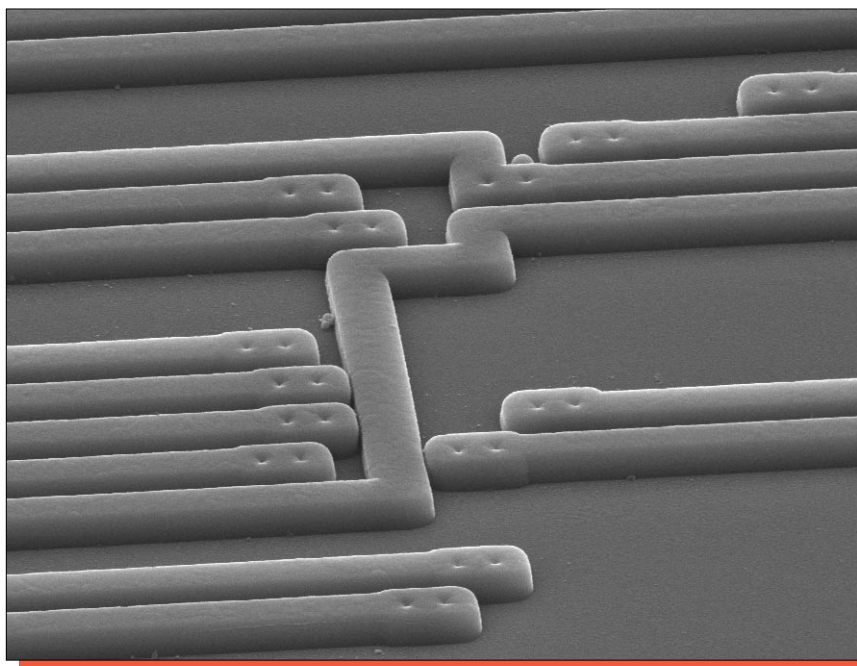
Mag. 10,000x



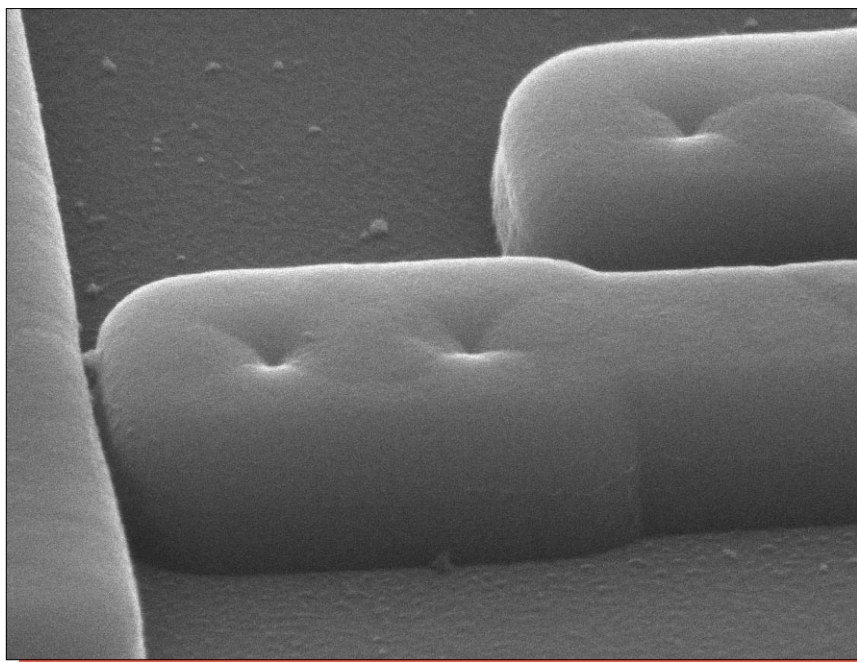
Mag. 13,000x

Figure 9. Glass etch section views illustrating general device structure.



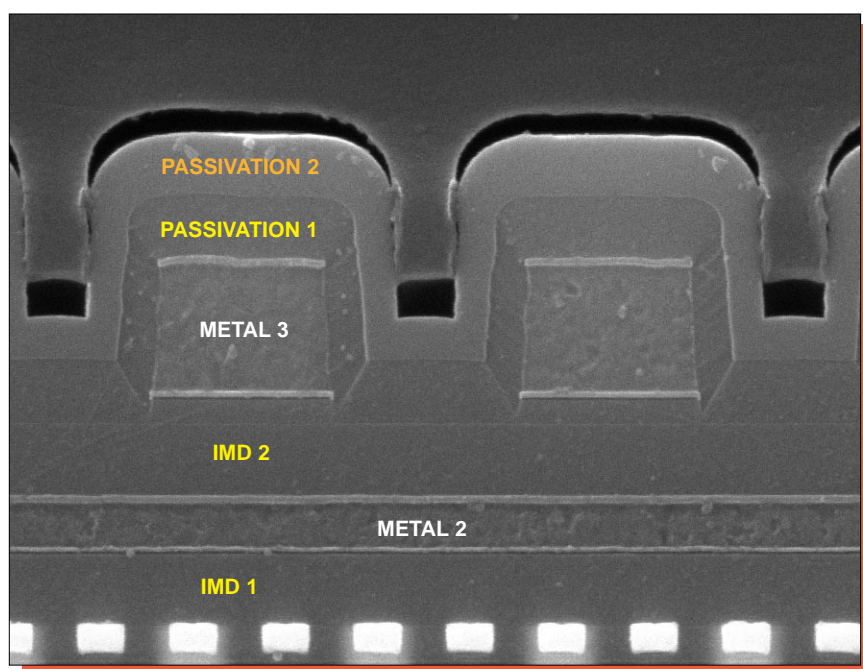


Mag. 3000x

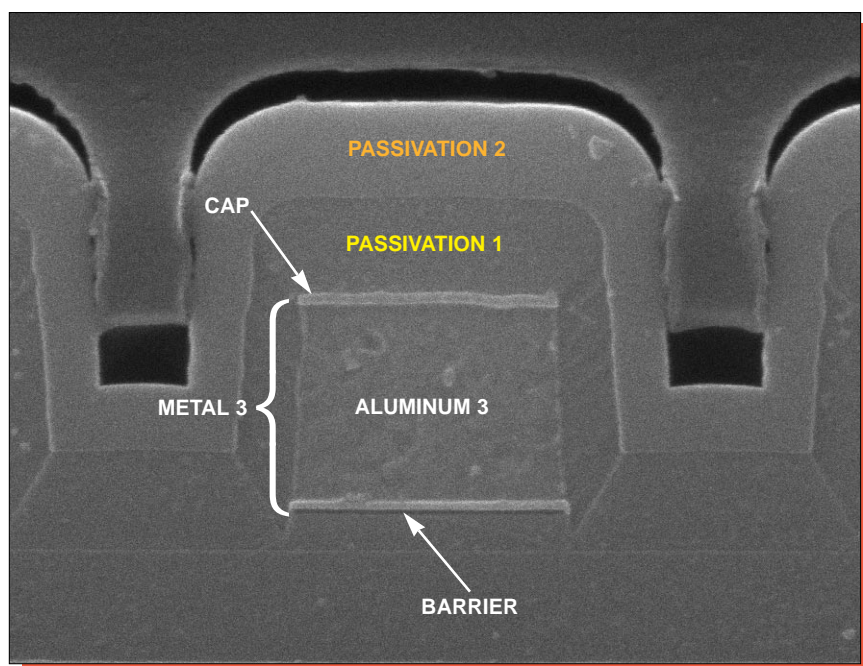


Mag. 15,000x

Figure 10. SEM views of general passivation coverage. 55°.

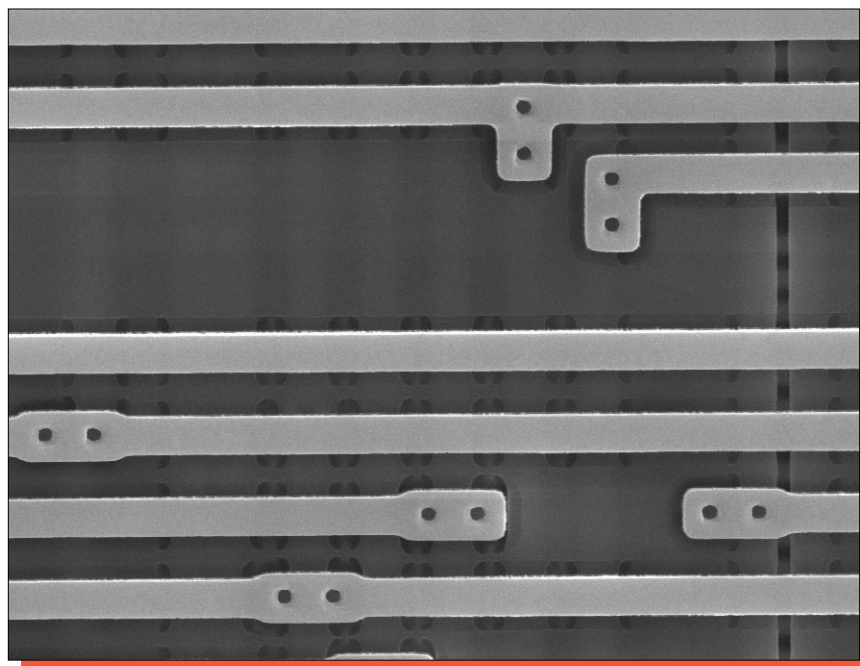


Mag. 17,000x

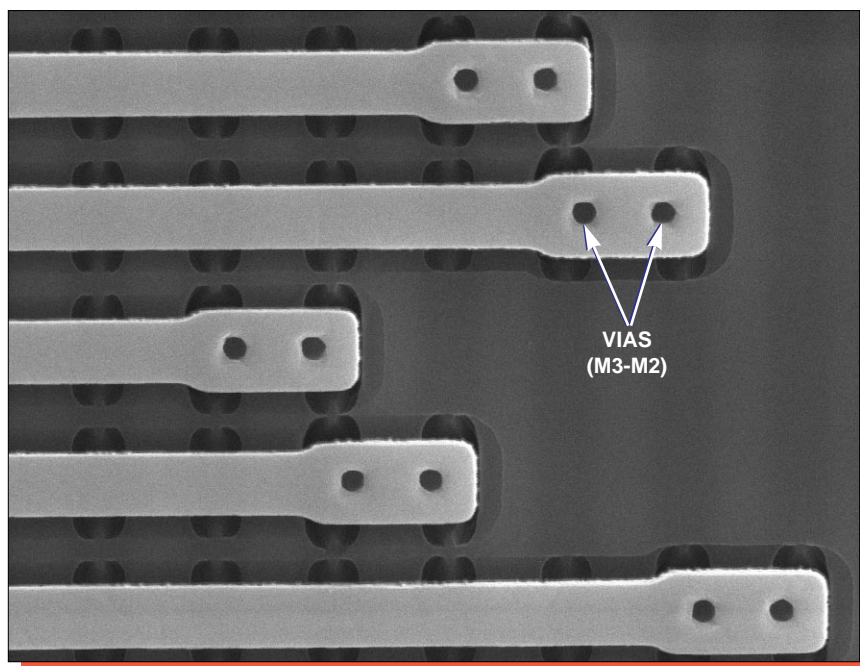


Mag. 26,000x

Figure 11. SEM section views of metal 3 line profiles.



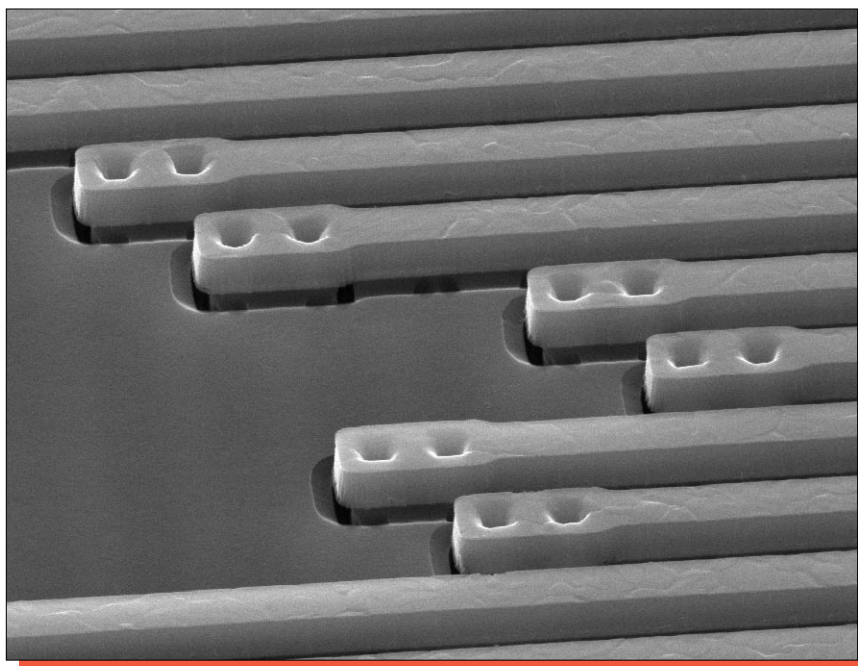
Mag. 3700x



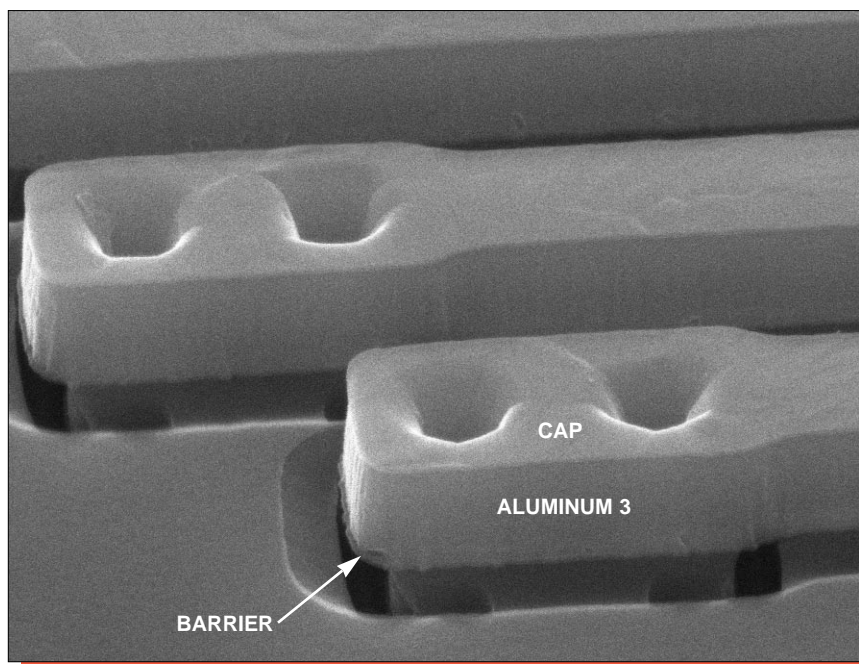
Mag. 6000x

Figure 12. Topological SEM views illustrating metal 3 patterning. 0°.



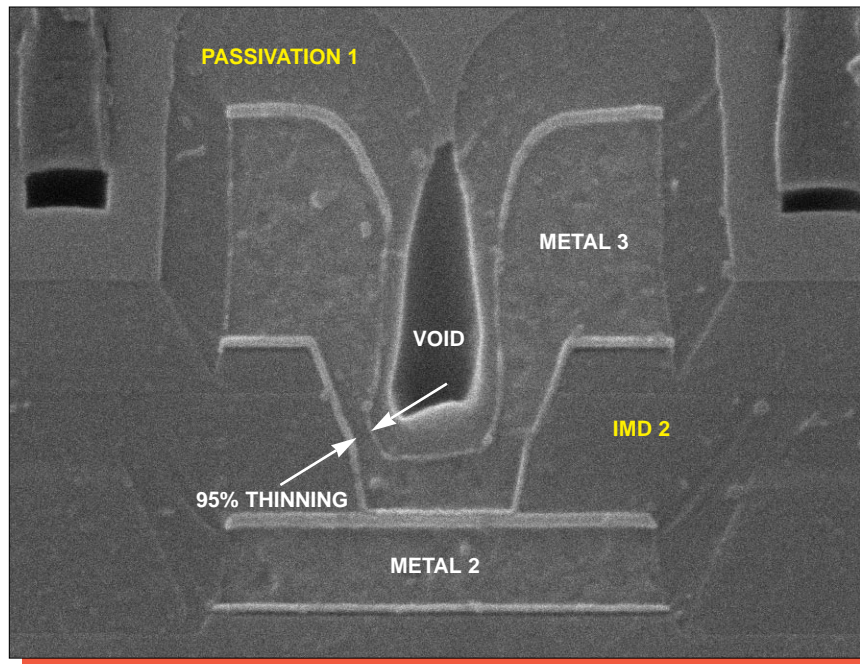


Mag. 5500x

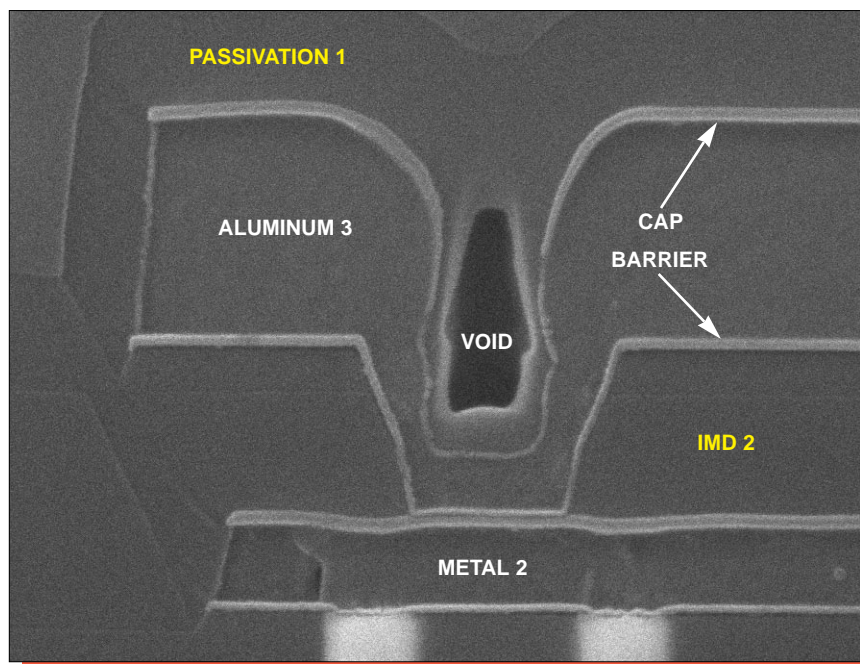


Mag. 15,000x

Figure 13. SEM views of general metal 3 integrity. 55°.



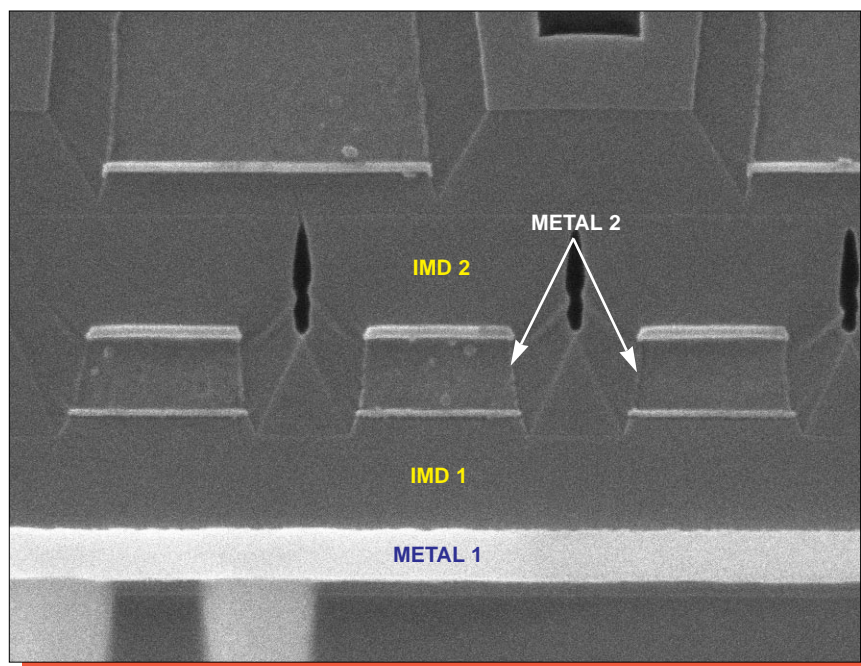
Mag. 30,000x



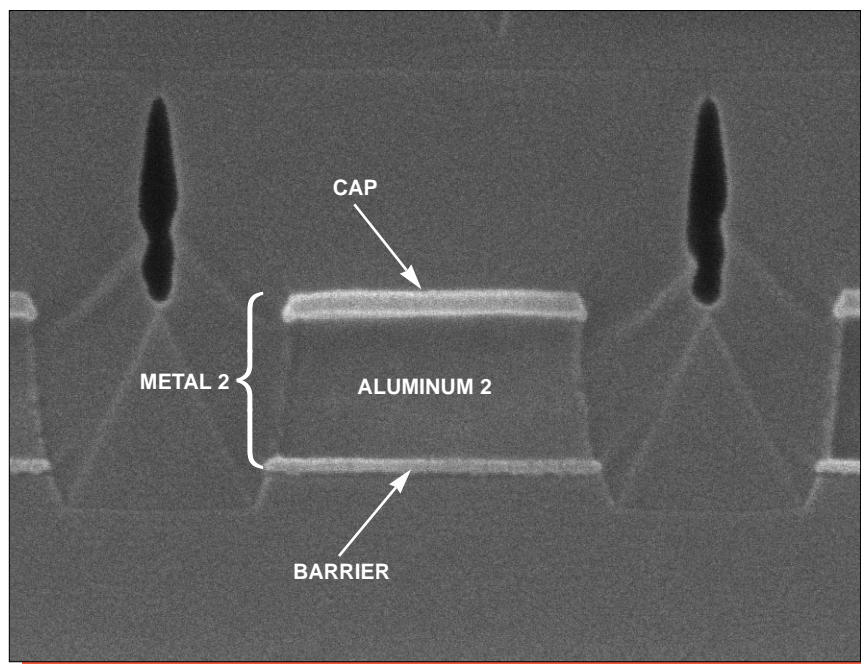
Mag. 32,000x

Figure 14. SEM section views of M3-to-M2 vias.





Mag. 26,000x



Mag. 52,000x

Figure 15. SEM section views of metal 2 line profiles.

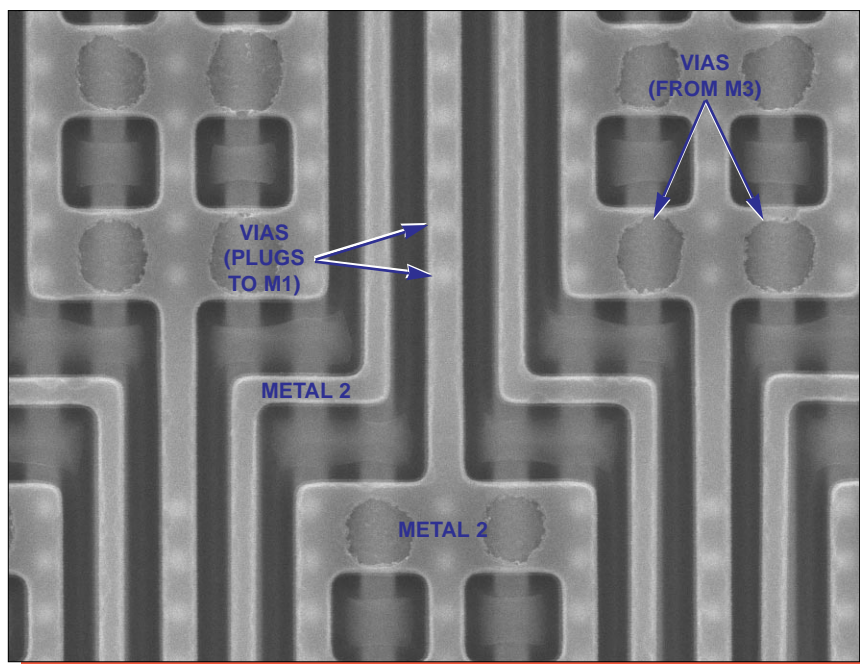
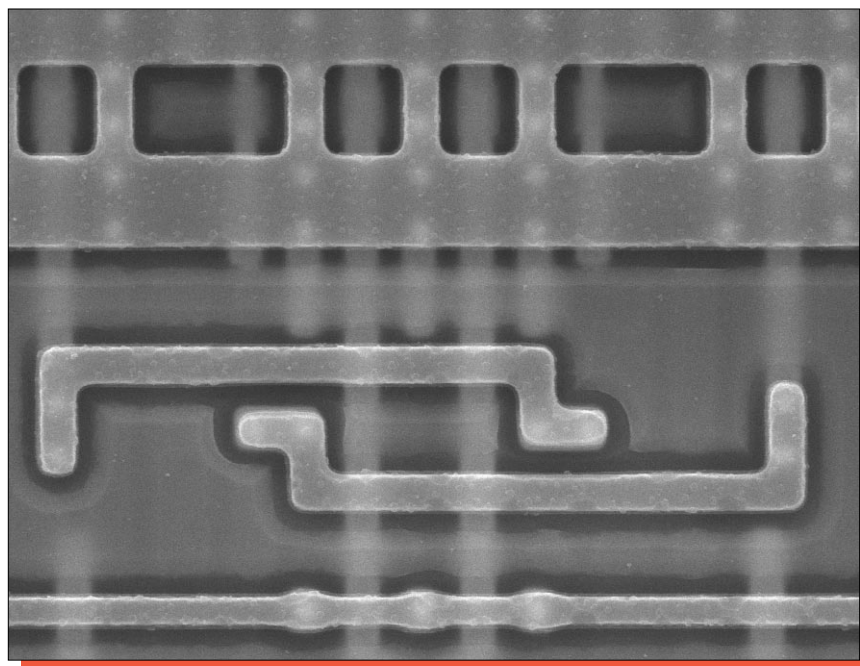
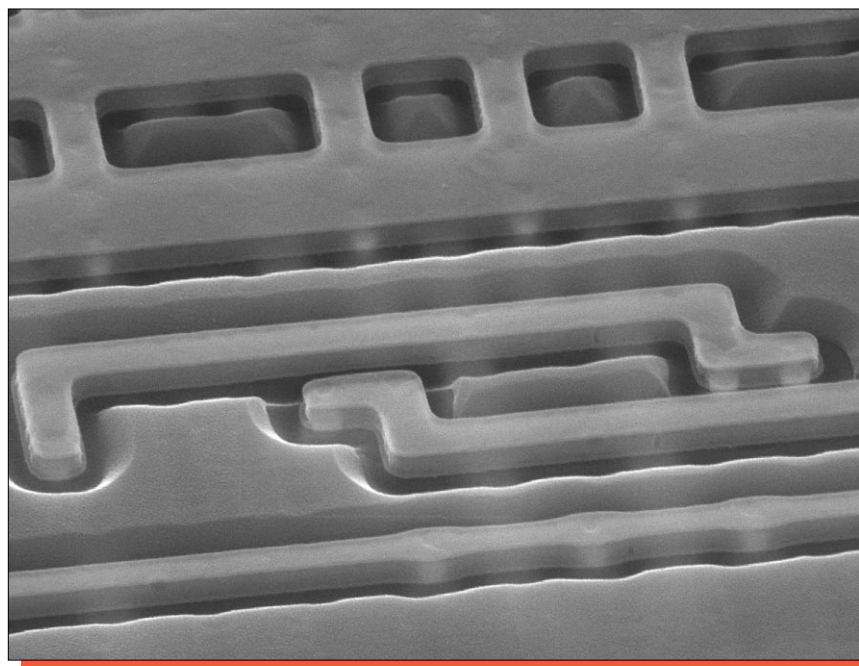
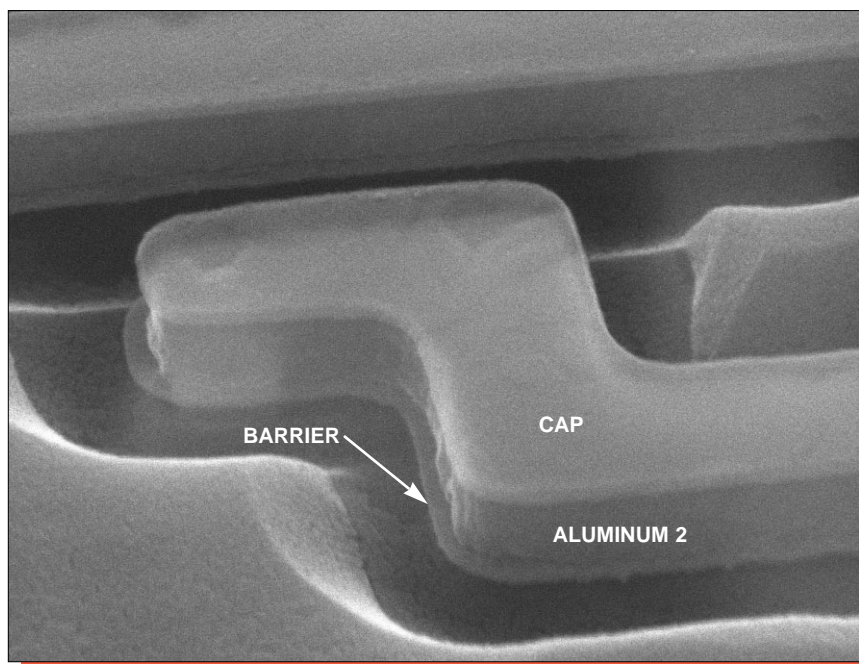


Figure 16. Topological SEM views illustrating metal 2 patterning. Mag. 6000x, 0°.



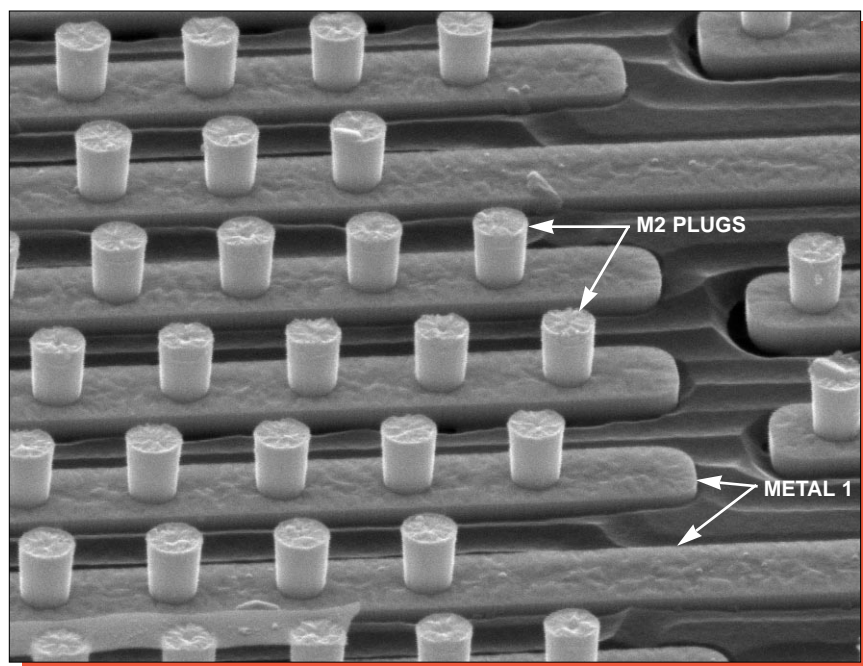
Mag. 8000x



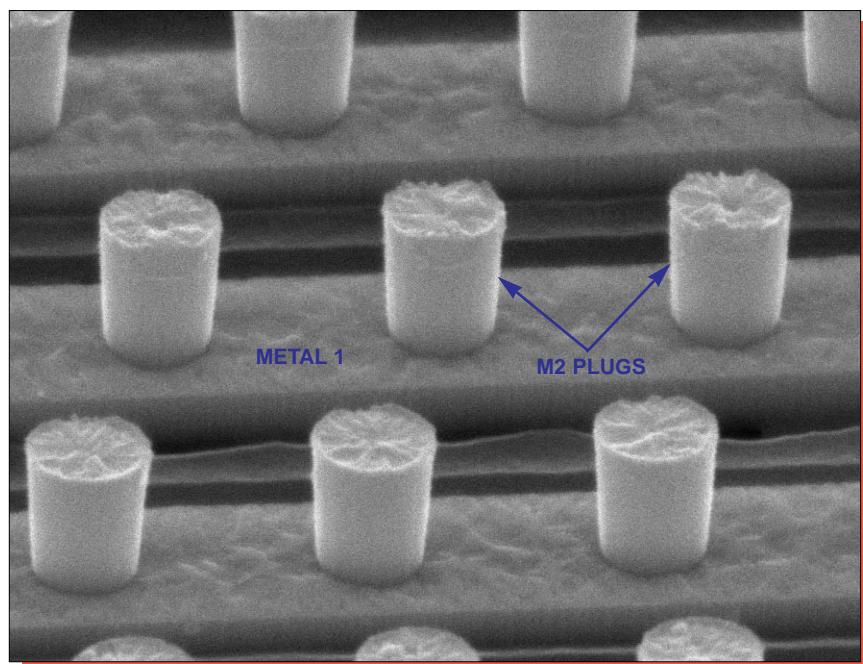
Mag. 30,000x

Figure 17. Perspective SEM views of general metal 2 integrity. 50°.



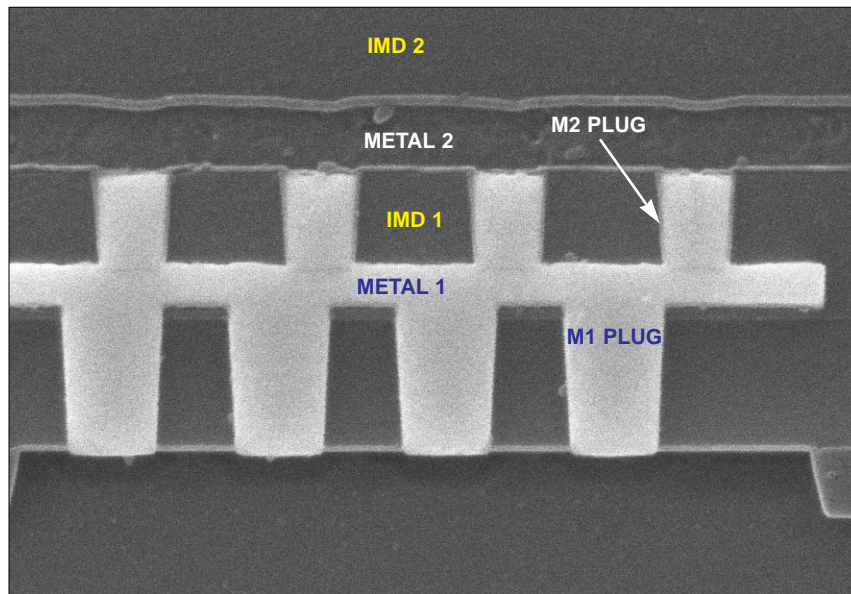


Mag. 15,400x

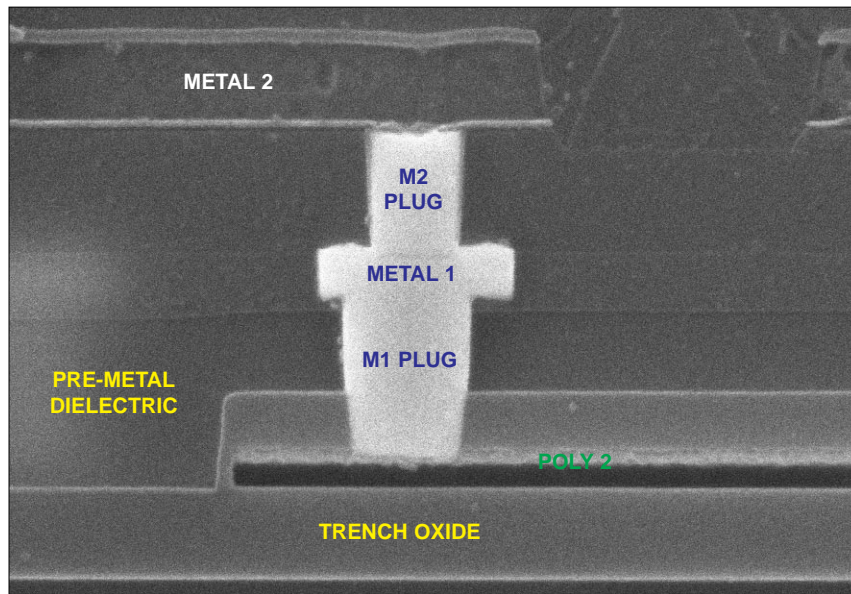


Mag. 35,000x

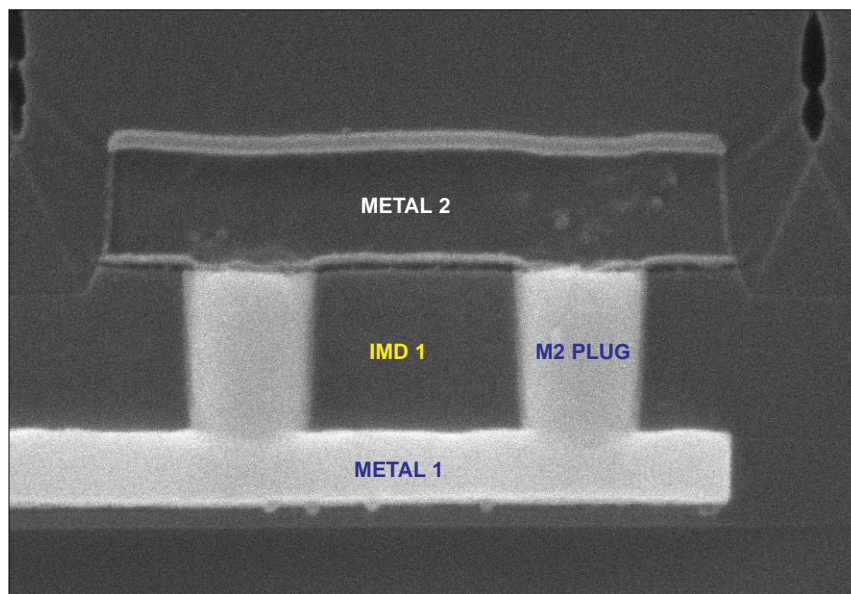
Figure 18. SEM views of metal 2 tungsten plugs. 55°.



Mag. 25,000x



Mag. 30,000x



Mag. 40,000x

Figure 19. SEM section views of M2-to-M1 vias.



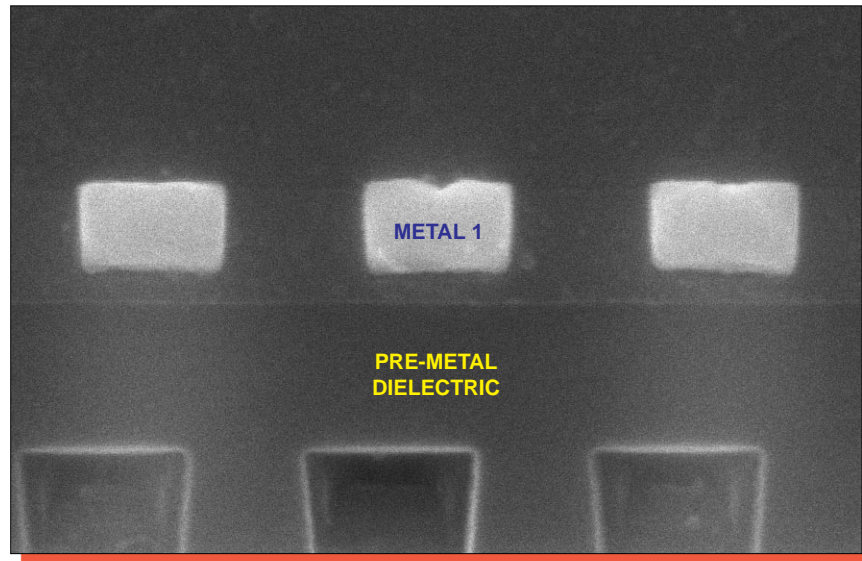


Figure 20. SEM section view of metal 1 line profiles. Mag. 52,000x.

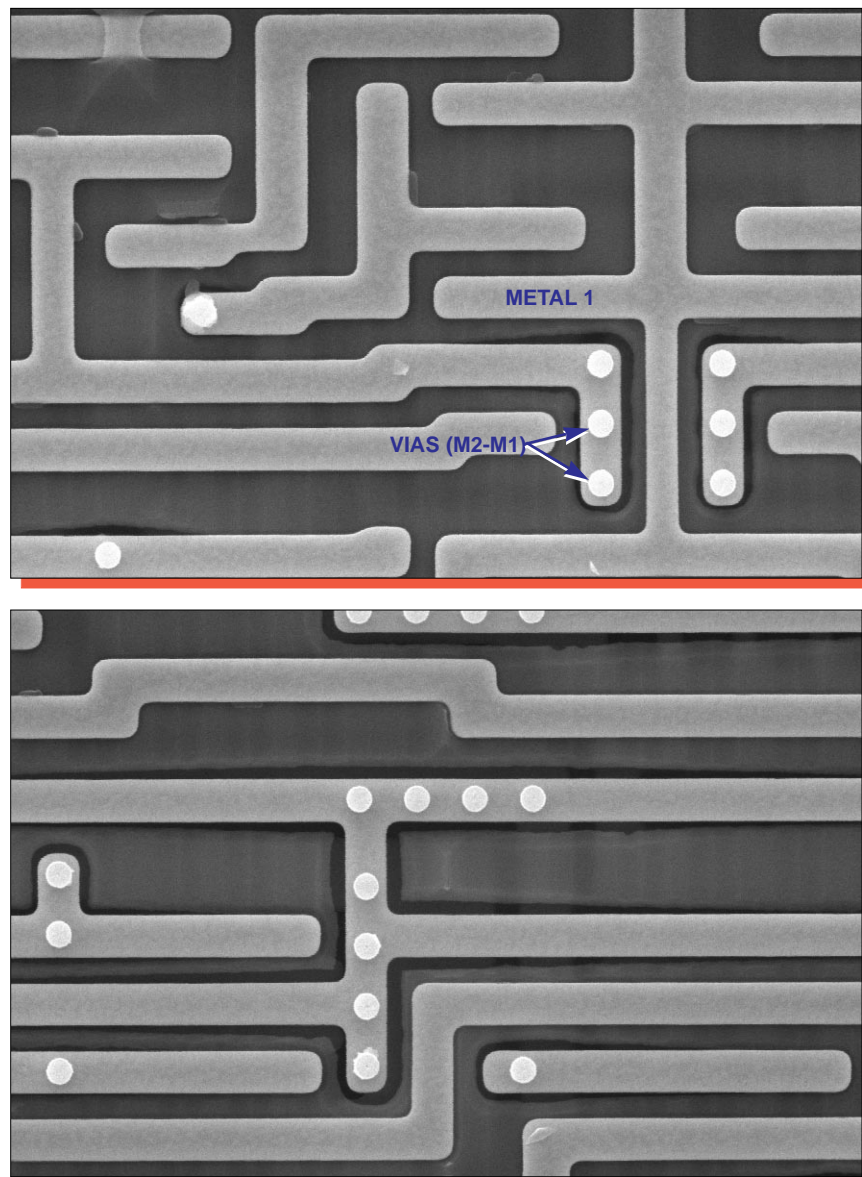
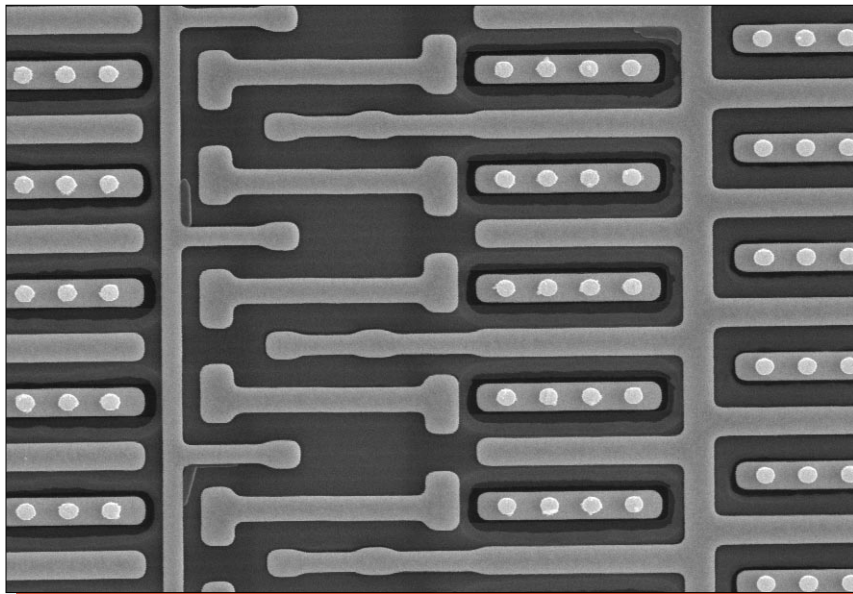
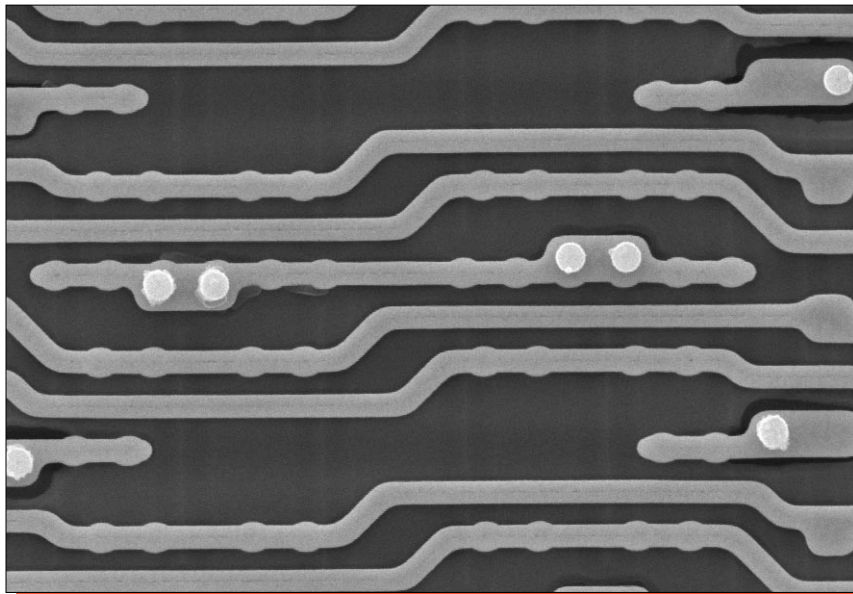


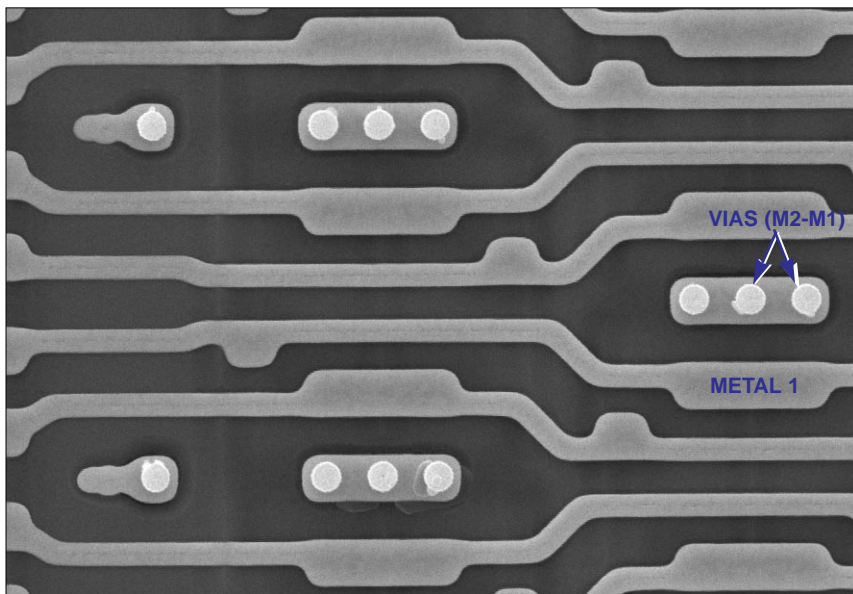
Figure 21. Topological SEM views illustrating metal 1 patterning. Mag. 7000x, 0°.



Row Decode,  
Mag. 5000x



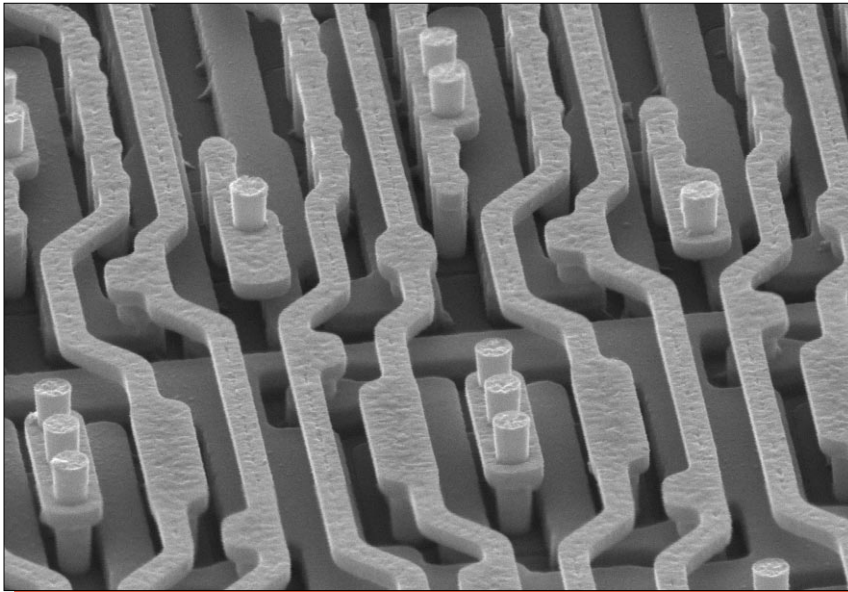
Column Decode,  
Mag. 8000x



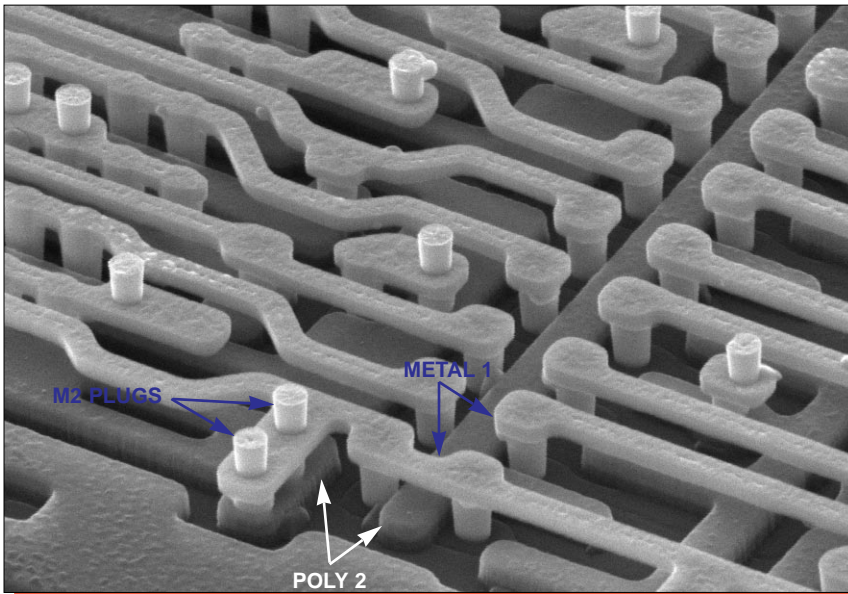
Column Decode,  
Mag. 8000x

Figure 22. Topological SEM views illustrating metal 1 patterning in the decode areas. 0°.

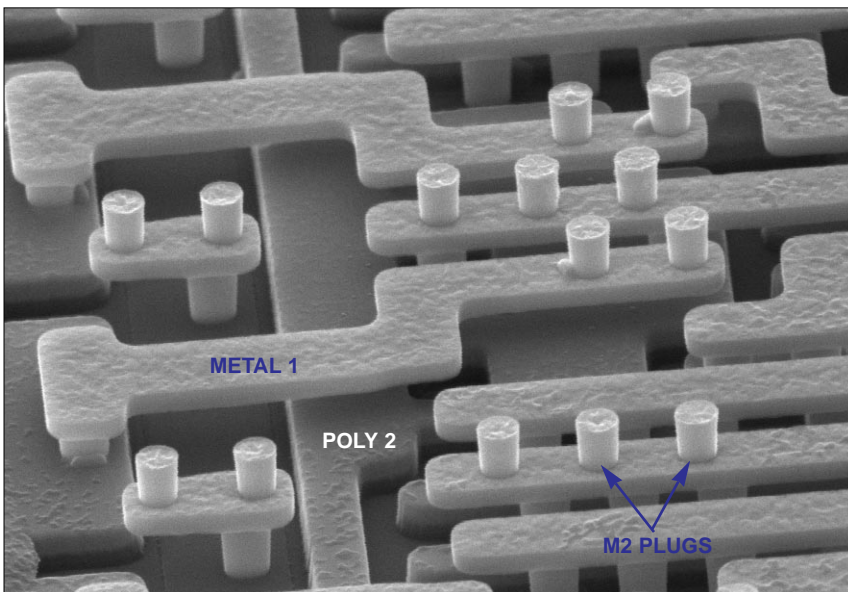




Mag. 10,000x

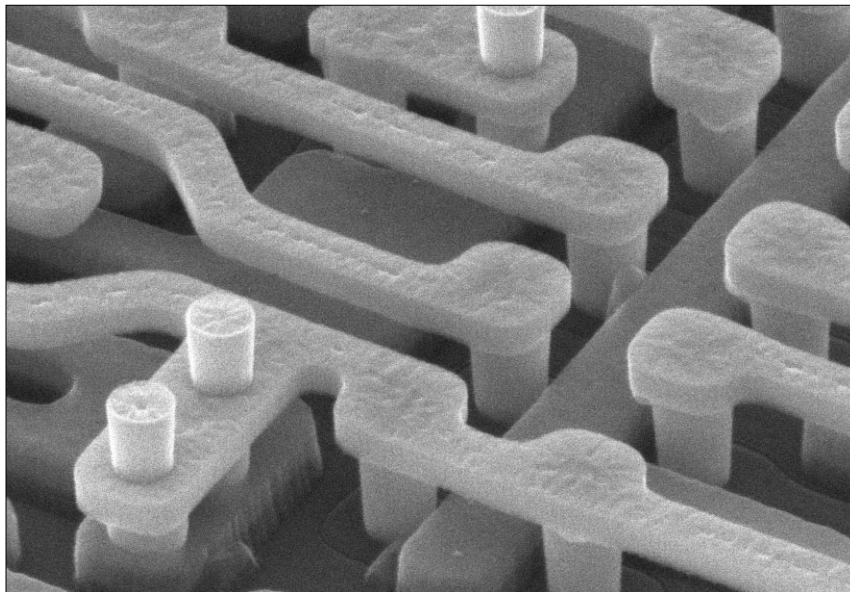


Mag. 10,000x

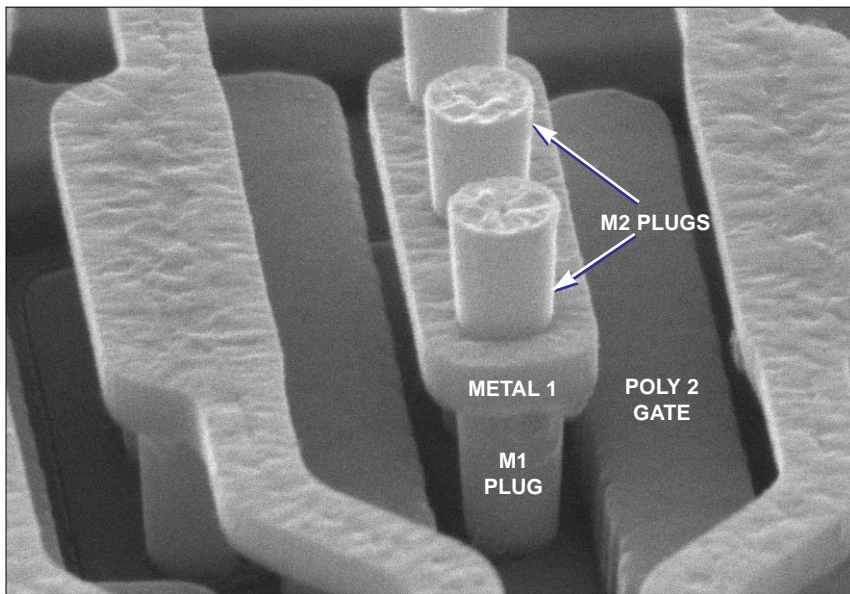


Mag. 12,000x

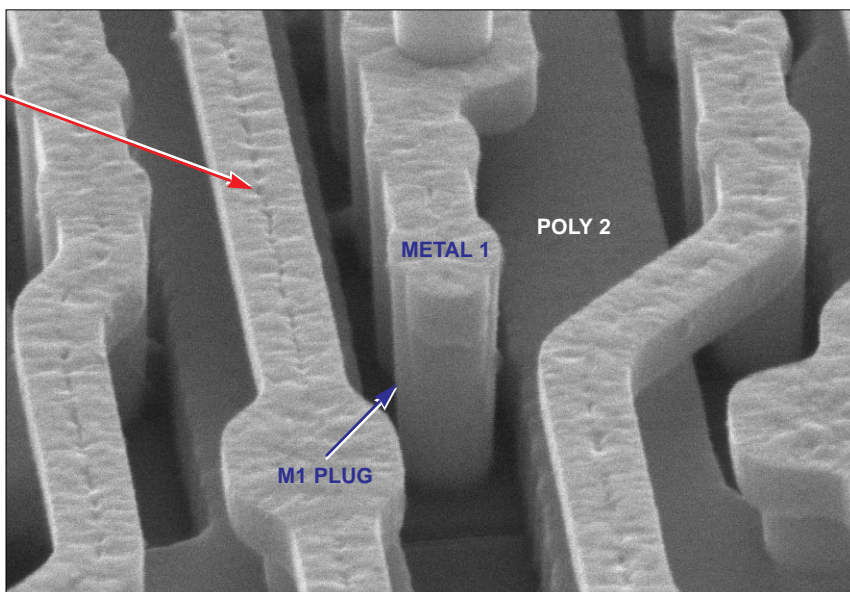
Figure 23. Perspective SEM views illustrating general metal 1 integrity. 60°.



Mag. 20,000x



Mag. 30,000x

EVIDENCE OF  
DAMASCENE  
METAL 1

Mag. 30,000x

Figure 24. Detail SEM views of general metal 1 integrity. 60°.



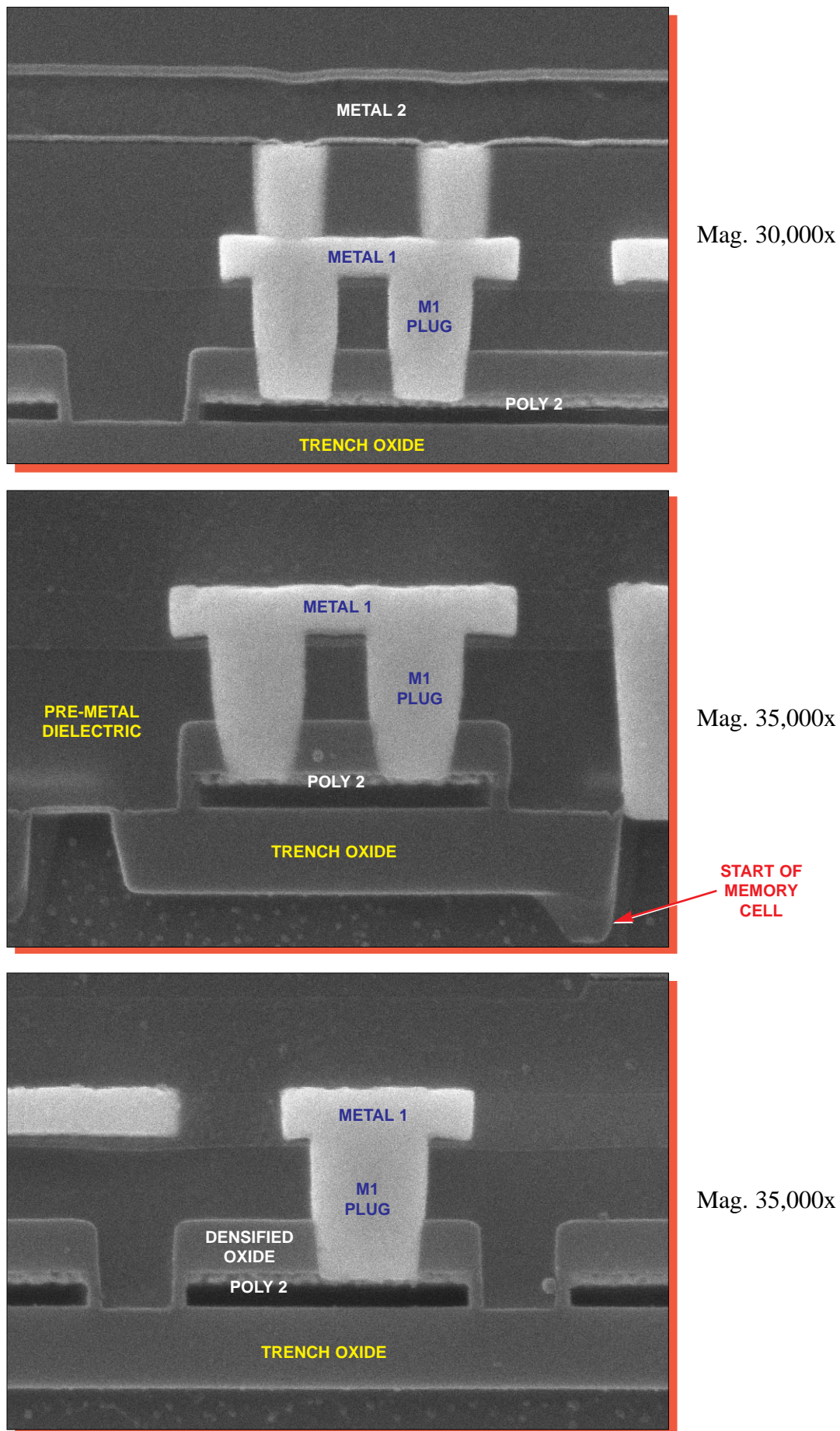
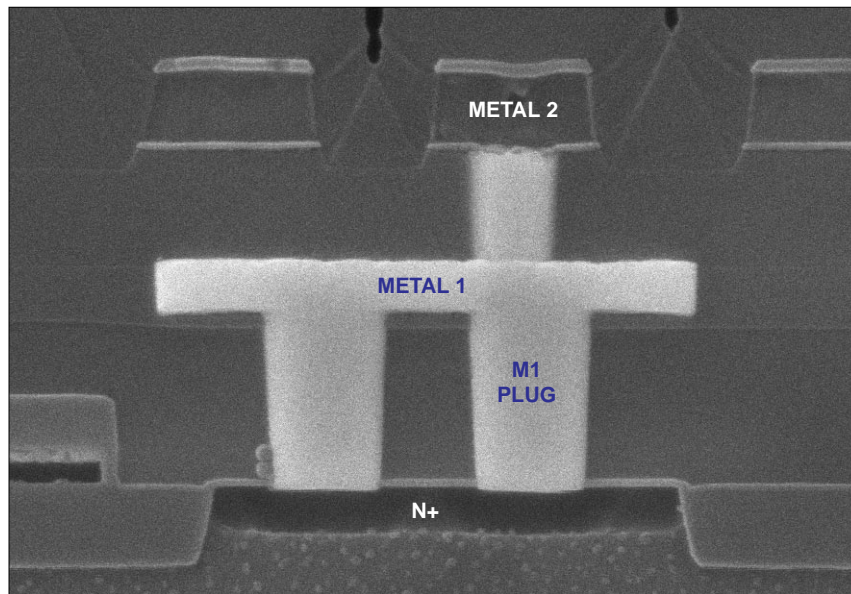
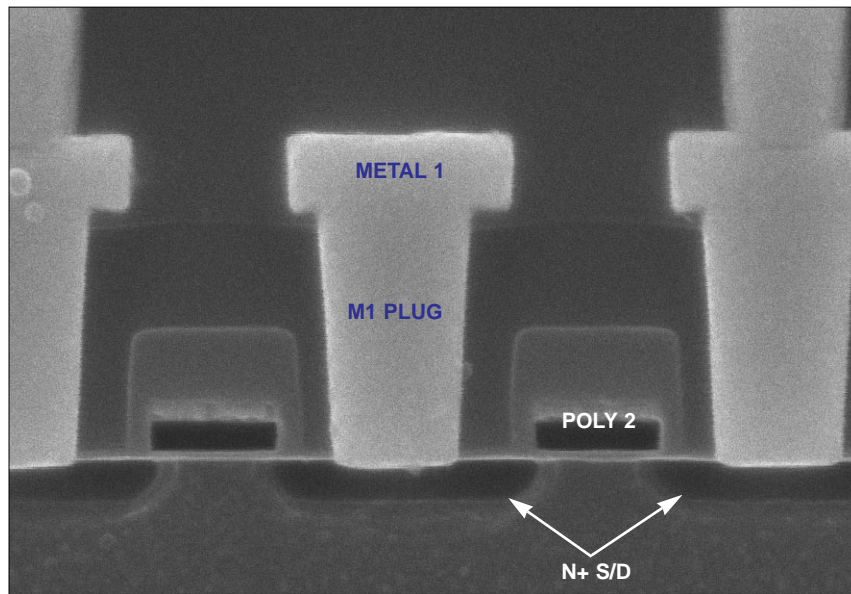


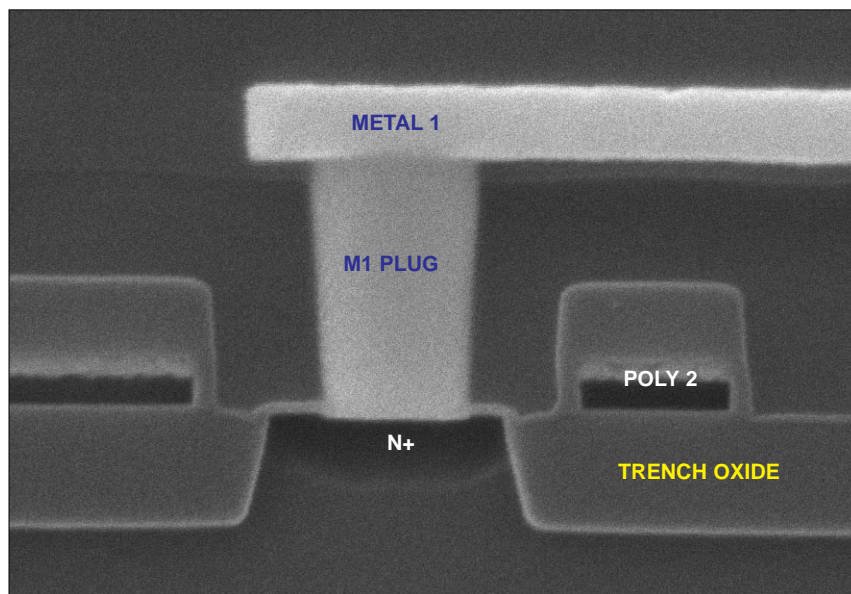
Figure 25. SEM section views of metal 1-to-poly 2 contacts.



Mag. 26,000x



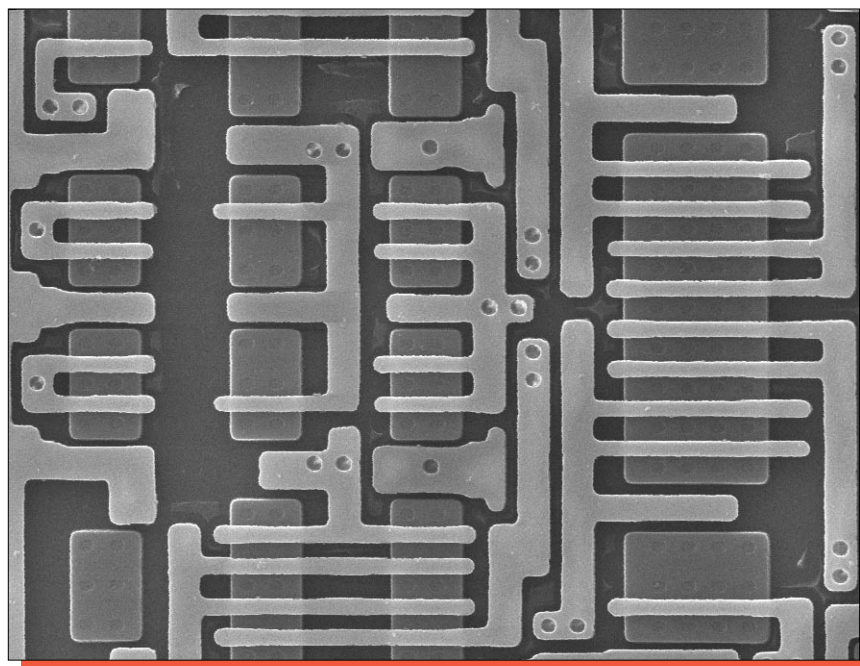
Mag. 40,000x



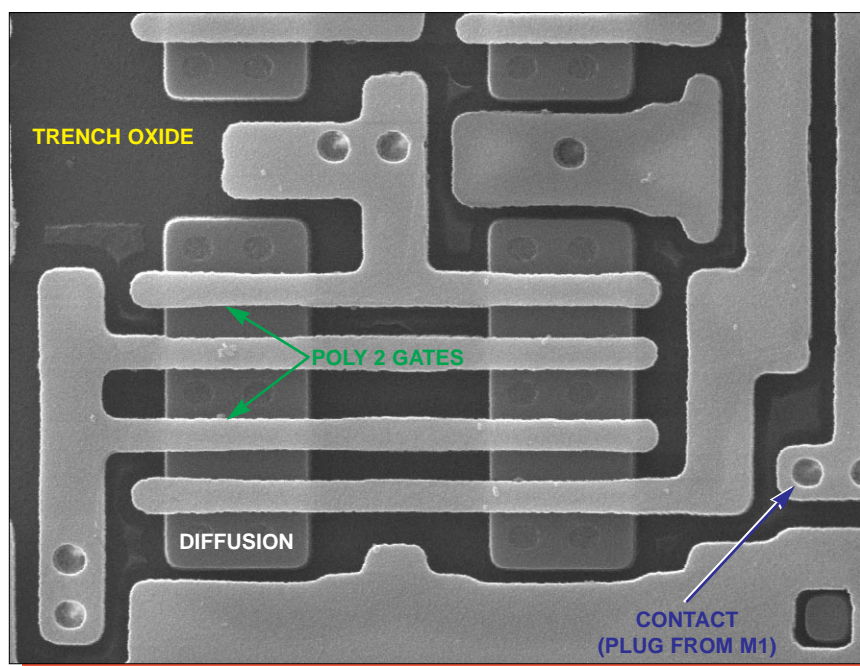
Mag. 40,000x

Figure 26. SEM section views of metal 1-to-N+ diffusion contacts.



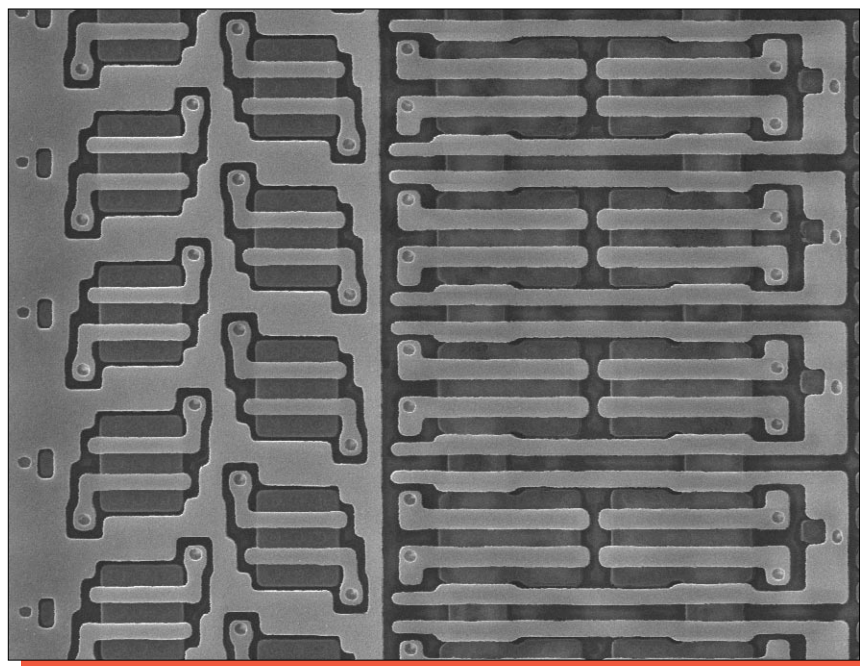


Mag. 4000x

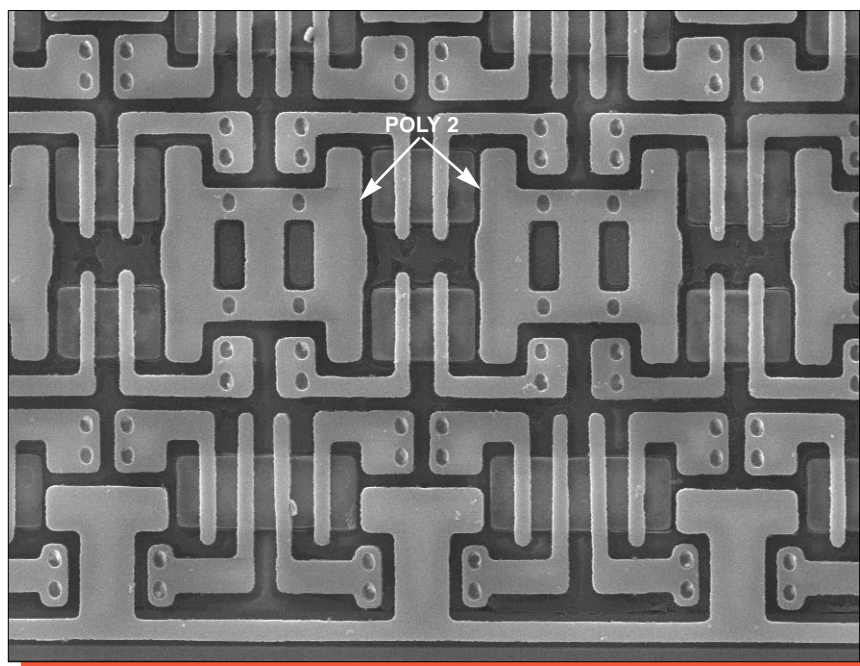


Mag. 8000x

Figure 27. Topological SEM views illustrating poly 2 patterning. 0°.

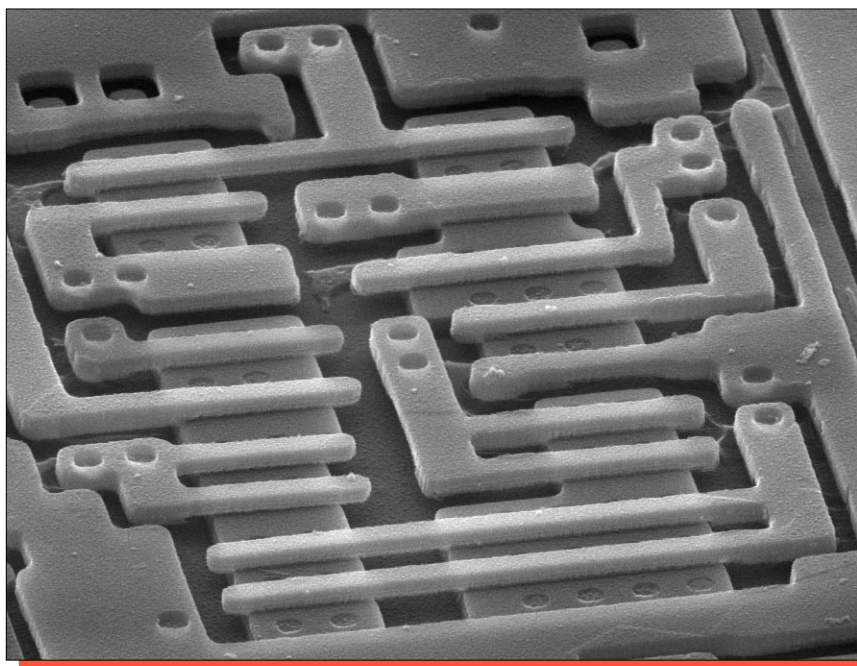


Mag. 3200x

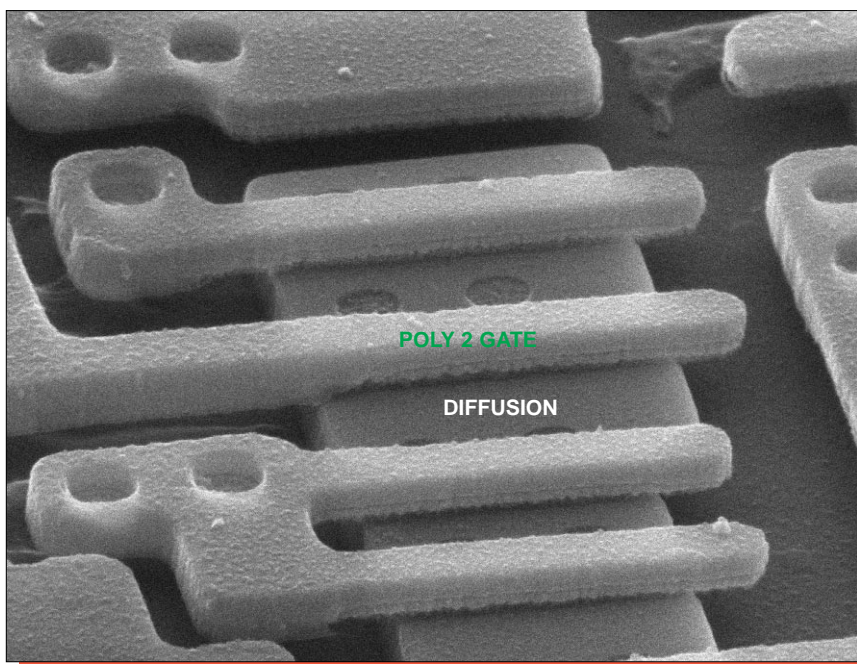


Mag. 4000x

Figure 28. Topological SEM views illustrating poly 2 patterning in the decode areas. 0°.



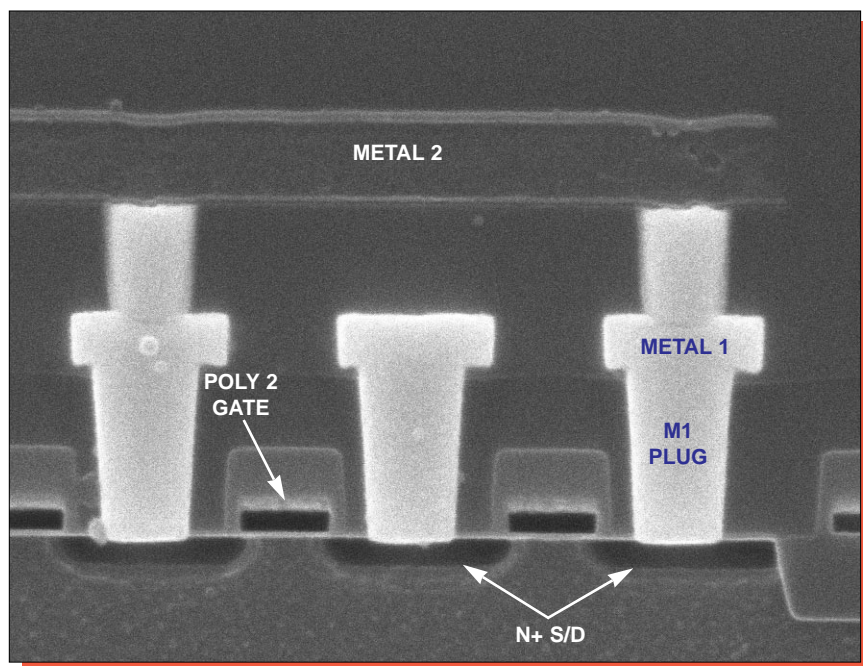
Mag. 7000x



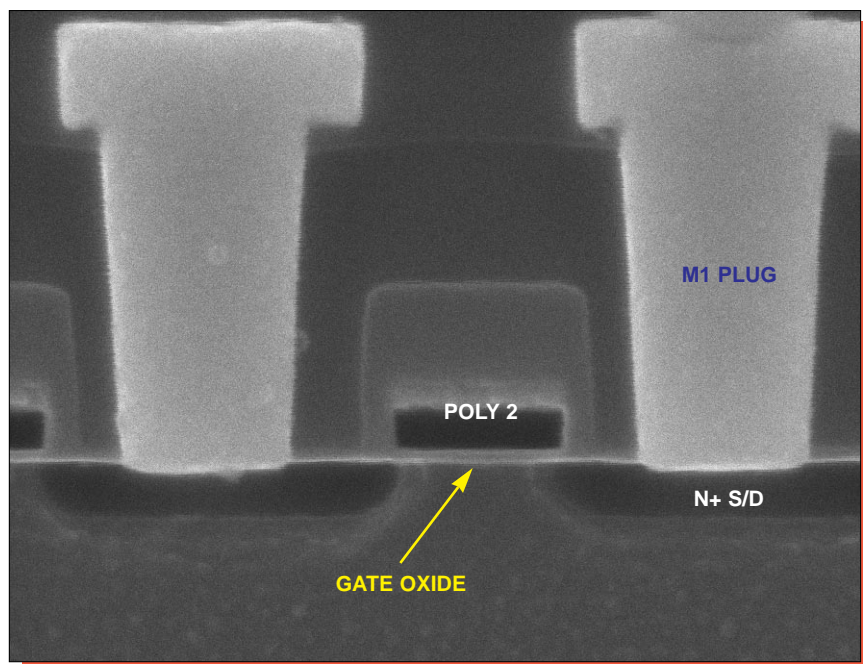
Mag. 17,000x

Figure 29. Perspective SEM views of poly 2. 55°.



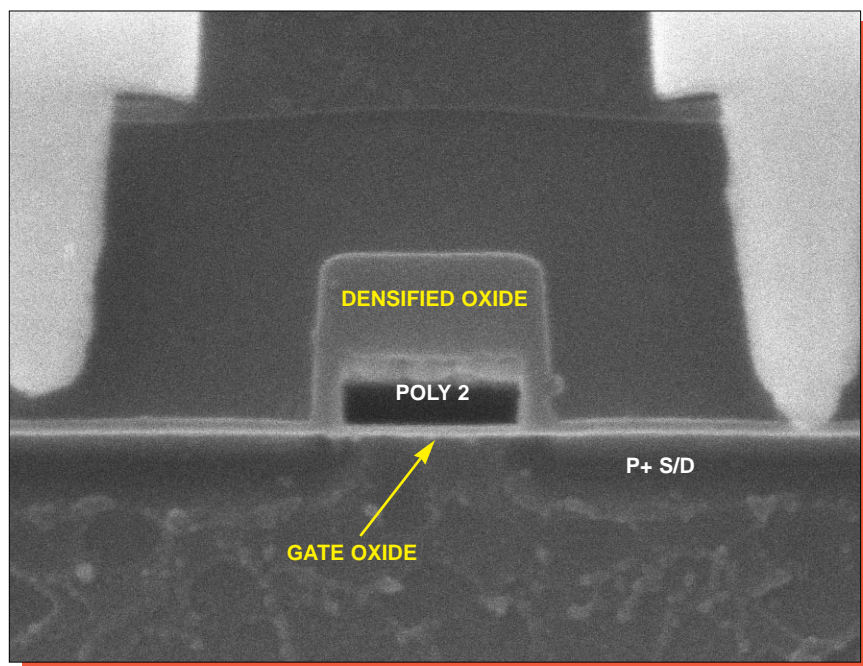


Mag. 26,000x

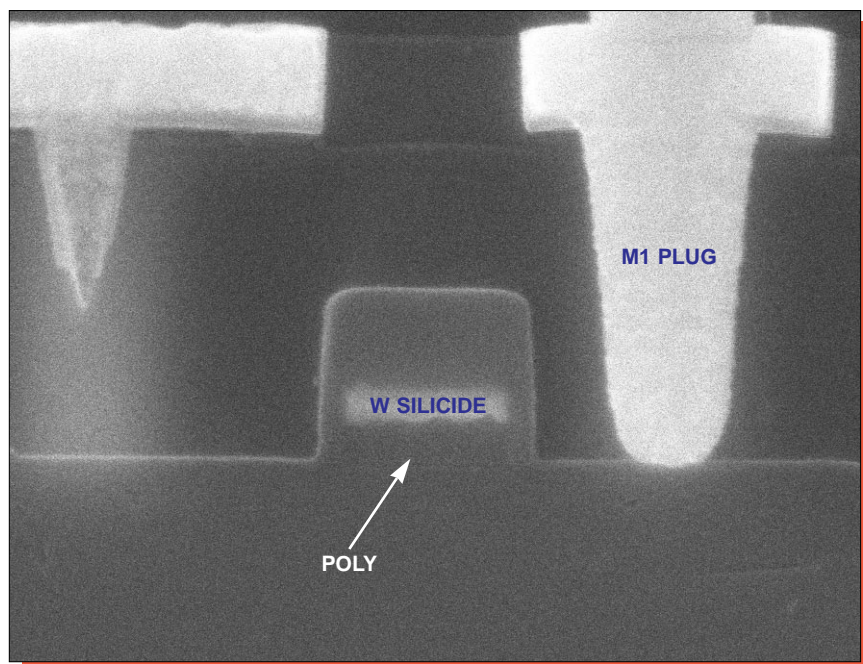


Mag. 52,000x

Figure 30. SEM section views of N-channel transistors.

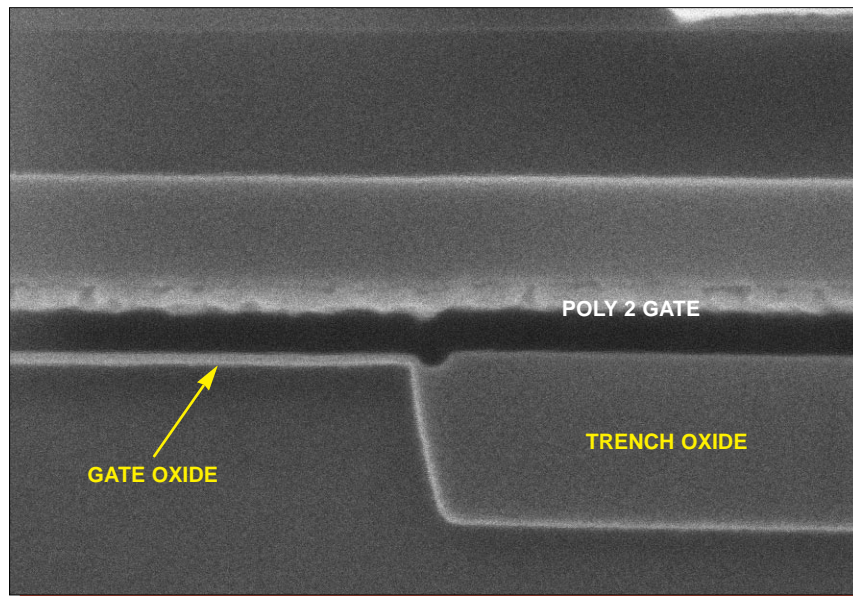


P-channel

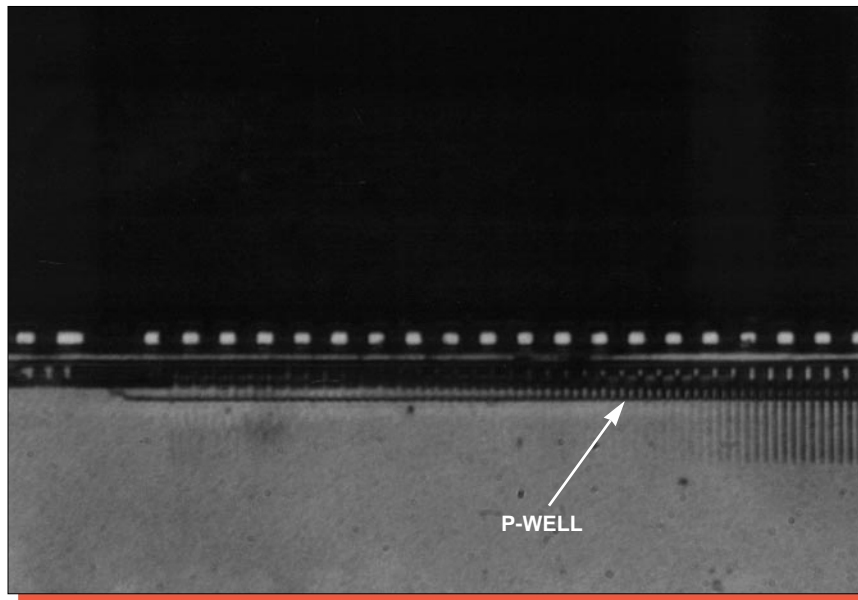


glass etch

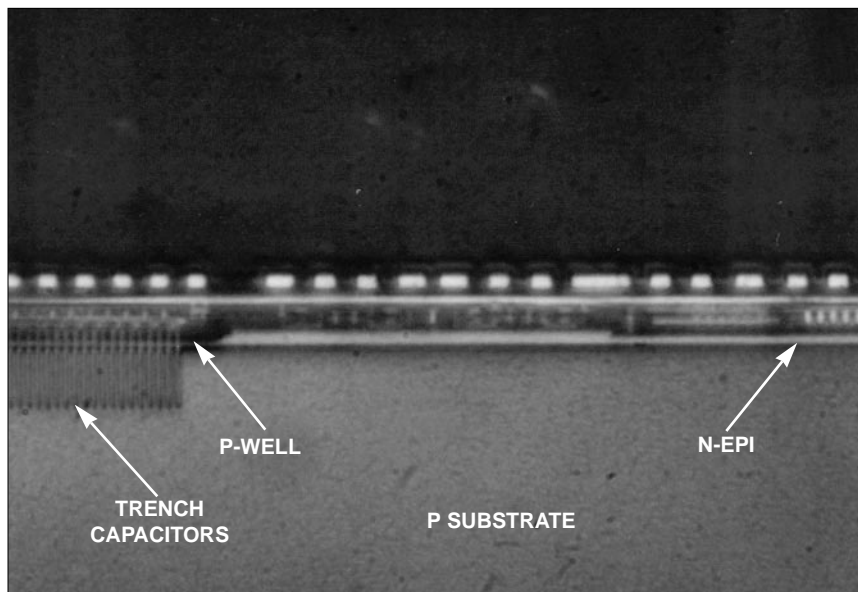
Figure 31. SEM section views of typical transistors. Mag. 52,000x.



Mag. 52,000x



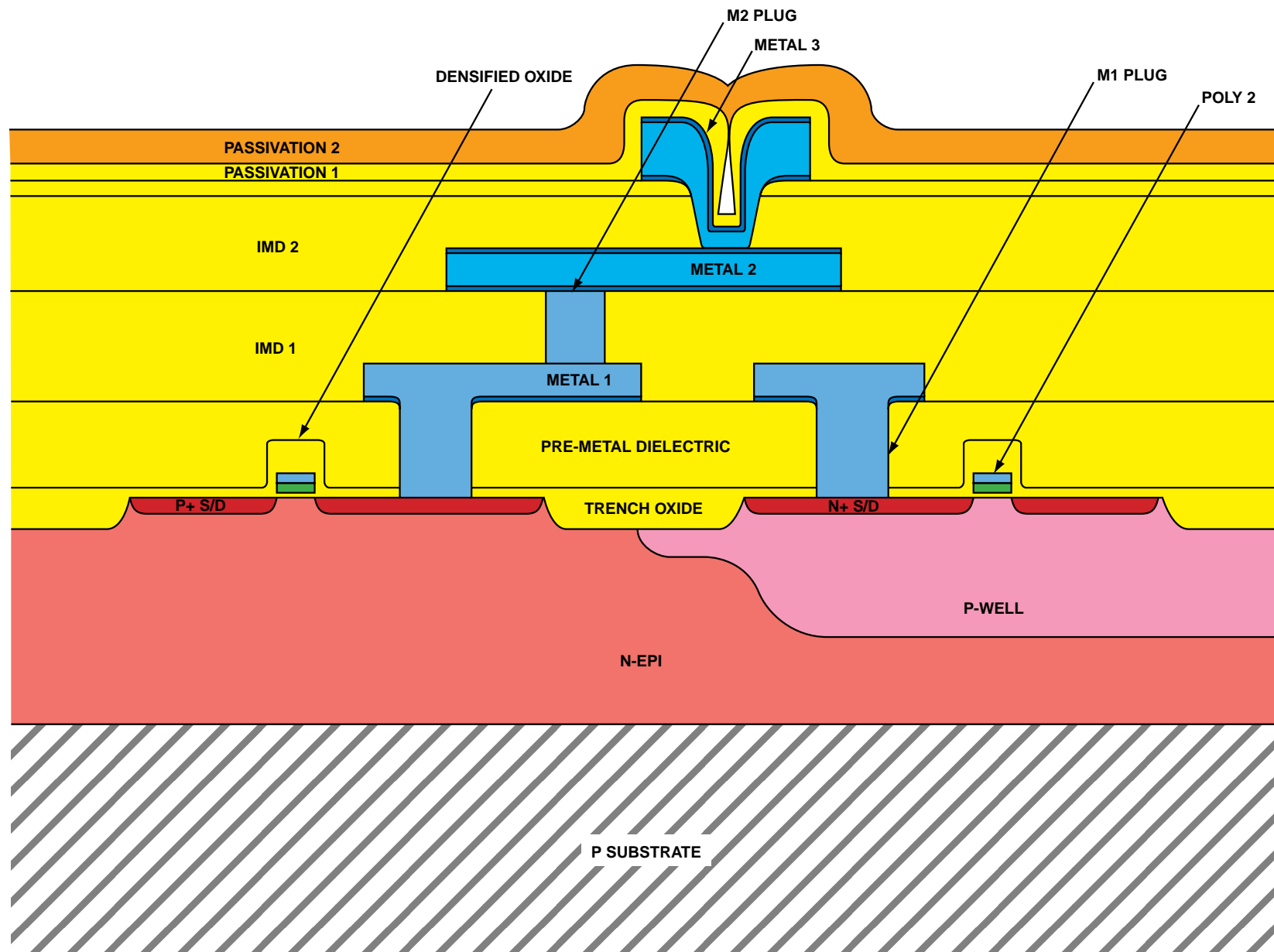
Mag. 1600x



Mag. 1600x

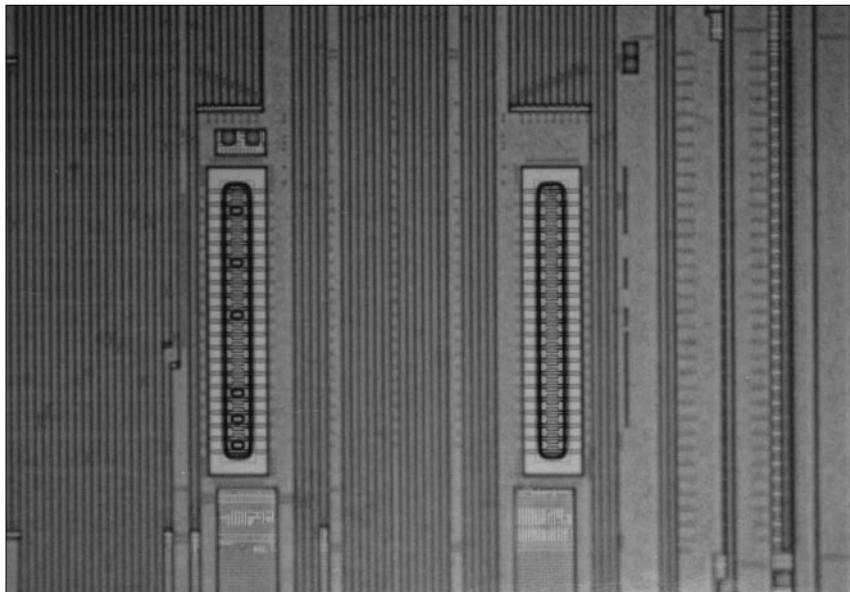
Figure 32. Section views of a trench/gate oxide interface and well structure.



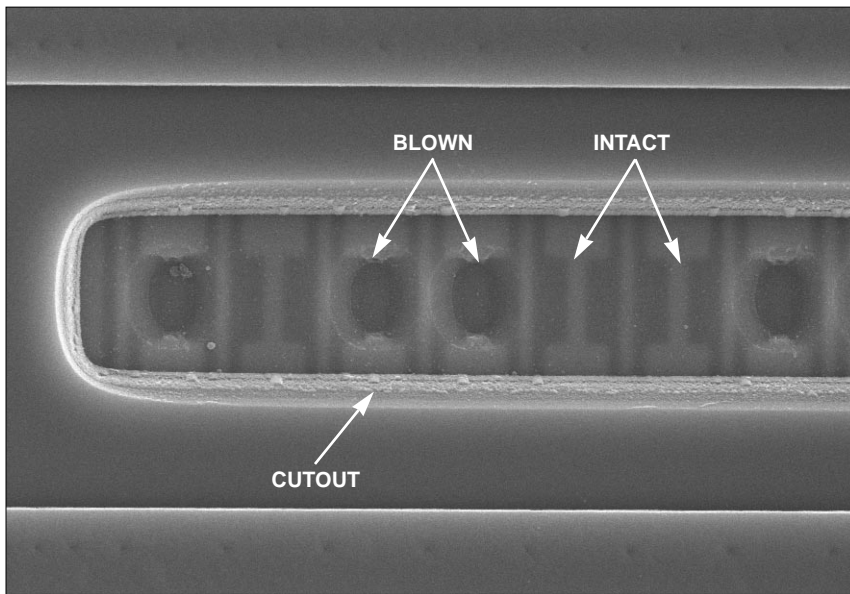


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,  
 Red = Diffusion, and Gray = Substrate

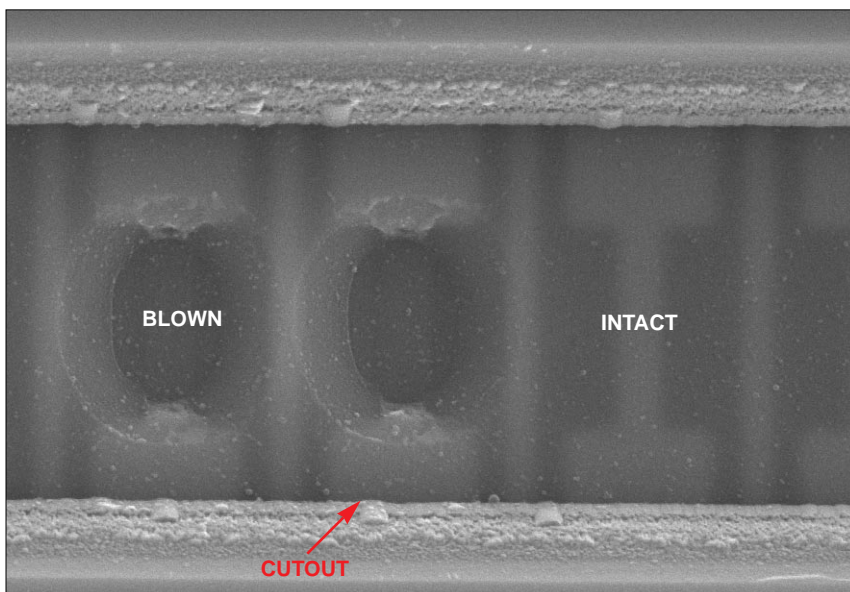
Figure 33. Color cross section drawing illustrating device structure.



Mag. 320x



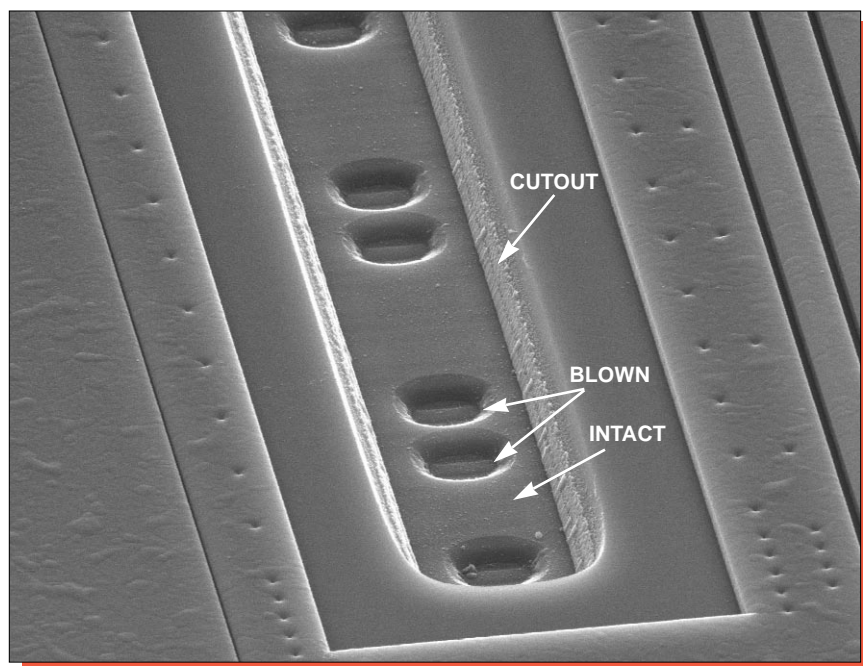
Mag. 2500x



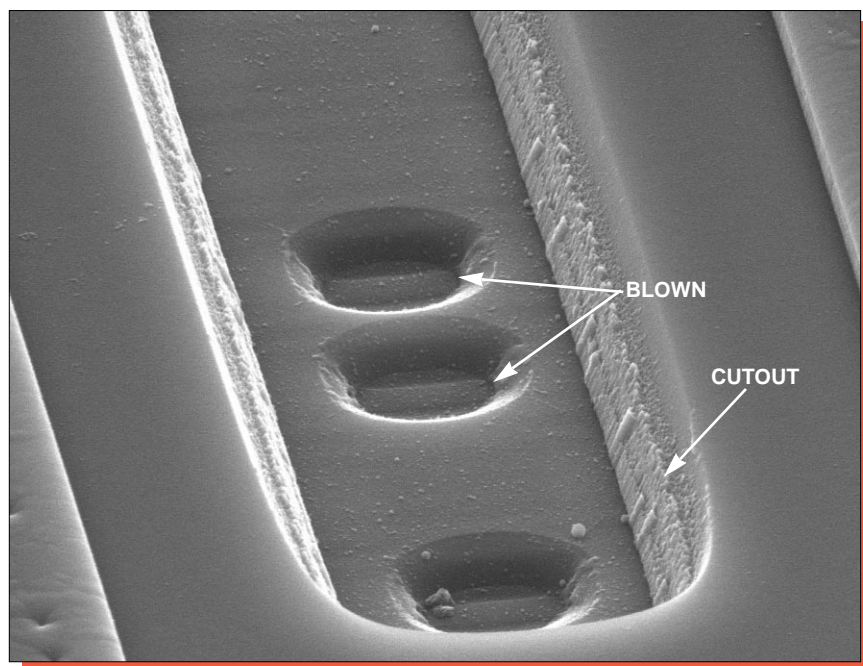
Mag. 6000x

Figure 34. Topological views of poly 2 fuses. 0°.



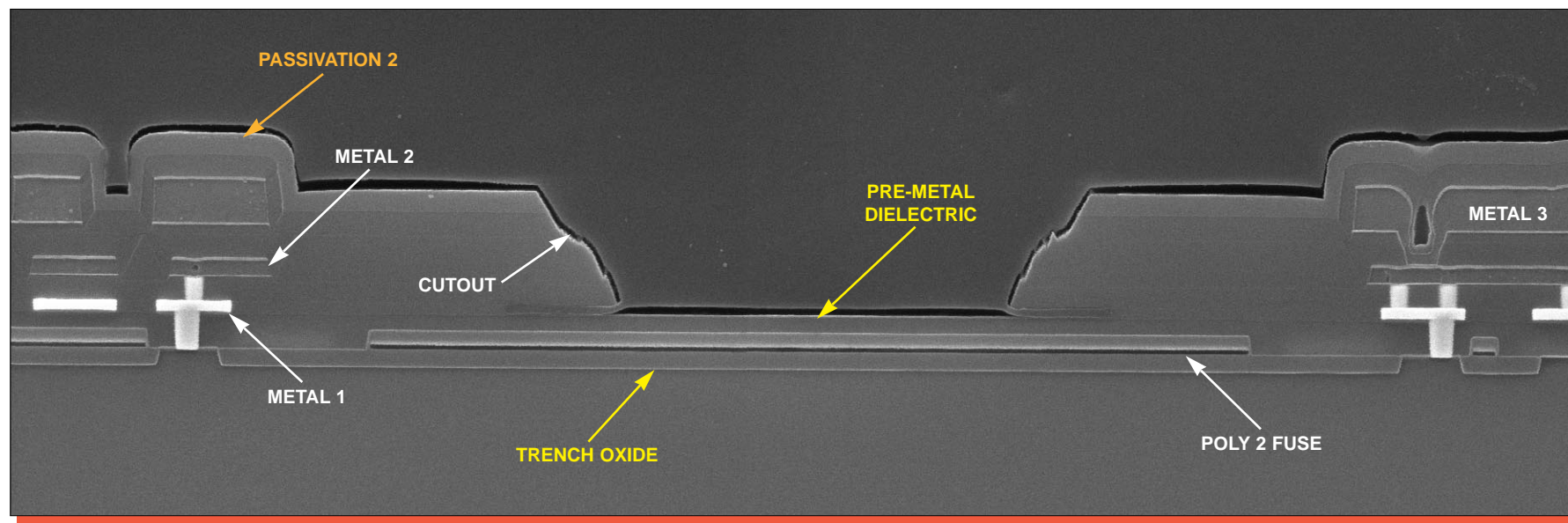


Mag. 2500x

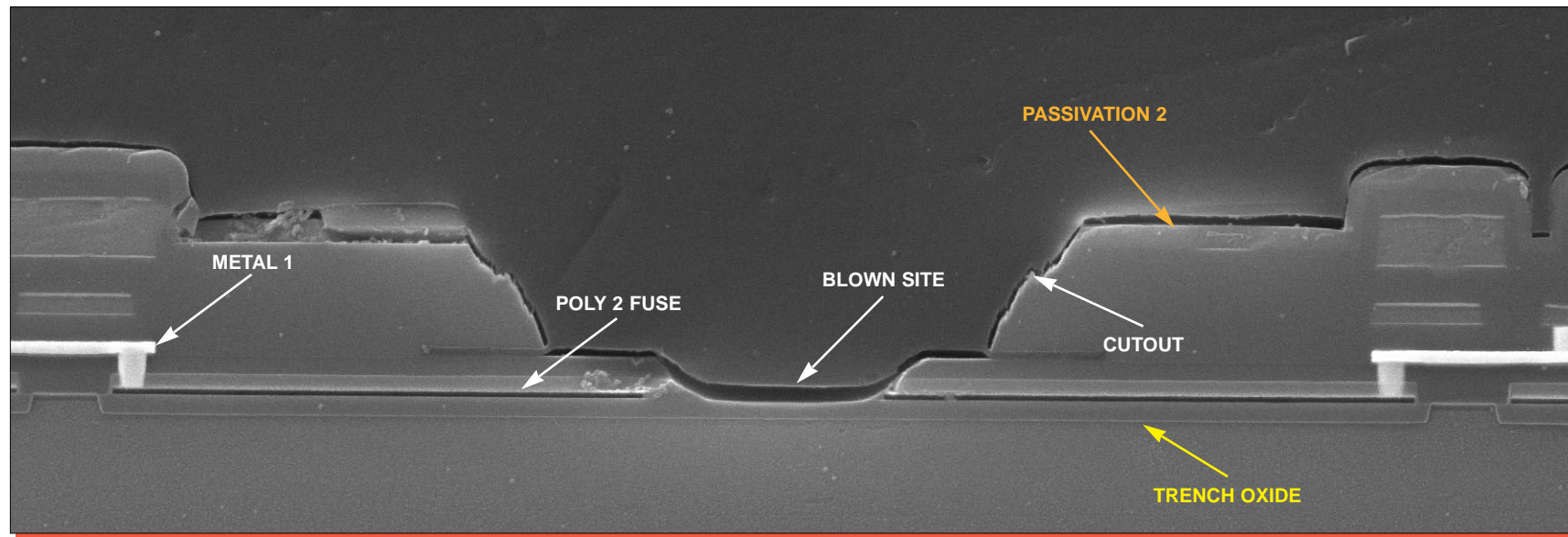


Mag. 5000x

Figure 35. Perspective SEM views of poly 2 fuses. 55°.



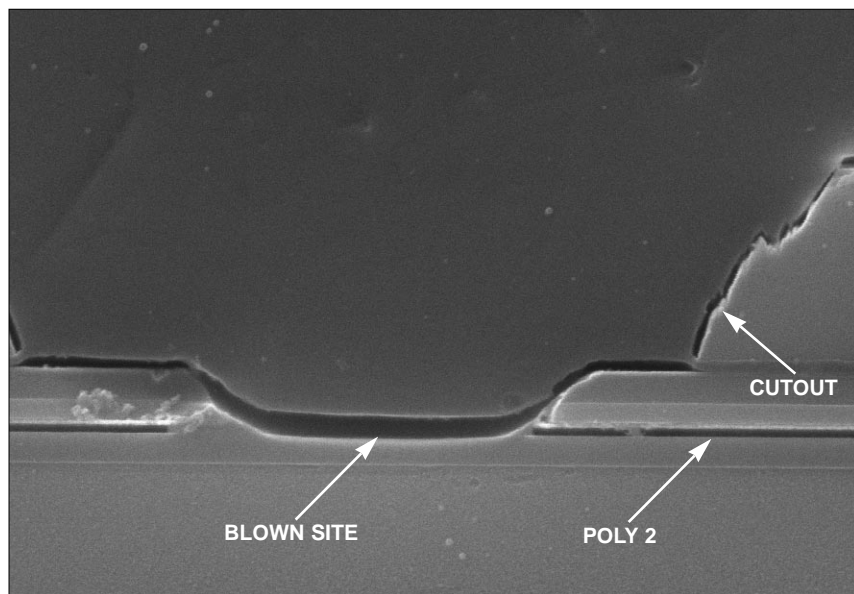
intact



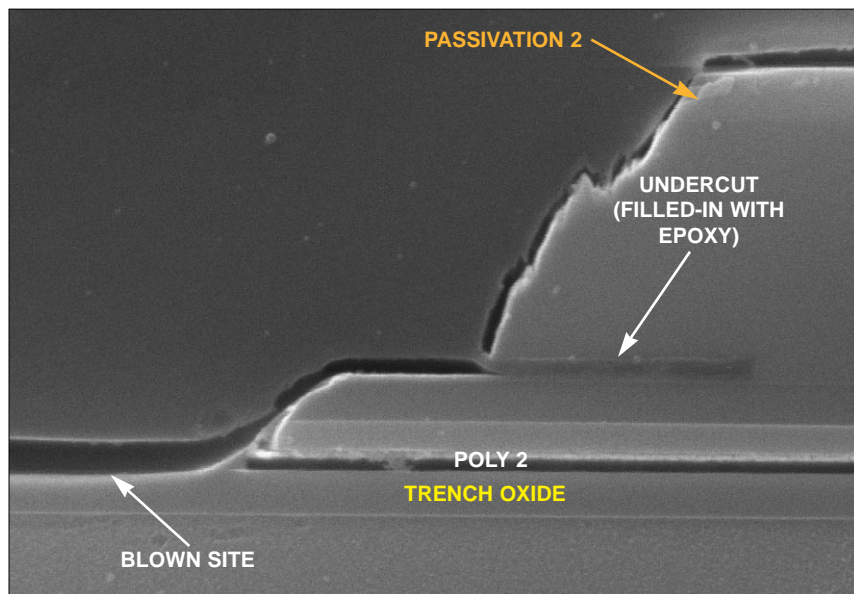
blown

Figure 36. SEM section views of intact and blown poly 2 fuses. Mag. 7000x.

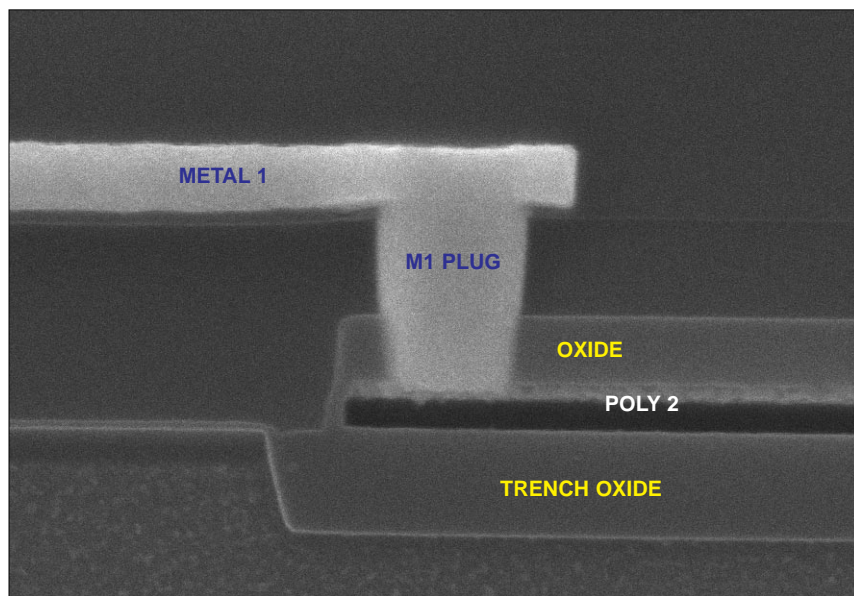




Mag. 10,000x



Mag. 15,000x



Mag. 35,000x

Figure 36a. SEM section details of a blown fuse.

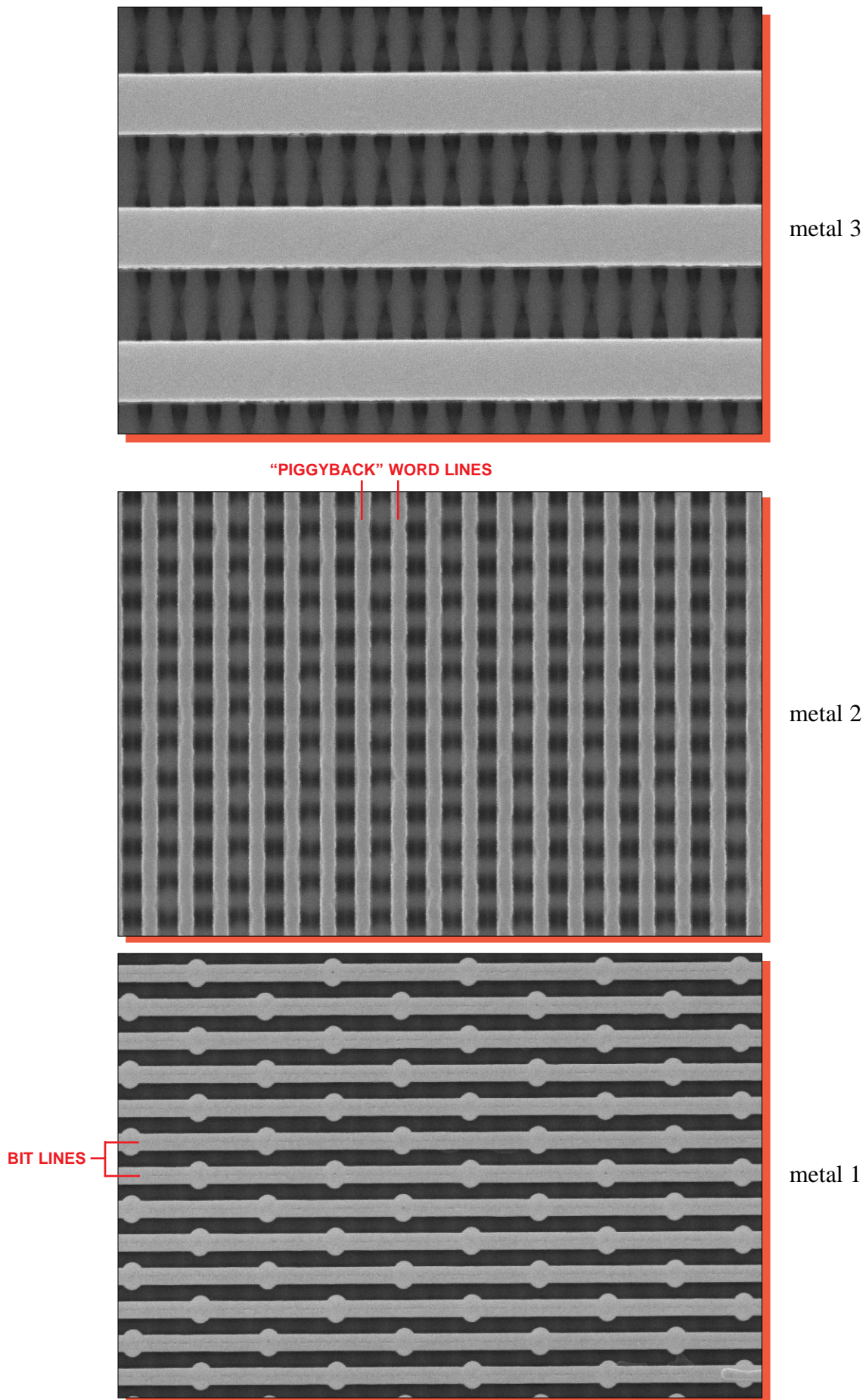
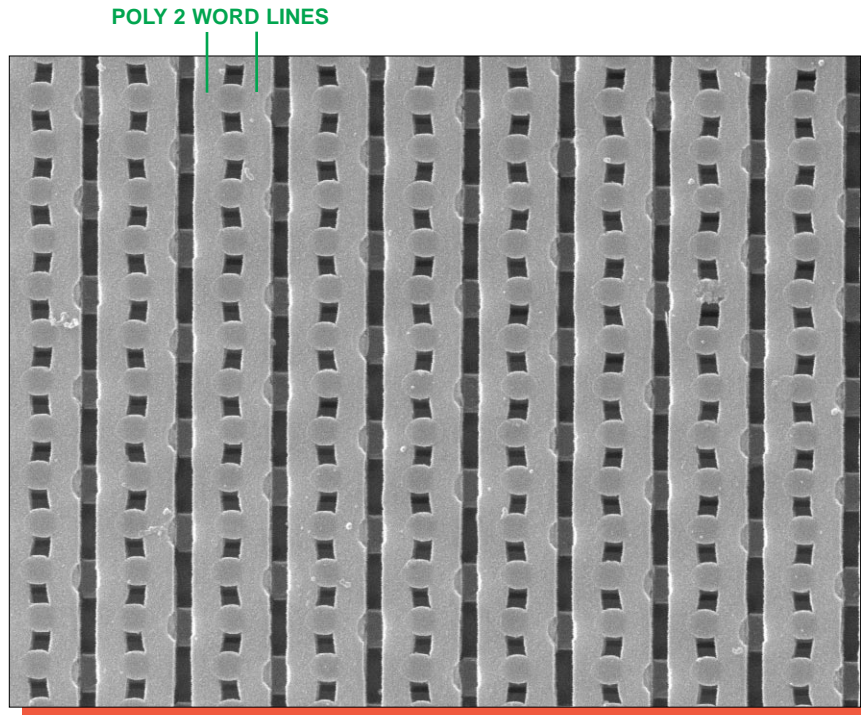
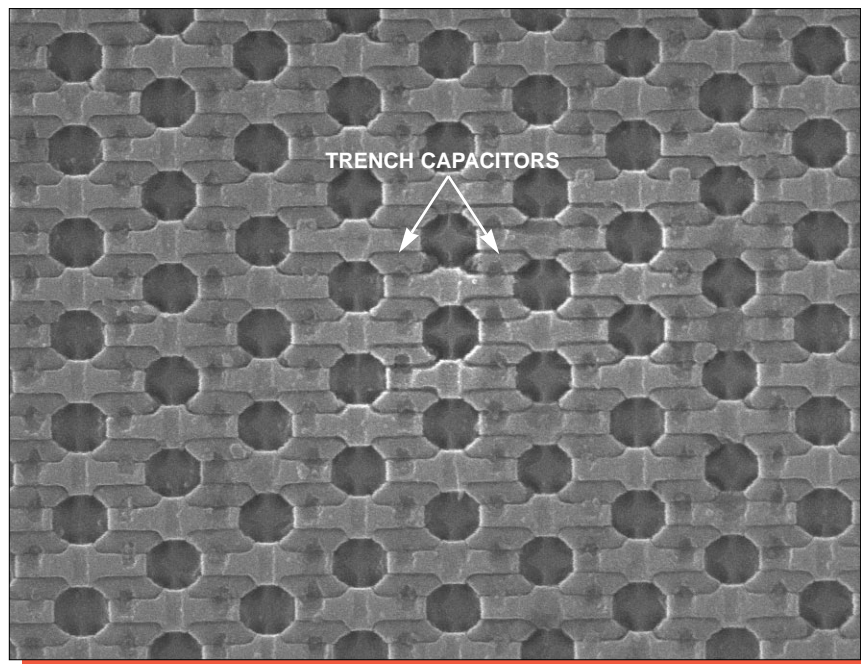


Figure 37. Topological SEM views of the cell array. Mag. 8000x, 0°.



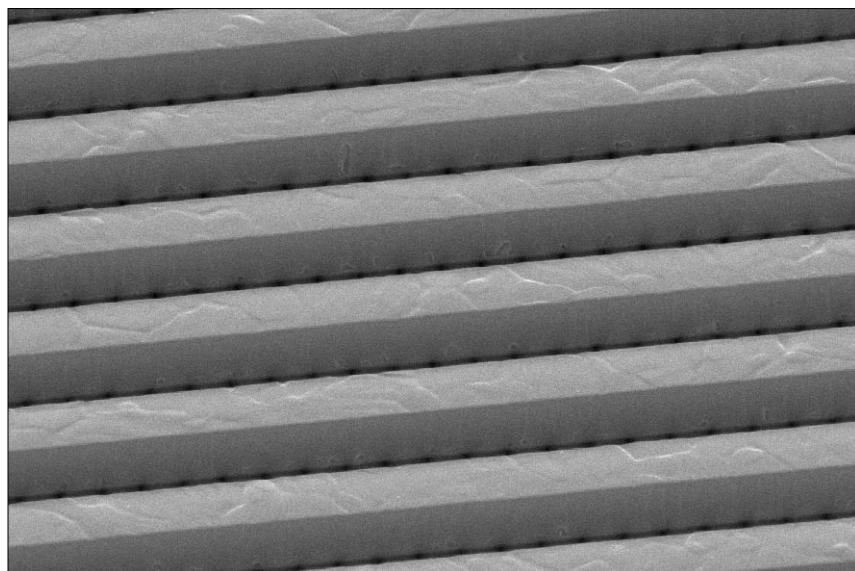


poly 2 and 3

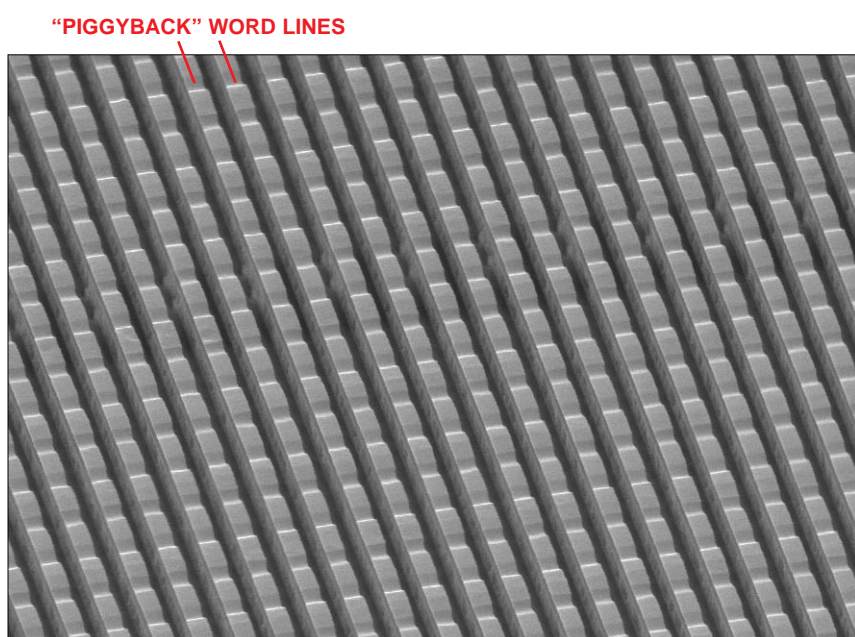


delayed to substrate

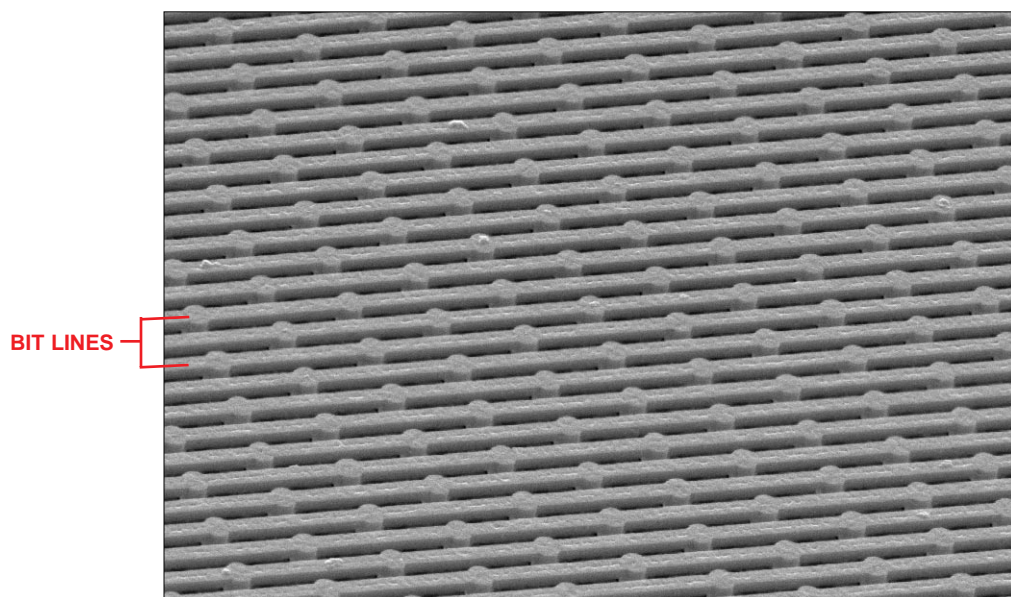
Figure 37a. Topological SEM views of the cell array. Mag. 8000x, 0°.



metal 3



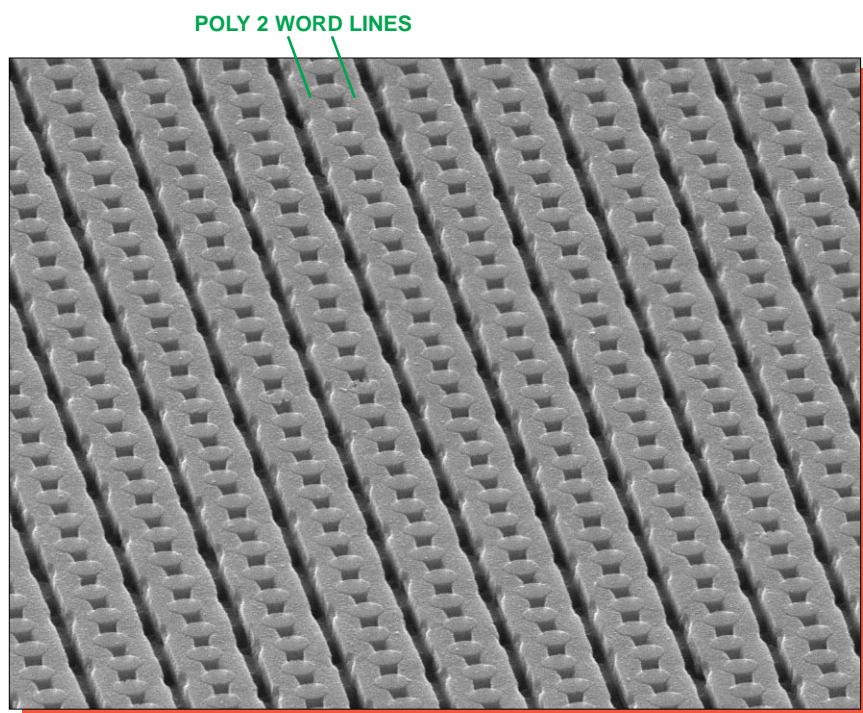
metal 2



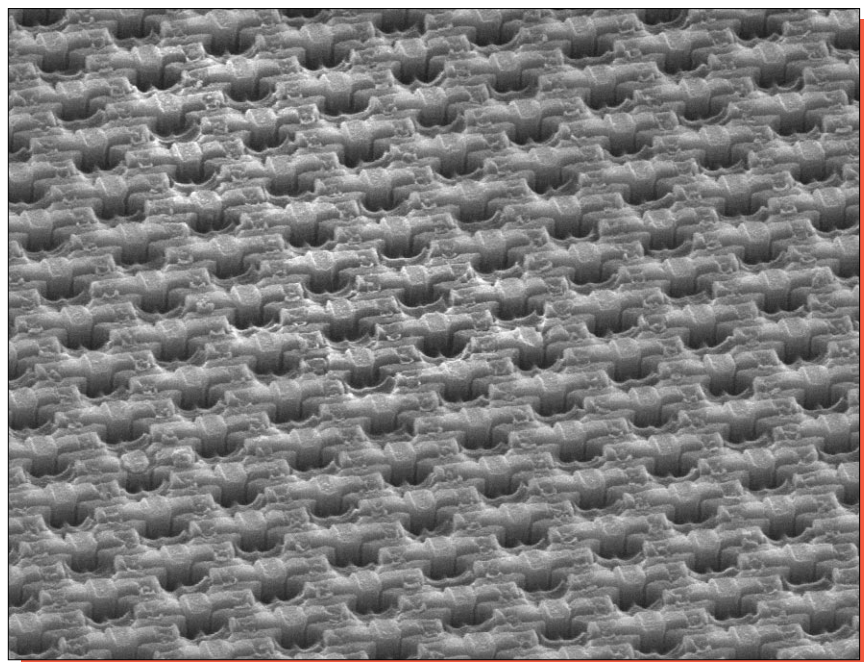
metal 1

Figure 38. Perspective SEM views of the cell array. Mag. 7000x, 55°.





poly 2 and 3



delayed to substrate

Figure 38a. Perspective SEM views of the cell array. Mag. 7000x, 55°.

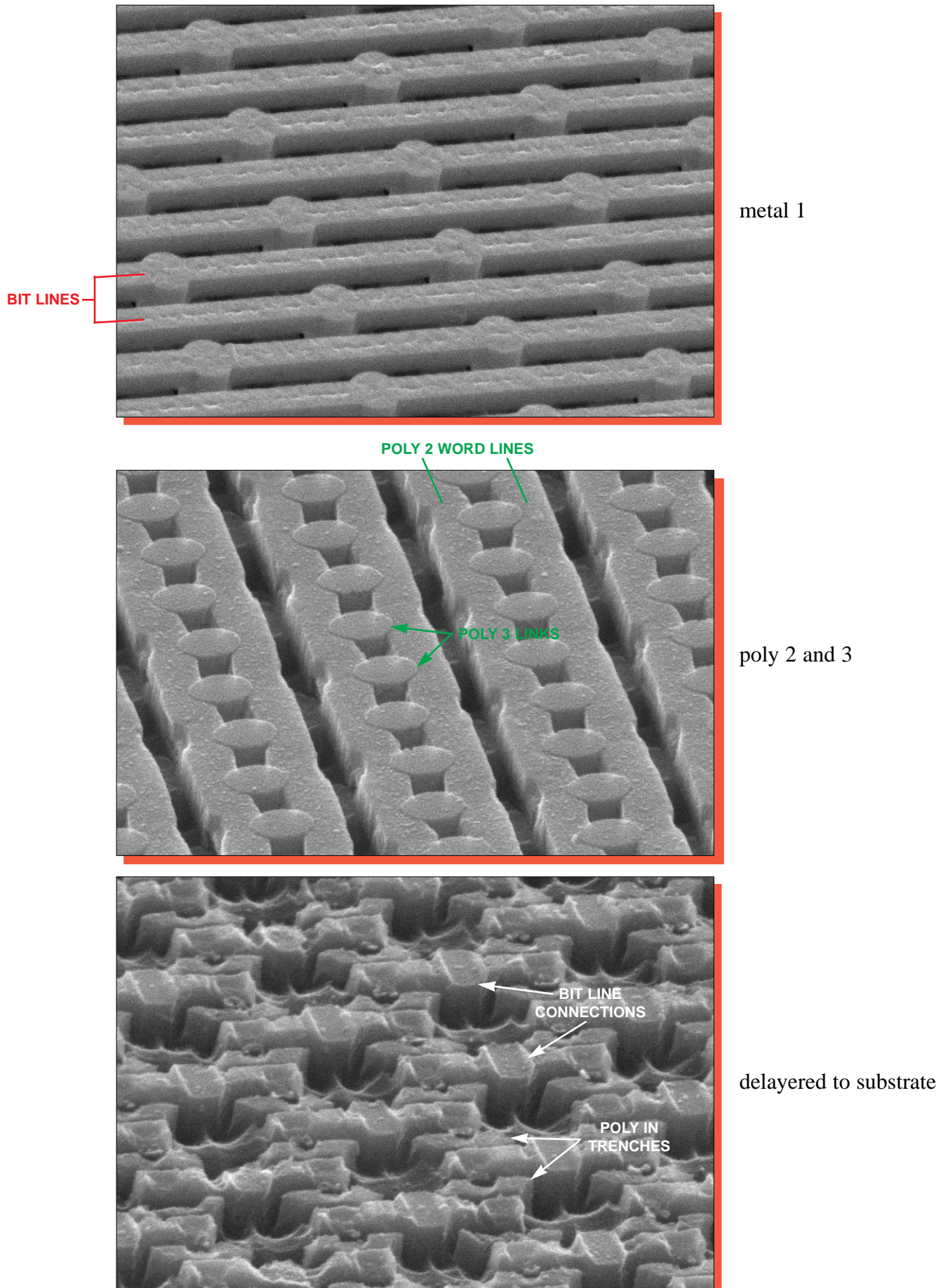
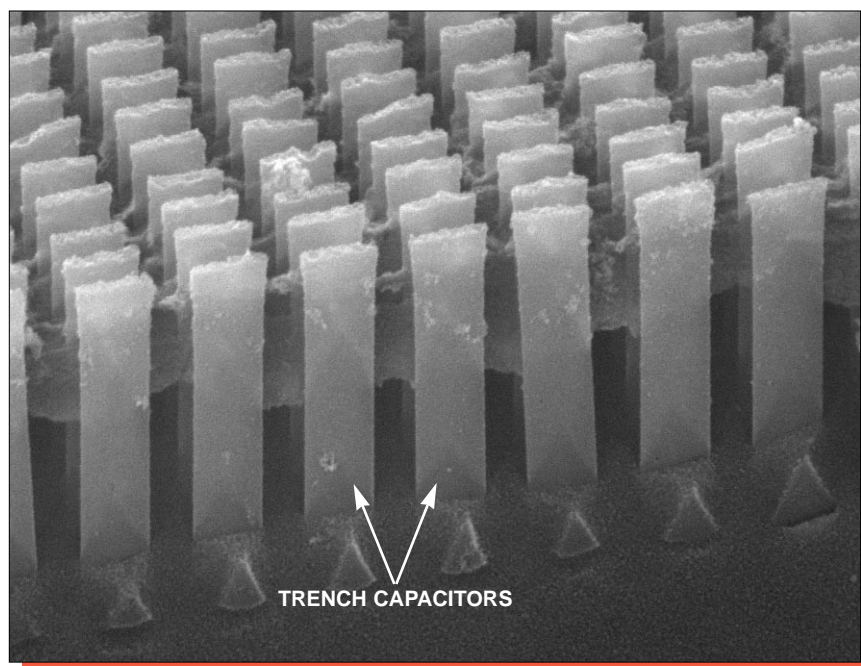
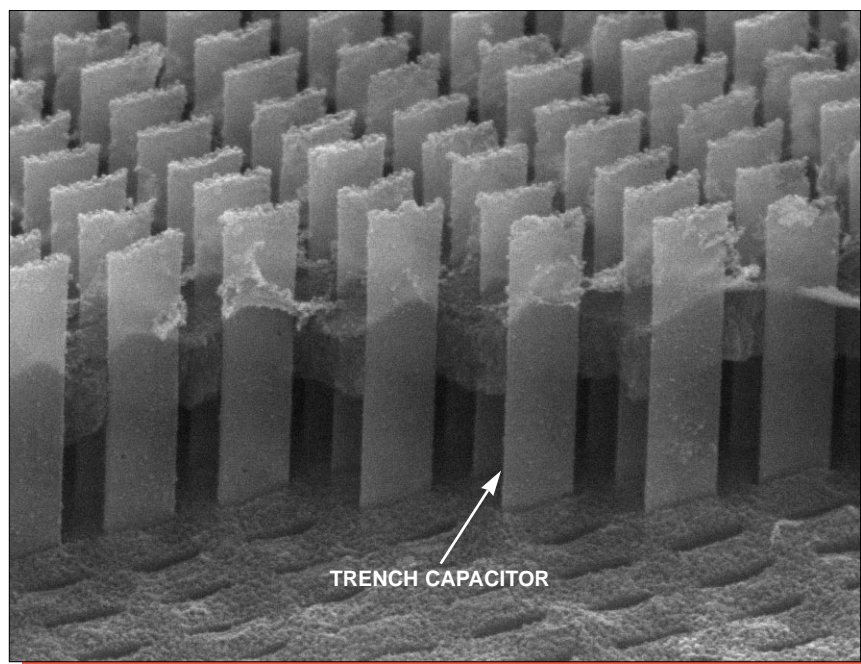


Figure 39. Detail views of DRAM cells. Mag. 20,000x, 55°.



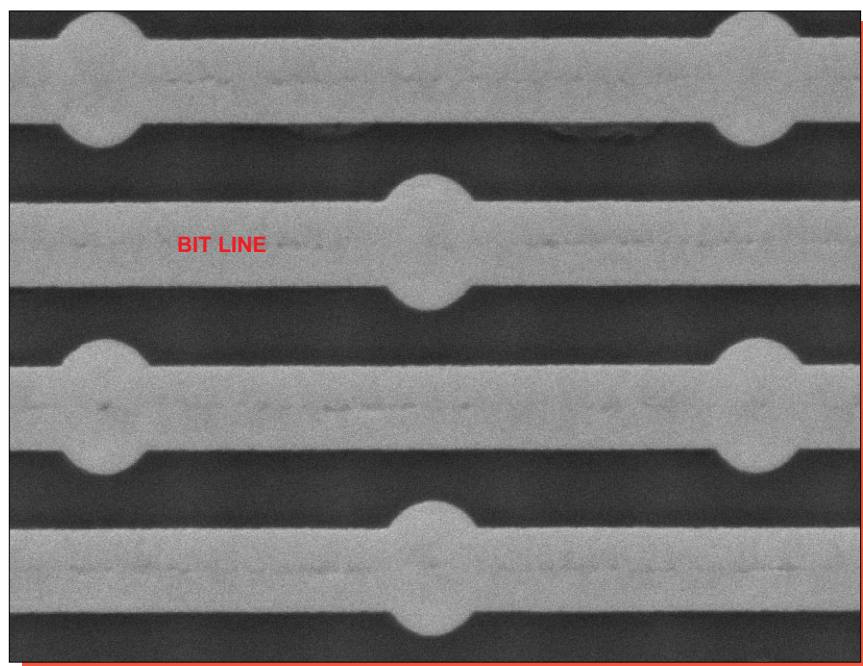


Mag. 10,000x

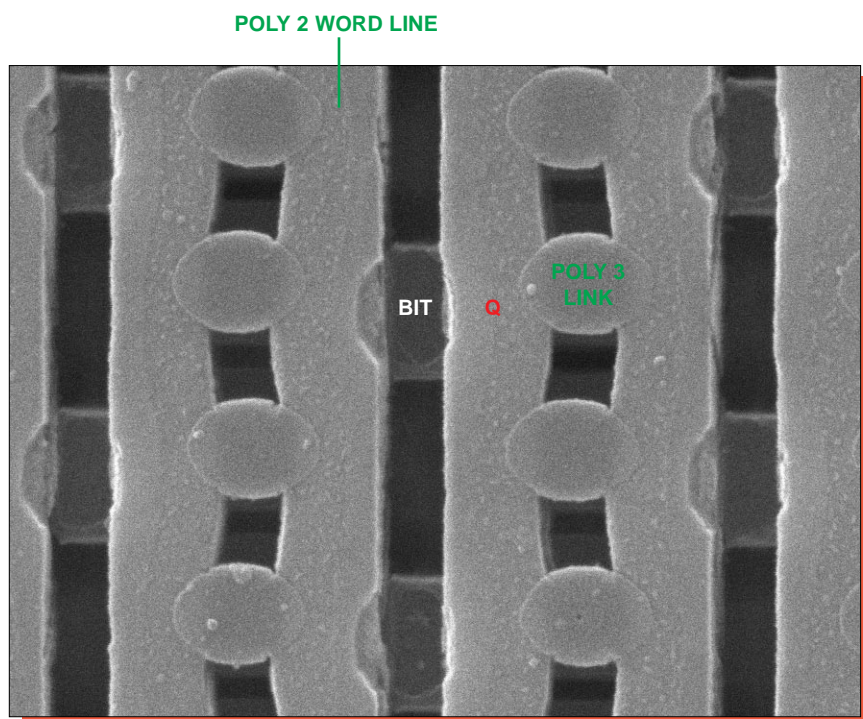


Mag. 11,000x

Figure 40. Perspective views illustrating trench capacitors (substrate etched). 55°.

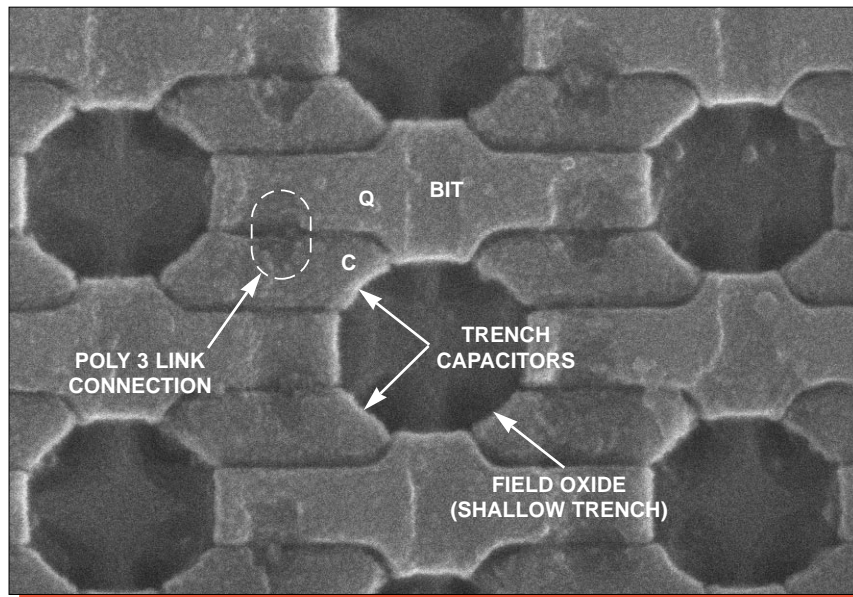


metal 1

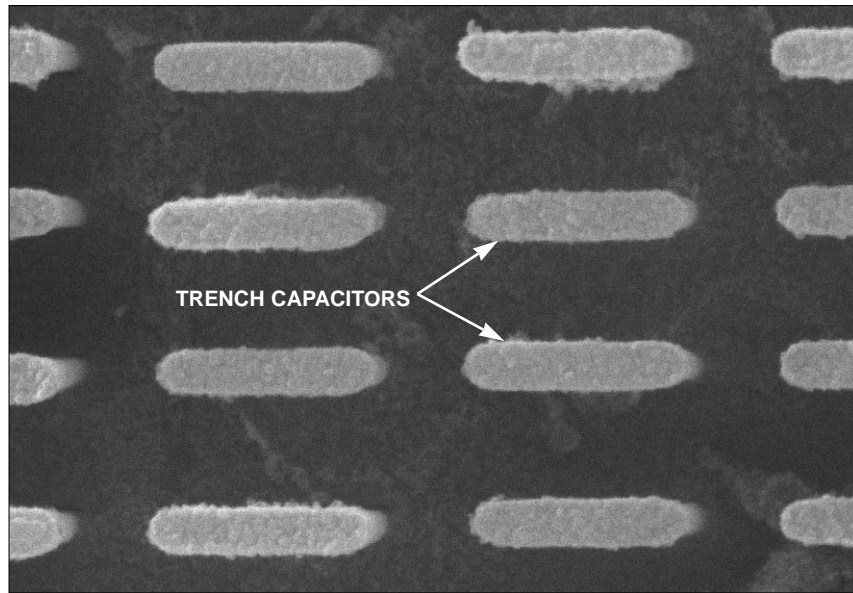


poly 2 and 3

Figure 41. Detailed topological SEM views of DRAM cells. Mag. 30,000x, 0°.



delayered to substrate



trench capacitors

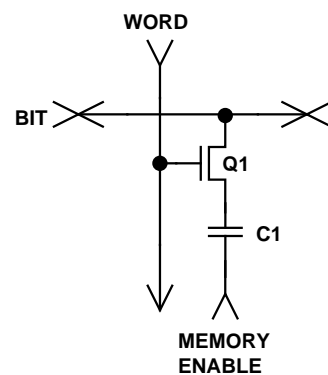
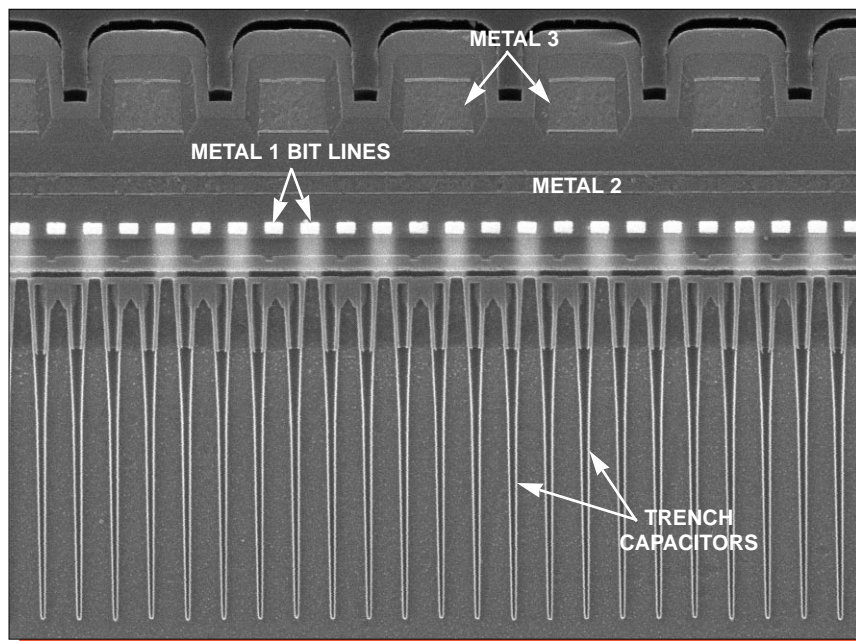
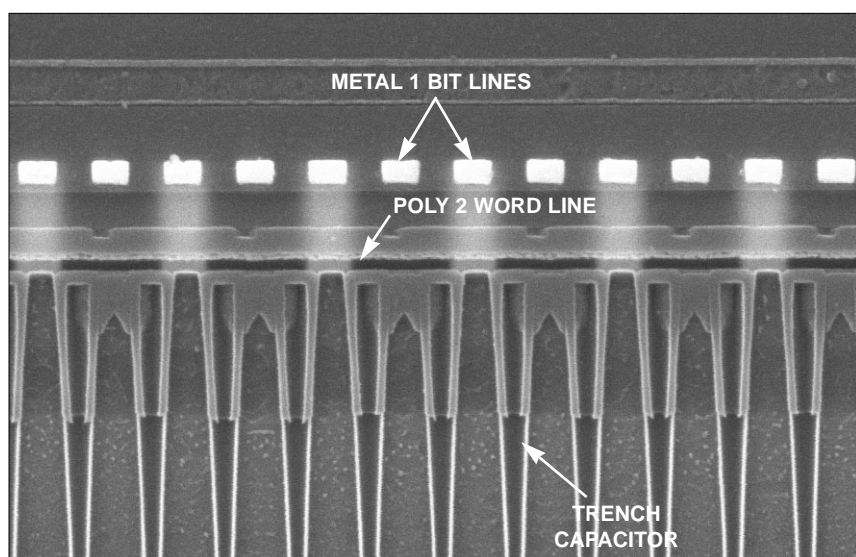


Figure 41a. Detail topological SEM views of DRAM cells with the cell schematic.  
Mag. 30,000x, 0°.

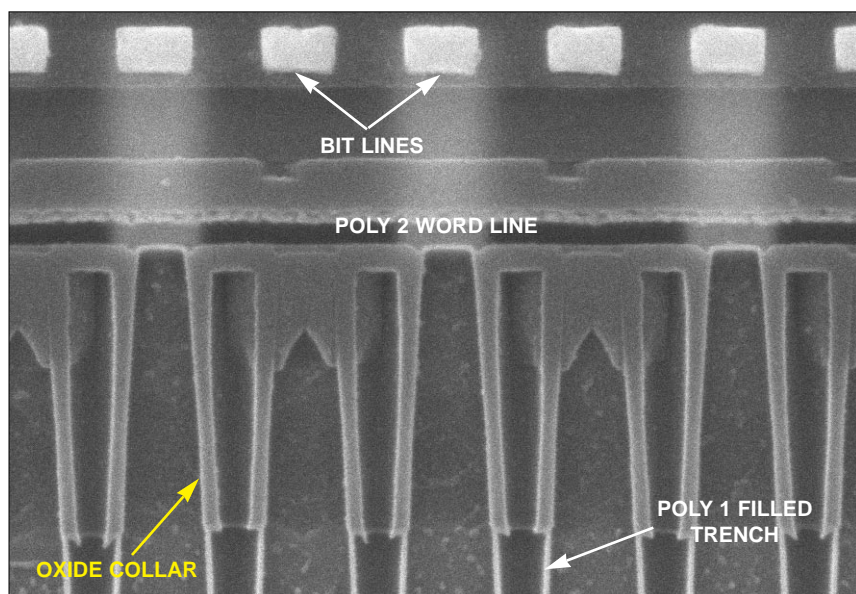




Mag. 6500x



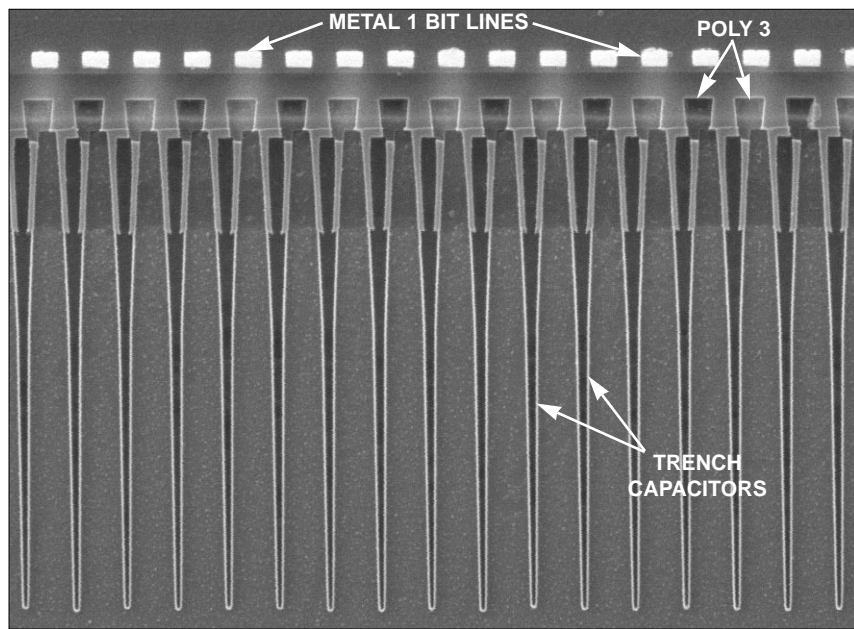
Mag. 13,000x



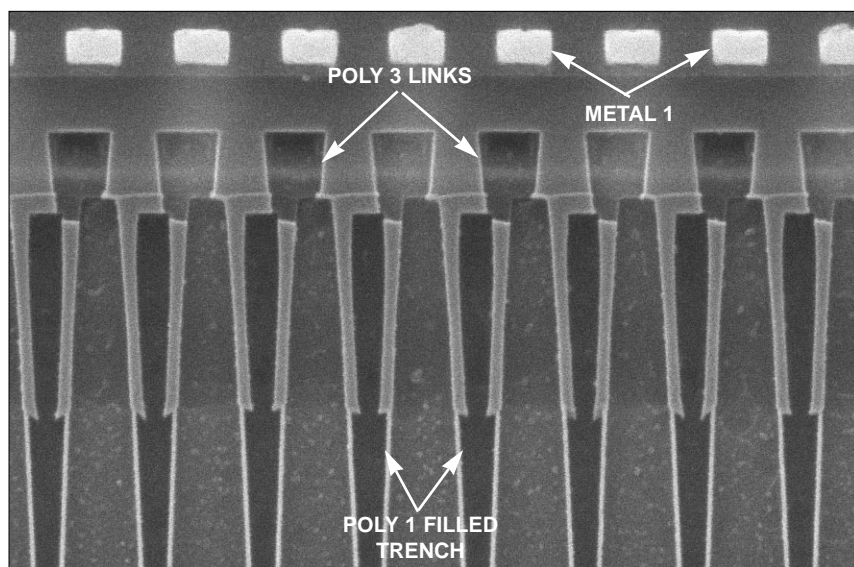
Mag. 26,000x

Figure 42. SEM section views of DRAM cells (parallel to word lines).

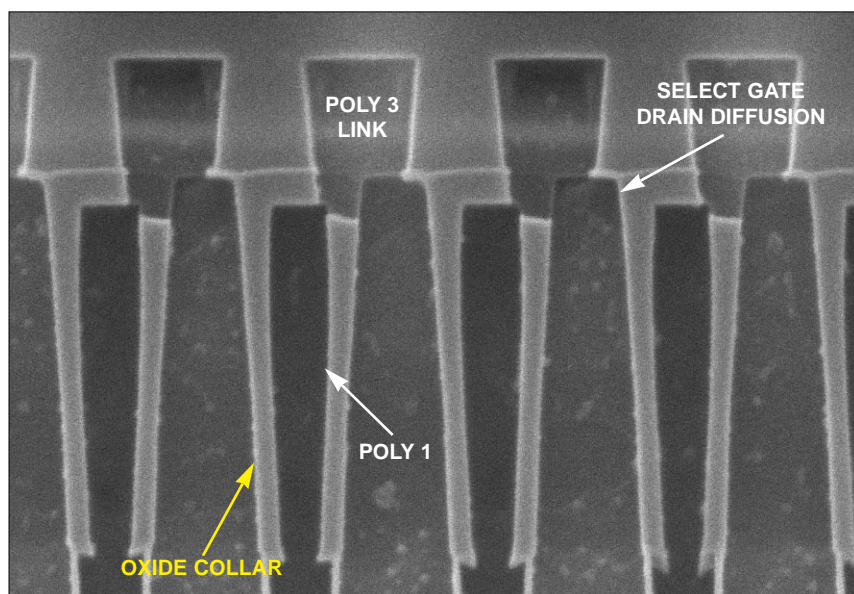




Mag. 9000x

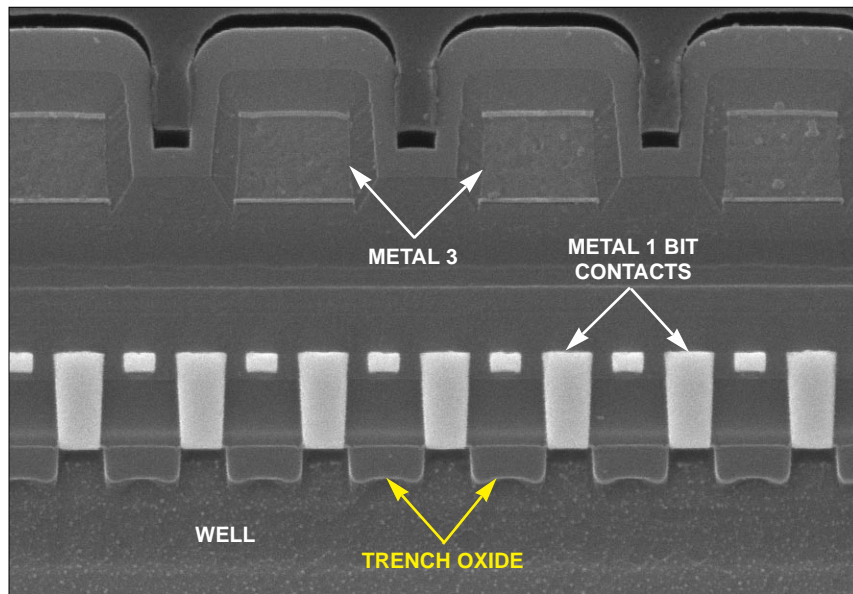


Mag. 20,000x

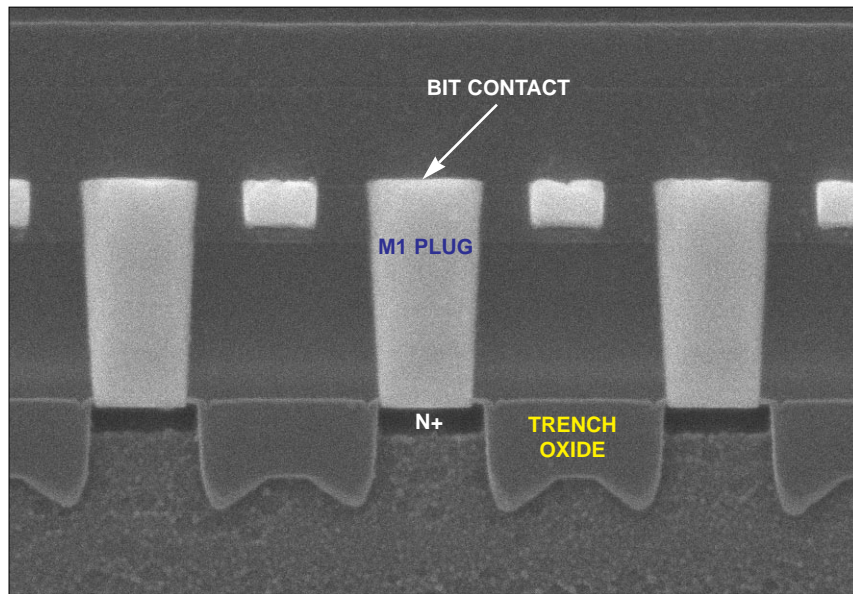


Mag. 35,000x

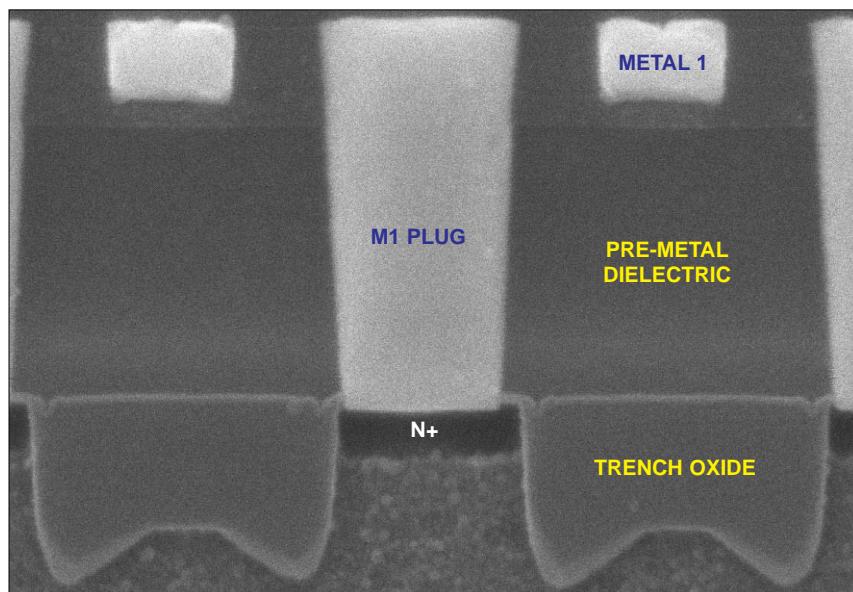
Figure 43. SEM section views of DRAM cells illustrating poly 3 link connection.



Mag. 11,000x



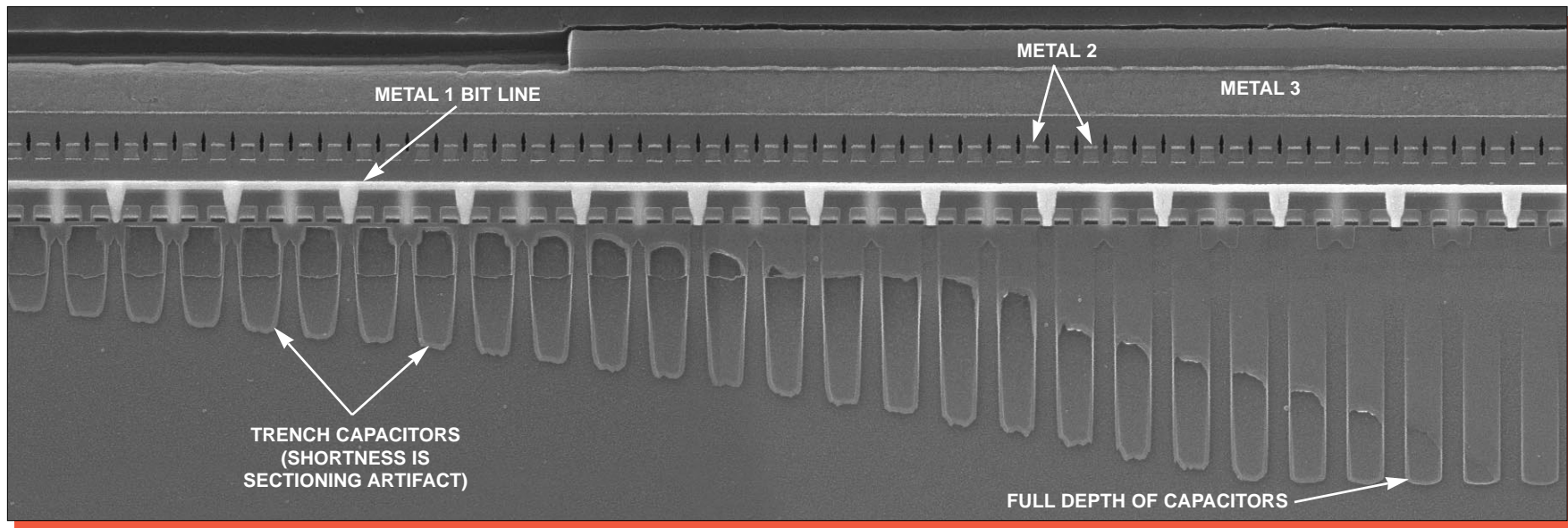
Mag. 26,000x



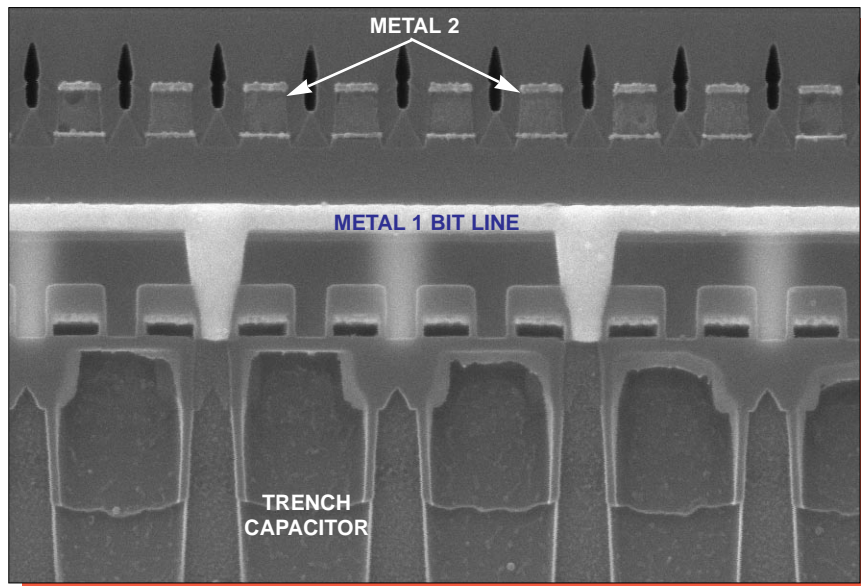
Mag. 45,000x

Figure 44. SEM section views of DRAM cells illustrating bit line contacts.

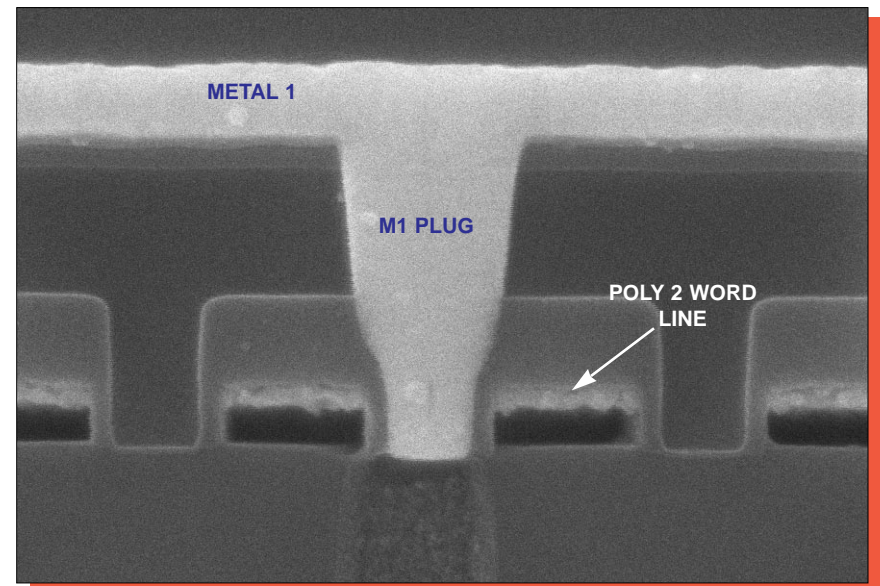




Mag. 5500x

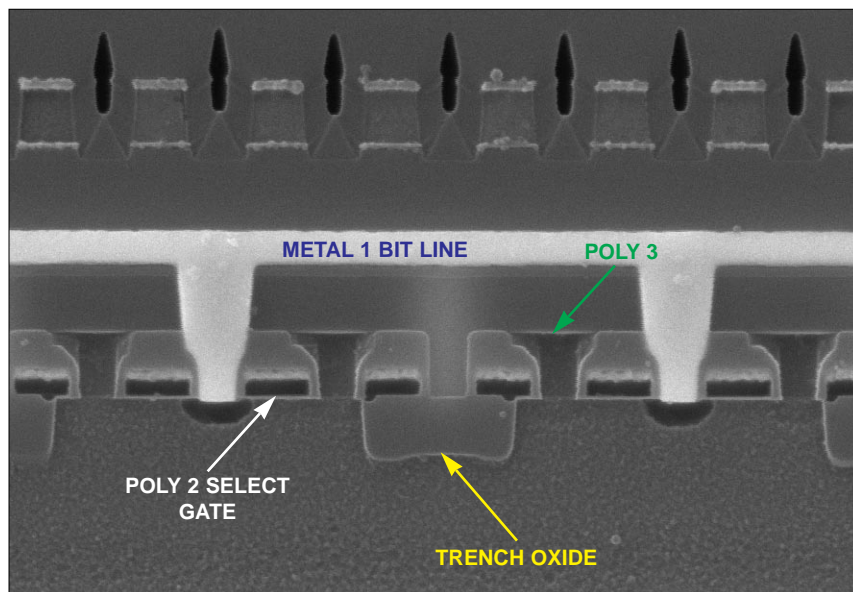


Mag. 15,000x

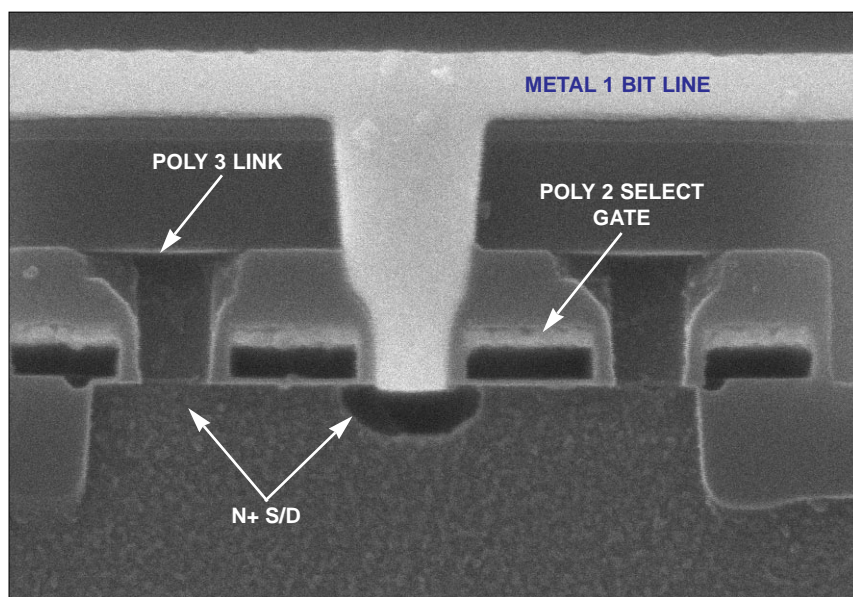


Mag. 45,000x

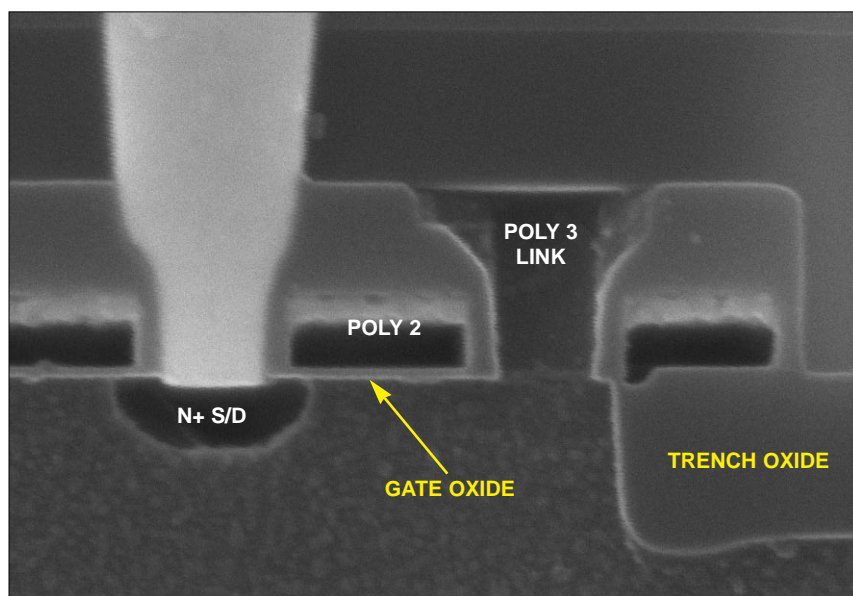
Figure 45. SEM section views of DRAM cells (parallel to bit lines).



Mag. 20,000x



Mag. 40,000x



Mag. 60,000x

Figure 46. SEM section views of DRAM cells illustrating bit line contacts and select gates.