

Construction Analysis

Atmel AT27C512R 512K UVEPROM

Report Number: SCA 9612-516



INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Atmel AT27C512R 512K UVEPROM. Three devices packaged in 28-pin Ceramic Dual In-Line Packages (CERDIPs) with a quartz window were received for the analysis. Devices were date coded 9619.

MAJOR FINDINGS

Questionable Items:¹

- Several bond lifts occurred during wirepull tests on Samples 2 and 3.

Special Features:

- Titanium silicided diffusions.
- Tungsten plugs used at all contacts.
- Planarized final passivation.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 28-pin Ceramic Dual In-Line Packages (CERDIPs). A quartz window was present over the die.
- The package consisted of two ceramic halves held together by a glass frit. The die was mounted to the cavity floor using a silver-filled glass.
- Die separation was by sawing.
- Wirebonding was by the ultrasonic wedge bond method (backward bonded) using 1.3 mil O.D. aluminum wire.
- All pins were connected and pins 14 and 28 (Vcc and GND) had multiple bonding wires. A cavity bonding post was employed which biased the substrate to GND.

Die Process:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- No die coat was present.
- Passivation consisted of a layer of oxynitride over a layer of silicon-dioxide. The SiO₂ had been given a minimal planarizing etch.
- Metallization consisted of a single layer of aluminum with a titanium-nitride barrier and a titanium adhesion layer. Tungsten plugs were used at all contacts.
- Pre-metal dielectric consisted of a layer of borophosphosilicate glass (BPSG) over densified oxides. The glass was reflowed prior to contact cuts only.

TECHNOLOGY DESCRIPTION (continued)

- Two layers of poly were used on the die. Polycide 2 (poly and titanium silicide) was used to form all gates on the die and the select/word lines in the EPROM cell array. Poly 1 (no silicide) was used exclusively in the cell to form the floating gates. Direct poly-to-diffusion (buried) contacts were not used. Interpoly dielectric consisted of oxide only. Definition of the poly was by a dry etch of normal quality.
- Standard implanted N⁺ and P⁺ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. A titanium silicide was present on all diffusions (salicide process).
- Local oxide (LOCOS) isolation. A slight step was present in the oxide at the edge of the well indicating a twin-well process was used.
- The memory cells used a stacked poly EPROM design. Metal was used to form the bit lines. Polycide 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates.
- Redundancy fuses were not present.

ANALYSIS RESULTS I

Package and Assembly:

Figures 1 - 7

Questionable Items:¹

- Wirepull tests caused several bond lifts (Figure 7).

General Items:

- Devices were packaged in 28-pin Ceramic Dual In-Line Packages (CERDIPs) with quartz windows.
- Overall package quality: Good. No significant defects were noted in the external or internal portions of the package. No cracks or chips were noted in the ceramic or glass frit seal.
- Leadframe: The leadframe was constructed of iron-nickel. No voids or cracks were noted at lead exits.
- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present. A silver-filled glass was used to attach the die to the header. Rolled aluminum due to the sawing was present in the scribe lane. This could shake loose in some cases and possibly cause a short to occur.
- Wirebonding was by the ultrasonic wedge bond method using 1.3 mil O.D. aluminum wire. The clearance of the wires from the edge of the die was minimal due to the backward bonding technique used. Most bond pull strengths were normal; however, seven bond lifts occurred on Sample 2 out of the 24 wires tested, and two bond lifts occurred on Sample 3 out of 24 wires tested. The bonds lifted at an average force of 3.5 grams. A cavity bonding post was employed which biased the substrate to GND.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process:

Figures 8 - 28

Questionable Items:¹ None.

Special Features:

- Tungsten plugs used at all contacts.
- Titanium-silicided diffusions.

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: A layer of oxynitride over a layer of silicon-dioxide. As mentioned, the first layer (SiO₂) had been given a slight planarizing etch. Overlay integrity test indicated defect-free passivation. Edge seal was good.
- Metallization: A single layer of metal consisting of aluminum with a titanium-nitride barrier and a titanium adhesion layer. Tungsten plugs were used at all contacts.
- Metal patterning: The metal layer was patterned by a dry etch of normal quality. Alol contacts were completely surrounded by aluminum.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II (continued)

- Metal defects: No voiding, notching, or neckdown was noted in the metal layer. No silicon nodules were noted following the removal of the metal layer.
- Metal step coverage: Aluminum thinning did not exceed 40 percent due to the presence of the tungsten plugs. MIL-STD allows up to 70 percent metal thinning for contacts of this size.
- Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) over various densified oxides was used under the metal. Reflow was performed prior to contact cuts only. No problems were found.
- Contact defects: Contact cuts were defined by dry-etch process. Minor over-etching of the contacts was noted, but is not considered to be a problem.
- Polysilicon: Two layers of poly were used on the die. Polycide 2 (poly and titanium silicide) was used to form all gates on the die and the select/word lines in the EPROM cell array. Poly 1 (no silicide) was used exclusively in the cell to form the floating gates. Direct poly-to-diffusion (buried) contacts were not used. Interpoly dielectric consisted of oxide only. Definition was by a dry etch of normal quality.
- Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. Titanium silicide was present over all diffusions (salicide process).
- Local oxide (LOCOS) isolation was used. No problems were noted. The slight step present in the oxide at the well boundary indicates a twin-well process was employed.
- EPROM: Memory cell consisted of a stacked poly EPROM design. Metal was used to form the bit lines. Poly 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates. Interpoly dielectric consisted of oxide only. Cell pitch was 2.2 x 2.3 microns.
- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Delid

Internal optical inspection

SEM of passivation and assembly features

Passivation integrity test

Wirepull test

Passivation removal

SEM inspection of metal

Metal removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	NP*
Die attach quality	N
Dicing quality	N
Die attach method	Silver-filled glass
Dicing method	Sawn
Wirebond method	Ultrasonic wedge bonds using 1.3 mil aluminum wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Contact coverage	G
Contact registration	G

**Bond lifts on Samples 2 and 3.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS (TOP)

ATMEL LOGO
AT27C512R
20DMA
9619

(BOTTOM)

5DO314-18704C
1 PHILIPPINES - F
5D9601

WIREBOND STRENGTH

Wire material: 1.3 mil O.D. aluminum
Die pad material: aluminum

<u>Sample #</u>	2	3
# of wires pulled:	24	24
Bond lifts:	7	2
Force to break - high:	6g	6g
- low:	3g	2.5g
- avg.:	4.3g	4.1g
- std. dev.:	0.8	1.1

DIE MATERIAL ANALYSIS

Overlay passivation: A layer of oxynitride over a layer of silicon dioxide.

Metallization: Aluminum (Al) with a titanium-nitride (TiN) barrier and a titanium adhesion layer.

Polycide 2: Titanium (Ti) silicide.

Salicide: Titanium (Ti) silicide.

Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) containing 3.5 wt. % phosphorus and 3.0 wt. % boron over various densified oxides.

HORIZONTAL DIMENSIONS

Die size:	3.4 x 3.2 mm (133 x 125 mils)
Die area:	10.9 mm ² (16,625 mils ²)
Min pad size:	0.11 x 0.13 mm (4.5 x 5.0 mils)
Min pad window:	0.1 x 0.11 mm (3.8 x 4.5 mils)
Min pad space:	18 microns
Min metal width:	1.3 micron
Min metal space:	1.1 micron
Min metal pitch:	2.4 microns
Min contact:	0.8 micron
Min poly 2 width:	0.55 micron
Min poly 2 space:	0.6 micron
Min gate length - (N-channel):*	1.1 micron (peripheral circuits)
- (P-channel):*	1.55 micron
N-channel gate length in array:	0.7 micron
Cell size:	5 microns ²
Cell pitch:	2.2 x 2.3 microns

*Physical gate length.

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (19 mils)
----------------	------------------

Layers:

Passivation 2:	1.0 micron
Passivation 1:	0.35 micron
Metal - aluminum:	0.8 micron
- barrier:	0.05 micron (approximate)
Pre-metal dielectric:	0.4 - 0.95 micron
Oxide on poly 2:	0.1 micron
Poly 2 - silicide:	0.05 micron (approximate)
- poly:	0.25 micron
Interpoly dielectric:	0.05 micron (approximate)
Poly 1:	0.15 micron
Local oxide:	0.35 micron
N+ S/D:	0.25 micron
P + S/D:	0.3 micron
N-well:	4.5 microns (approximate)
P-well:	Could not delineate

HORIZONTAL DIMENSIONS

Die size:	3.4 x 3.2 mm (133 x 125 mils)
Die area:	10.9 mm ² (16,625 mils ²)
Min pad size:	0.11 x 0.13 mm (4.5 x 5.0 mils)
Min pad window:	0.1 x 0.11 mm (3.8 x 4.5 mils)
Min pad space:	18 microns
Min metal width:	1.3 micron
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Min metal pitch:	2.4 microns
Min contact:	0.8 micron
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Min gate length - (N-channel):*	1.1 micron (peripheral circuits)
- (P-channel):*	1.55 micron
N-channel gate length in array:	0.7 micron
Cell size:	5 microns ²
Cell pitch:	2.2 x 2.3 microns

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (19 mils)
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Passivation 2:	1.0 micron
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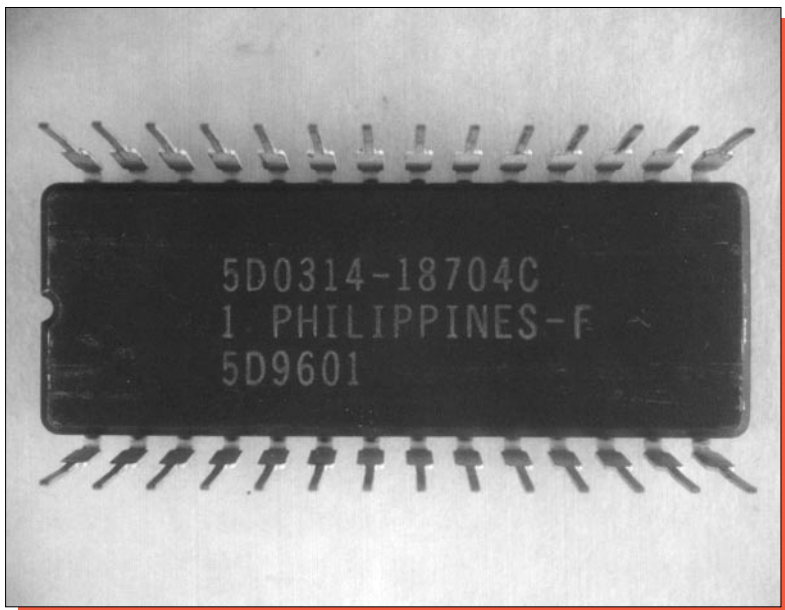
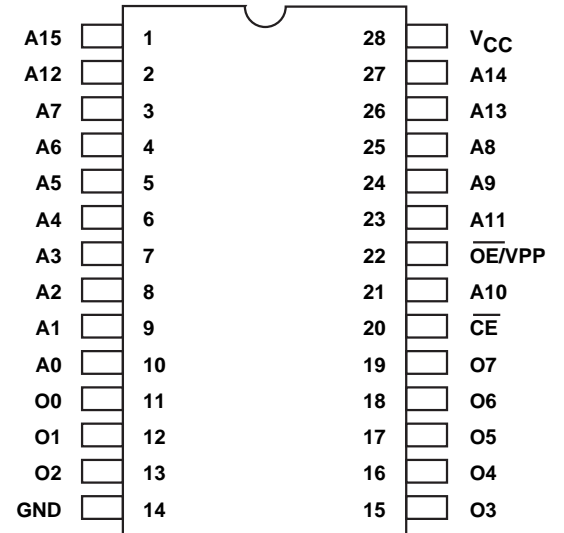
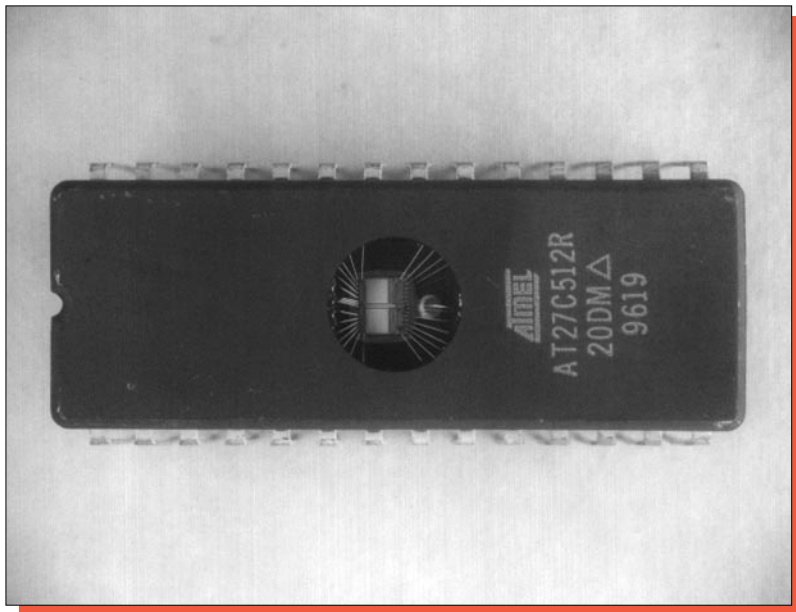


Figure 1. Package photographs and pinout of the Atmel AT27C512R. Mag. 2.5x.

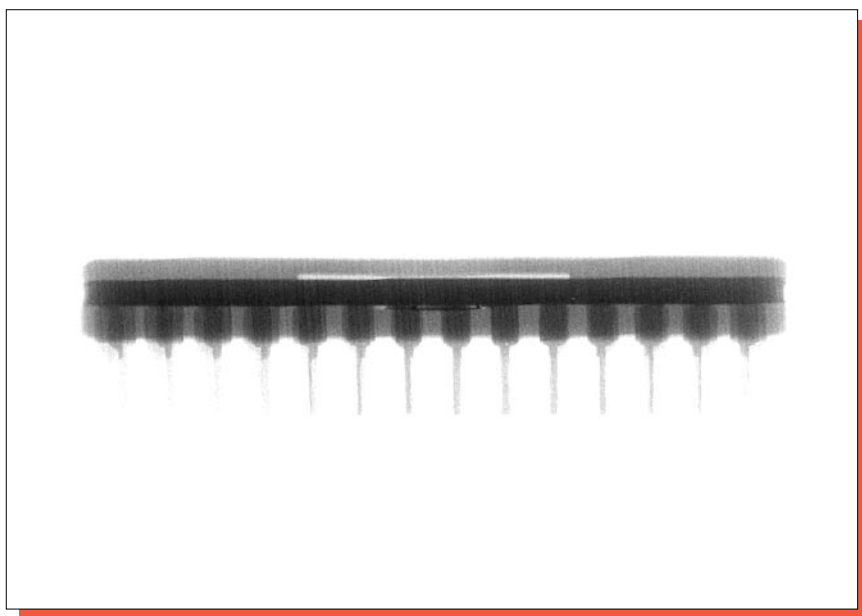
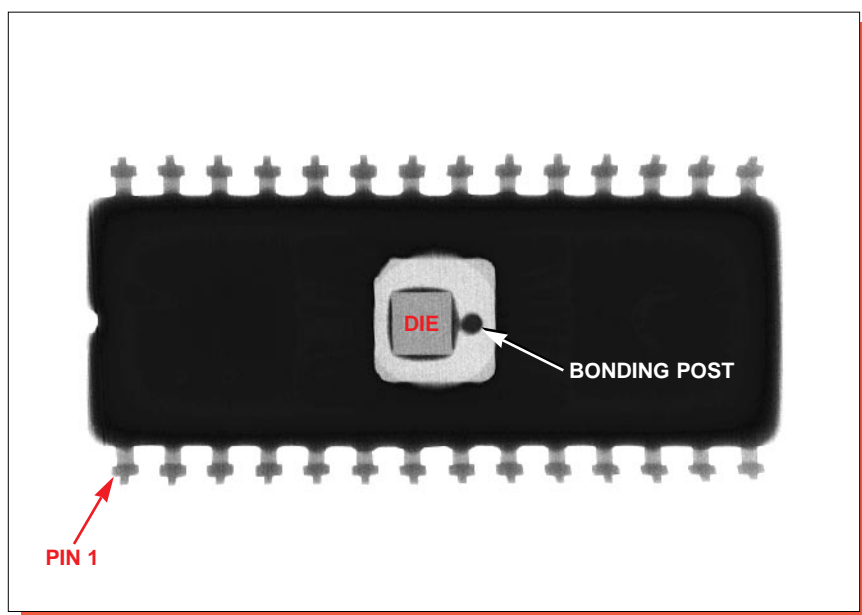
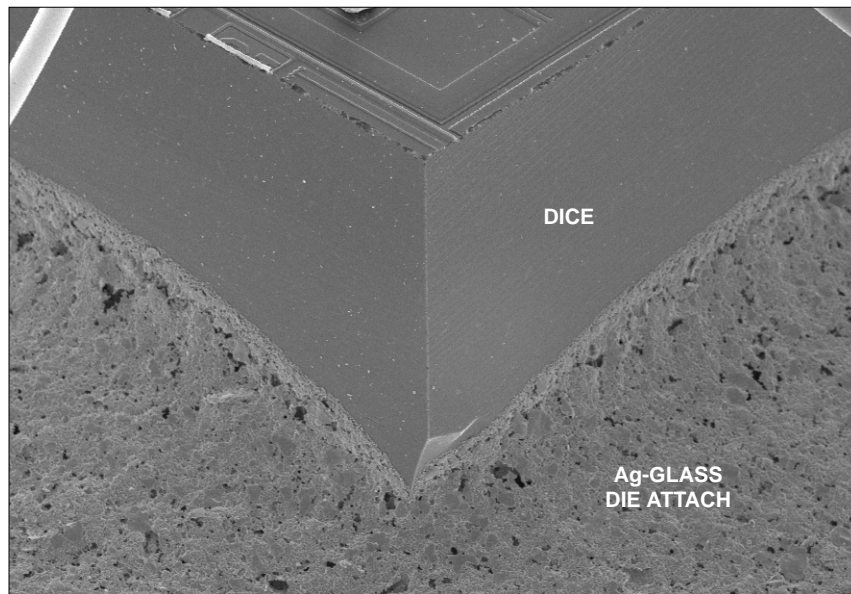
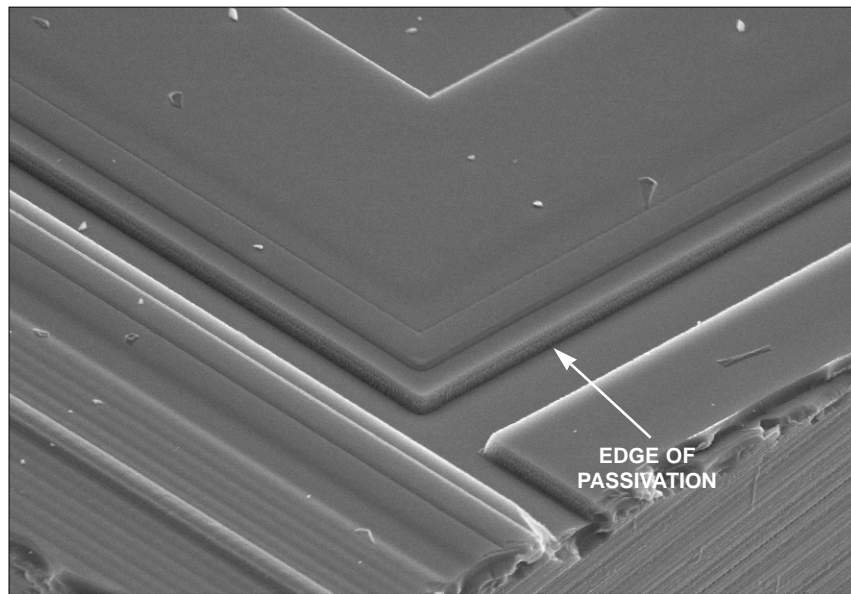


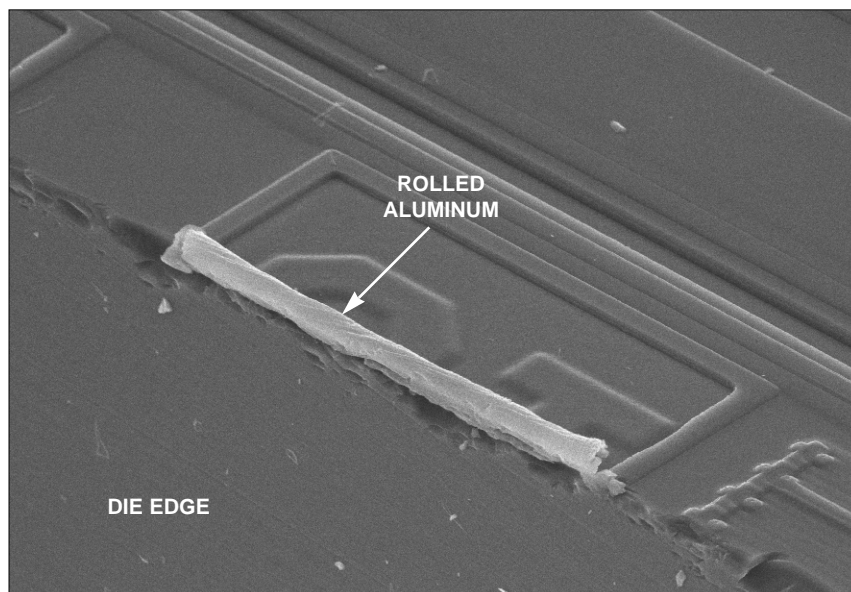
Figure 2. X-ray views of the package. Mag. 2.5x.



Mag. 130x

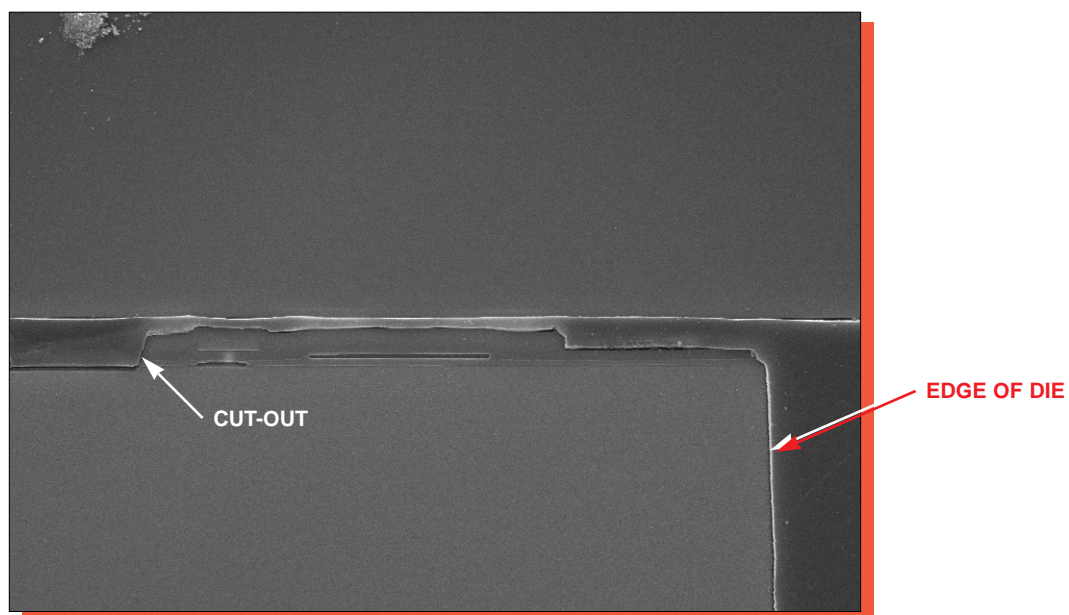


Mag. 1100x

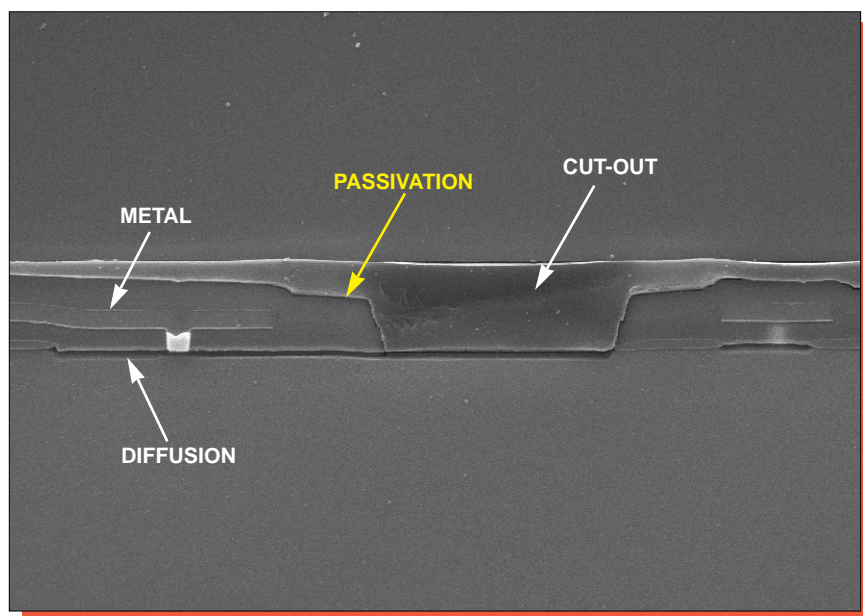


Mag. 810x

Figure 3. Perspective SEM views of dicing, die attach, and edge seal. 60°.

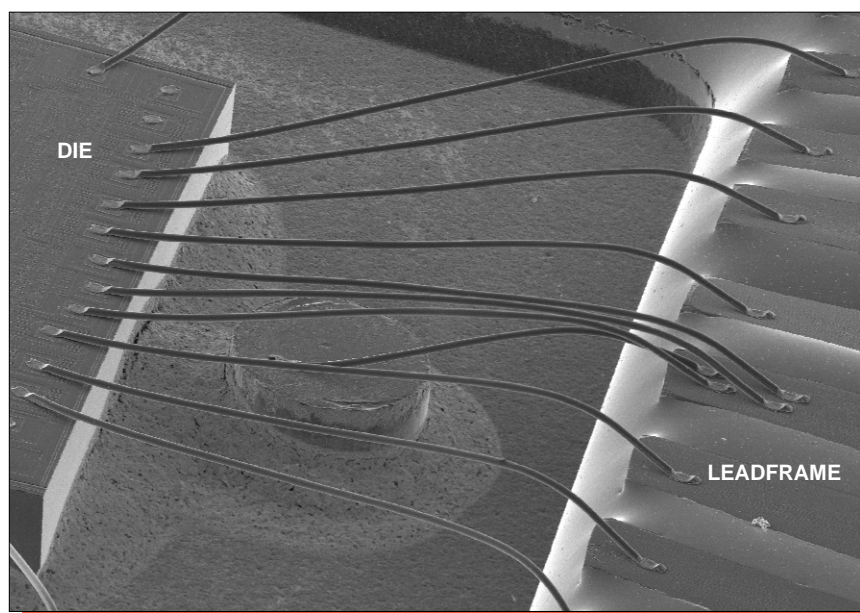


Mag. 1600x

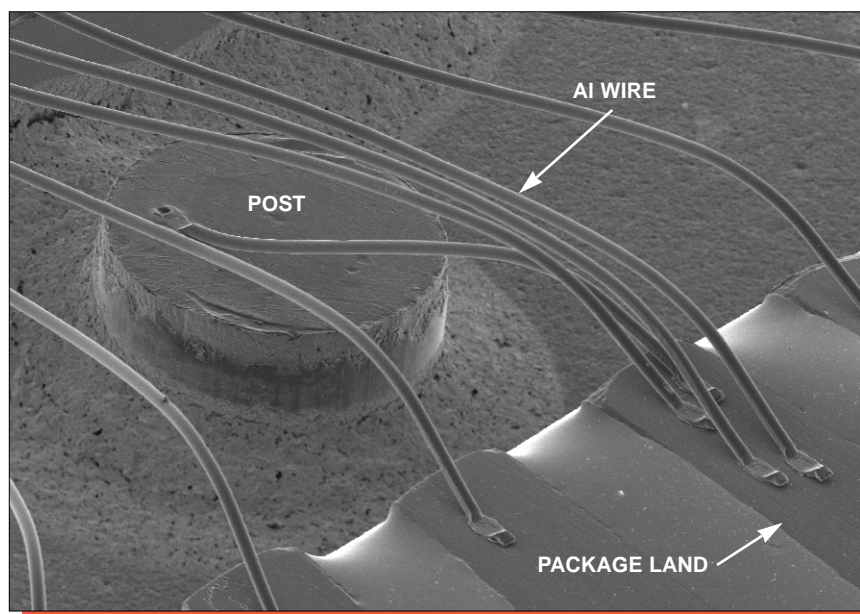


Mag. 3100x

Figure 4. SEM section views of the edge seal.



Mag. 30x



Mag. 55x

Figure 5. SEM views illustrating backward wirebonding. 60°.

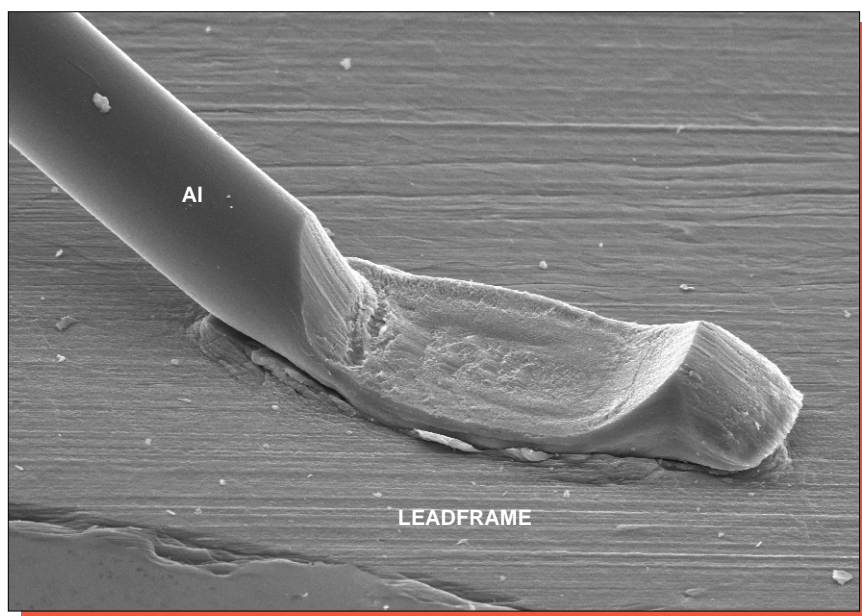
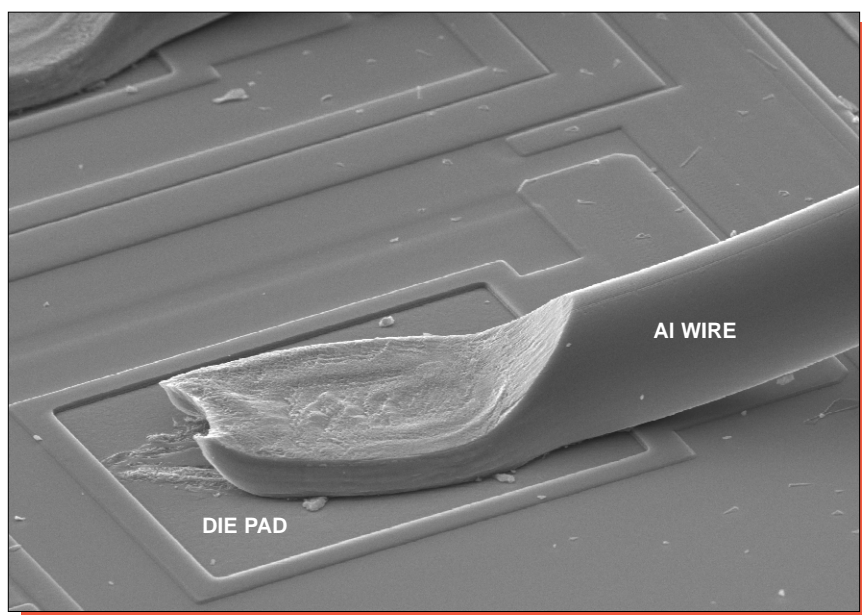
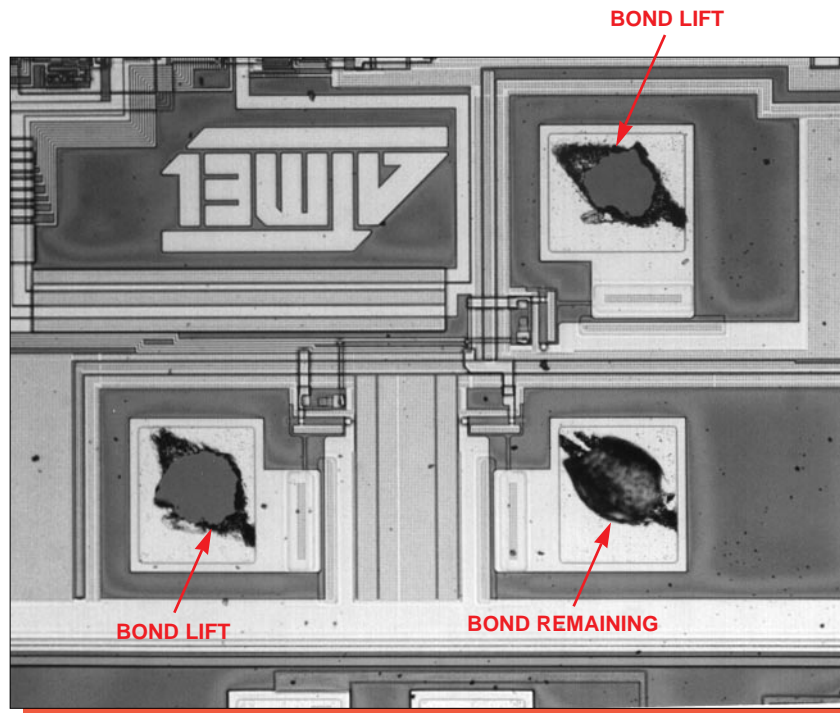
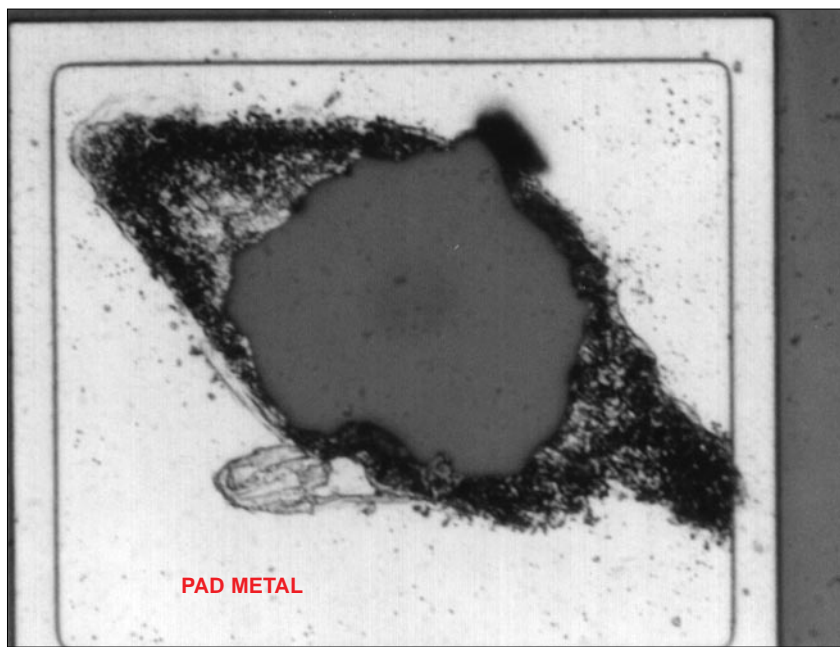


Figure 6. SEM views of typical wirebonds. Mag. 600x, 60°.



Mag. 160x



Mag. 800x

Figure 7. Optical views of bond lifts following wire pull test.

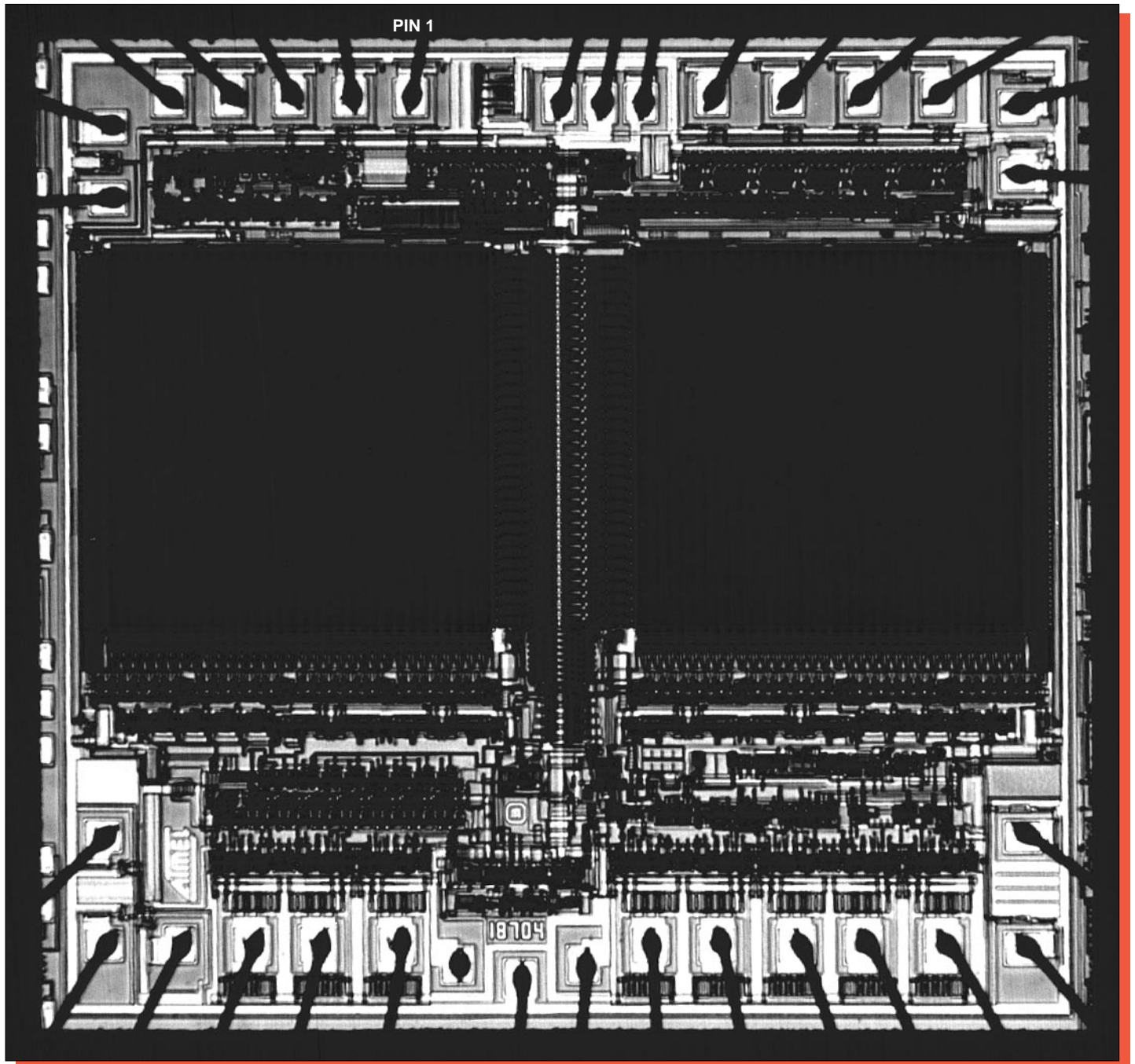
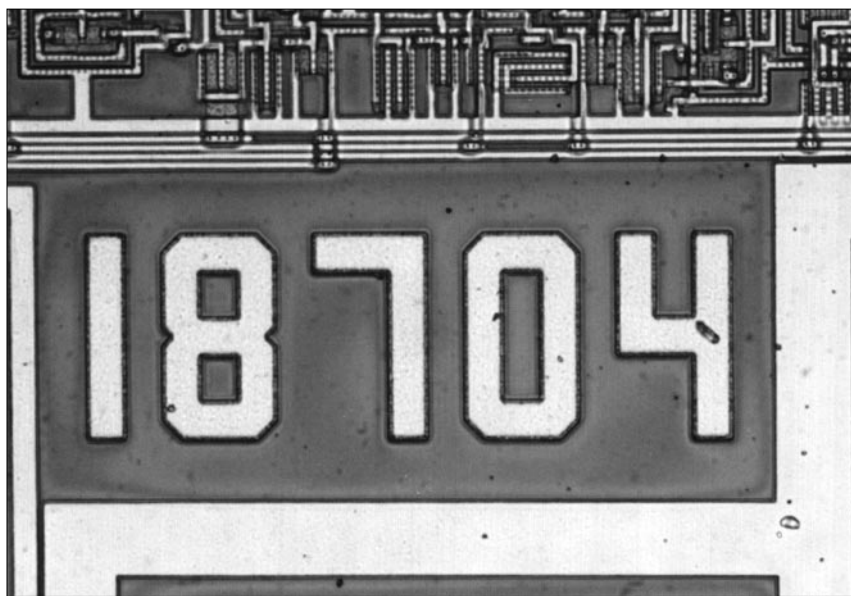


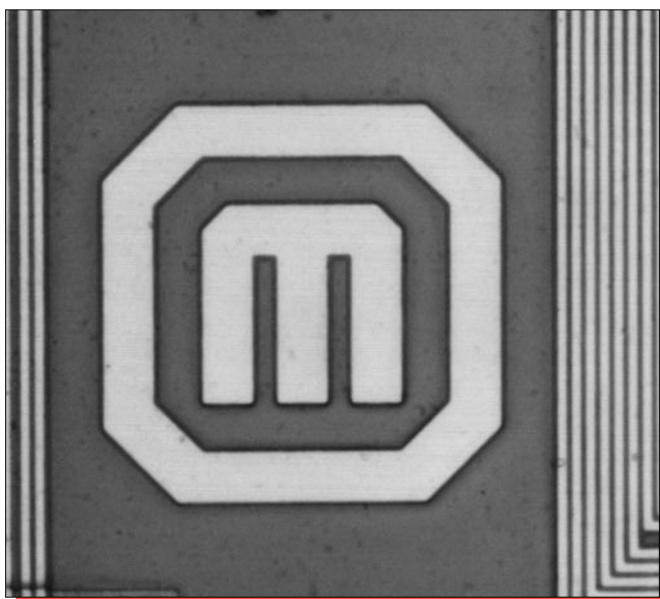
Figure 8. Whole die photograph of the Atmel AT27C512R. Mag. 54x.



Mag. 400x

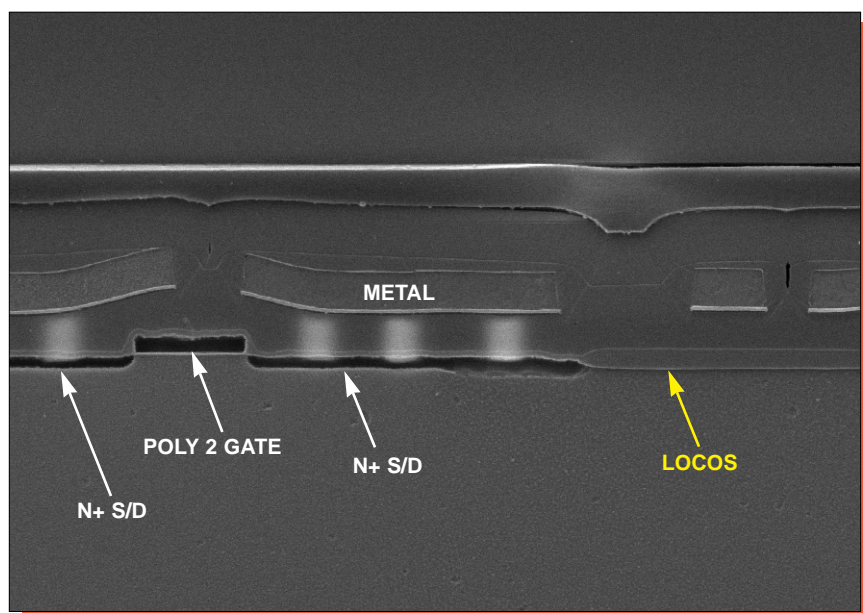


Mag. 500x

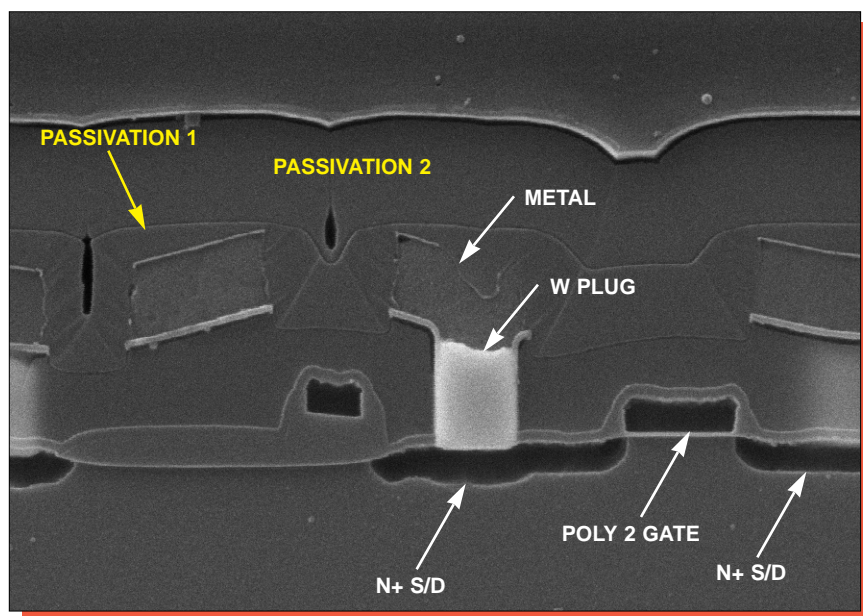


Mag. 800x

Figure 9. Optical views of markings on the die surface.

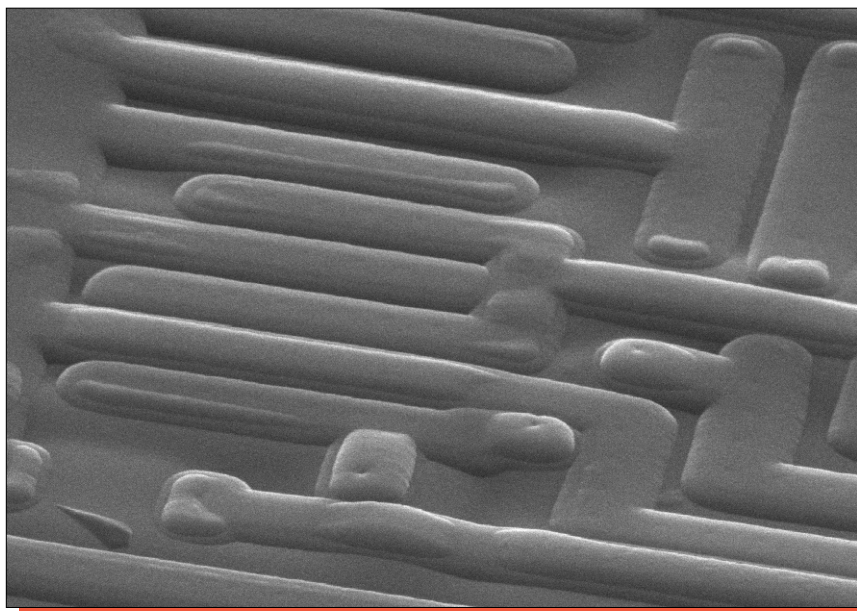


Mag. 6500x

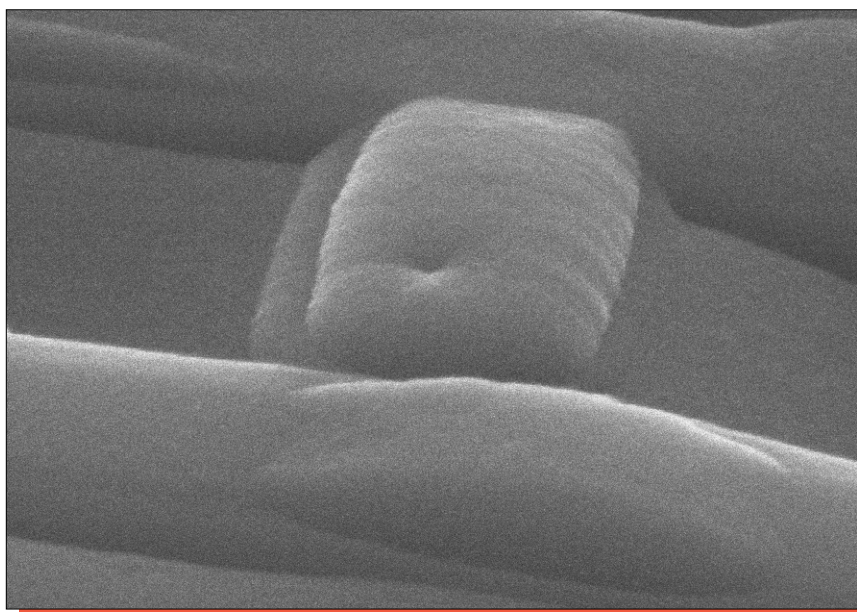


Mag. 13,000x

Figure 10. SEM section views of general construction.

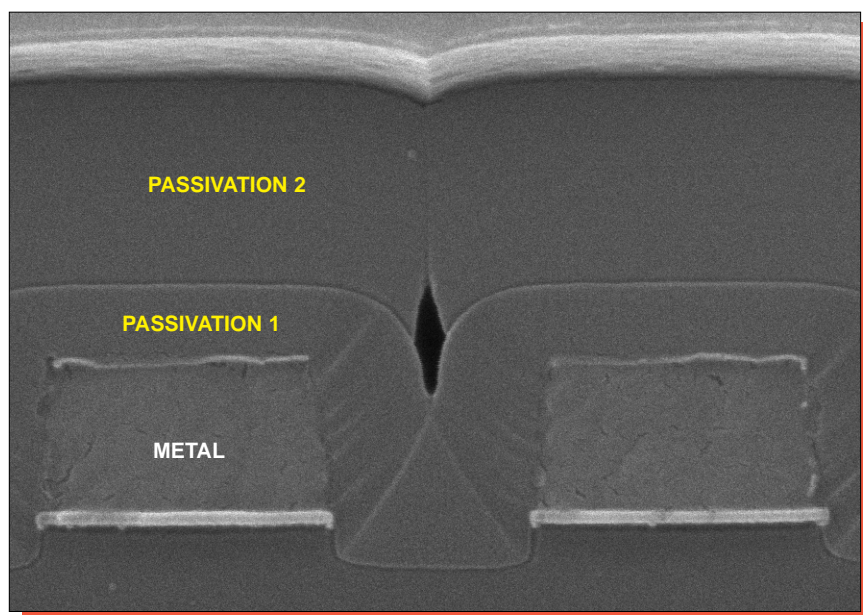


Mag. 4000x

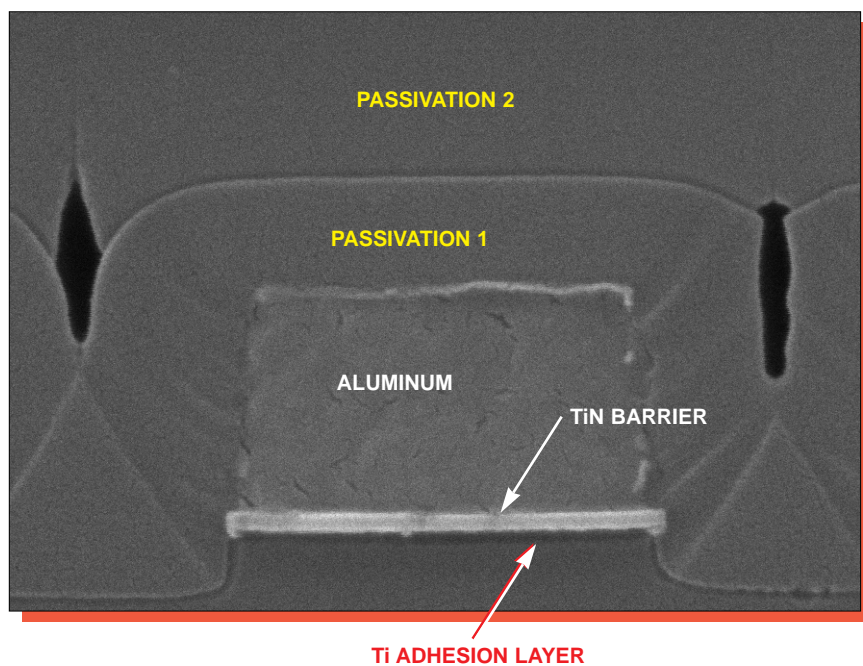


Mag. 15,000x

Figure 11. Perspective SEM views illustrating general overlay passivation coverage. 60°.



Mag. 26,000x



Mag. 40,000x

Figure 12. SEM section views of metal line profiles.

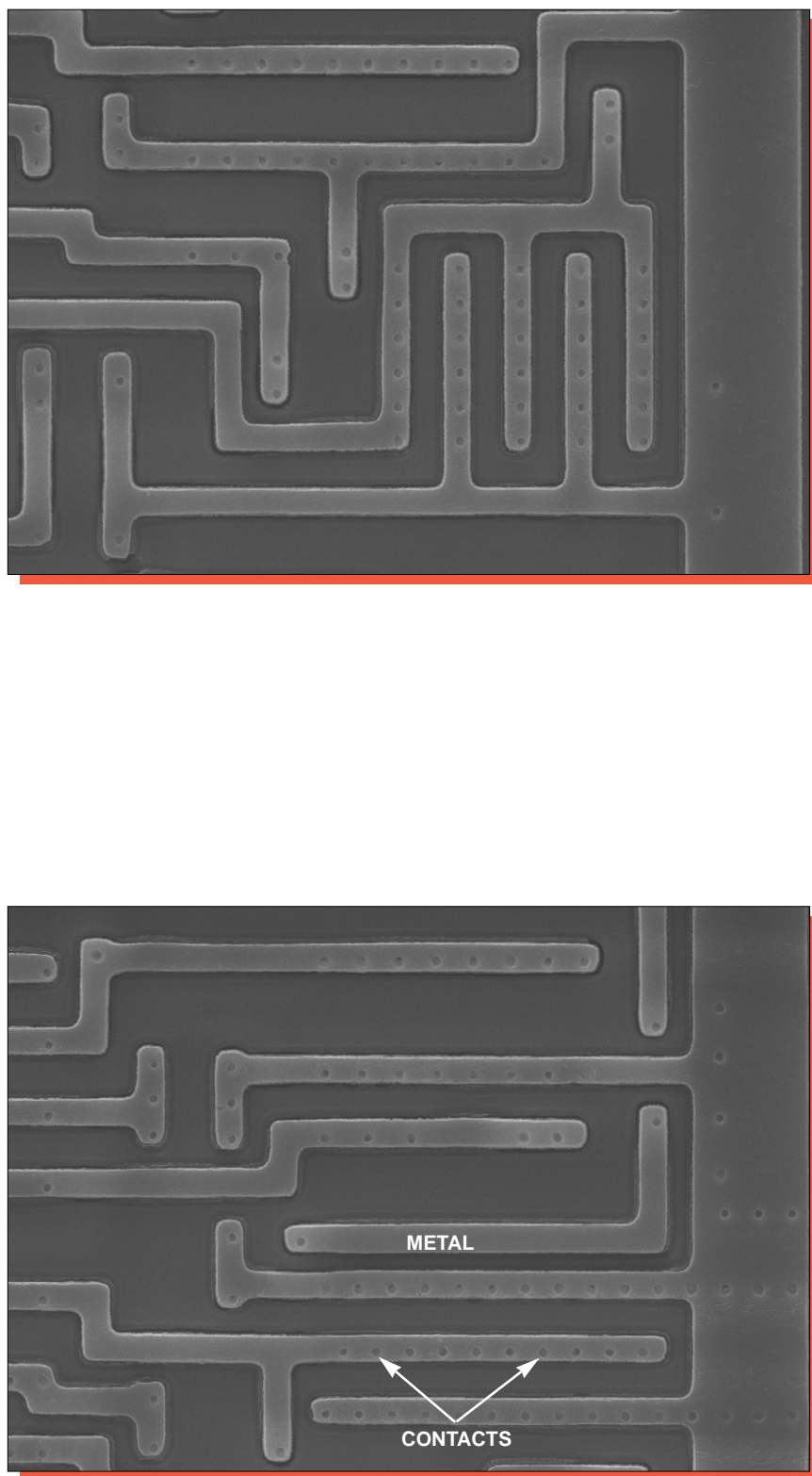
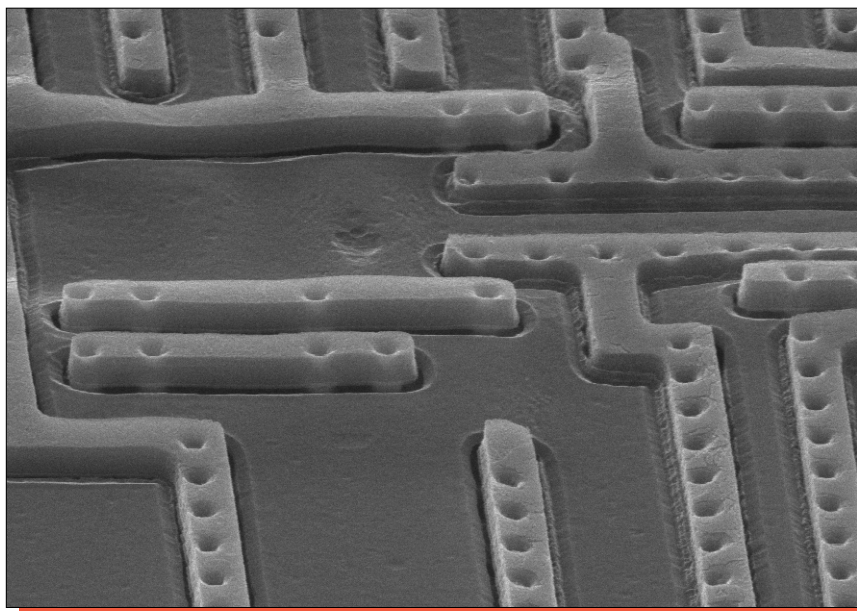
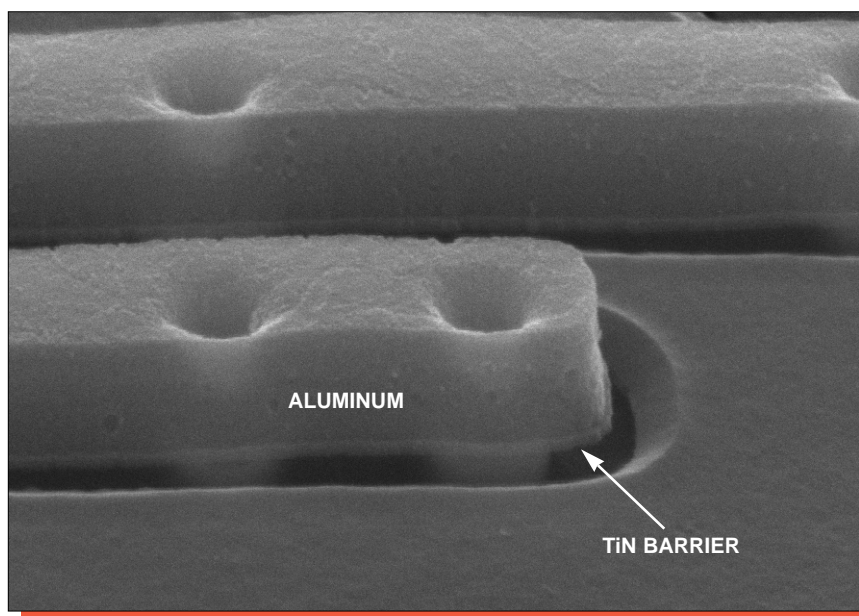


Figure 13. Topological SEM views illustrating metal patterning. Mag. 2800x, 0°.

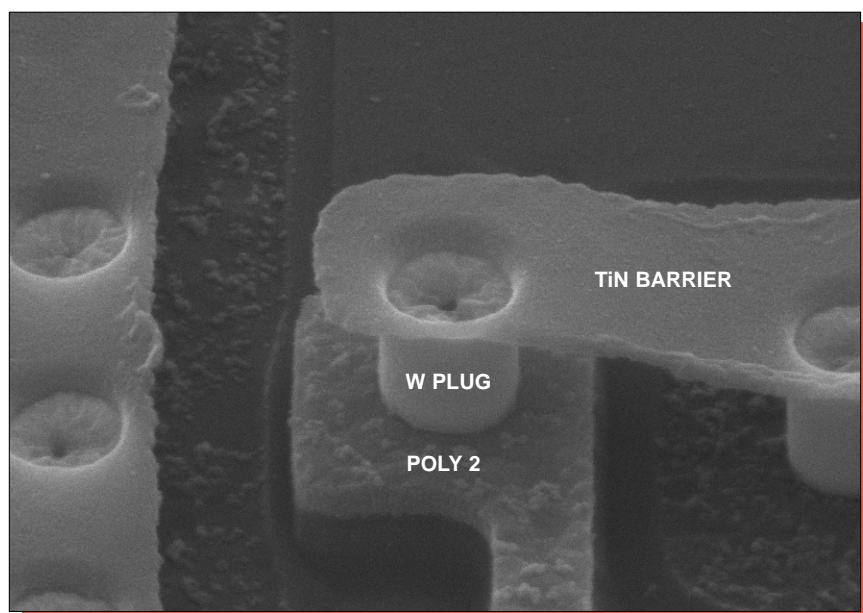


Mag. 5200x

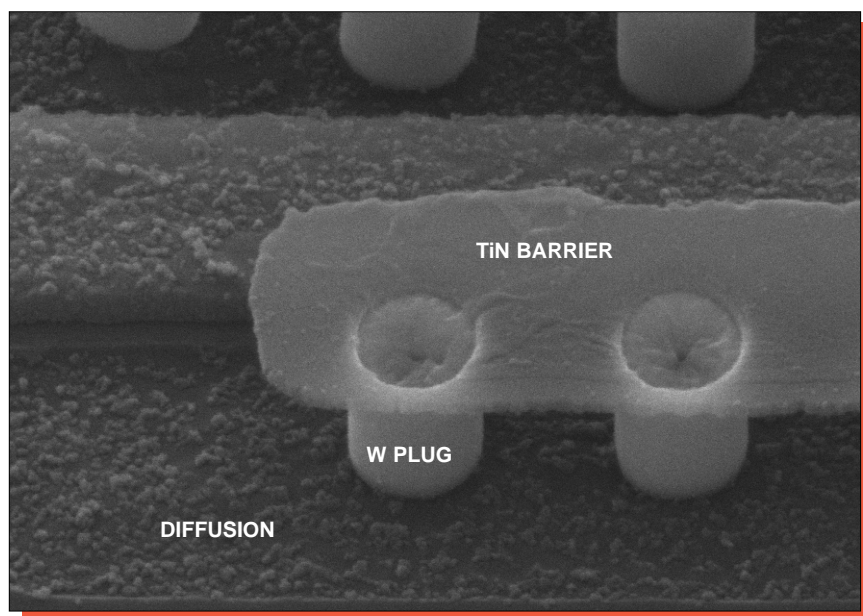


Mag. 21,000x

Figure 14. SEM views illustrating metal step coverage. 60°.

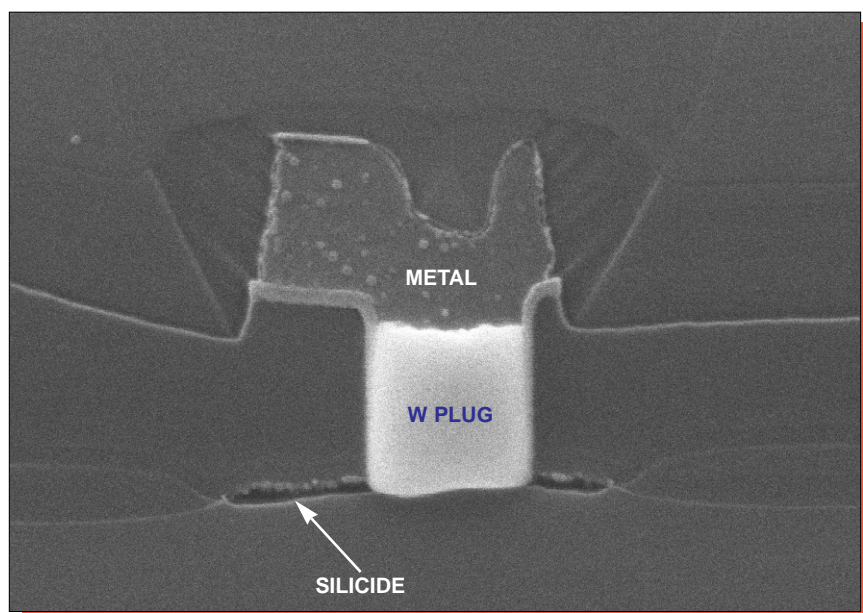


metal-to-poly

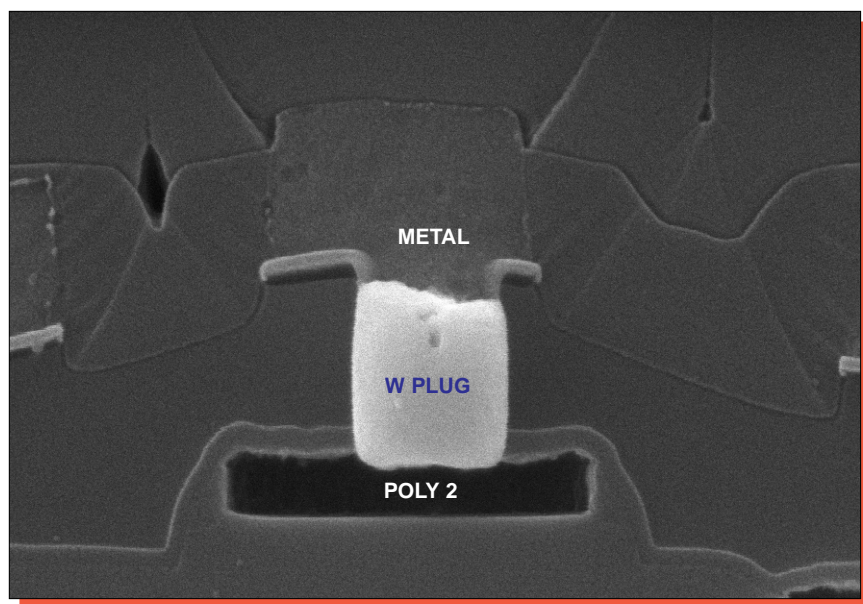


metal-to-diffusion

Figure 15. SEM views illustrating barrier following the removal of aluminum. Mag. 21,000x, 45°.

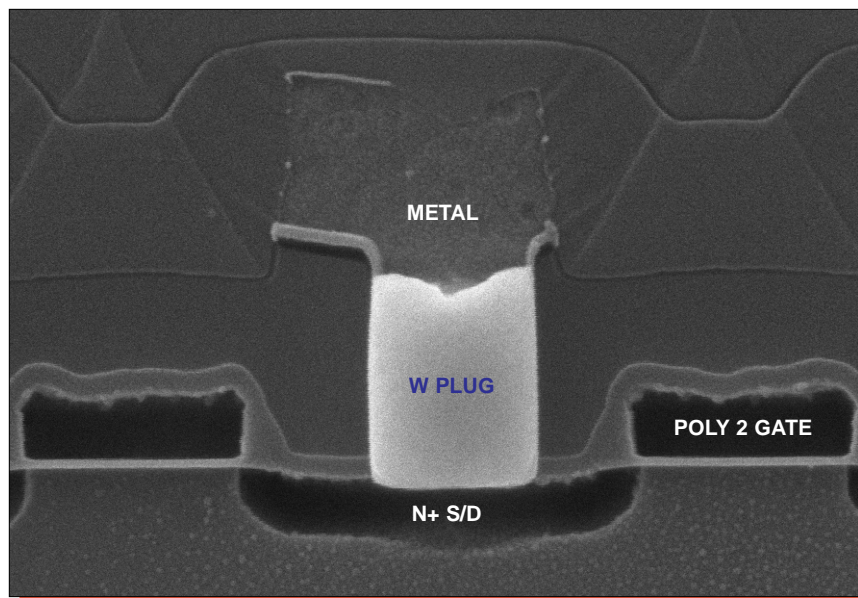


metal-to-diffusion, glass etch, Mag. 26,000x

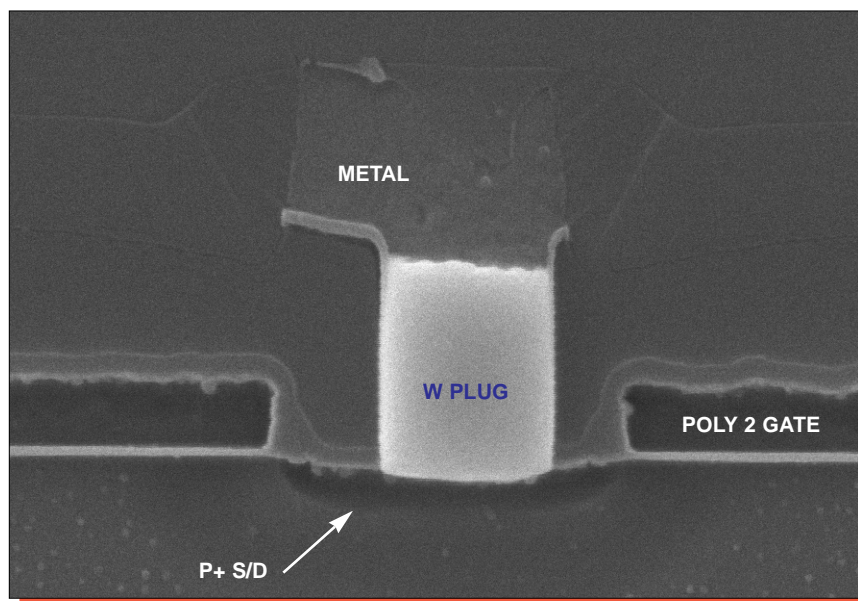


metal-to-poly 2, silicon etch, Mag. 26,000x

Figure 16. SEM section views of typical metal contacts.

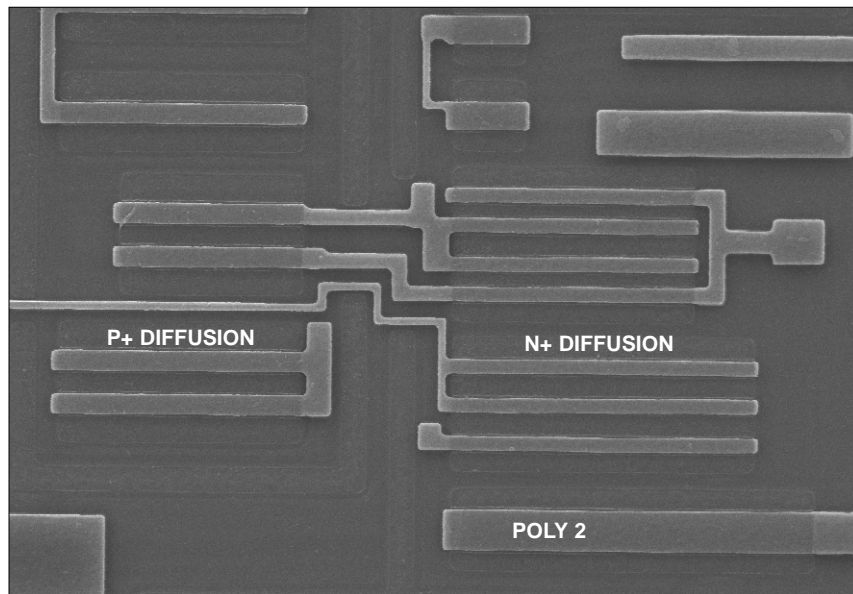


metal-to-N+

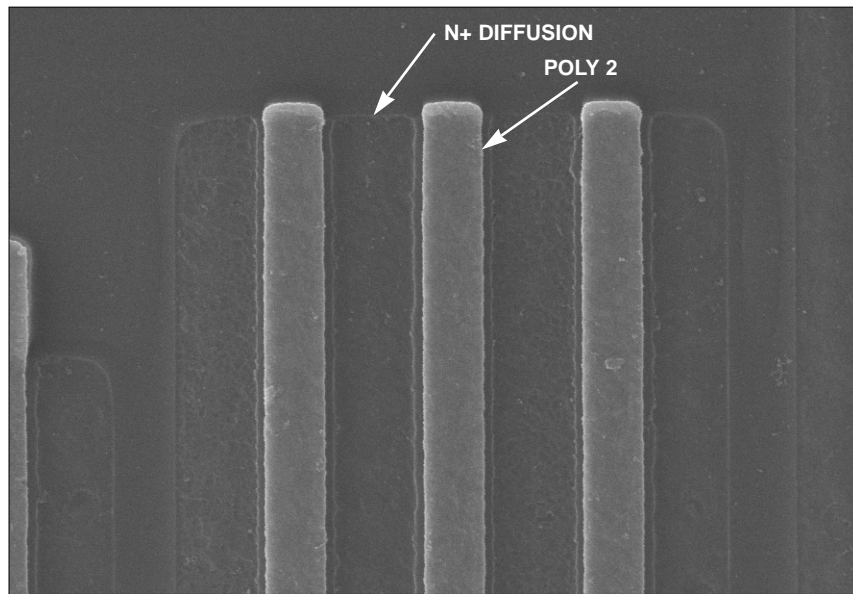


metal-to-P+

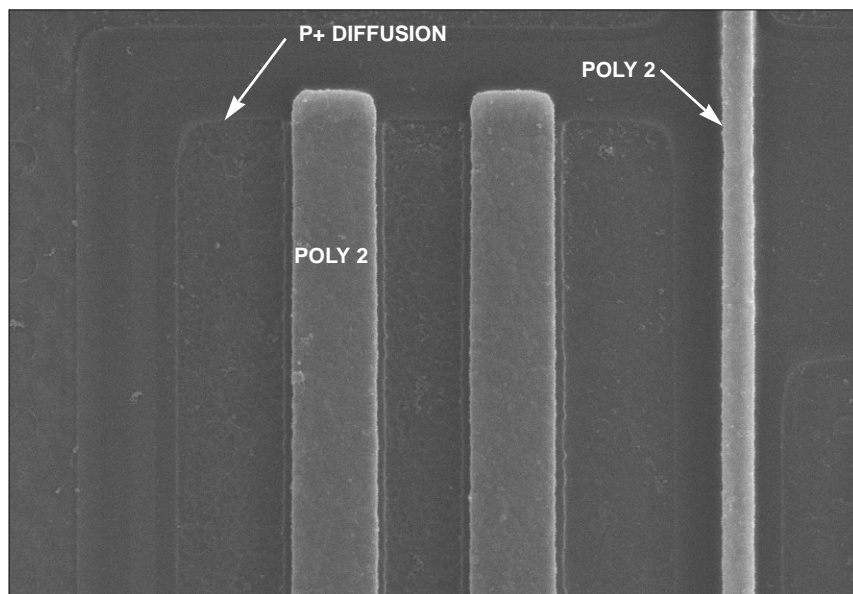
Figure 17. SEM section views of typical metal contacts. Mag. 26,000x.



Mag. 1600x

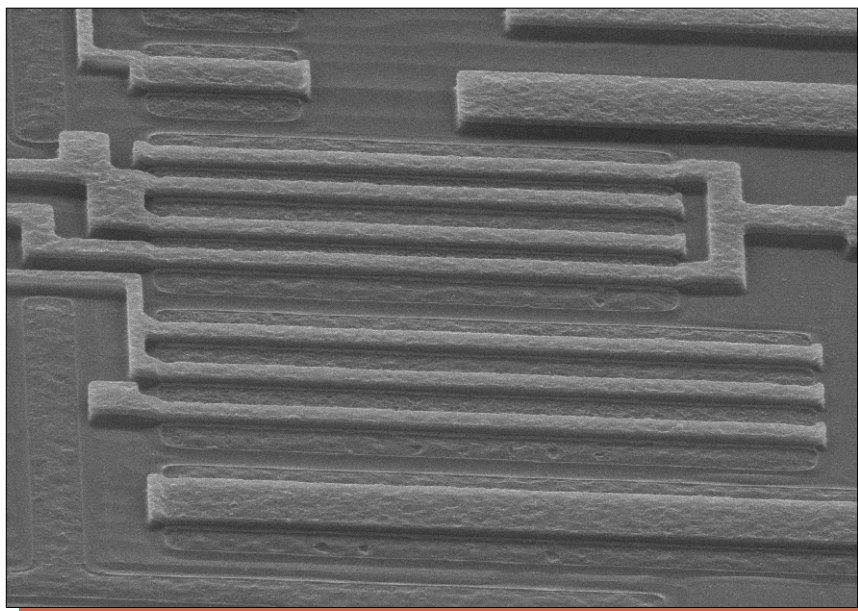


N-channel,
Mag. 6500x

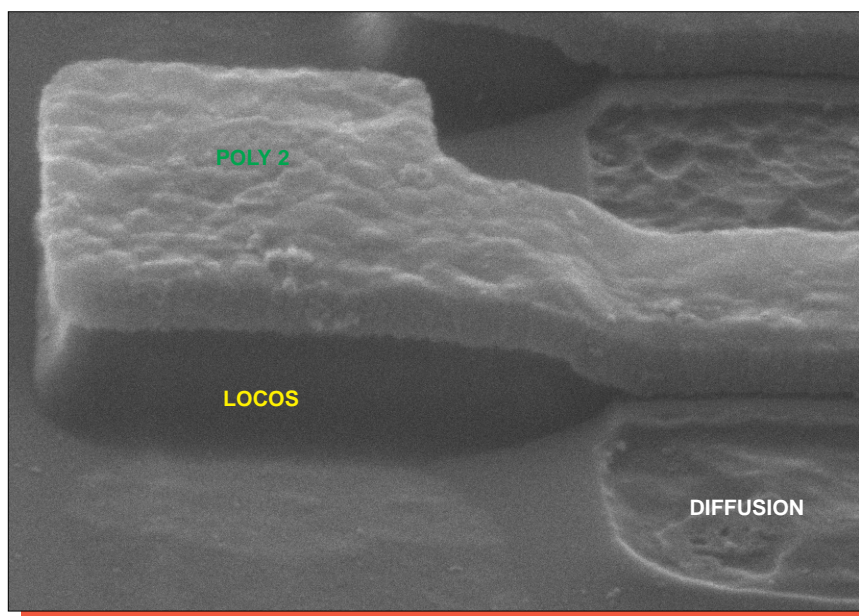


P-channel,
Mag. 6500x

Figure 18. Topological SEM views of poly 2 patterning. 0°.



Mag. 3600x



Mag. 30,000x

Figure 19. SEM views of poly 2 coverage. 60°.

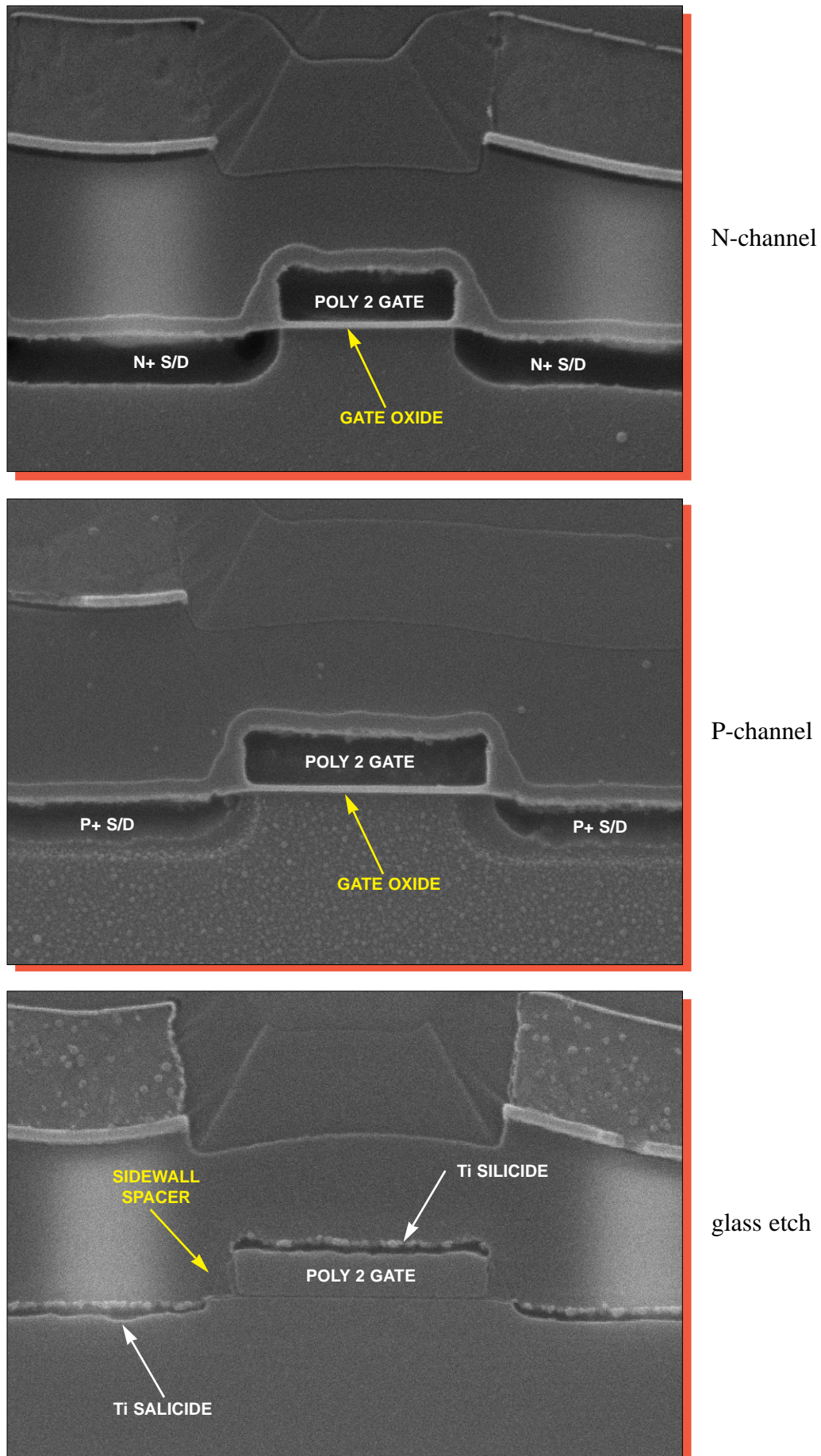


Figure 20. SEM section views of typical transistors. Mag. 26,000x.

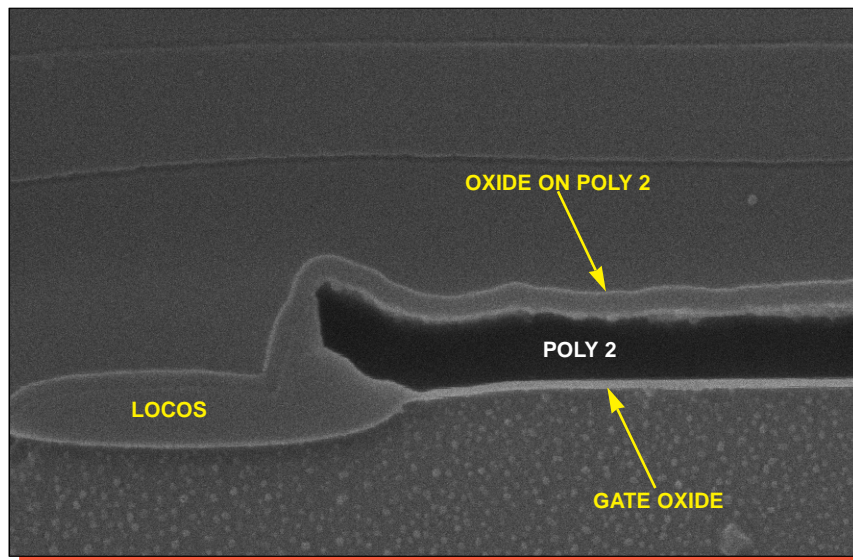
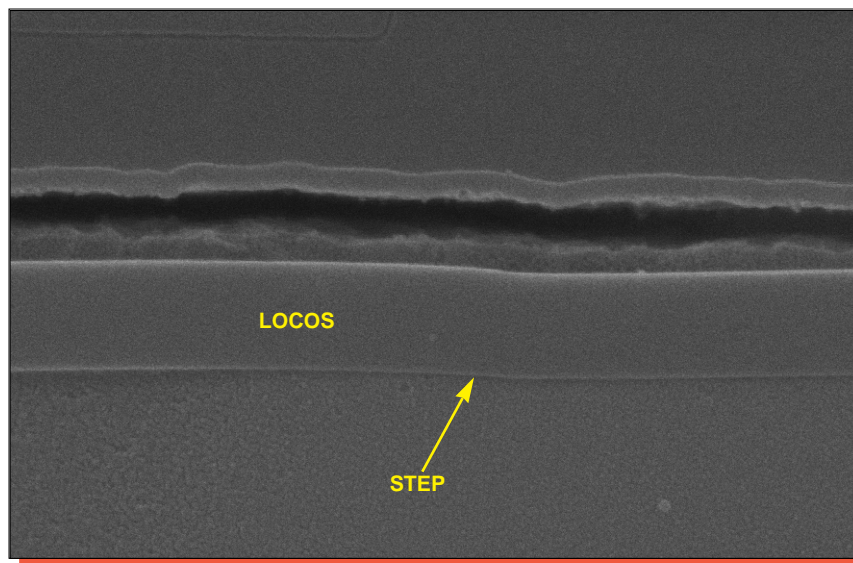
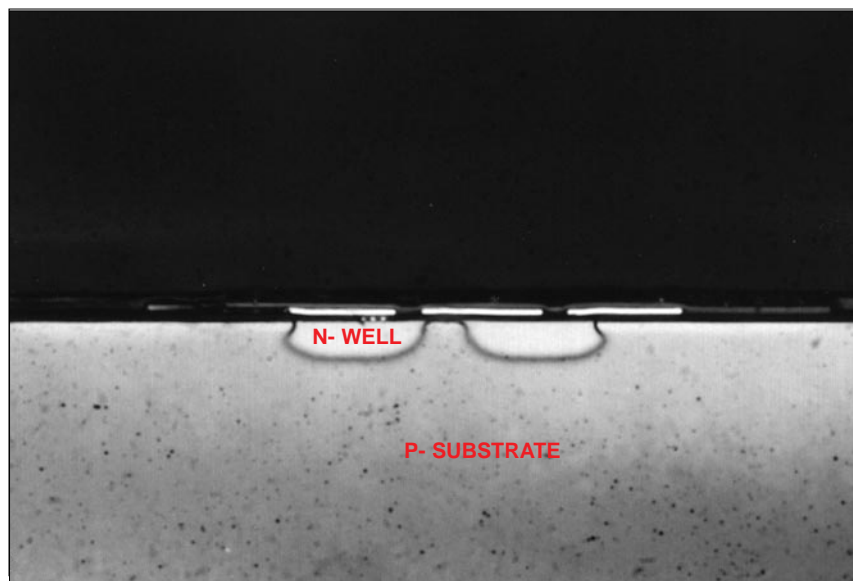


Figure 20a. SEM section view of a local oxide birdsbeak. Mag. 26,000x.



Mag. 26,000x



Mag. 800x

Figure 21. SEM section views of the well structure.

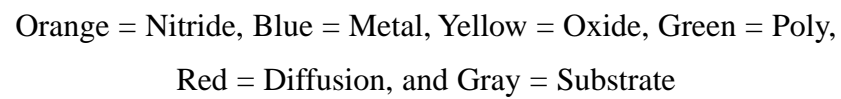
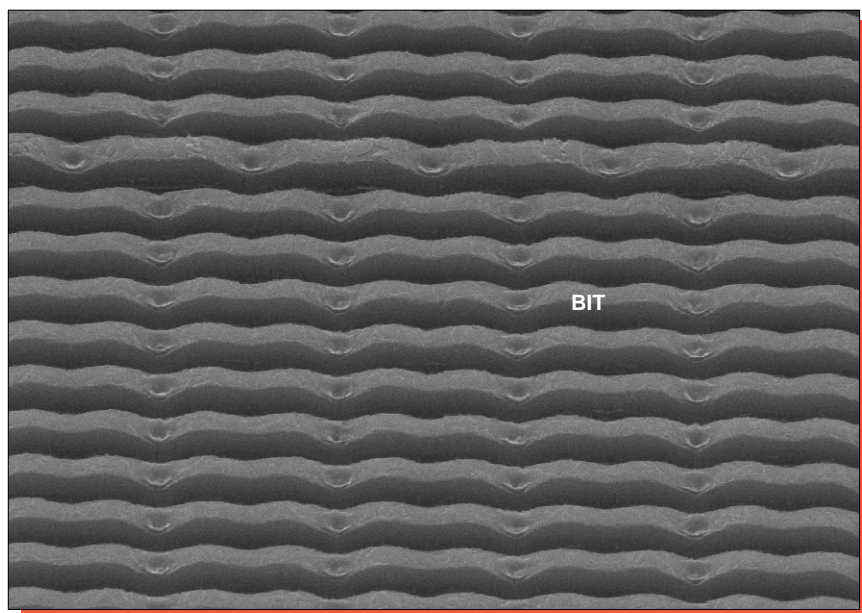
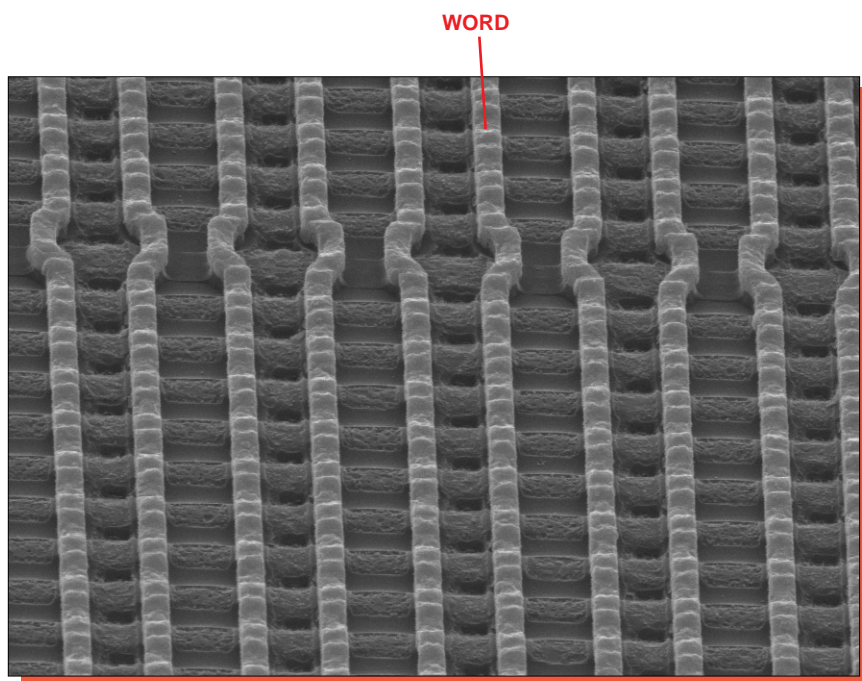


Figure 21a. Color cross section drawing illustrating device structure.

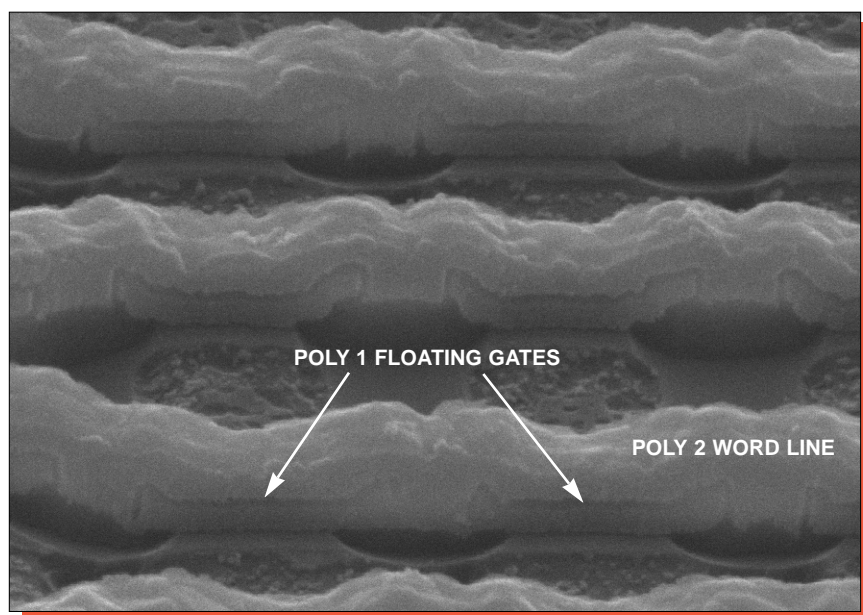


metal

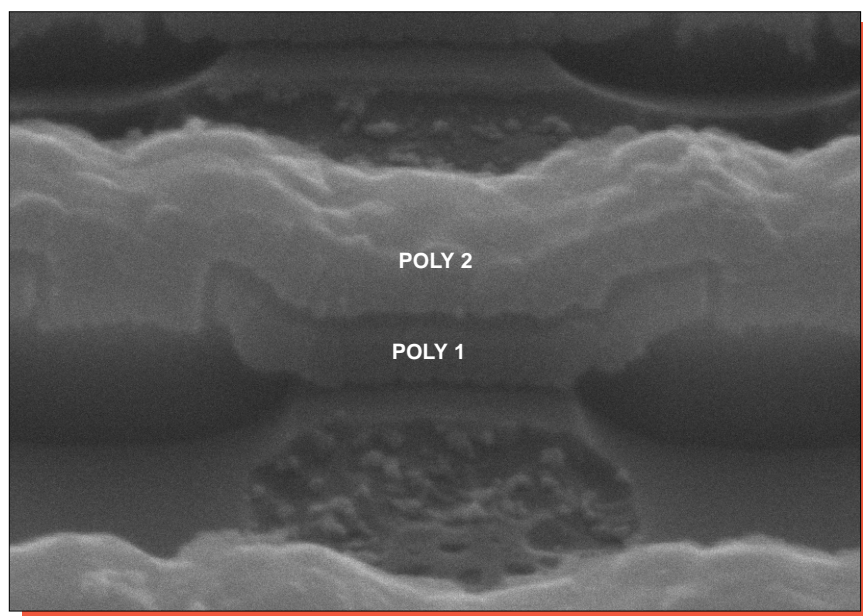


unlayered

Figure 22. Topological SEM views of EPROM cell array. Mag. 5200x, 60°.



Mag. 21,000x



Mag. 40,000x

Figure 22a. Topological SEM views of a single EPROM cell at the poly layer. 60°.

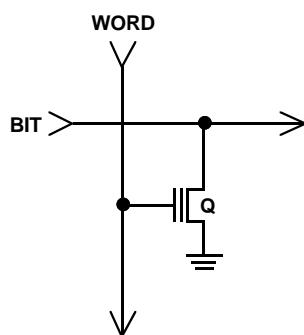
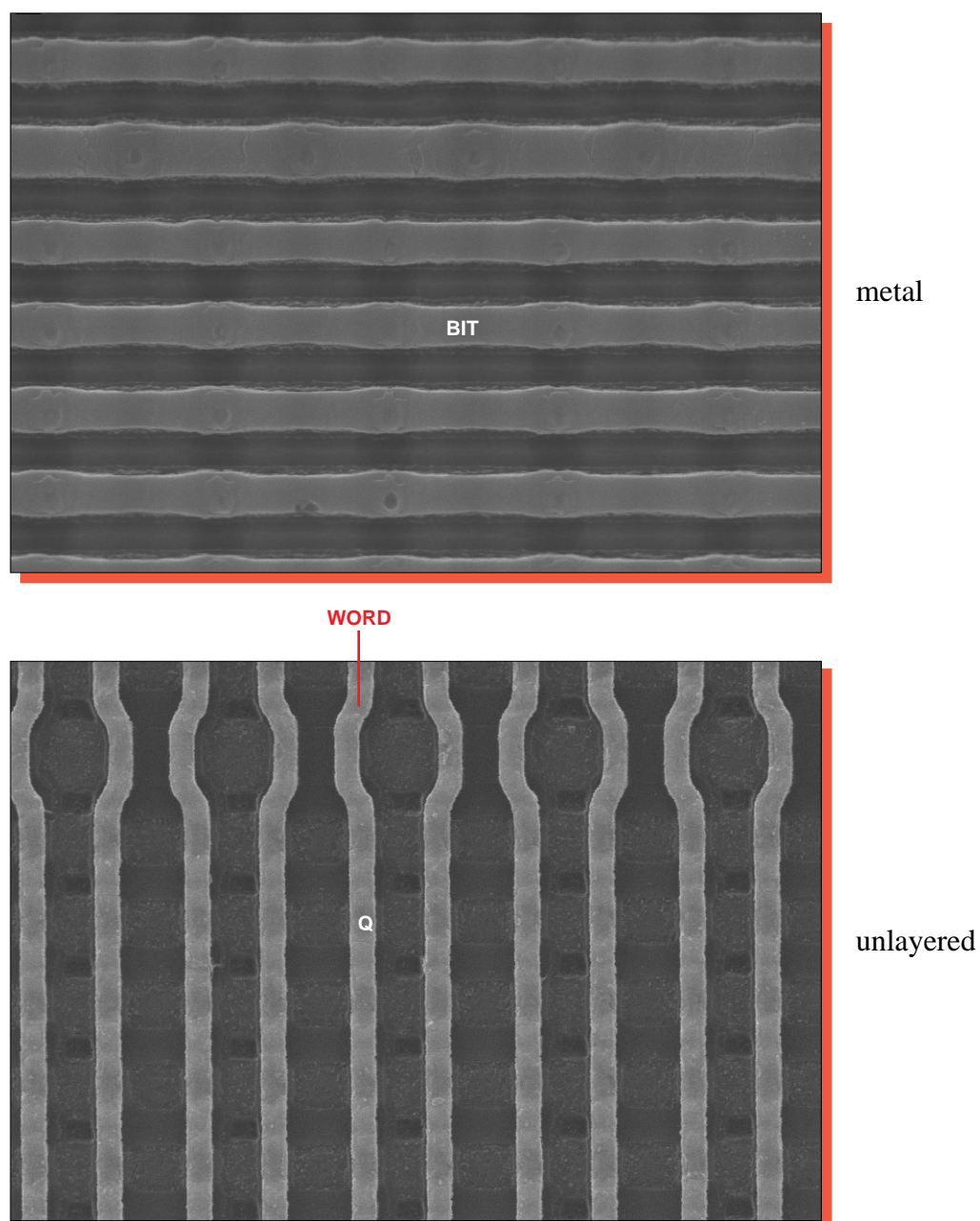
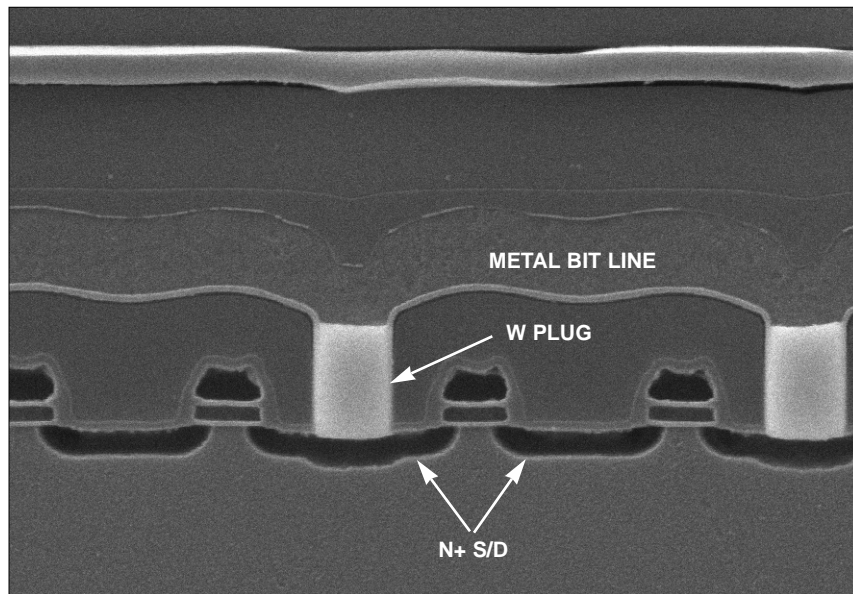
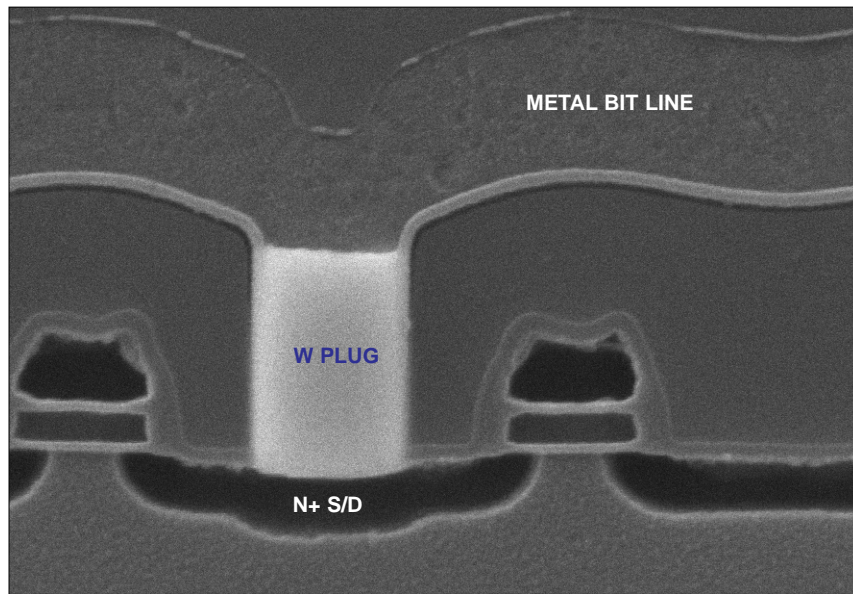


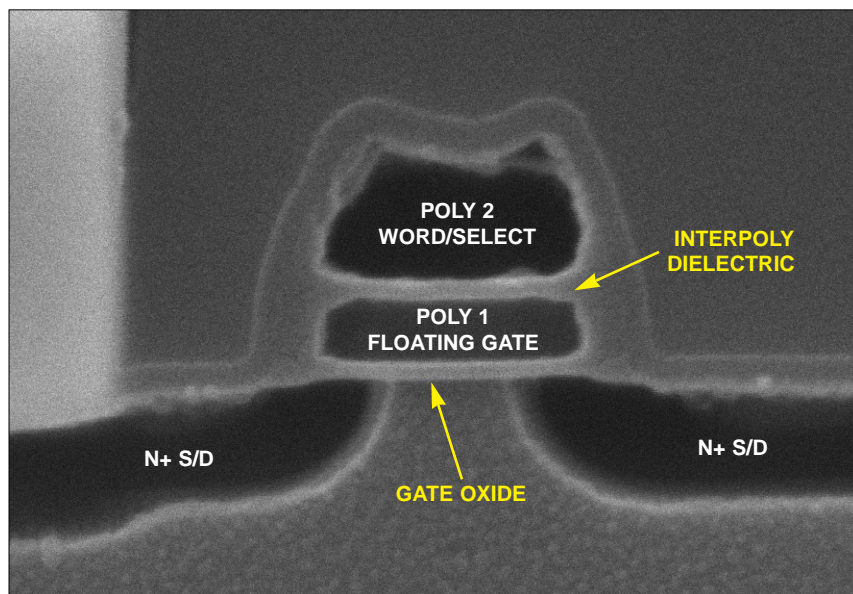
Figure 23. Topological SEM views and schematic of EPROM cell. Mag. 5200x, 0°.



Mag. 13,000x

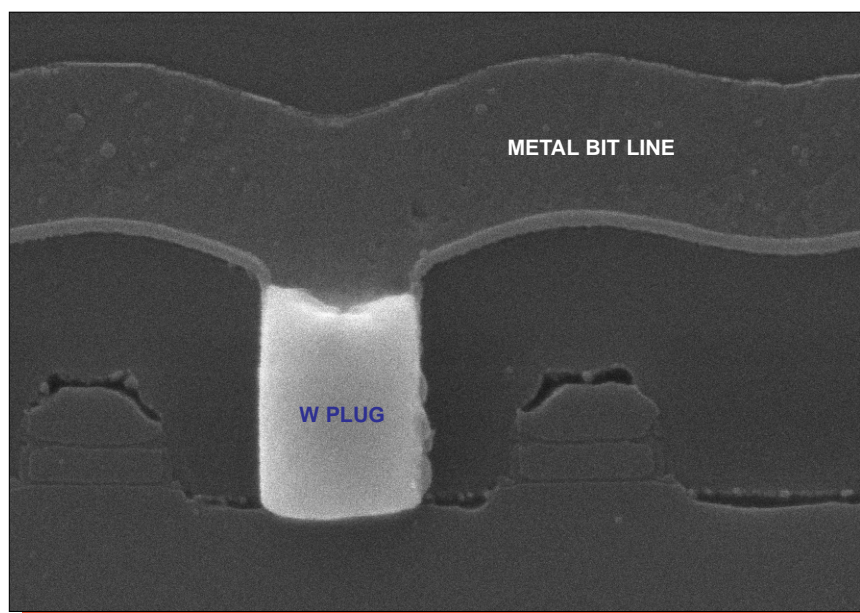


Mag. 26,000x

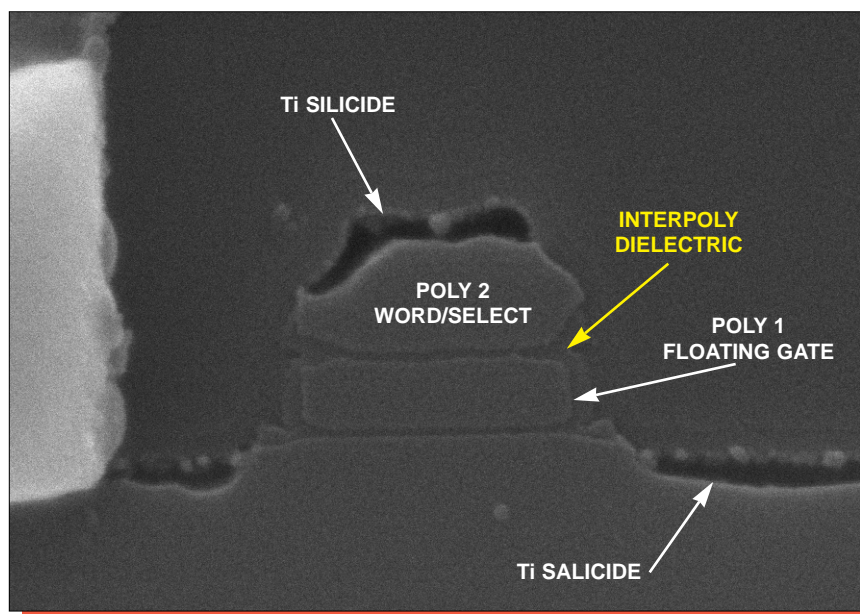


Mag. 52,000x

Figure 24. SEM section views of the EPROM cell (parallel to bit lines). Silicon etch.

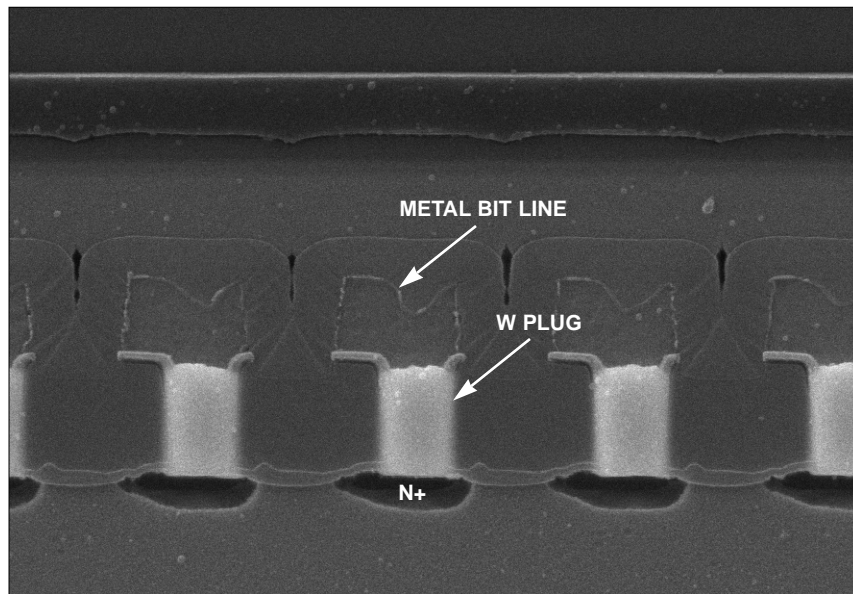


Mag. 26,000x

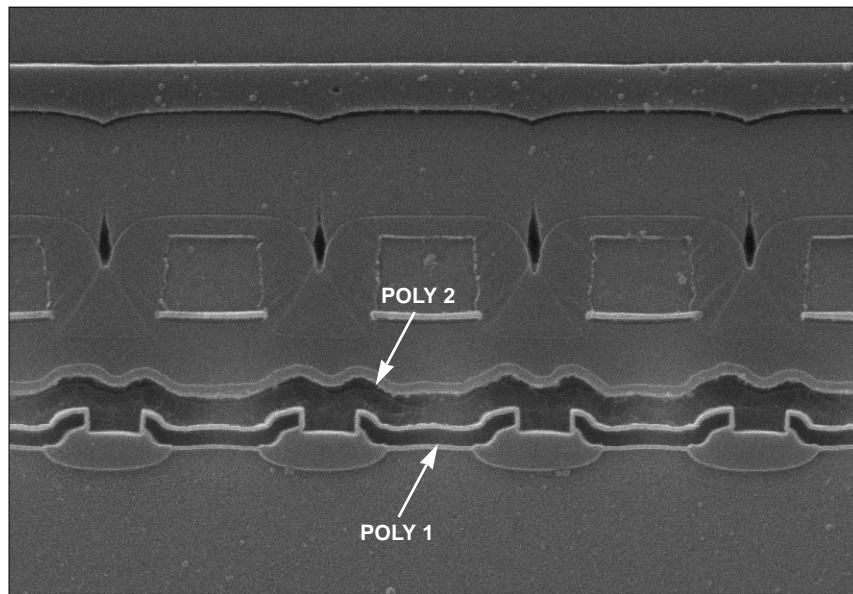


Mag. 52,000x

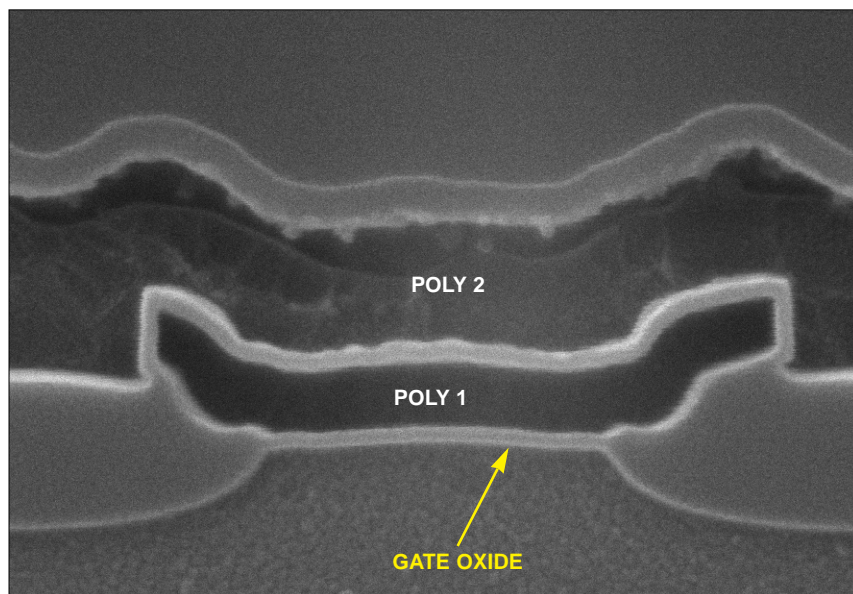
Figure 25. SEM section views of EPROM cell array (parallel to bit line). Glass etch.



Mag. 13,000x

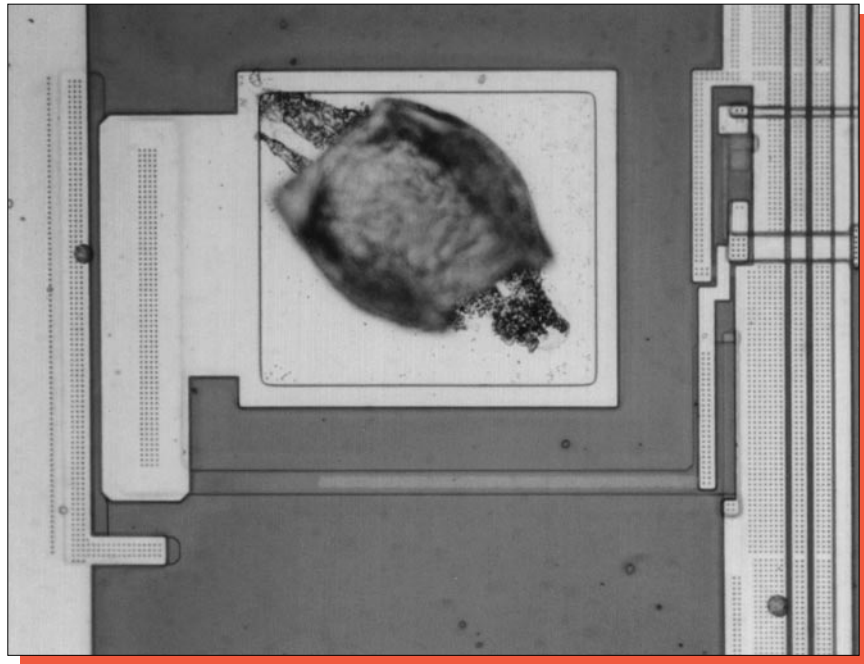


Mag. 13,000x

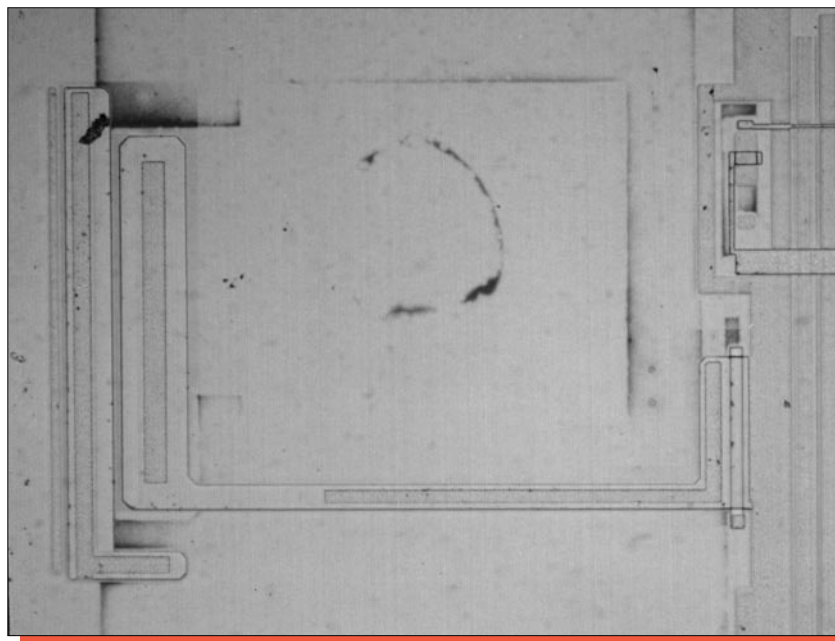


Mag. 52,000x

Figure 26. SEM section views of the EPROM cell (parallel to word line).

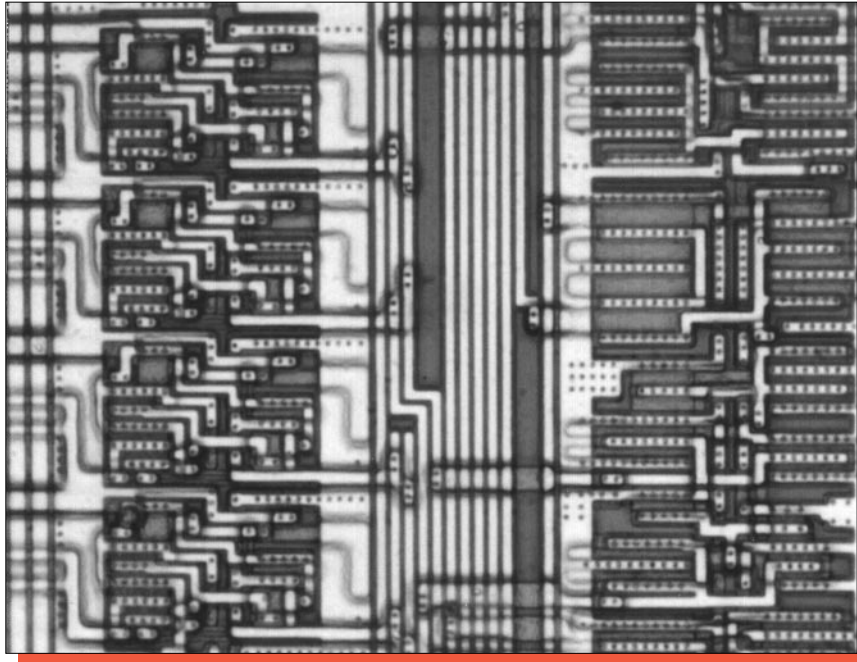


intact

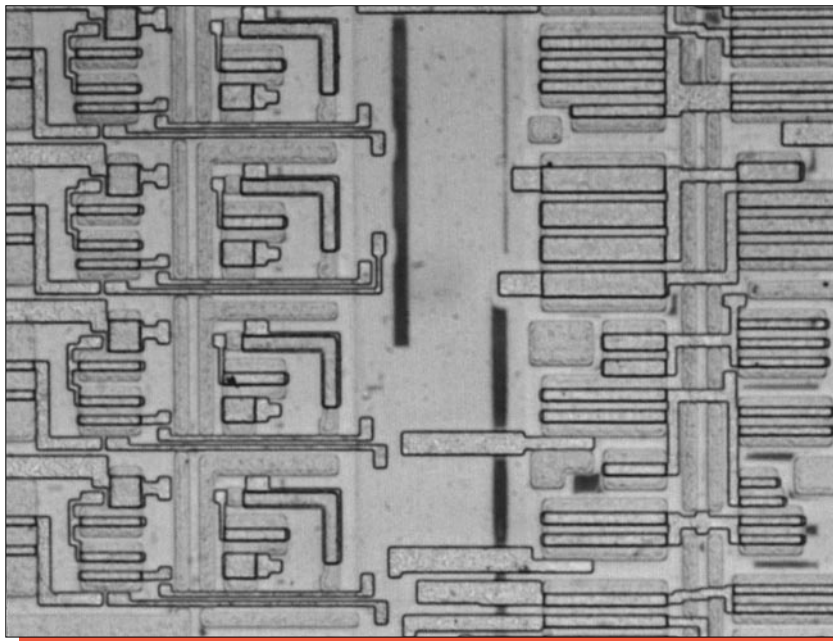


unlayered

Figure 27. Optical views of input protection. Mag. 400x.



intact



unlayered

Figure 28. Optical views of general circuitry. Mag. 800x.