Construction Analysis

Panasonic MN150808KJAG Microcontroller

Report Number: SCA 9612-514

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Panasonic (Matsushita) MN150808KJAG Microcontroller. One device was supplied for the analysis. The device was encapsulated in a 64-pin Plastic Quad Flat Pack (PQFP) package date coded 9503.

MAJOR FINDINGS

Questionable Items:[1]

- Silicon nodules in aluminum occupied up to 65 percent[2] of the line width (Figure 8).

Special Features:

- On-chip SRAM (6T) and NAND MROM.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

ANALYSIS RESULTS

Die Process and Design: **Figures 1 - 21**

Questionable Items:[1]

- Silicon nodules in aluminum occupied up to 65 percent[2] of the line width (Figure 8).

Special Features:

- On-chip SRAM (6T) and NAND MROM.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an N substrate. No epi was present. A single layer of metal and a single layer of polysilicon were used.

- Design implementation: Die layout was clean. Alignment was good at all levels.

- Surface defects: No toolmarks, masking defects, or contamination areas were found.

- Final passivation: A layer of nitride over a thin layer of silicon-dioxide. Passivation integrity tests indicated defect-free passivation. Edge seal was also good.

- Metallization: A single layer of silicon-doped aluminum. No cap or barrier metals were employed.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS (continued)

- Metal patterning: The aluminum was defined by a dry etch of normal quality. Metal lines were widened slightly at contacts. Contacts were completely surrounded by aluminum and contact coverage was 100 percent.

- Metal defects: No notching or voiding was found. Silicon nodules occupied up to 65 percent of the line widths. Silicon nodules >50 percent of the line width cause an increase in the aluminum's susceptibility to electromigration.

- Metal step coverage: Aluminum thinning up to 60 percent at contact edges. MIL-STD-883D allows up to 70 percent metal thinning for contacts of this size. Virtually no metal thinning was noted outside contact areas.

- Contacts: Contact cuts appeared to be formed by a dry-etch followed by a wet-etch. No overetching of contacts were noted and no silicon mound growth was present at contacts.

- Pre-metal glass: A single layer of reflow glass (probably BPSG) over densified oxide. The glass was reflowed prior to contact cuts only. A thin nitride layer was present under the reflow glass. Its purpose is not known. No problems were found.

- Polysilicon: A single layer of polysilicon (no silicide) was employed. Polysilicon was used to form all gates on the die. Definition and coverage was good.

- Isolation: Standard recessed field oxide. No problems were present at the birdsbeaks or elsewhere. A step was present in the field oxide at the well boundaries indicating the presence of a twin-well process.

ANALYSIS RESULTS (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of MOS transistors. Oxide sidewall spacers were not used. No salicide was employed on diffusions.

- Wells: Twin-wells were used in an N substrate. As mentioned a step was present in the field oxide at the well boundaries. No epi layer was present.

- Buried contacts: Direct poly-to-diffusion contacts were not employed.

- Fuses: Fuses were not employed on this device.

- Capacitors: Poly-to-diffusion capacitors were employed fairly extensively. No problems were found.

- NAND MROM array: Metal was used to form the bit lines and poly was used to form the word lines. An N+ diffusion was used to distribute GND. The NAND MROM stack was 3.5 x 34 microns (119 microns^2).

- 6T SRAM array: Metal was used to form the bit lines and poly was used to form all the gates. The individual cell was 21 x 36 microns (756 microns^2).

HORIZONTAL DIMENSIONS

Die size:	4.3 x 5.2 mm (170 x 205 mils)
Die area:	22 mm^2 (34,850 $mils^2$)
Min pad size:	0.1 x 0.13 mm (4.3 x 5.3 mils)
Min pad window:	0.1 x 0.1 mm (3.9 x 3.9 mils)
Min pad spacing:	7 microns (0.3 mils)
Min pad-to-metal:	2.5 microns (0.09 mils)
Min metal 1 width:	1.5 micron
Min metal 1 space:	2.5 microns
Metal 1 pitch:	4.0 microns
Min contact:	2.0 microns (round)
Min contact space (continuous):	1.4 micron
Min poly width:	1.5 micron
Min poly space:	1.3 micron
Min gate length* - (N-channel):	1.5 micron
- (P-channel):	2.0 microns
Cell size (6T SRAM):	756 $microns^2$
Cell pitch (6T SRAM):	21 x 36 microns
Cell size (NAND MROM stack):	119 $microns^2$
Cell pitch (NAND MROM stack):	3.5 x 34 microns

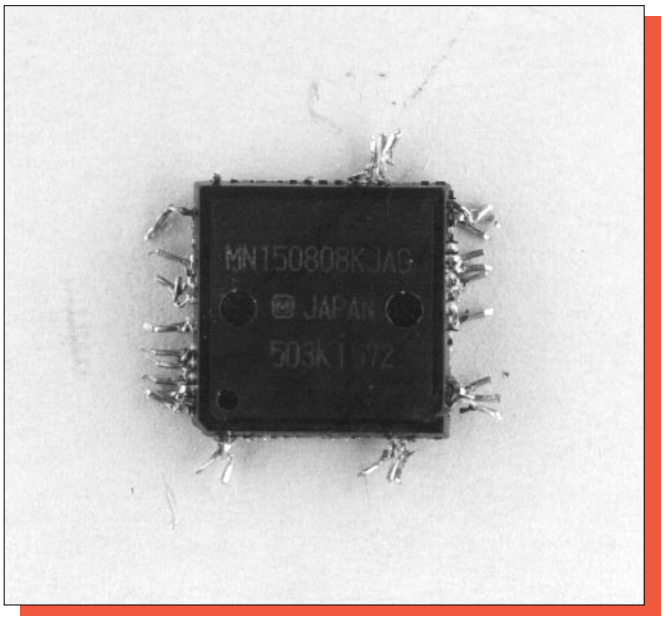
**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.4 mm (15 mils)

Layers

Passivation 2:	0.7 micron
Passivation 1:	0.2 micron
Metal:	0.9 micron
Pre-metal glass:	0.6 micron (average)
Polysilicon:	0.35 micron
Field oxide:	0.6 micron
N+ S/D diffusion:	0.3 micron
P+ S/D diffusion:	0.2 micron
P-well:	Could not delineate
N-well:	6 microns



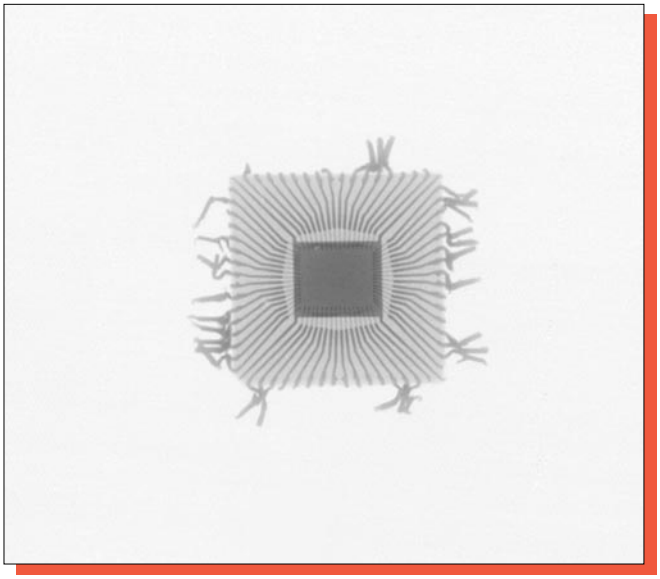


Figure 1. Package photograph and x-ray view of the Panasonic MN150808KJAG.
Mag. 2x.

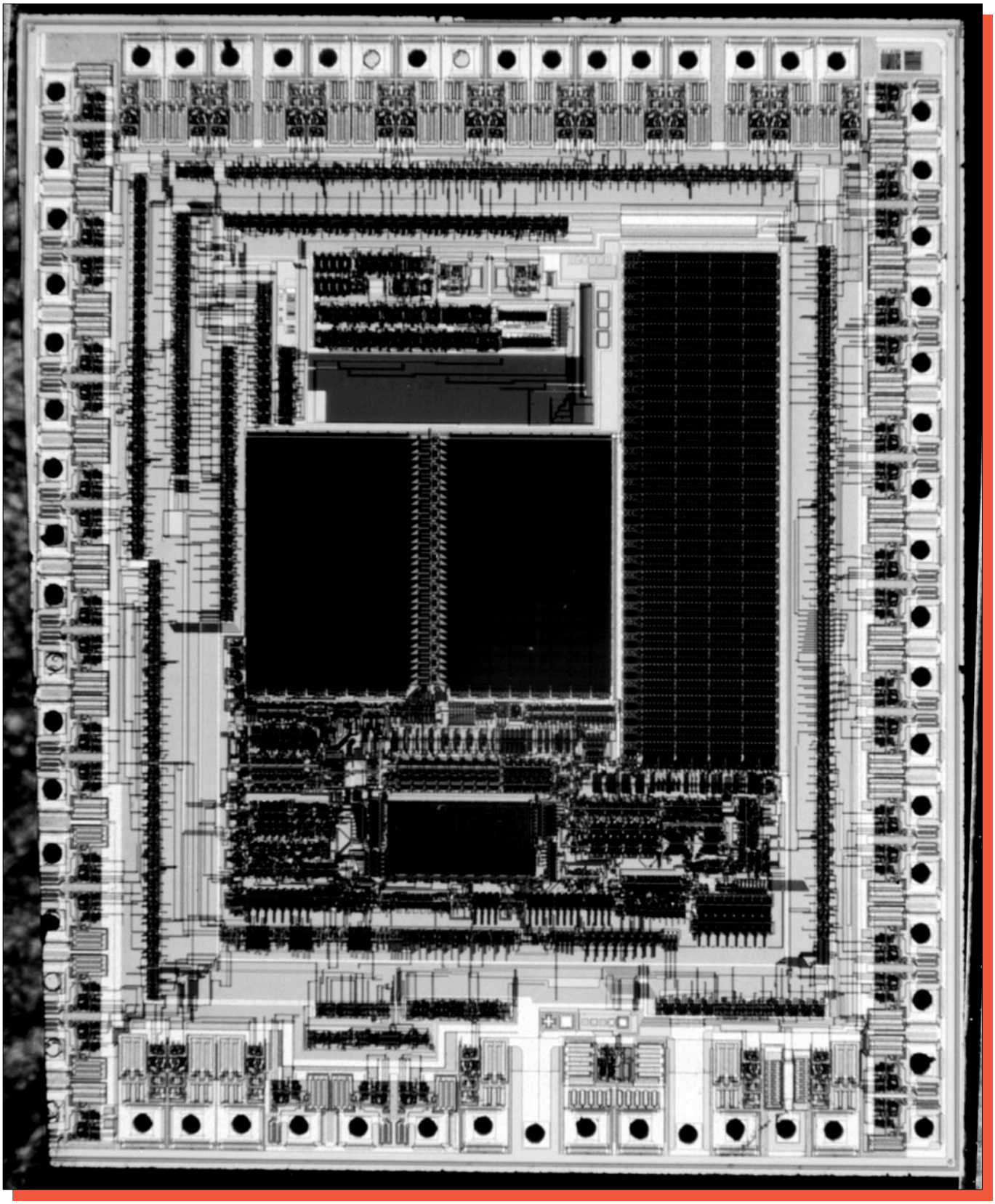


Figure 2. Whole die photograph of the Panasonic MN150808KJAG. Mag. 40x.

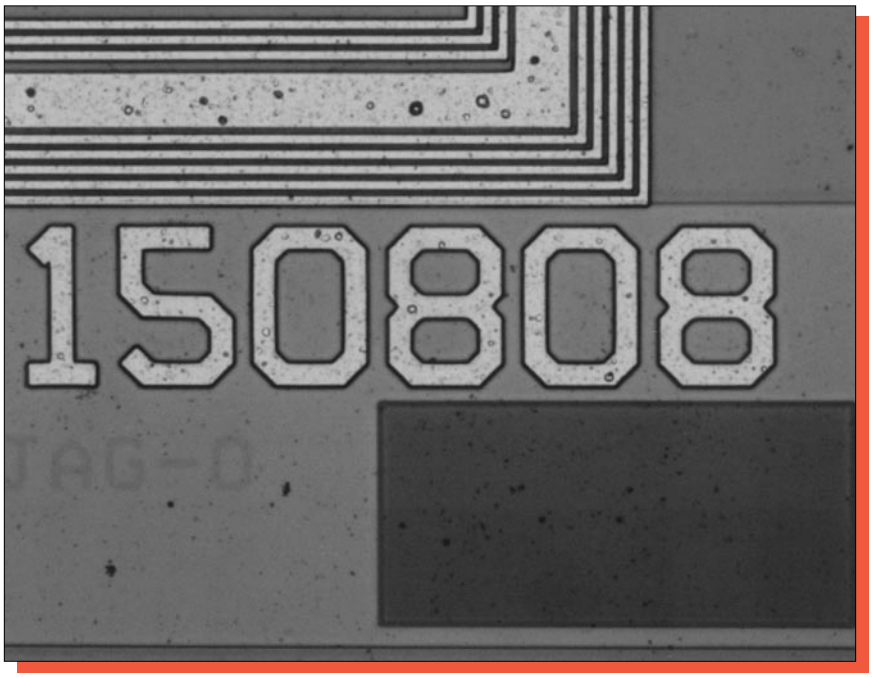
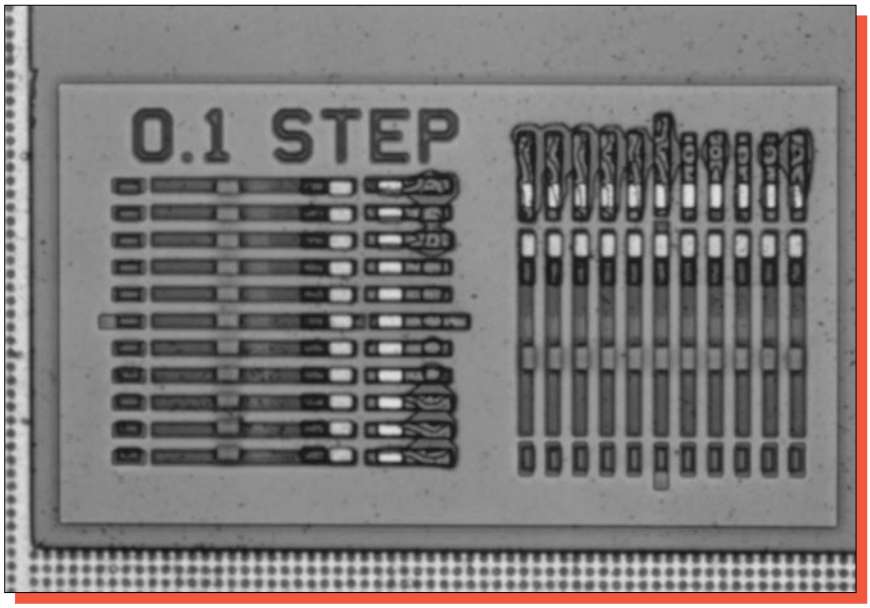
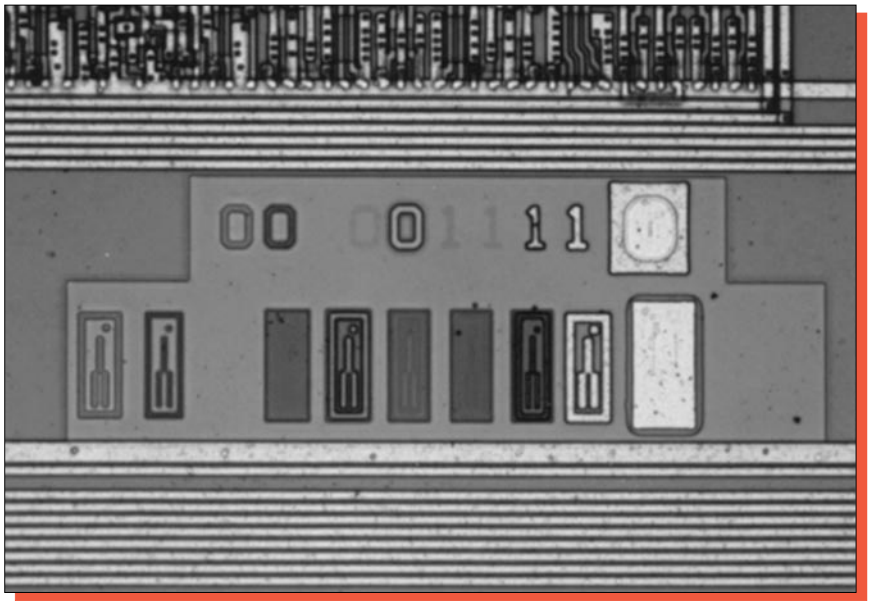


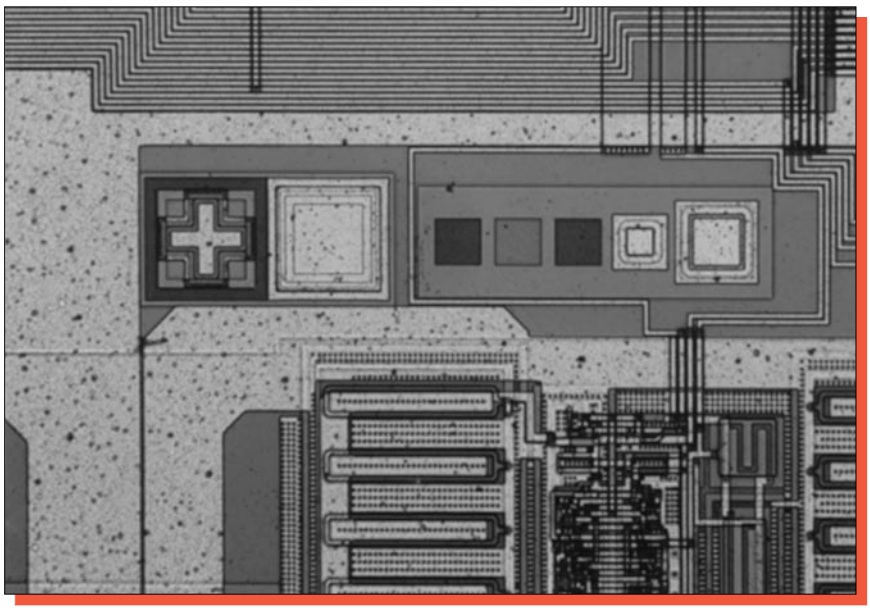
Figure 3. Die identification markings. Mag. 500x.



Mag. 500x

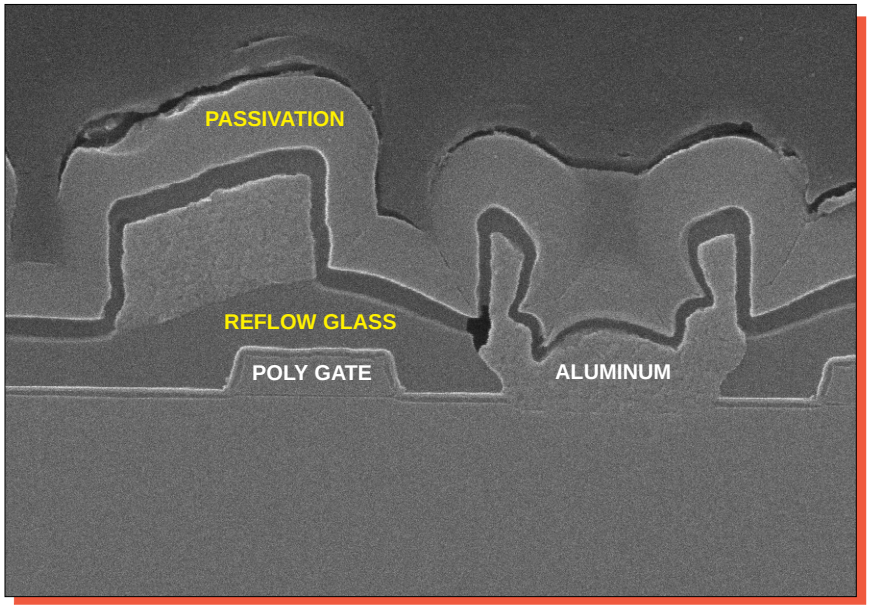


Mag. 400x

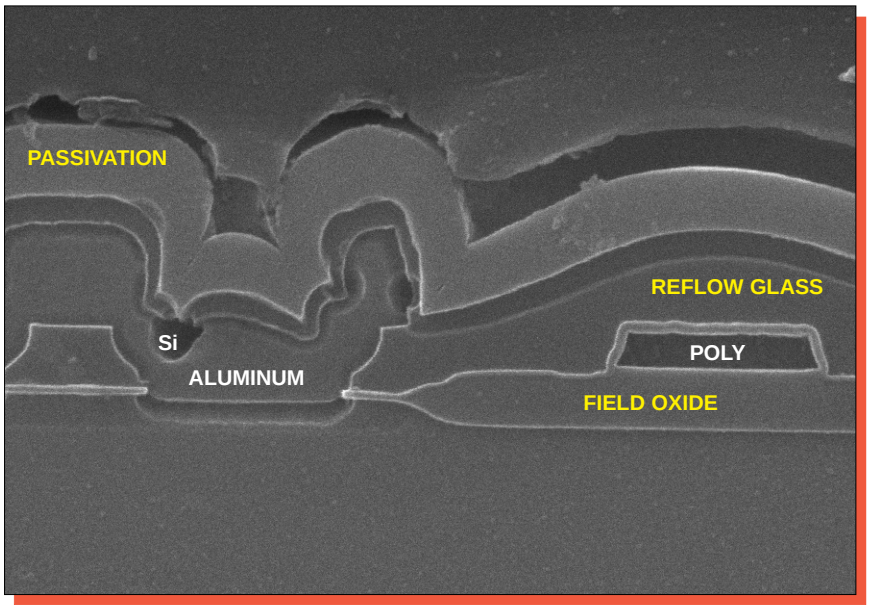


Mag. 200x

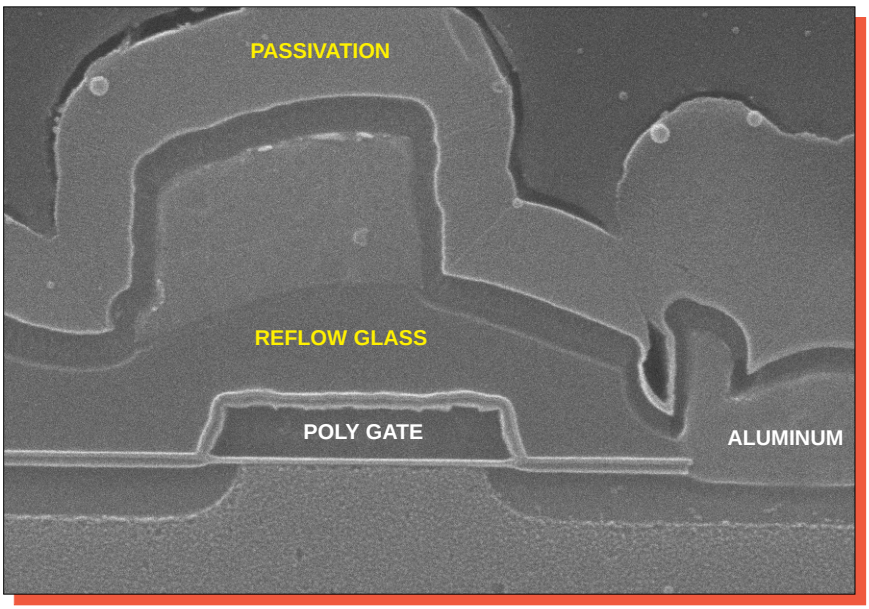
Figure 3a. Additional markings and alignment keys from the die surface.



glass-etch,
Mag. 13,000x

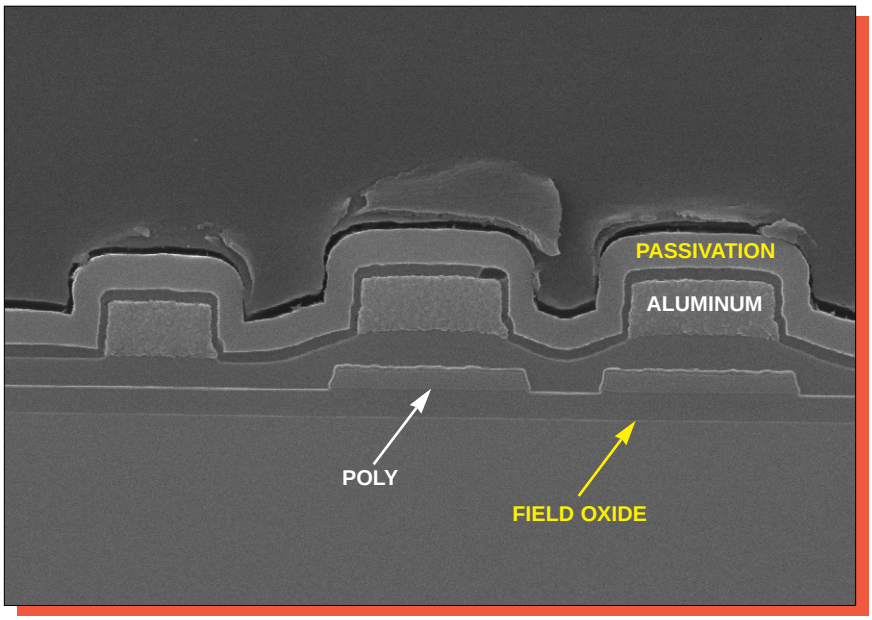


Mag. 13,000x

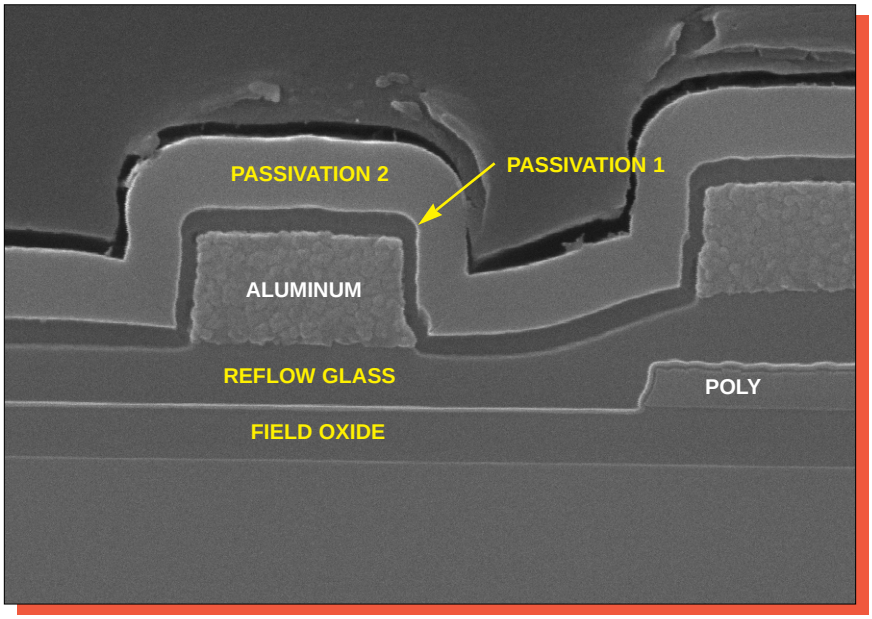


silicon-etch,
Mag. 20,000x

Figure 4. SEM section views illustrating general structure.

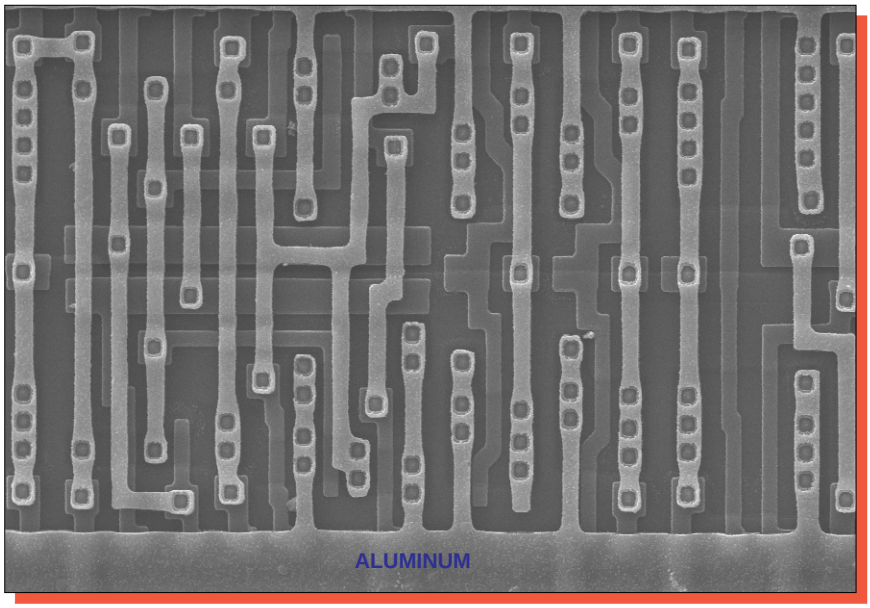


Mag. 6500x

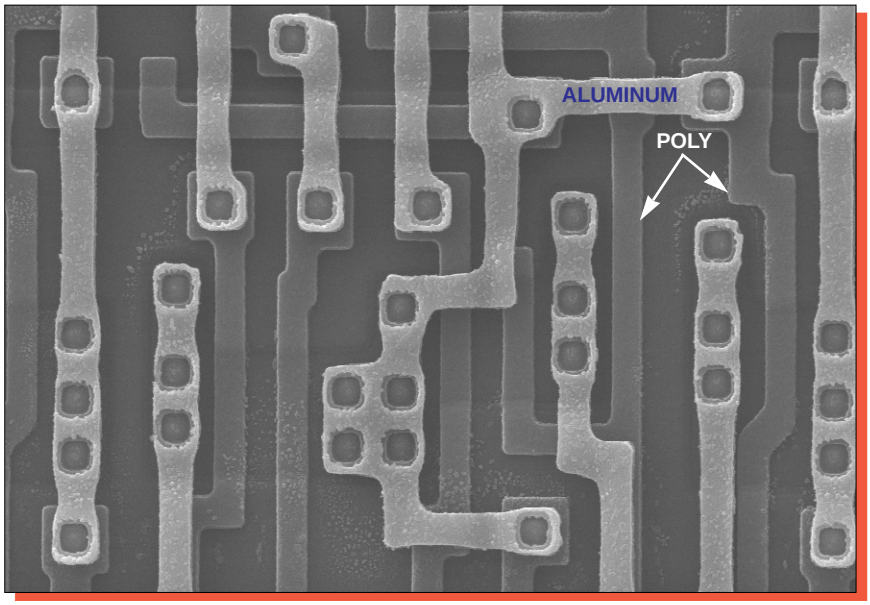


Mag. 13,000x

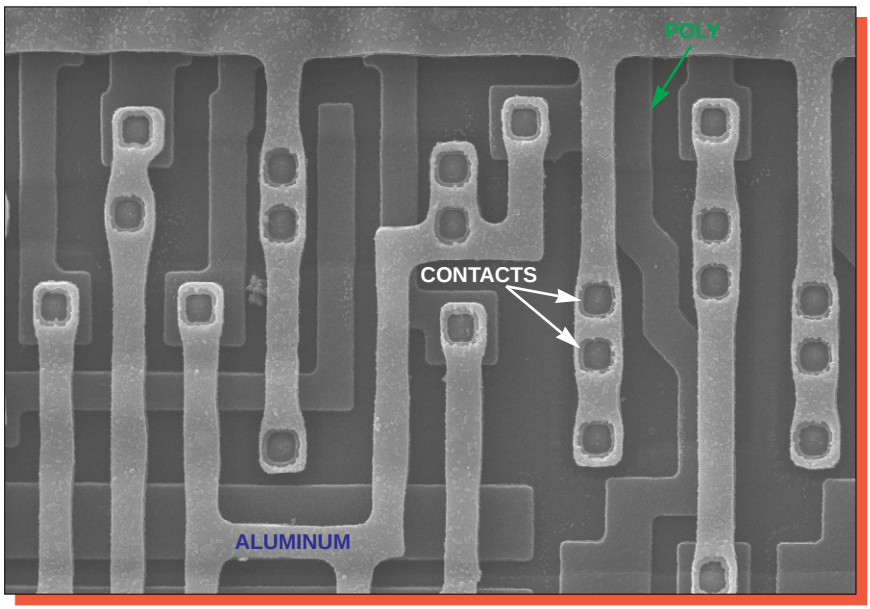
Figure 5. SEM section views illustrating metal line profiles. Glass etch.



Mag. 1200x

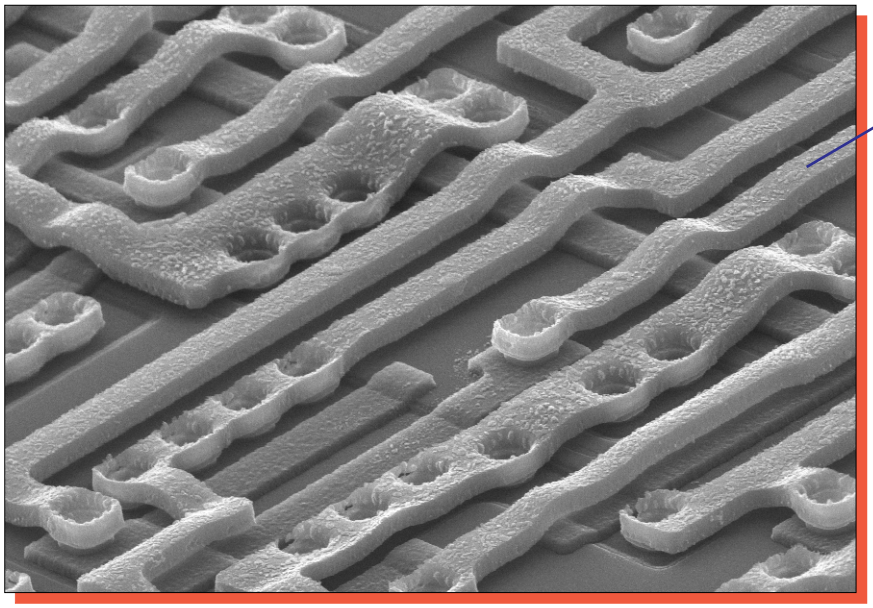


Mag. 2400x

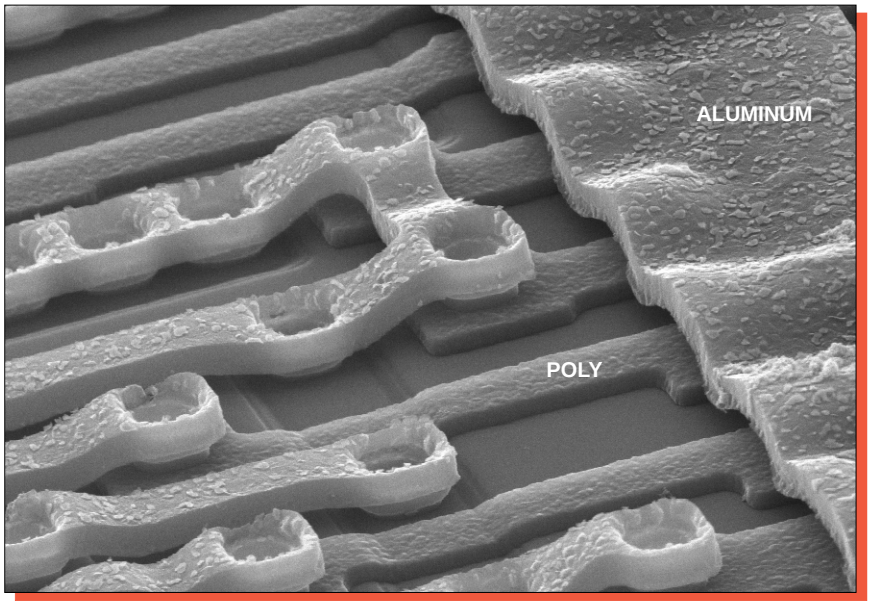


Mag. 2400x

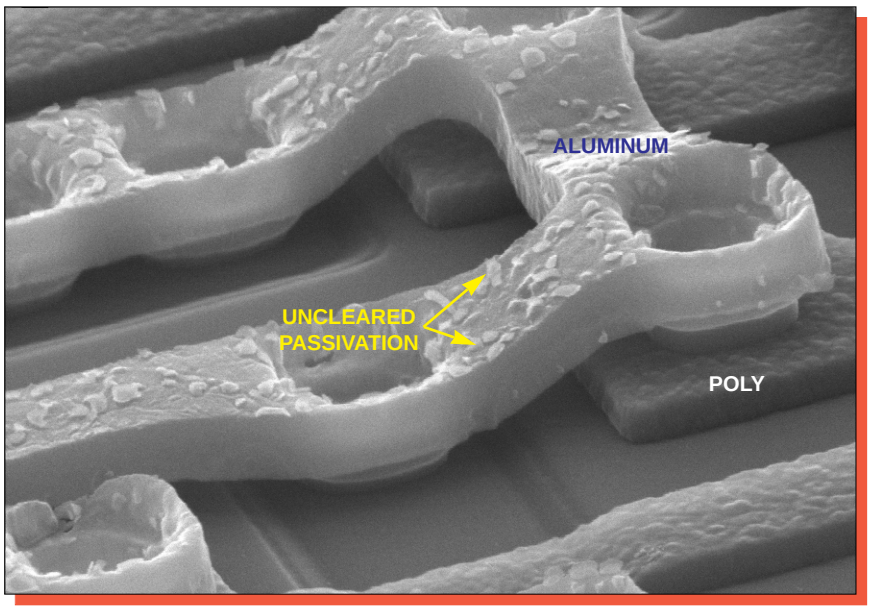
Figure 6. Topological SEM views illustrating metal patterning. 0°.



Mag. 3000x

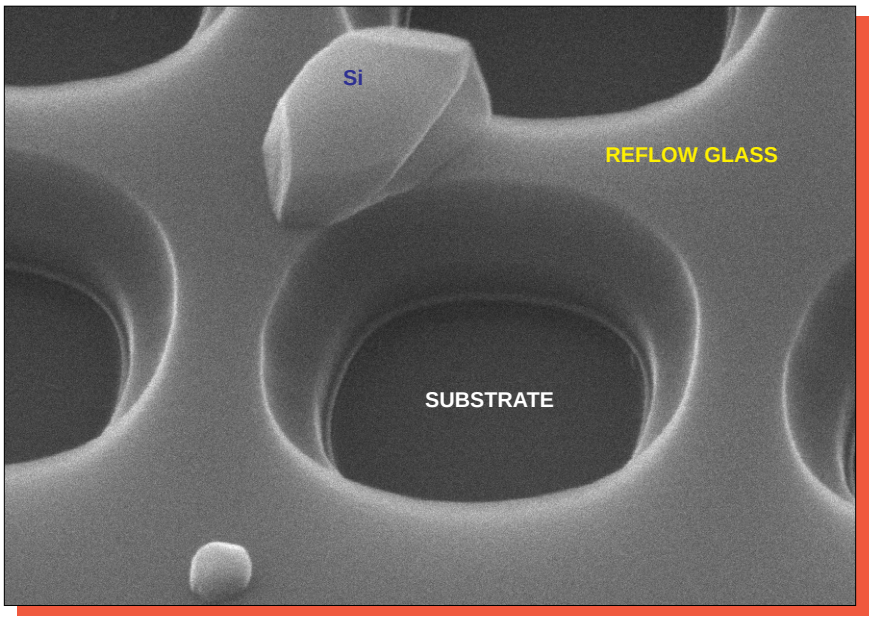


Mag. 5000x

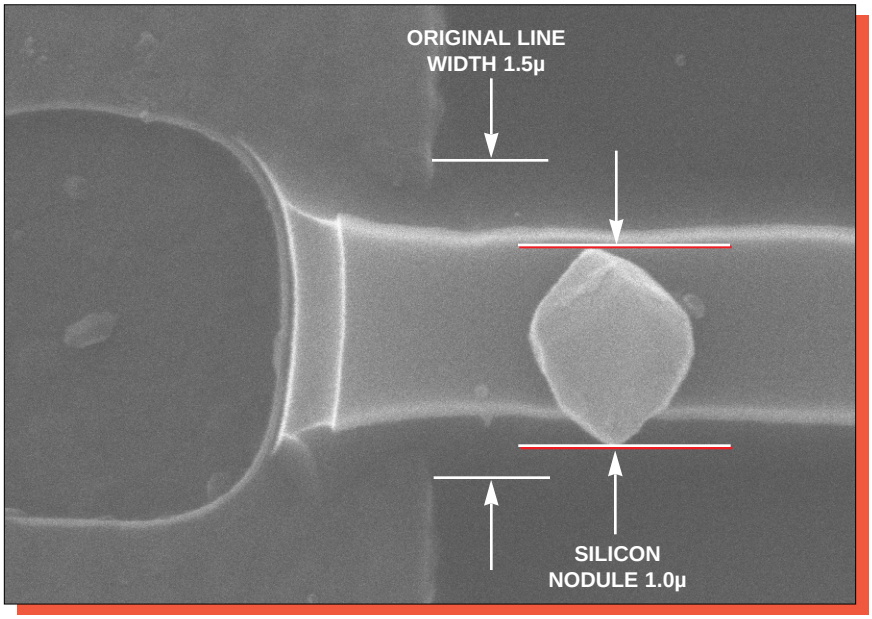


Mag. 10,000x

Figure 7. SEM views illustrating metal step coverage. 60°.

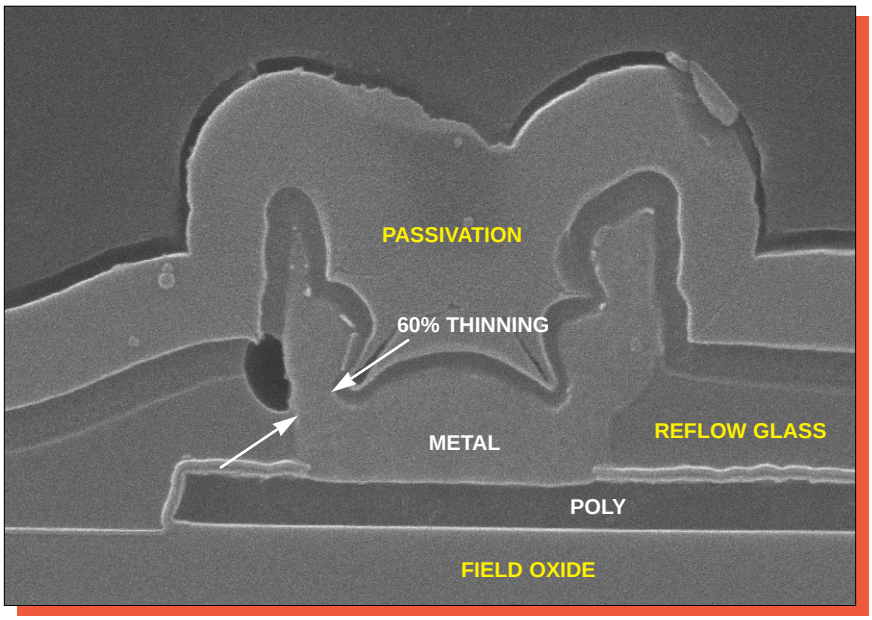


Mag. 20,000x, 45°

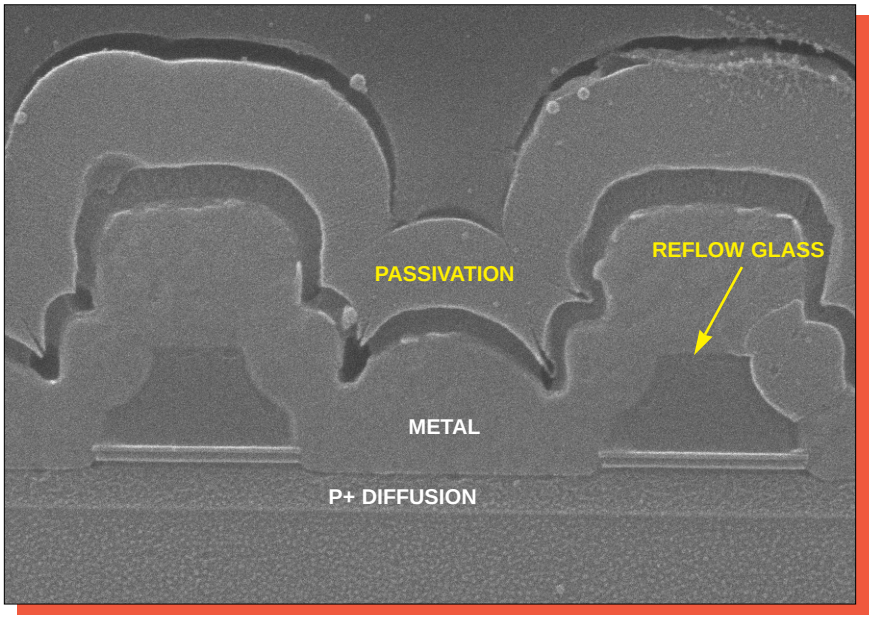


Mag. 20,000x, 0°

Figure 8. SEM views illustrating a contact cut and a silicon nodule.

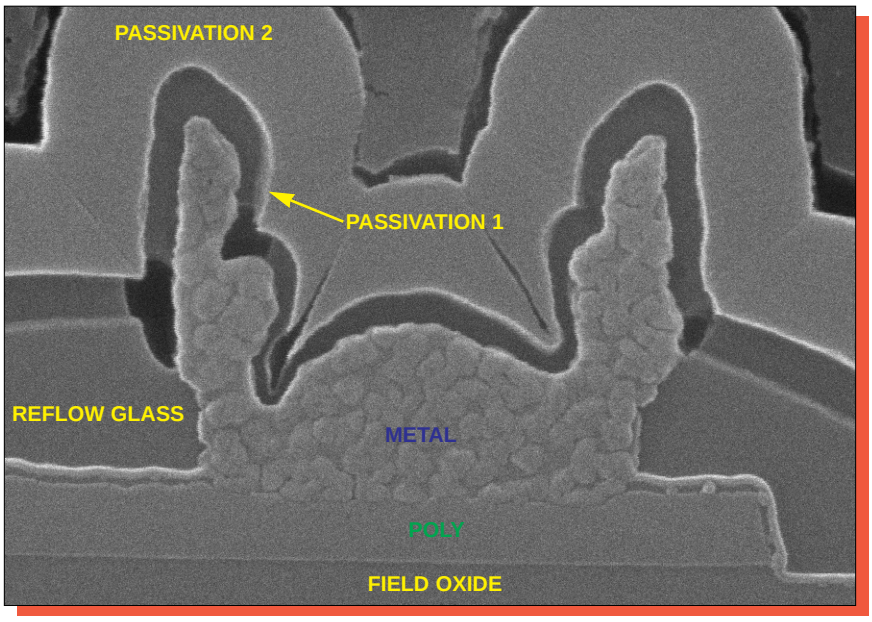


metal-to-poly



metal-to-diffusion

Figure 9a. SEM section views of typical contacts. Mag. 20,000x.



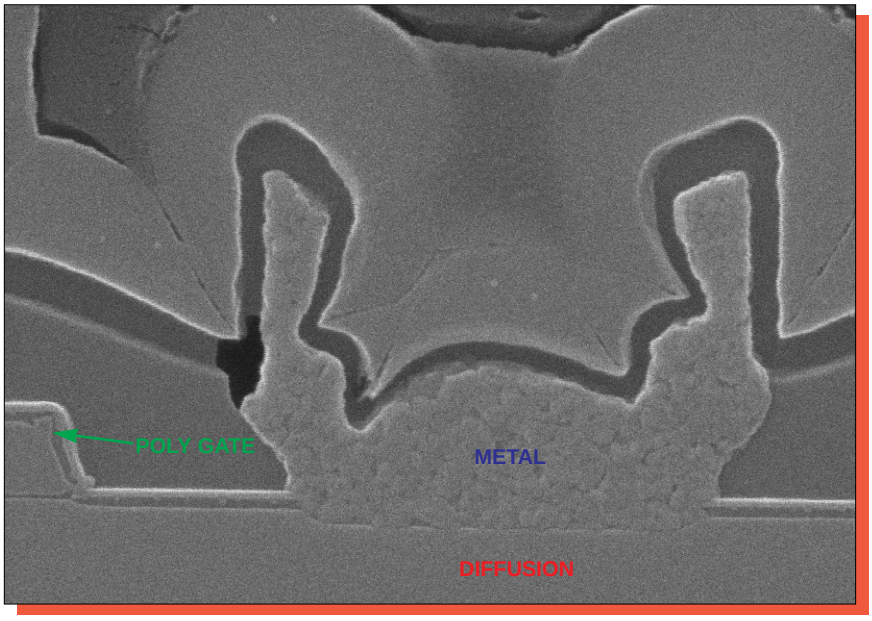
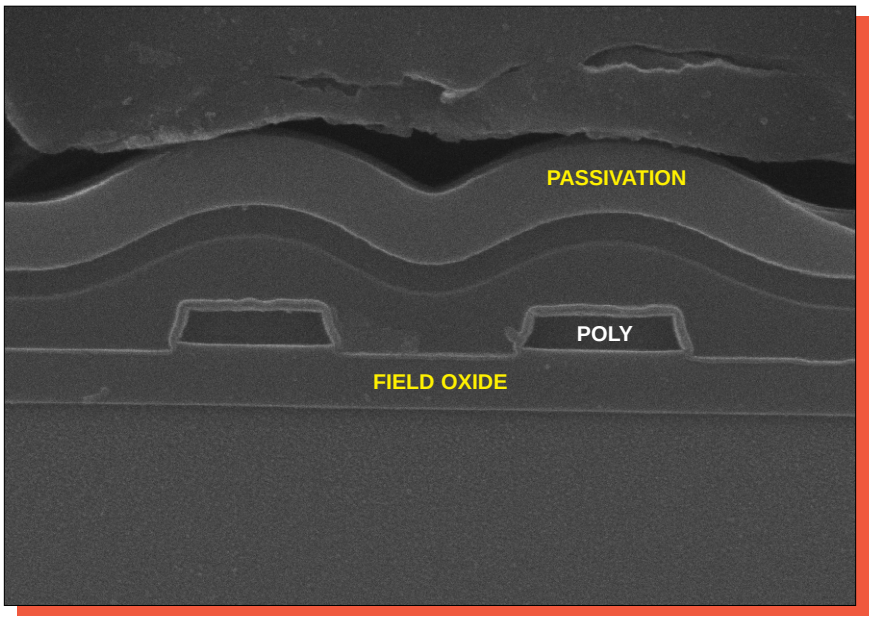
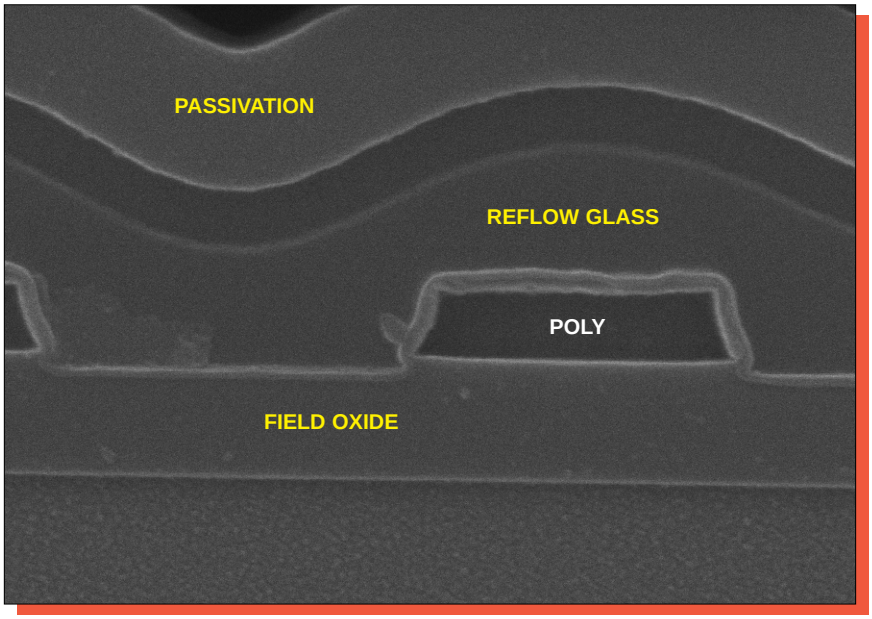


Figure 9b. SEM details of contacts. Glass etch, Mag. 26,000x.

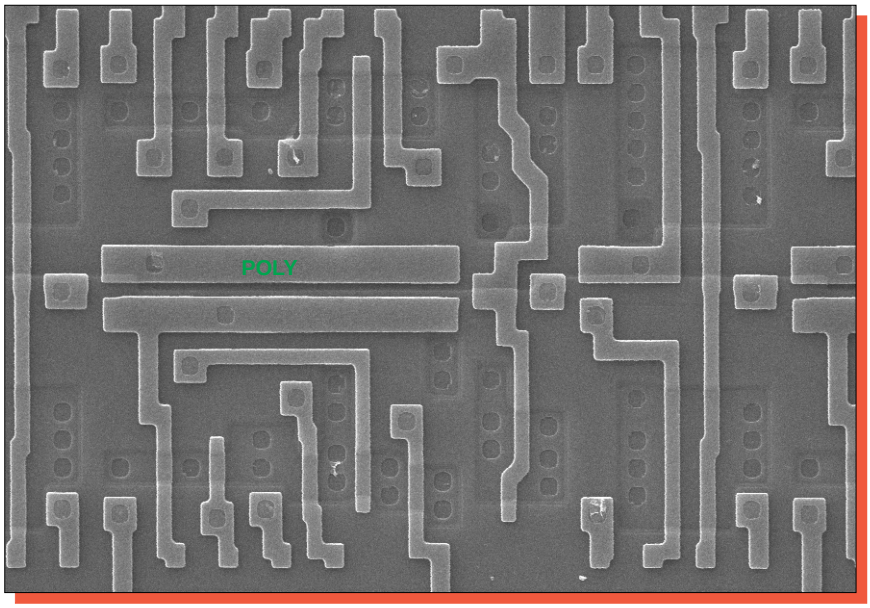


Mag. 13,000x

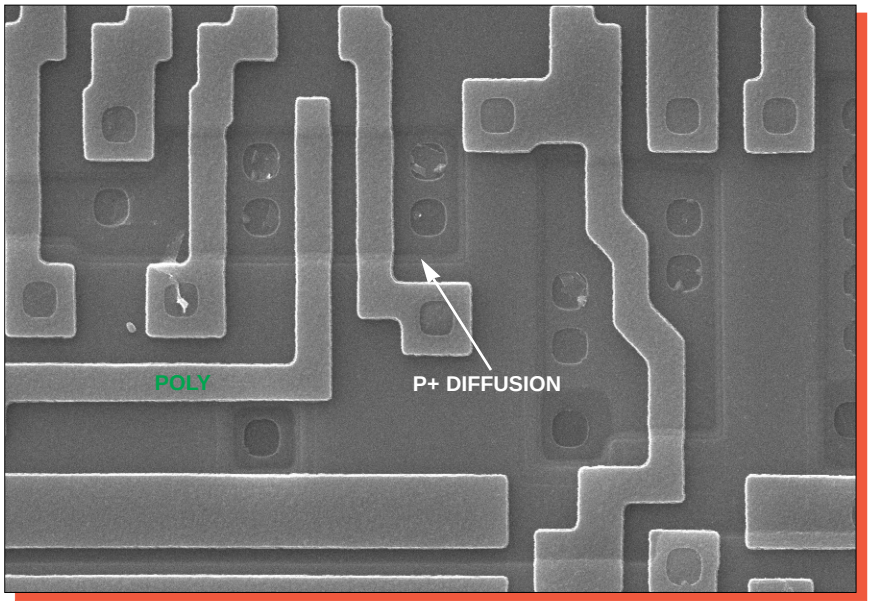


Mag. 26,000x

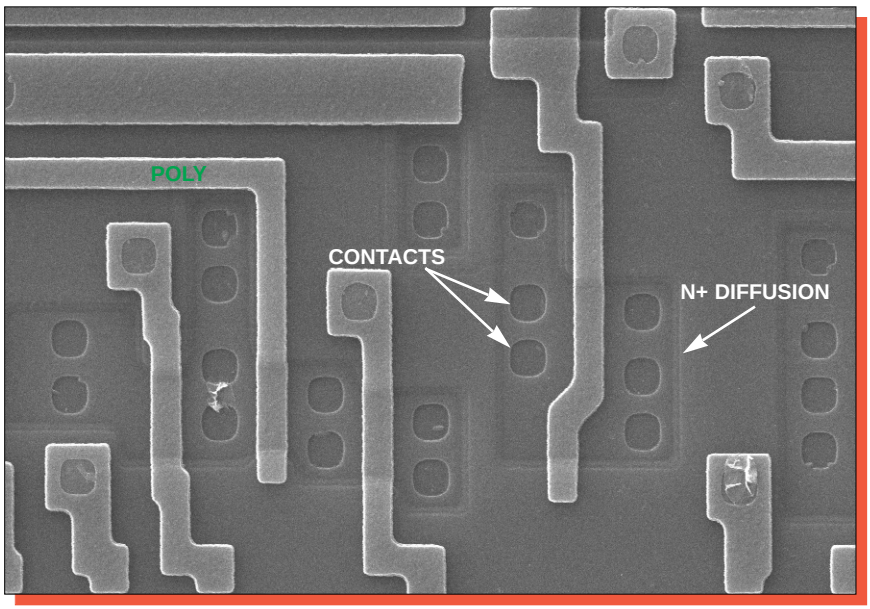
Figure 10. SEM views illustrating poly line profiles.



Mag. 1200x

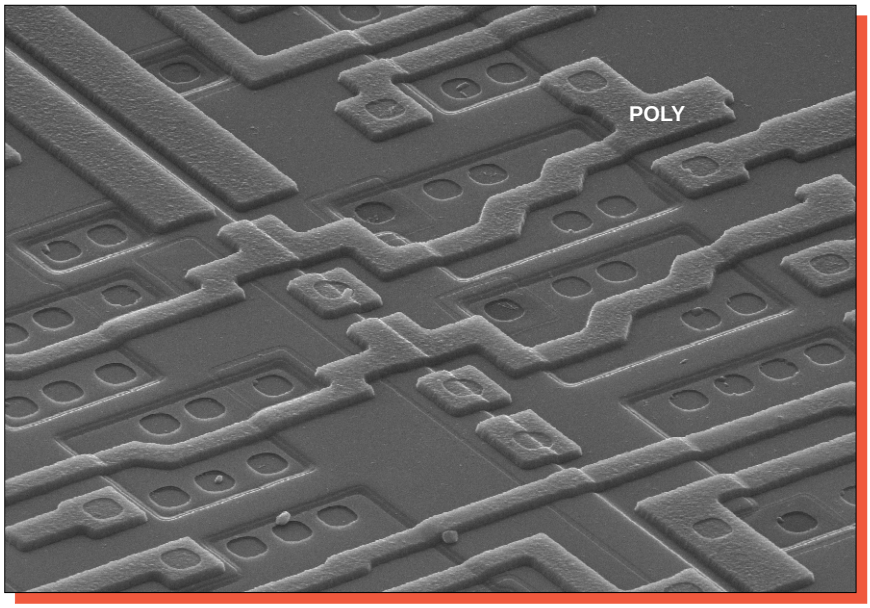


Mag. 2400x

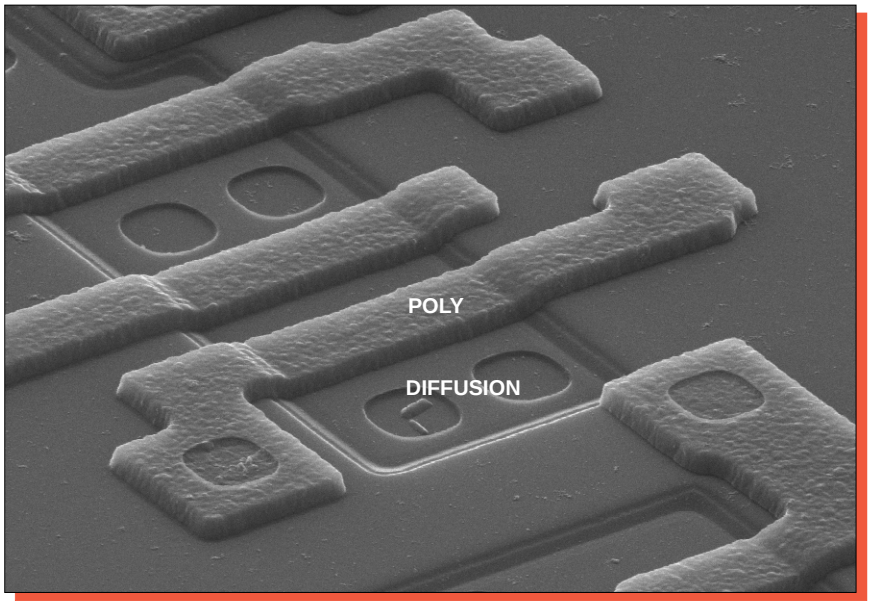


Mag. 2400x

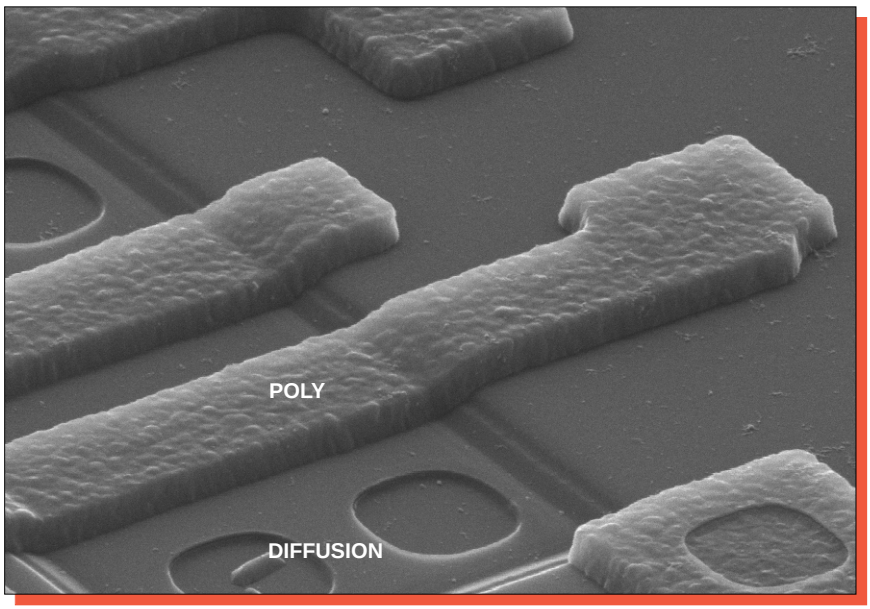
Figure 11. Topological SEM views illustrating poly patterning. 0°.



Mag. 2500x

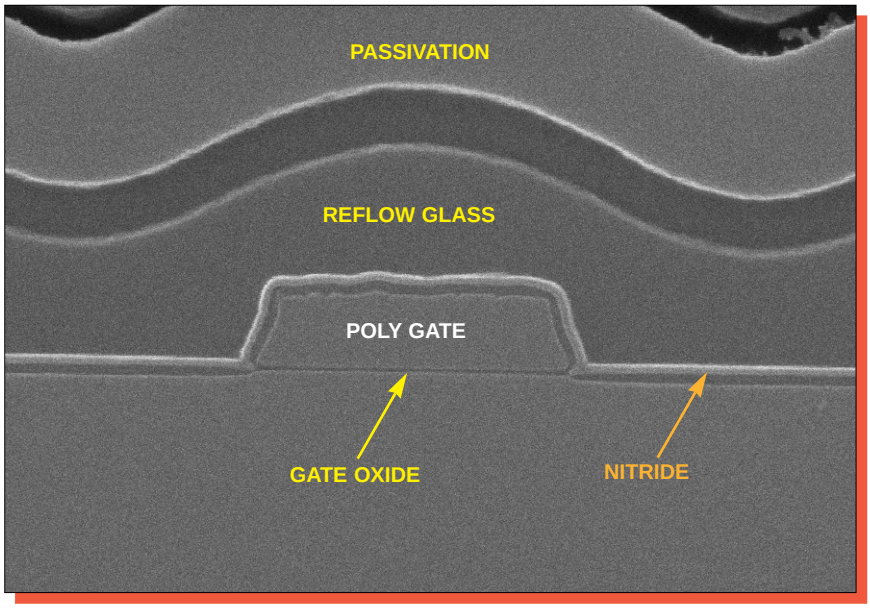


Mag. 6000x

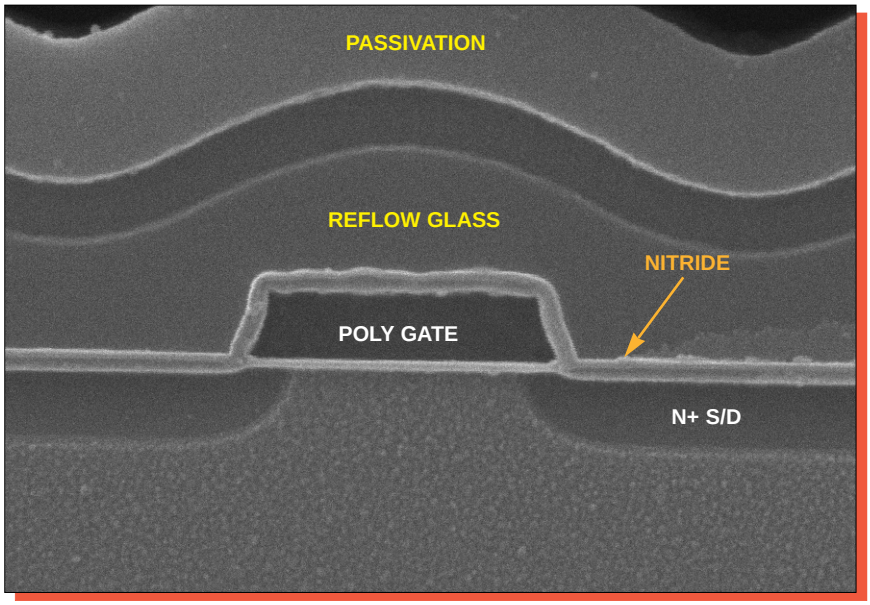


Mag. 10,000x

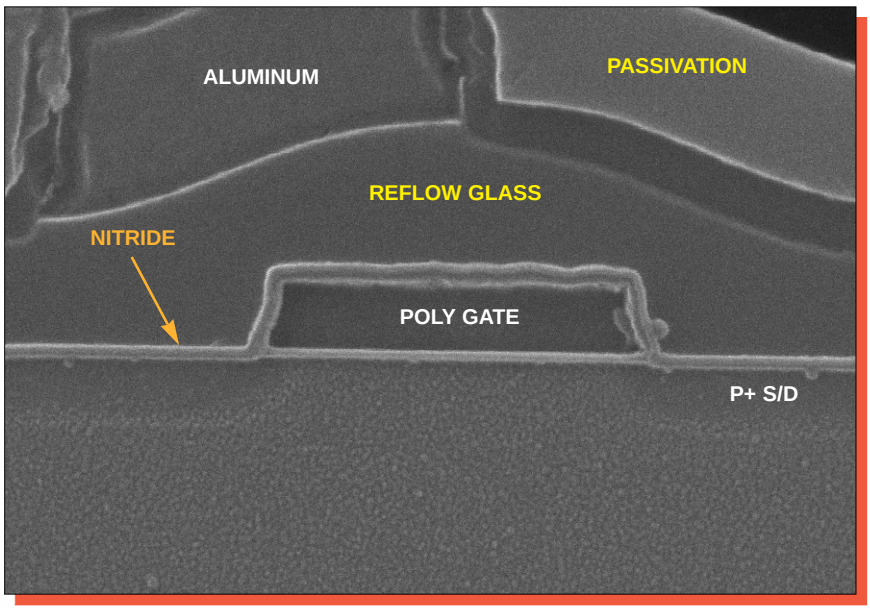
Figure 12. SEM views illustrating poly coverage. 60°.



glass etch

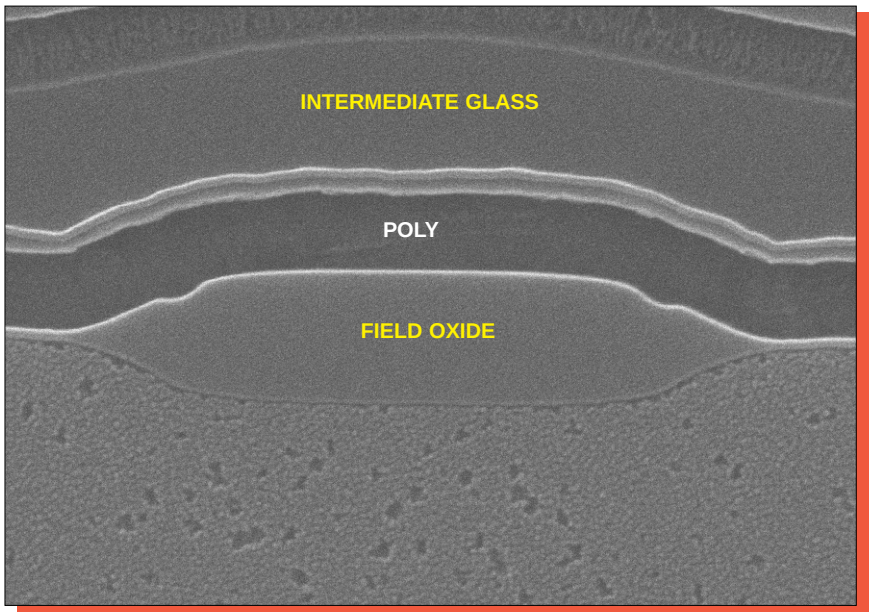


N-channel

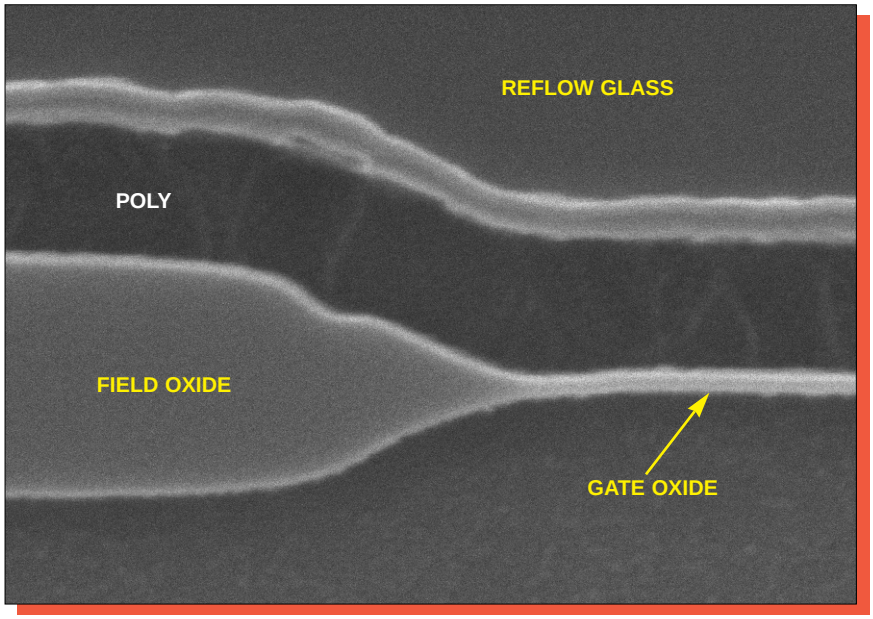


P-channel

Figure 13. SEM views illustrating typical gate structures. Mag. 26,000x.

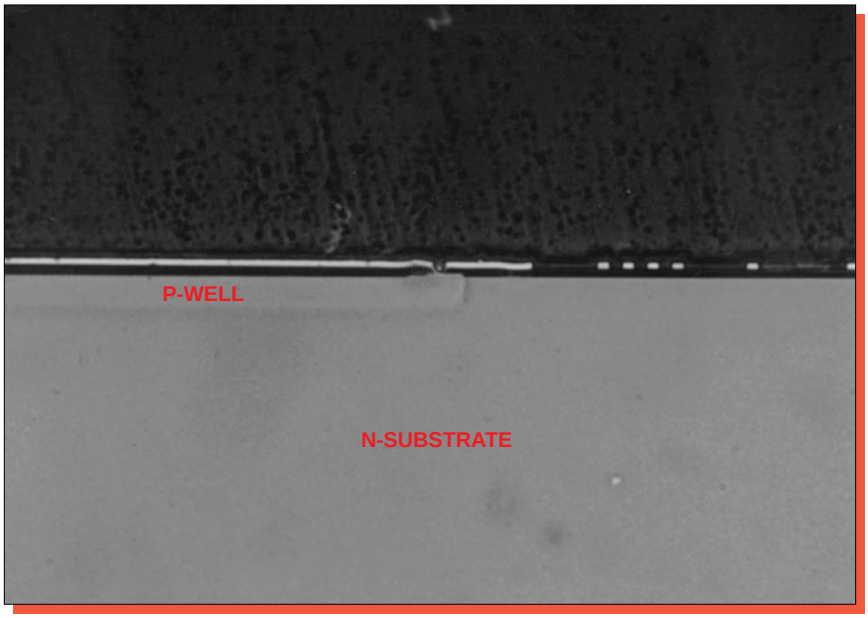


Mag. 30,000x

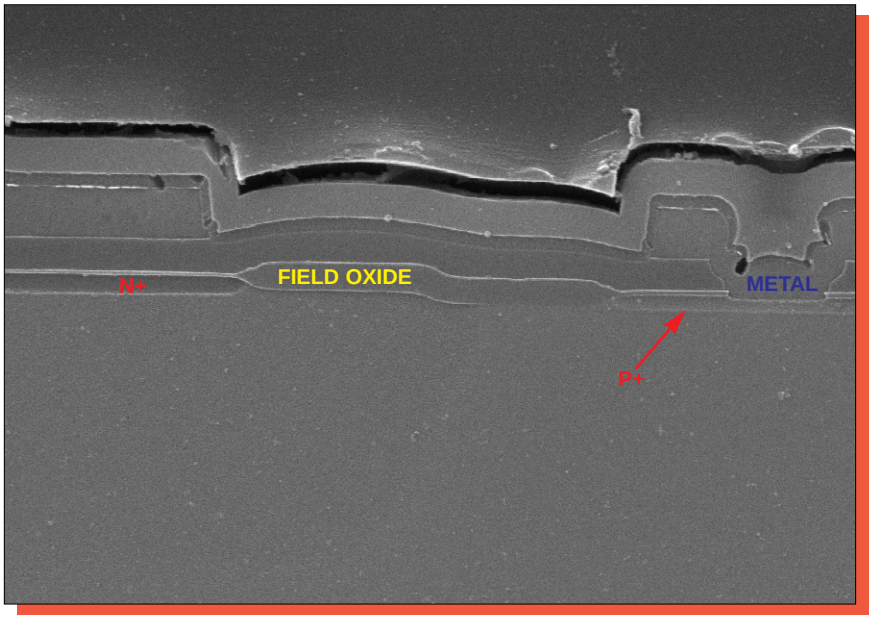


Mag. 52,000x

Figure 14. Section views illustrating field oxide isolation and a typical birdsbeak.

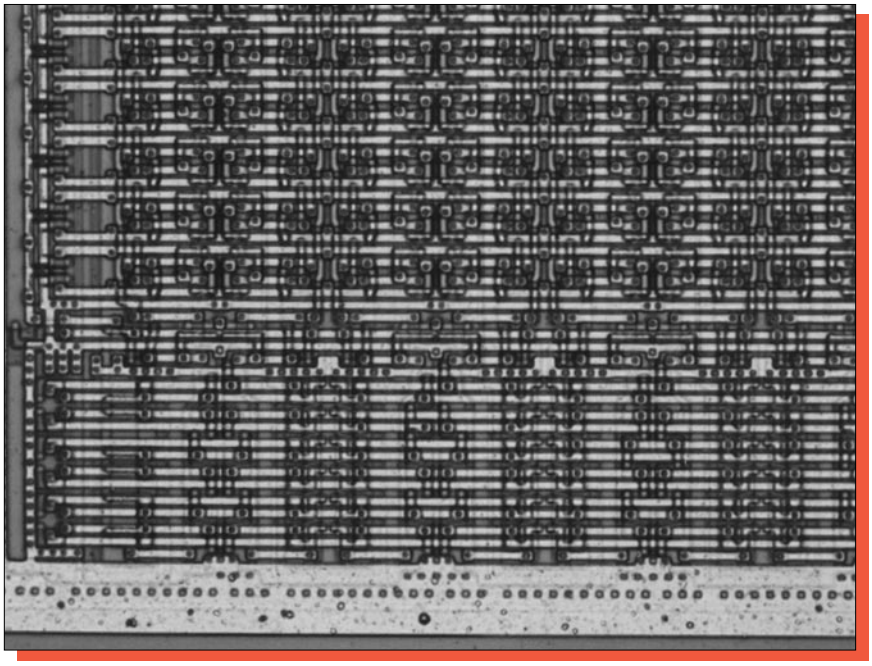


Mag. 800x

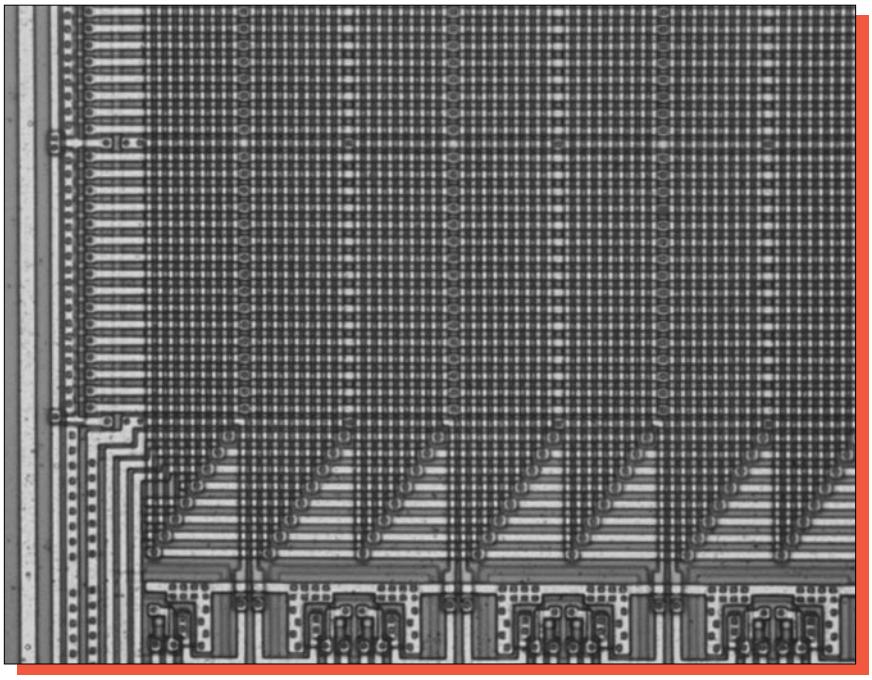


Mag. 6500x

Figure 15. Section views illustrating well structure and a step in local oxide.

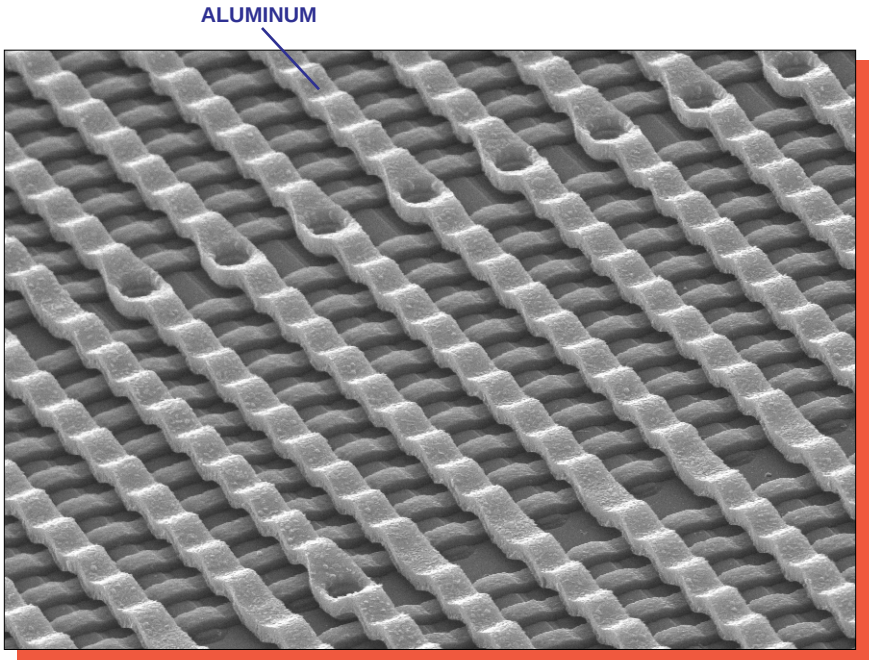


6T SRAM

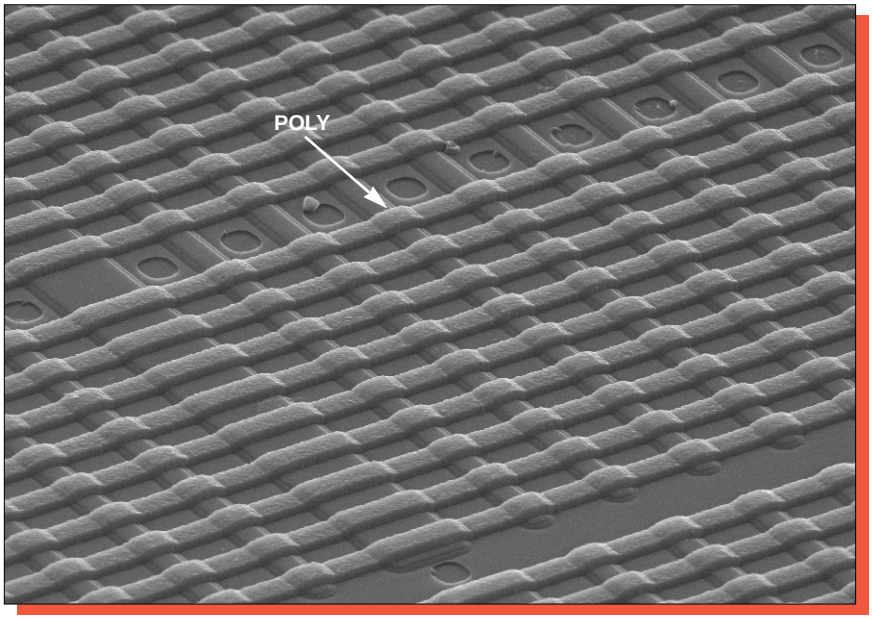


NAND ROM

Figure 16. Optical views of cell arrays. Mag. 400x.

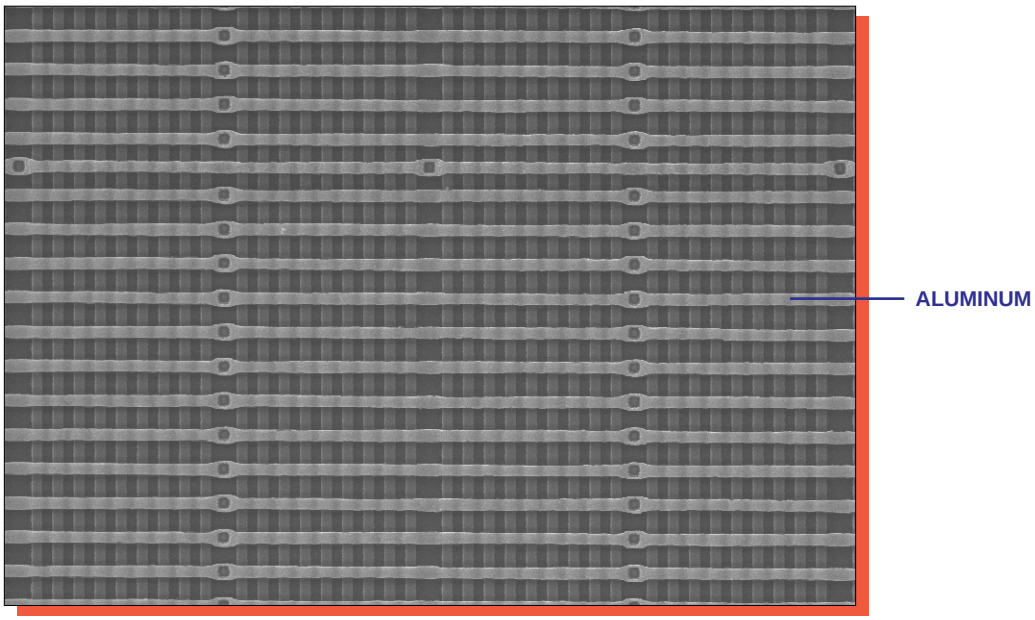


metal

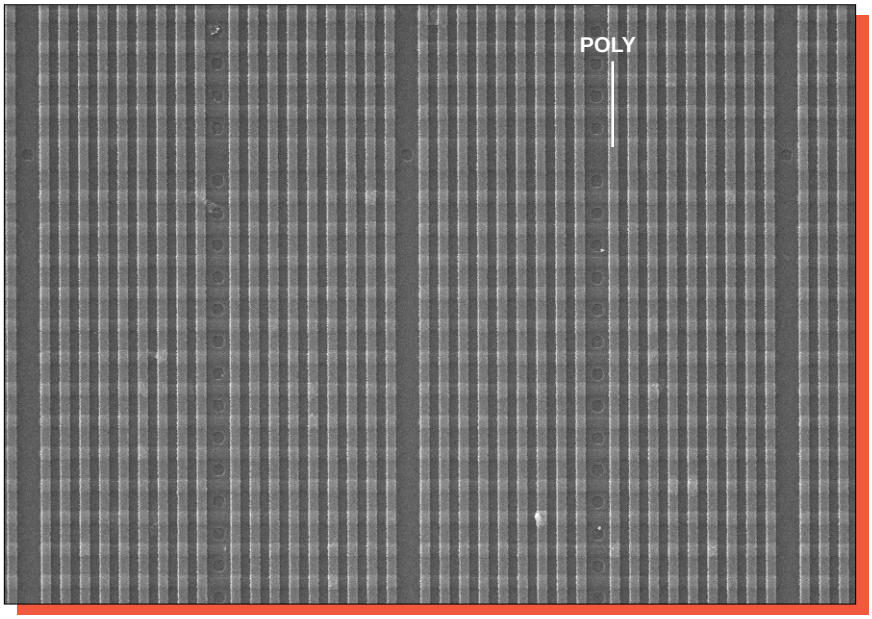


unlayered

Figure 17. SEM views illustrating the NAND ROM cell array. Mag. 2500x, 60°.

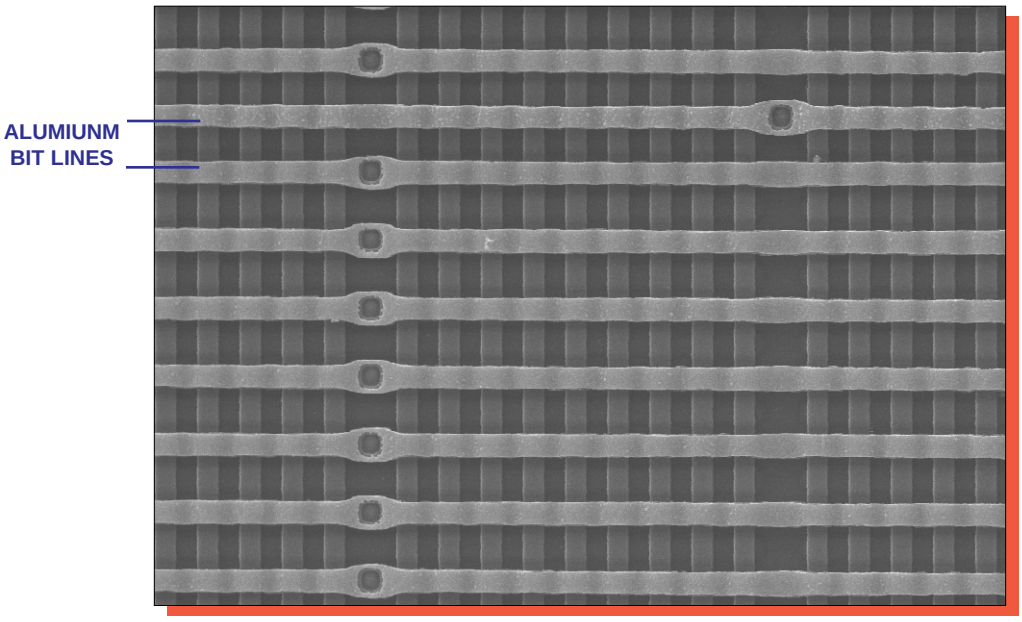


metal

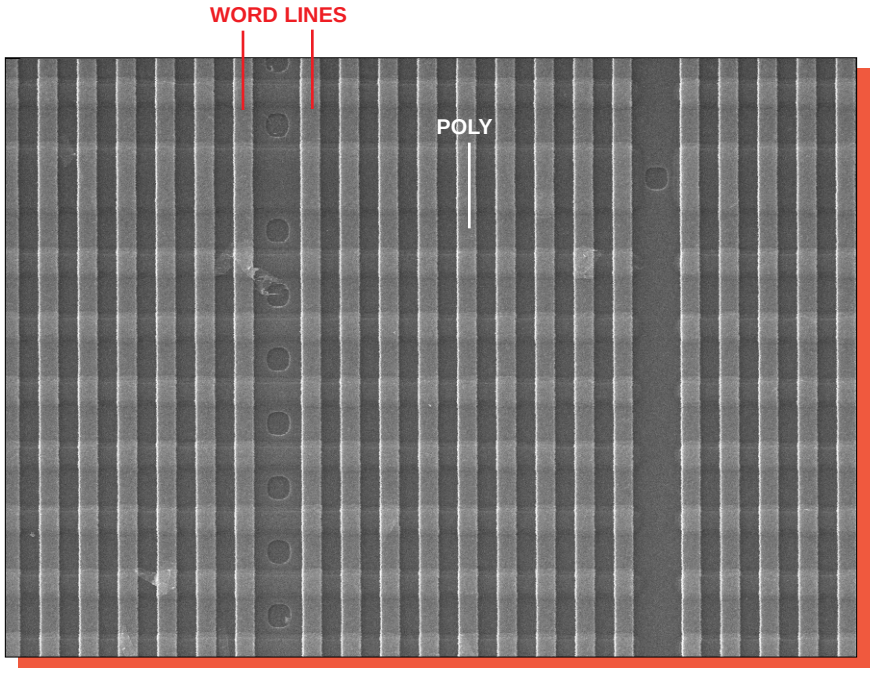


unlayered

Figure 17a. Topological SEM views illustrating the NAND ROM cell array. Mag. 775x, 0°.

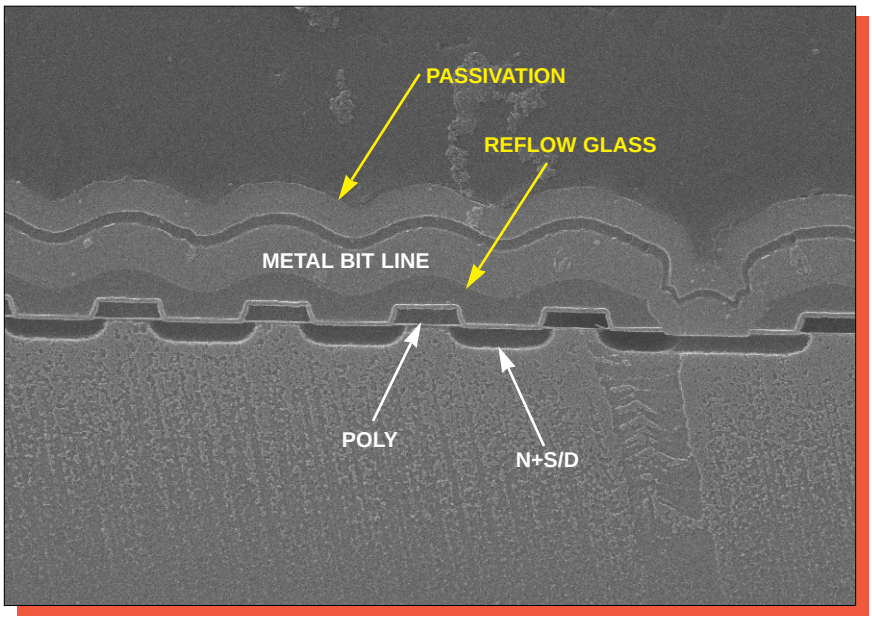


metal

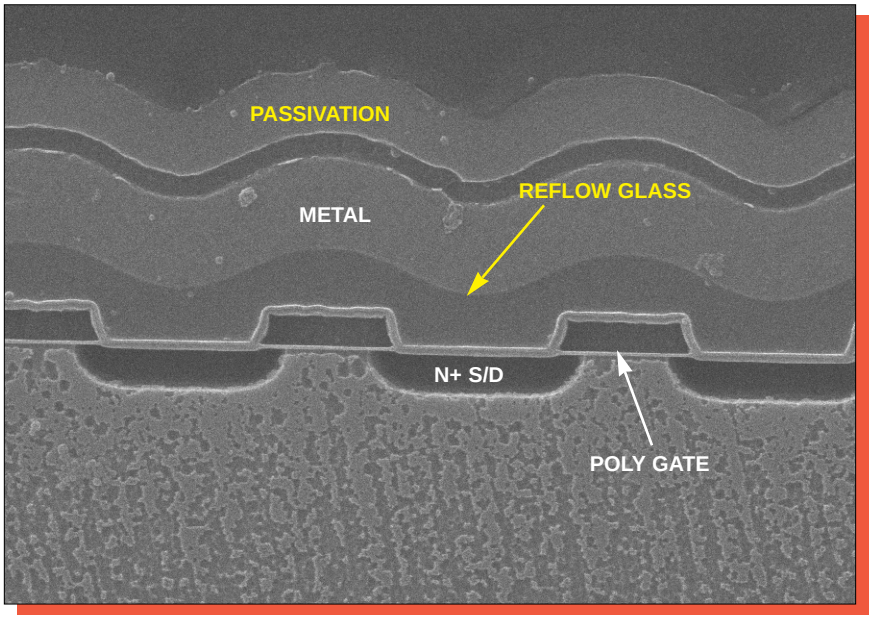


unlayered

Figure 17b. Topological SEM views of the NAND ROM cell array. Mag. 1500x, 0°.

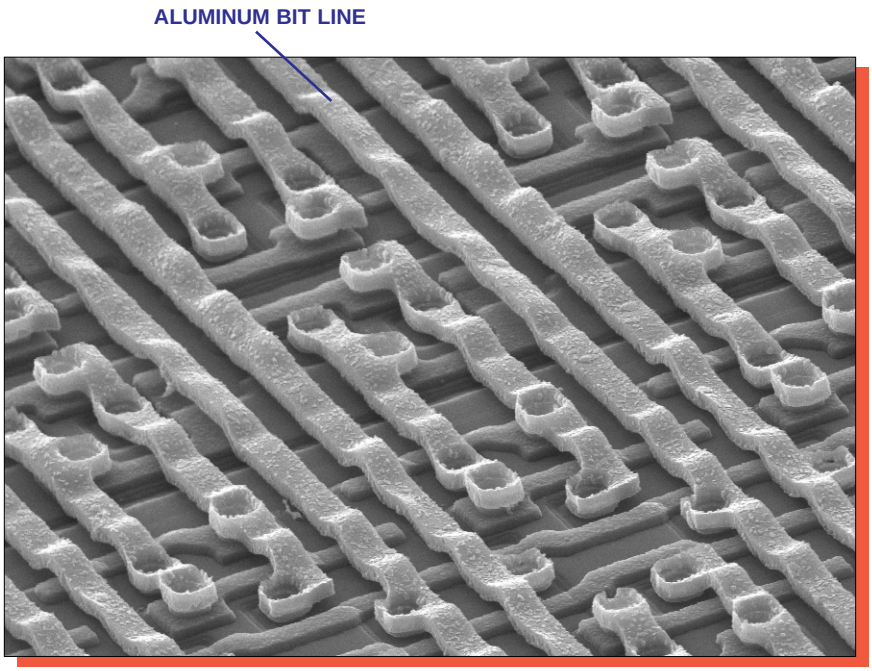


Mag. 6000x

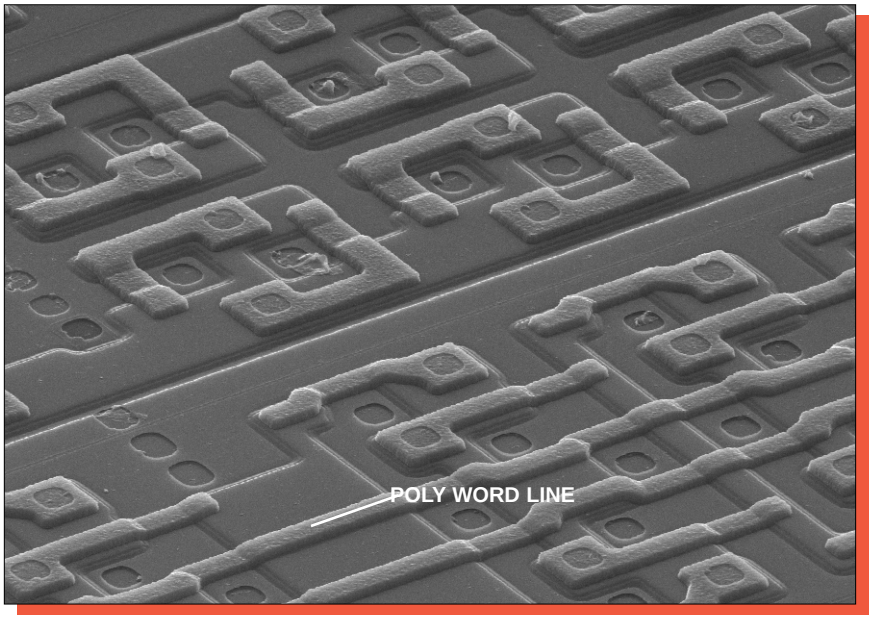


Mag. 12,000x

Figure 17c. SEM section views of the NAND ROM cell array.

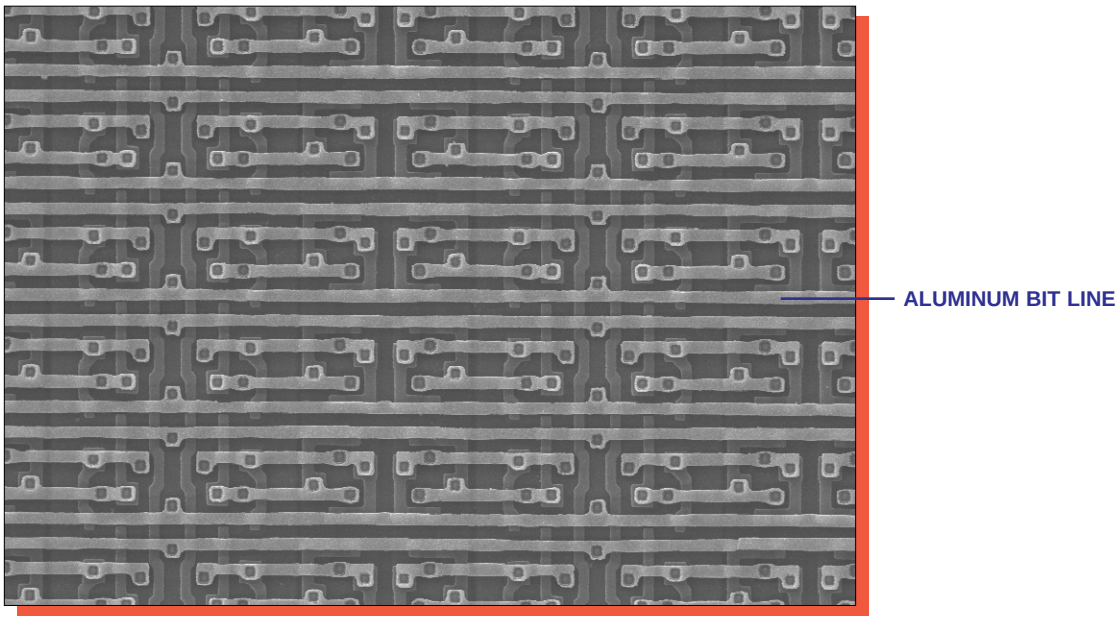


metal

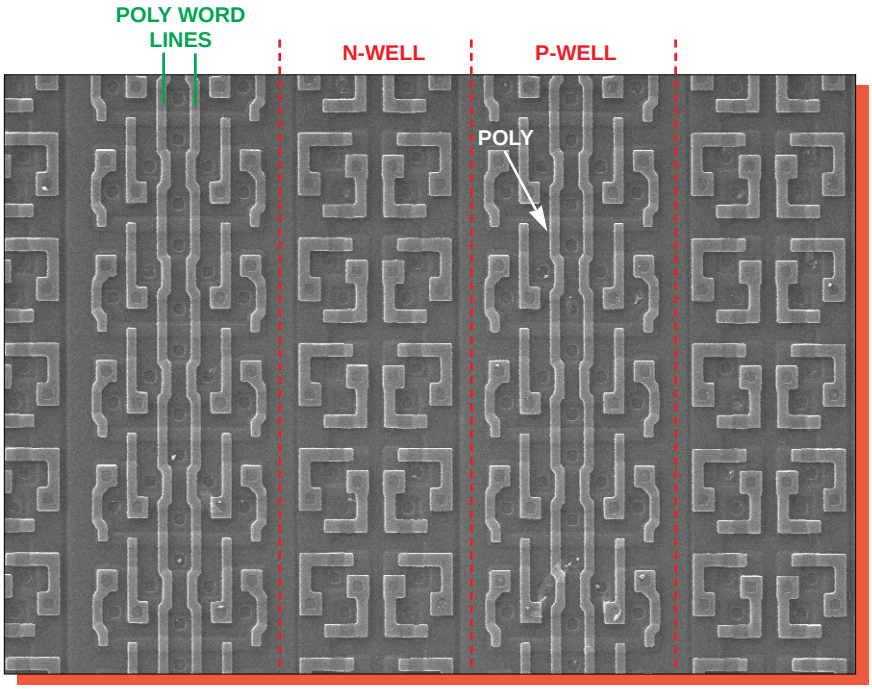


unlayered

Figure 18. SEM views illustrating the 6T SRAM cell array. Mag. 2500x, 60°.

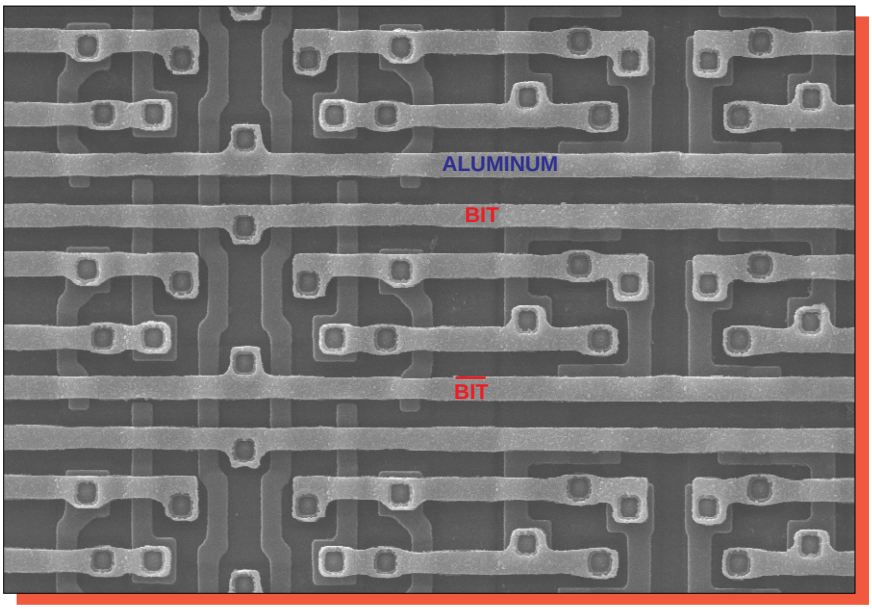


metal

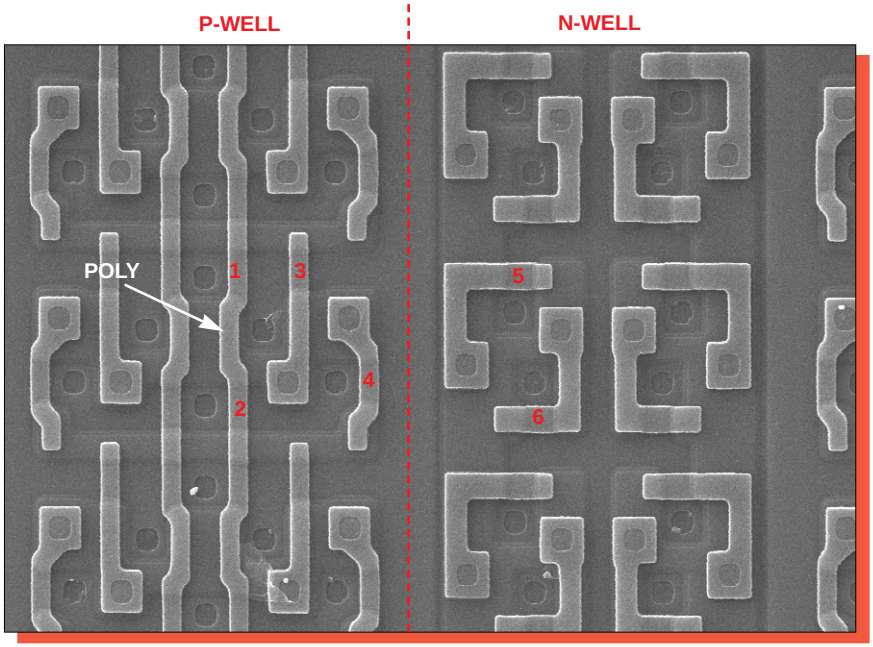


unlayered

Figure 18a. Topological SEM views illustrating the 6T SRAM cell array. Mag. 775x, 0°.



metal



unlayered

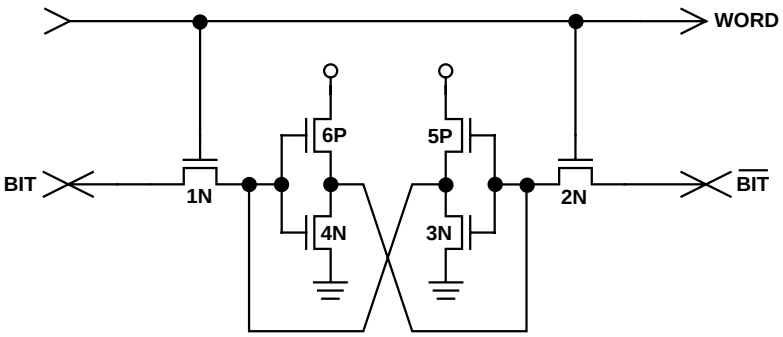
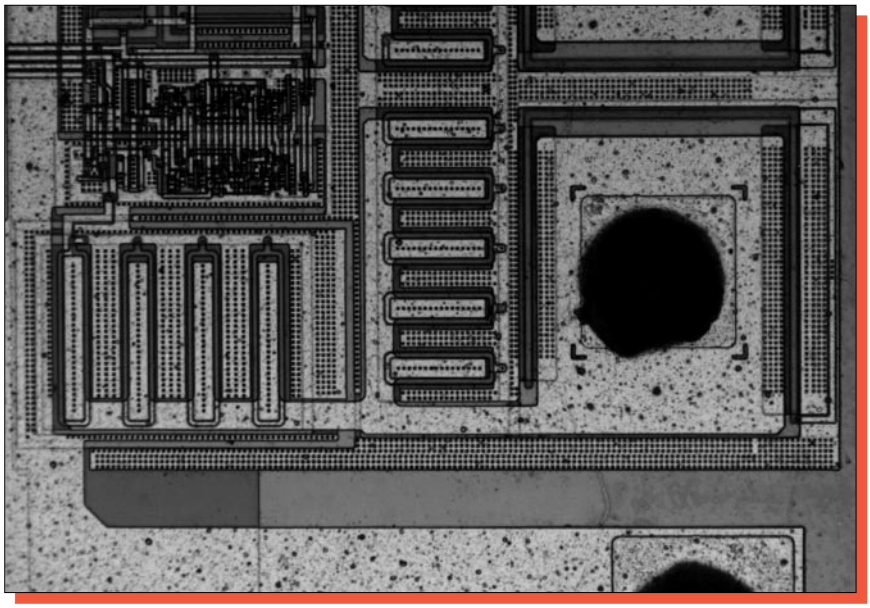
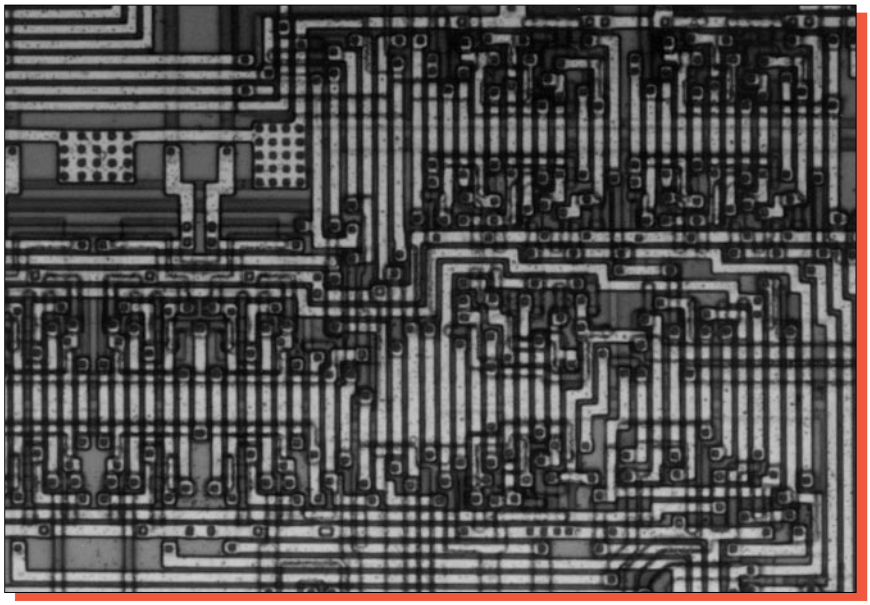


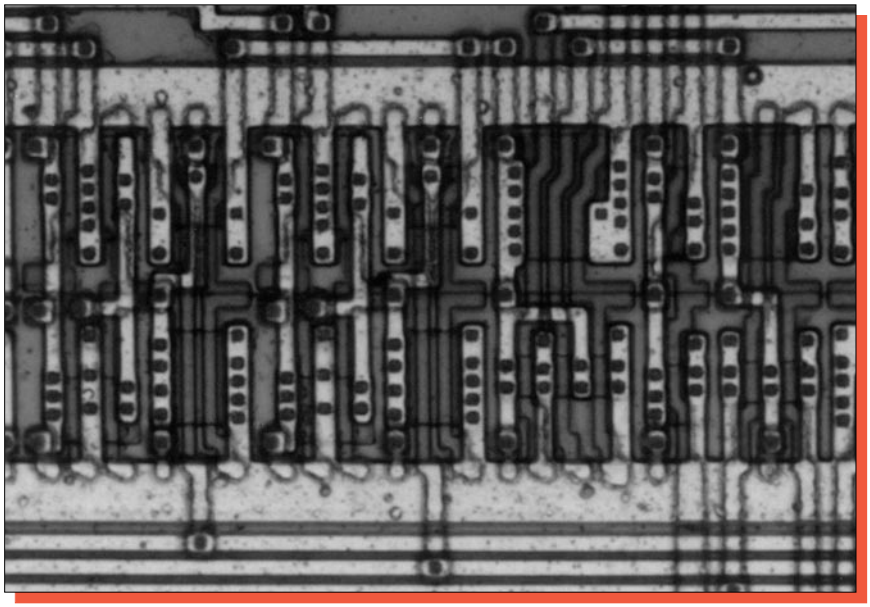
Figure 18b. Topological SEM view illustrating 6T SRAM cell array along with schematic. Mag. 1500x, 0°.



Mag. 200x



Mag. 500x



Mag. 800x

Figure 19. Optical views illustrating typical I/O structure and typical circuitry.

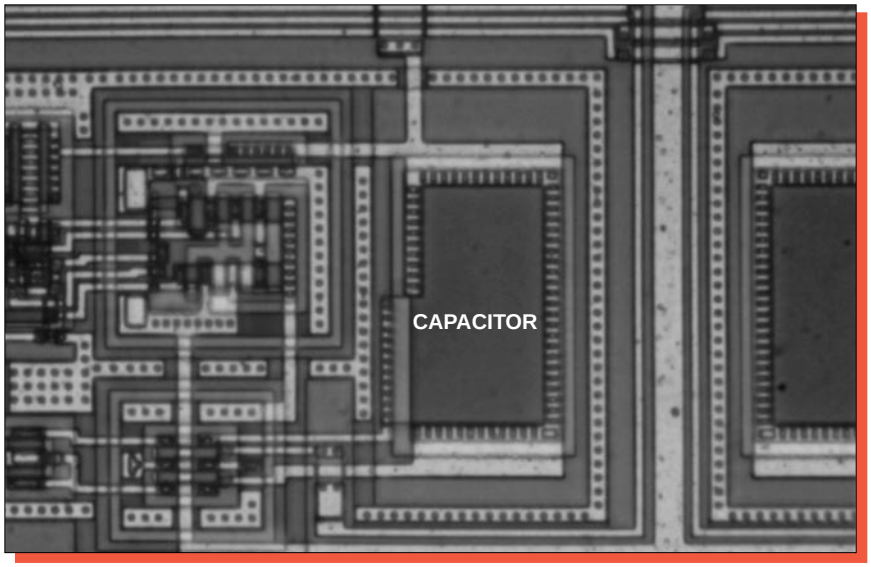
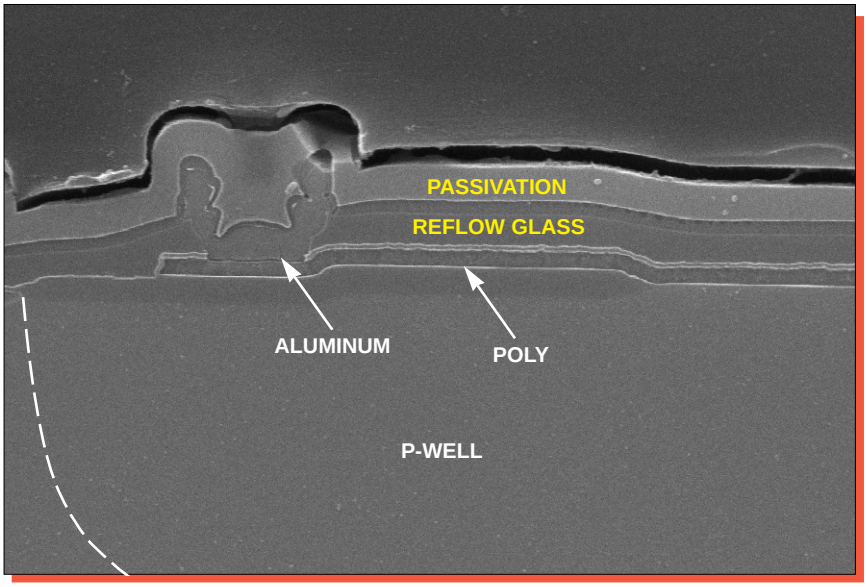
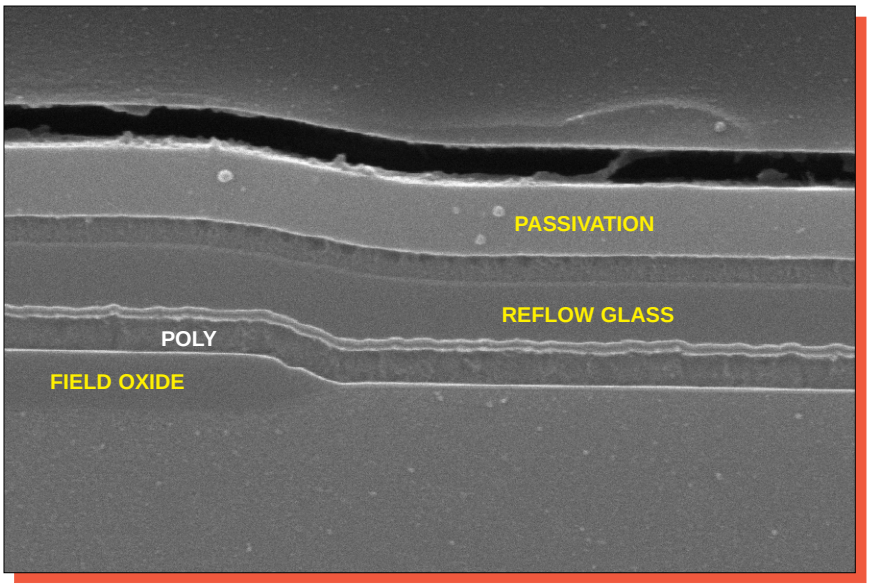


Figure 20. Optical view of a typical capacitor. Mag. 400x.



Mag. 6500x



Mag. 13,000x

Figure 21. SEM section views of typical capacitor.