# **Construction Analysis**

# Samsung KM684000ALG-7 4 Meg. SRAM



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#### **INTRODUCTION**

This report describes a construction analysis of the Samsung KM684000ALG-7, 4 Mbit (512K x 8 bit) SRAM. Three devices packaged in 32-pin plastic SOP packages were received for the analysis. All samples were date coded 606Y (9606). Special emphasis was requested on areas affected by packaging.

# **MAJOR FINDINGS**

Questionable Items:<sup>1</sup> None.

#### **Special Features:**

- Very complex four layer poly process.
- Thin-film stacked PMOS load transistor (TFT) SRAM cell.
- Multiple-well CMOS process, no epi.
- Reflowed aluminum 1 contacts.

<sup>1</sup>*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.* 

#### **TECHNOLOGY DESCRIPTION**

# Assembly:

- The devices were packaged in 32-pin plastic Small Outline Packages (SOPs) with gull-wing leads for surface mount applications.
- Lead-locking leadframe design (anchors) on all pins. Pins 16 and 32 had a split leadframe design to allow multiple bonding on these pins. Pin 16 (GND) was connected internally to the paddle for biasing purposes. Additional ground points were made with wirebonds contacting the paddle.
- The stamped leadframe was constructed of iron-nickel (FeNi) and plated externally with tin-lead (SnPb) solder.
- Internal leadframe plating was by gold over silver over a copper flash. Internal plating was present beneath the die and at paddle edges only. No die backside plating was present.
- A dimpled paddle was employed for added strength.
- Die separation by sawn dicing (full depth).
- Die attach was by silver-filled epoxy.
- Wirebonding by the thermosonic ball bond method using 1.2 mil gold wire.
- A thin, even polyimide die coat was employed and patterned around fuses, bond pads, and die corners.

#### TECHNOLOGY DESCRIPTION (continued)

#### Die Process

- Fabrication process: Selective oxidation CMOS process employing multiple wells in a P-substrate. No epi was present.
- Final passivation: A layer of nitride over a thin layer of glass.
- Metallization: Metal 2 consisted of silicon-doped aluminum defined by dry-etch techniques. It did not use a cap or barrier layer. Metal 1 consisted of aluminum and employed a titanium-nitride cap and barrier. A thin titanium layer remained below the titanium-nitride. Standard vias and aluminum-filled (reflowed) contacts were employed. Special patterning of metal 2 and 1 bus lines was used at the corners of the die. Both metals employed slotted lines, beveled (angled) corners and multiple contact arrays. Metal 2 also contained some cutouts and had some isolated vias.
- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of a multilayered glass followed by a spin-on-glass (SOG) and another layer of glass.
- Pre-metal dielectric: A layer of reflow glass over a layer of silicon-nitride, over various densified oxides in the peripheral circuitry. Another layer of reflow glass and another layer of nitride were present in the memory array over poly 4.
- Polysilicon: Four layers of polysilicon were employed. Poly 1 was used to form all standard gates on the die. Polycide 2 (poly 2 and tungsten silicide) was used as a third metal to distribute word lines and ground in the array, and to form all fuses. Polycide 2 was also used as a layer of interconnect throughout peripheral circuitry and made direct contact to N+ diffusions and poly 1. Unusual Polycide 2 features were used in the decode circuitry (Figure 33). Poly 3 was used to form PMOS thin film transistor (TFT) gates and as an interconnect for bit line contacts. A very thin Poly 4 was used for the body of TFTs and to distribute Vcc.

## **<u>TECHNOLOGY DESCRIPTION</u>** (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and were left in place.
- Wells: Multiple-wells in a P substrate. A P-well was located within a deep N-well in the cell array only.
- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present. All redundancy fuses were formed with Polycide 2.
- Memory cells: The memory cells consisted of two select gates, two storage gates, two PMOS thin film transistors, and some apparent cross-coupling capacitor regions. Metal 1 formed the bit lines, poly 1 was used to form the storage and select gates. Polycide 2 was used to distribute ground along with metal 1 and 2. Polycide 2 also formed the word lines. Poly 3 formed the PMOS thin film transistor (TFT) gates and was used as interconnect for bit line contacts. Poly 4 formed the TFT bodies and Vcc distribution.

# ANALYSIS RESULTS I

#### Assembly:

#### **Figures 1 - 8**

#### **Questionable Items:**<sup>1</sup>

• Relatively poor die dicing, resulted in considerable chipping at the top of die edges. No cracks were found and no serious concern exists.

#### **Special Features:**

• Patterned polyimide die coat cleared at die corners.

#### **General Items:**

- Overall package quality: Good. No significant defects were found on the external or internal portions of the packages. No voids or cracks were noted in the plastic. The encapsulant compound consisted of an epoxy-resin with a silica filler. The filler was shaped in the form of beads. The leadframe was formed by a stamping process. Externally, tinning of the leads was complete. Internal silver plating was present beneath the die.
- Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. Normal intermetallic formation was found at the ball bonds. All bond pull strengths were normal and no bond lifts occurred (see page 10). The die surface was covered with a patterned polyimide die coat (cleared over bonding pads, fuses, and die corners). The bond pad structure used both metals 1 and 2 in direct contact.
- Die attach: An adequate amount of silver-filled epoxy. No problems were found.
- Die dicing: Die separation was by sawing (full depth) and showed normal to poor quality workmanship. Some large chips and metal slivers were present at the die surface.

<sup>1</sup>*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.* 

# ANALYSIS RESULTS II

#### **Die Process and Design:**

#### **Figures 9 - 60**

#### **Questionable Items:**<sup>1</sup>

• Metal 2 aluminum thinning up to 85 percent<sup>2</sup> at vias (Figure 28) and silicon nodules consumed up to 85 percent of some M2 lines (Figure 26). These are not considered serious concerns.

#### **Special Features:**

- Multiple well CMOS process.
- Reflowed aluminum contacts.
- Thin-film stacked PMOS load transistors (TFT) SRAM cell using four layers of poly.

#### **General Items:**

- Fabrication process: Complex selective oxidation CMOS process employing multiple wells in a P-substrate (no epi). No significant problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A layer of nitride over a thin layer of glass. Passivation integrity

<sup>1</sup>*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.* 

<sup>2</sup>Seriousness depends on design margins

#### ANALYSIS RESULTS II (continued)

tests indicated defect-free passivation. Edge seal was also good. (A patterned polyimide die coat was used on these dice).

- Metallization: Metal 2 consisted of silicon-doped aluminum defined by a dryetch technique. It did not use a cap or barrier. Metal 1 consisted of aluminum and employed a titanium-nitride cap and barrier. A thin titanium layer was left below the titanium-nitride. Standard vias (M2 to M1) and aluminum-filled contacts (M1 to silicon) were employed. Vias of various sizes and shapes were present. Both metals employed slotted metal lines, beveled/angled corners and multiple contact arrays.
- Metal patterning/metal defects: Both metal layers were defined by a dry-etch. Some large silicon-nodules were noted following the removal of the metal 2 layer. They consumed up to 85 percent of metal 2 line widths (see Figure 24).
- Metal step coverage: Metal 2 aluminum thinned up to 85 percent at vias. Typical metal 2 thinning was 80 percent. Military standards allow up to 70 percent metal thinning at contacts of this size. Virtually no metal 1 thinning was present due to the use of aluminum reflow at contacts.
- Vias and contacts: Via and contact cuts appeared to be defined by a two-step etch. Some minor over-etching was found at contacts. Standard vias and aluminum-filled contacts were employed. Vias (M2) were of various sizes and shape. Both metals employed multiple contact arrays.
- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of a multilayered glass followed by a spin-on glass (SOG) for planarization, and another layer of glass. No problems were found.

#### ANALYSIS RESULTS II (continued)

- Pre-metal dielectric: A single layer of reflow glass (BPSG) over various densified oxides in peripheral circuit areas. A thin nitride layer was present below the reflow glass. An additional layer of nitride and reflow glass was used in the memory array.
- Polysilicon: Four layers of polysilicon were employed. Poly 1 was used to form all standard gates on the die. Polycide 2 (poly 2 and tungsten silicide) was used to distribute word lines and ground in the array. Polycide 2 was also used as a layer of interconnect throughout peripheral circuitry and made direct contact to N+ diffusions and poly 1. In addition, Polycide 2 was used for redundancy fuses and for some undefined special structures (Figure 33). Poly 3 was used to form PMOS thin film transistor (TFT) gates and as an interconnect for bitline contacts. A very thin Poly 4 was used for the body of TFTs and to distribute Vcc. No problems were found in any of these layers.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. An LDD process was used employing oxide sidewall spacers. The spacers were left in place. No problems were found in any of these areas.
- Wells: Multiple-wells were used in a P-substrate (no epi). Definition was normal. Standard N- and P-wells were used throughout most of the die. A P-well within a deep N-well was present beneath the array only.
- Buried contacts: Poly 4 and 3 formed interpoly/buried contacts in the cell array only, and as mentioned polycide 2 contacted poly 1 and N+ directly. Again no problems were apparent here either.

#### ANALYSIS RESULTS II (continued)

- Fuses: All redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present. All redundancy fuses were formed with Polycide 2.
- Memory cells: The memory cells consisted of two select gates, two storage gates, two PMOS thin film transistors, and some apparent cross-coupling capacitor regions. Metal 1 formed the bit lines, poly 1 was used to form the storage and select gates. Polycide 2 was used to distribute ground along with metal 1 and 2. Polycide 2 also formed the word lines. Poly 3 formed the PMOS thin film transistors (TFT) gates and was used as a interconnect for bit line contacts. Poly 4 formed the TFT bodies and Vcc distribution. Cell pitch was 2.65 x 5.3 microns (11.9 microns<sup>2</sup>).

# **PROCEDURE**

The devices were subjected to the following analysis procedures:

External inspection
X-ray
Package section and material analysis
Decapsulate
Internal optical inspection
SEM inspection of assembly features and passivation
Wirepull test
Passivation integrity test
Delayer to metal 2 and inspect
Aluminum removal (metal 2), inspect silicon nodules
Delayer to metal 1 and inspect
Aluminum removal (metal 1), inspect barrier
Delayer to poly/substrate and inspect poly and substrate
Die sectioning (90° for SEM)*
Measure horizontal dimensions
Measure vertical dimensions
Die material analysis

\*Delineation of cross-sections is by silicon etch unless otherwise indicated.

# **OVERALL QUALITY EVALUATION:** Overall Rating: Normal

# **DETAIL OF EVALUATION**

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	G
Die attach quality	Ν
Dicing quality	NP
Die attach method	Silver-filled epoxy
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.

Die surface integrity:		
Toolmarks (absence)	G	
Particles (absence)	G	
Contamination (absence)	G	
Process defects (absence)	Ν	
General workmanship	Ν	
Passivation integrity	G	
Metal definition	Ν	
Metal integrity	NP*	
Metal registration	G	
Contact coverage	G	
Contact registration		

\*85 percent metal 2 aluminum thinning and large silicon nodules. G = Good, P = Poor, N = Normal, NP = Normal/Poor

# PACKAGE MARKINGS

# <u>TOP</u>

# **BOTTOM**

Samples 1 & 2:	SEC KOREA 606Y KM684000ALG-7	4KJ 014 X AA (plus molded markings)
Sample 3:	"	4KJ 003 X AA

(plus molded markings)

# WIREBOND STRENGTH

Wire material:	1.2 mil diameter gold	
Longest wire:	47 mils	
Die pad material:	aluminum	
Material at package lands:	silver	
# of wires pulled:	30	
Bond lifts:	0	
Force to break - high:	11.0 g	
- low:	6.0 g	
- avg.:	8.6 g	
- std. dev.:	1.2	

# PACKAGE MATERIAL ANALYSIS

Encapsulant compound:	Epoxy-resin with a silica bead filler.
Leadframe:	Iron-nickel (FeNi).
External pin plating:	Tin-lead (SnPb) solder.
Internal plating:	Gold (Au) on Silver (Ag) on a flash of copper (Cu).
Die attach:	Silver (Ag)-filled epoxy.
Die coat:	Spun-on and patterned polyimide (visual).

# **DIE MATERIAL ANALYSIS**

Die coat:	Polyimide.
Overlay passivation:	A layer of nitride over a thin layer of glass.
Metallization 2:	Silicon-doped aluminum.
Interlevel dielectric 1 (M2 to M1):	Two layers of silicon-dioxide with a planarizing glass (SOG) between.
Metallization 1:	Aluminum with a titanium-nitride cap and barrier over a thin titanium adhesion layer.
Pre-metal dielectric:	A layer of BPSG reflow glass over a thin layer of silicon-nitride, over densified oxide in the peripheral circuit area. An additional layer of BPSG reflow glass over a thin layer of silicon nitride were present between polycide 2 and poly 3 in the memory array.
Polycide:	Tungsten-silicide on polysilicon 2.

# HORIZONTAL DIMENSIONS

Die size:	6.6 x 11.8 mm (275 x 468 mils)	
Die area:	77.8 mm <sup>2</sup> (128,700 mils <sup>2</sup> )	
Min pad size:	0.12 x 0.12 mm (4.7 x 4.7 mils)	
Min pad window:	0.10 x 0.10 mm (4.3 x 4.3 mils)	
Min pad space:	0.08 mm (3.2 mils)	
Min pad pitch:	0.20 mm (7.9 mils)	
Min pad to metal:	18 microns	
Min metal 2 width:	1.4 micron	
Min metal 2 space:	1.4 micron	
Min metal 2 pitch:	2.8 microns	
Min via:	1.3 micron	
Min via space - continuous:	0.55 micron	
Min via pitch - continuous:	1.8 micron	
Min metal 1 width:	0.6 micron	
Min metal 1 space:	0.8 micron	
Min metal 1 pitch:	1.4 micron	
Min contact:	0.85 micron	
Min contact space - continuous:	0.45 micron	
Min contact pitch - continuous:	1.3 micron	
Min poly 4 width:	0.4 micron	
Min poly 4 space:	0.5 micron	
Min poly 3 width:	0.8 micron	
Min poly 3 space:	0.4 micron	
Min polycide 2 width:	0.35 micron	
Min polycide 2 space:	0.65 micron	
Min polycide 2 pitch:	1.0 micron	
Min poly 1 width:	0.65 micron	
Min poly 1 space:	0.5 micron	
Min poly 1 pitch:	1.4 micron	
Min gate length <sup>*</sup> - (N-channel):	0.65 micron	
- (P-channel):	0.8 micron	
Sidewall spacer width:	0.15 micron (approximate)	
Cell size:	11.7 microns <sup>2</sup>	
Cell pitch:	2.6 x 4.5 microns	

\*Physical gate length.

# **VERTICAL DIMENSIONS**

Die thickness: Die attach: 0.3 mm (12.0 mils) 27 microns

# <u>Layers</u>

Die coat (polyimide):	9.5 microns
Passivation 2:	0.5 micron
Passivation 1:	0.1 micron
Metal 2 - aluminum:	0.9 micron
Interlevel glass - glass 3:	0.3 micron
- glass 2 (SOG):	0.05 - 0.5 micron
- glass 1:	0.5 micron
Metal 1 - cap:	0.08 micron (approximate)
- aluminum:	0.7 micron
- barrier:	0.16 micron
Reflow glass 2:	0.6 to 0.7 micron
Poly 4:	0.02 micron (approximate)
Interpoly oxide 3 (TFT gate ox.):	0.02 micron (approximate)
Poly 3:	0.1 micron (approximate)
Reflow glass 1:	0.3 to 0.4 micron
Polycide 2 - silicide:	0.1 micron
- poly:	0.1 micron
Interpoly oxide 1:	0.1 micron (approximate)
Poly 1:	0.15 micron
Nitride layers:	0.04 micron (approximate)
Local oxide:	0.35 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.3 micron
N- well:	6 microns
Memory P-well (inside N-well):	3 microns
Peripheral P-well	could not delineate

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top view



A18	1	32		VCC
A16	2	31		A15
A14	3	30		A17
A12	4	29		WE
A7	5	28		A13
A6	6	27		A8
A5	7	26		A9
A4	8	25		A11
A3	9	24		ŌĒ
A2	10	23		A10
A1	11	22		CS
A0	12	21		I/O8
I/O1	13	20		I/07
I/O2	14	19		I/O6
I/O3	15	18		I/O5
٧ <sub>SS</sub>	16	17		I/O4
			1	

bottom view





Figure 3. Section view of the package illustrating general construction. Mag. 16x.



Mag. 40x





Figure 4. Package section views illustrating lead formation and lead exit.







Figure 6. Optical and SEM views illustrating typical ball bonds.



Mag. 800x

Mag. 6500x



Mag. 13,000x



Mag. 200x









Mag. 500x

Mag. 320x

Figure 11. Optical views of die markings and alignment keys.



Figure 12. Optical views of the die corners on the Samsung KM684000 ALG-7 device. Mag. 200x.



metal 2



Figure 13. Optical views of metal structure at the die corner. Mag. 200x.



Mag. 800x

Figure 14. Optical views of metal patterning.



metal 1, Mag. 200x



metal 2, Mag. 320x

Figure 15. Optical views illustrating slotted metal (GND) pad lines.



Mag. 1600x



Photo A, Mag. 10,000x

Figure 16. SEM section views of the die edge seal on the Samsung KM684000 ALG-7 device.



photo B





Figure 17. SEM section views of the die edge seal on the Samsung KM684000 ALG-7 device. Mag. 6500x.



passivation removed, Mag. 12,500x



passivation removed, Mag. 10,000x



90° section, glass etch, Mag. 10,000x


silicon etch, Mag. 13,000x



glass etch, Mag. 16,000x



Mag. 3000x



Mag. 10,000x

Figure 20. SEM views of passivation coverage.  $60^{\circ}$ .



Mag. 13,000x





Figure 21. SEM section views of metal 2 line profiles.



Mag. 3000x



Mag. 3000x

Mag. 3300x

Figure 22. Topological SEM views of metal 2 patterning. 0°.



Figure 23. SEM views of general metal 2 integrity.  $60^{\circ}$ .



Mag. 5000x, 60°





# Figure 24. SEM views of metal 2 silicon nodule coverage.







Figure 26. SEM section views of metal 2-to-metal 1 vias.



Mag. 26,000x







Mag. 4000x

Mag. 5000x

Mag. 6500x



Figure 29. SEM views of general metal 1 integrity.  $60^{\circ}$ .



Mag. 12,000x

Mag. 20,000x

Mag. 40,000x



metal 1-to-polycide 2







metal 1-to-diffusion, Mag. 13,000x



metal 1-to-N+, Mag. 26,000x



metal 1-to-P+, Mag. 26,000x





Figure 33. SEM views of polycide 2-to-diffusion contacts. Mag. 20,000x, 60°.







Figure 35. SEM view of polycide 2-to-poly 1 contacts. Mag. 26,000x, 60°.



Figure 36. SEM section views of typical polycide 2 contacts. Mag. 26,000x.



# Mag. 2000x



#### Mag. 4000x



Figure 38. Topological SEM views of poly patterning within column and row decode areas.  $0^{\circ}$ .



Figure 39. SEM views of poly 1 coverage.  $60^{\circ}$ .









Figure 41. SEM section views of typical transistors. Mag. 52,000x.

CELL ARRAY				
¥	=			
	N-WELL			
P-WELL	P-SUBS	TRATE	N-WELL	
· · · · · ·	1.1.			

Figure 42. Optical view of the well structure. Mag. 800x.



Figure 43. SEM section views of a step in the local oxide and a local oxide birdsbeak.





Figure 44. Optical views of redundancy fuses. Mag. 500x.







Figure 46. Topological SEM views of typical redundancy fuses. Mag. 3300x, 0°.



## Mag. 6500x



Mag. 13,000x



#### Mag. 6500x







metal 2







poly 4 and 3





Figure 51. Perspective SEM views of the SRAM cell array. Mag. 10,000x,  $60^{\circ}$ .



#### metal 1



unlayered

Figure 52. Topological SEM views of the GND connection in the array. Mag. 6500x,  $0^{\circ}$ .



Figure 53. Additional detailed views of the SRAM cell.  $60^{\circ}$ .



metal 1





## Figure 54. Detailed topological SEM views of the SRAM cell. Mag. 13,000x, $0^{\circ}$ .



poly 2 and 1 (under nitride)





Mag. 13,000x



Mag. 26,000x



Mag. 30,000x





Mag. 13,000x



Mag. 26,000x



Mag. 30,000x



silicon etch, Mag. 13,000x



glass etch, Mag. 13,000x



glass etch, Mag. 26,000x



Figure 59. Optical views of a typical input/output structure. Mag. 320x.
Samsung KM684000 ALG-7



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 60. Color cross section drawing illustrating device structure.