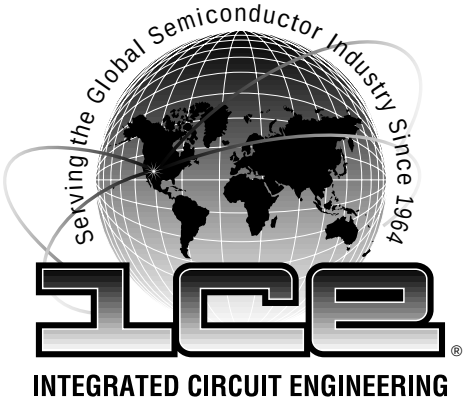
Construction Analysis

Maximum MAX662
12V DC-DC Converter

Report Number: SCA 9512-445



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INTRODUCTION

This report describes a construction analysis of the Maxim MAX662 12V DC-DC Converter. Eight devices, packaged in 8-pin small-outline packages, were supplied for the analysis. The devices were date coded 9537.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Fusible metal link networks to select resistance values (Figures 21 and 22).
- P-well resistor arrays (Figure 24).
- Circular poly gate structures (Figure 23).
- Six large transistor arrays (Figure 23a).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- 8-pin plastic Small Outline Package (SOP) for surface mount applications.
- Leadframe and header/paddle constructed of copper.
- External gull-wing leads plated with tin-lead and internally spot plated with silver.
- A silver-epoxy die attach was employed.
- Lead-locking provisions (anchors) were present at all pins.
- Multiple bonding wires were used at pin 7 (GND) to provide extra current-carrying capacity. All pins were connected.
- Thermosonic wirebonding using 1.0 mil O.D. gold wire.
- Dicing was by sawing (full depth).

Die Process and Design:

- The device was fabricated by a P-well CMOS process which utilized selective oxidation. No epi was present on the N substrate.
- Overlay passivation consisted of a layer of silicon-nitride over a layer of glass.
- A single level of silicon-doped aluminum interconnect was defined by a dry-etch technique. No cap or barrier metals were used.
- Intermediate glass consisted of a BPSG reflow glass over densified oxides.
- A single layer of dry-etched polysilicon was used to form all gates. No silicide was employed on the poly.

TECHNOLOGY DESCRIPTION (continued)

- Standard implanted N+ and P+ source/drain diffusions were used. No evidence of an LDD process was noted.

- No buried contacts (poly-to-diffusion) were employed.

- Design features: Two fusible metal link networks were employed to select resistance values. Two P-well resistor arrays which employed poly field plates over the resistors were present on the device . Circular poly gate structures were present in the periphery. Six large transistor arrays were present on the devices which occupied approximately 70 percent of the die area (see Figures 21 - 24).

ANALYSIS RESULTS I

Assembly: **Figures 1 - 7**

Questionable Items:[1] None.

General Items:

- The device was encapsulated in an 8-pin plastic Small Outline Package with gull-wing leads.

- Overall package quality: Good. No defects were found on the external or internal portions of the package. External pins were well formed and tinning of the leads was complete. No significant gaps were present at lead exits.

- Leadframe: Copper (Cu) leadframe externally tinned with tin-lead (SnPb) solder and spot plated internally with silver (Ag).

- Die attach: A silver-epoxy die attach of normal quality. No voids were noted.

- Die dicing: Die separation was by sawing (full depth) with normal quality and workmanship.

- Wirebonding: Thermosonic ball bond method using 1.0 mil O.D. gold wire. Wirebond placement was good. Wire clearance and spacing were normal. Ball bonds were well formed and intermetallic formation was complete. Bond pull strengths were good (see page 10) with no bond lifts.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process: **Figures 8 - 25**

Questionable Items:[1] None.

Special Features:

- Fusible metal link networks to select resistance values (Figures 21 and 22).
- P-well resistor arrays (Figure 24).
- Circular poly gate structures (Figure 23).
- Six large transistor arrays (Figure 23a).

General Items:

- Fabrication process: Selective oxidation CMOS process employing P-wells in an N substrate. No epi was used.
- Process implementation: Die layout was clean. Alignment was good at all levels and no damage, process defects, or contamination was found.
- Overlay passivation: A layer of silicon-nitride over a layer of glass. Overlay integrity tests indicated defect-free passivation. Edge seal was also good as the passivation extended past the metal at the die edge.
- Metallization: A single level of metallization, consisting of silicon-doped aluminum. No cap or barrier layers were used with the metal.
- Metal patterning: Metal was defined by a dry etch of good quality.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal step coverage: Virtually no metal thinning was noted at contacts or elsewhere.

- Metal defects: No voiding, notching or neckdown of the metal was found. Contacts were completely surrounded by metal. Silicon nodules occupied up to only 35 percent of metal line widths.

- Contact defects: None. Contact cuts appeared to be defined by a wet etch. No overetching of the contacts was found. No contact pitting was found and no significant silicon mound growth was present.

- Intermediate glass: A BPSG reflow glass over densified oxides. The glass was reflowed prior to contact cuts. No problems were found in this layer.

- Polysilicon: A single layer of dry-etched polysilicon (no silicide) was used to form all gates on the die. Definition of the poly layer was good and no problems were noted.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the transistors. No evidence of an LDD process was noted. No problems were found.

- No buried contacts were used on the device.

- Wells: P- wells were used in a N substrate. No epi layer was used. Definition of the wells was normal.

- Design features: Two fusible metal link networks were present on the device. These networks were used to select the resistance values of the P-well resistor arrays. Poly field plates were present over the resistors.

ANALYSIS RESULTS II (continued)

- Circular poly gate structures were present in the periphery. We presume the purpose for this design is balanced operation since orientation of gates does have an effect on operational characteristics. Six large transistor arrays were present on the device. These arrays occupied approximately 70 percent of the die area.

- ESD test: One device was subjected to an ESD test. All pins passed pulses of ±4000V.

- Latch-up test: One device was subjected to a latch-up test per JEDEC standard No. 17. Pins were tested from -200ma to +200ma. No pins latched-up on the device.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

ESD and Latch-up tests

X-ray

Package section

Decapsulation

Internal optical inspection

SEM of assembly features

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal

Remove aluminum and inspect

Delayer to polysilicon and inspect

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Lead conformity	G
Lead plating quality	G
Die placement	G
Die attach quality	N
Wire spacing	N
Wirebond placement	G
Wirebond quality	N
Dicing quality	N
Wirebond method	Thermosonic ball bonds using 1.0 mil gold wire
Die attach method	Silver-filled epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	G
Metal registration	N
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP	BOTTOM
MAX 662	PHILIPPINES YB
ACSA 537	MAX 537

WIREBOND STRENGTH

Wire material:	1.0 mil diameter gold
Die pad material:	aluminum
Material at package post:	silver

Sample #	**3**	**4**
# of wires tested:	9	9
Bond lifts:	0	0
Force to break - high:	11.0g	10.0g
- low:	6.0g	6.0 g
- avg.:	8.6g	8.3g
- std. dev.:	1.7	1.3

DIE MATERIAL ANALYSIS

Passivation:	Silicon-nitride over glass.
Metal 1:*	Silicon-doped aluminum. No copper was detected.
Intermediate glass:	BPSG reflow glass containing 5.7 wt. percent phosphorus and 3.6 wt. percent boron.

* *There is no known method for determining the exact amount of silicon and copper in the aluminum on a finished die.*

HORIZONTAL DIMENSIONS

Die size:	2.16 x 2.16 mm (85 x 85 mils)
Die area:	4.7 mm^2 (7225 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.1 x 0.1 mm (3.9 x 3.9 mils)
Min pad space:	0.07 mm (2.9 mils)
Min metal width:	3.1 microns
Min metal space:	2.3 microns
Min metal pitch:	5.4 microns
Min contact:	4.5 microns (round)
Min polycide width:	2.5 micron
Min polycide space:	2.5 micron
Min gate length (N-channel):	2.5 microns
(P-channel):	3.5 microns

VERTICAL DIMENSIONS

Die thickness:	(0.4 mm) 14.5 mils

Layers:

Passivation 2:	0.4 micron
Passivation 1:	0.3 micron
Metal:	1.0 micron
Intermediate glass:	0.7 micron
Oxide on poly:	0.25 micron
Poly:	0.35 micron
Local oxide:	0.75 micron
N+ source/drain:	0.3 micron
P+ source/drain:	0.45 micron
P- well:	6.0 microns

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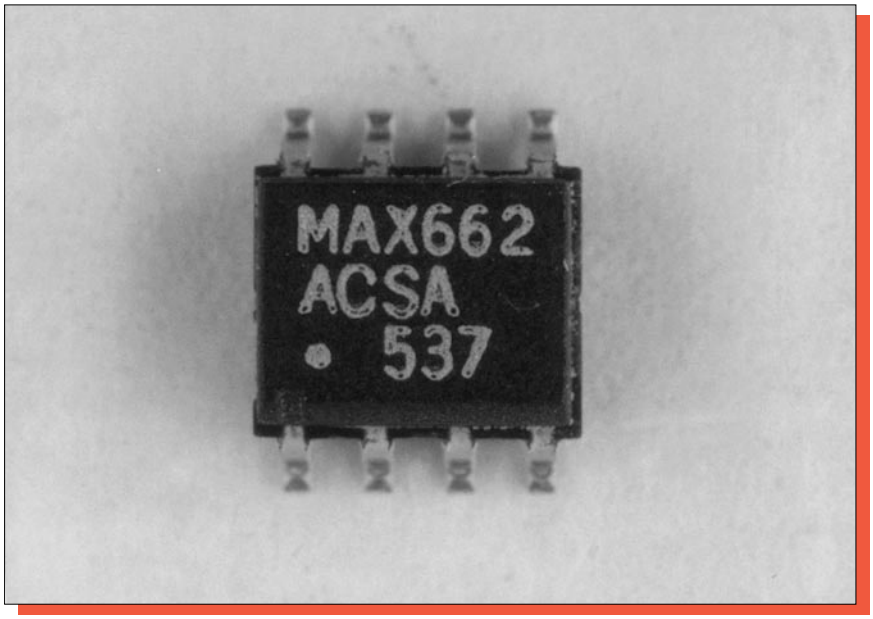
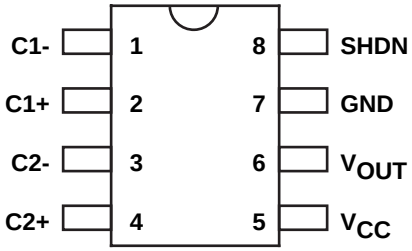




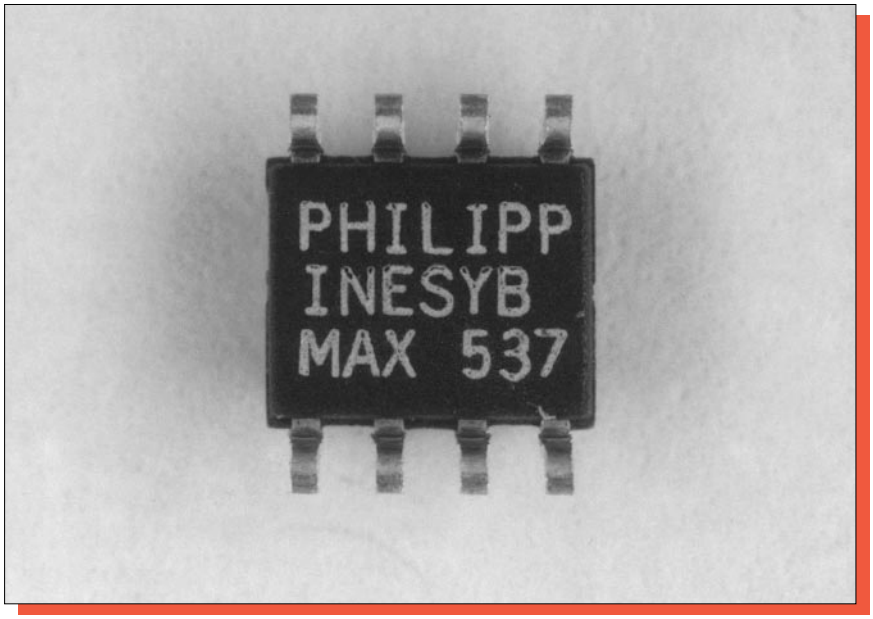
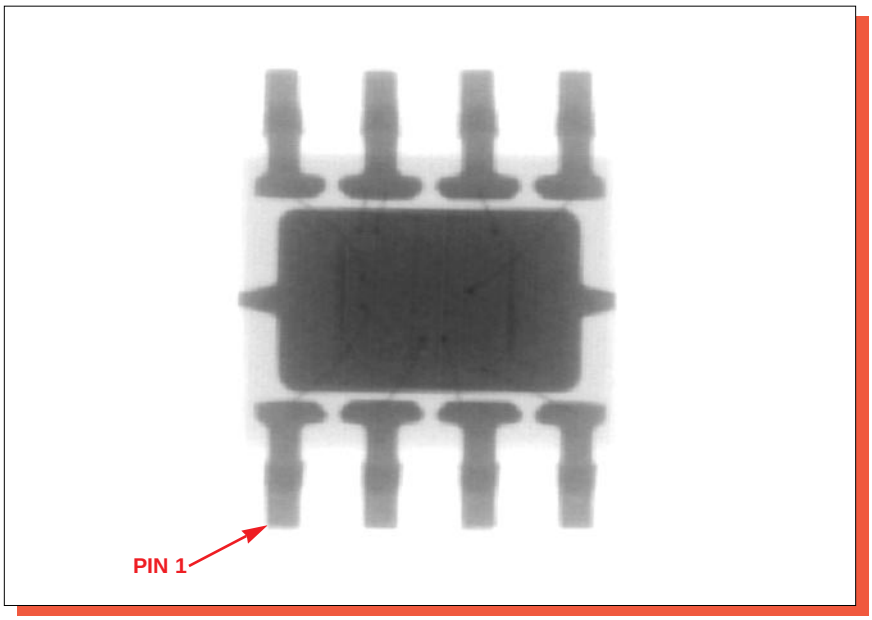


Figure 1. Package photographs and pinout diagram of the Maxim MAX662. Mag. 10x.



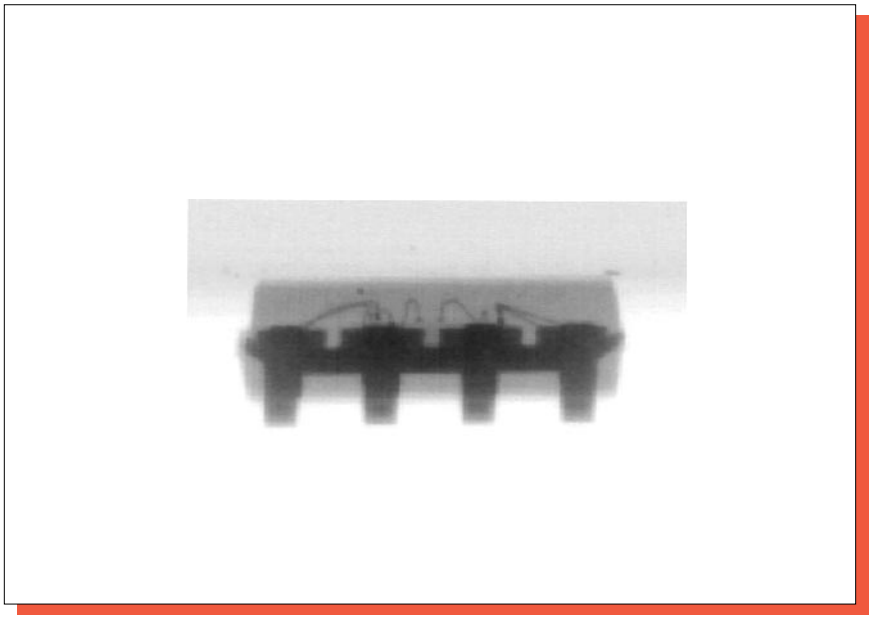


Figure 2. Topological and side x-ray views of the package. Mag. 10x.

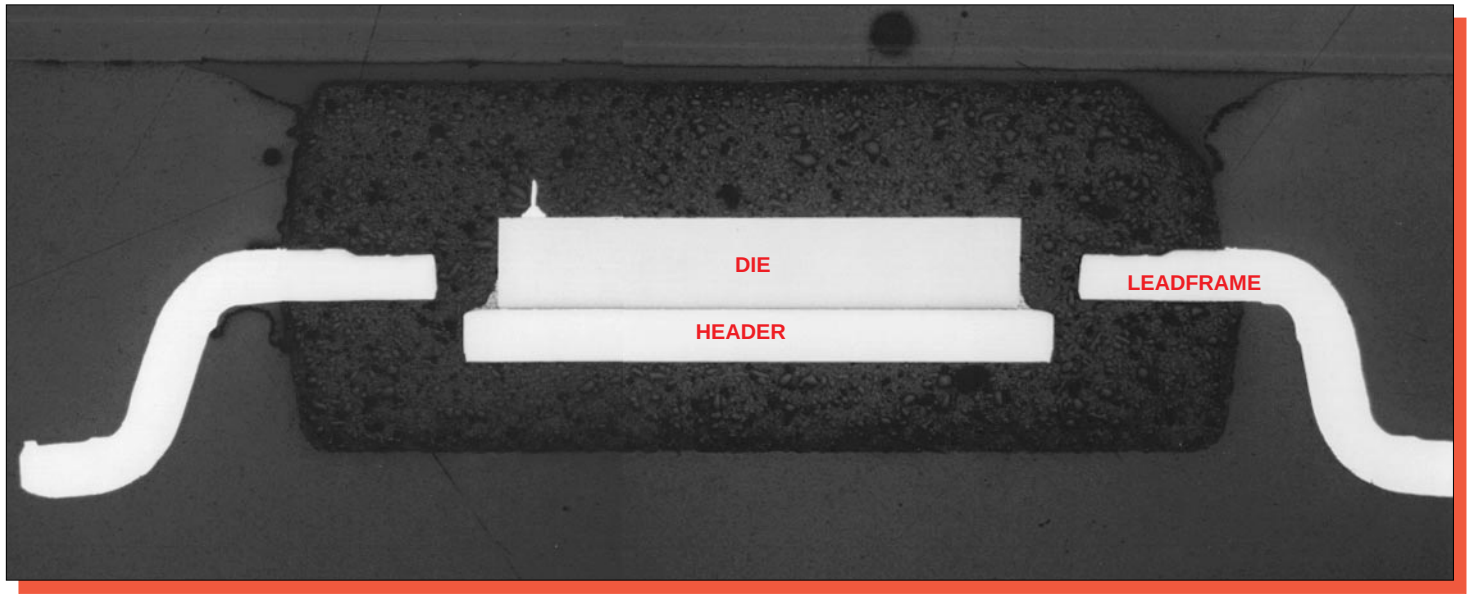
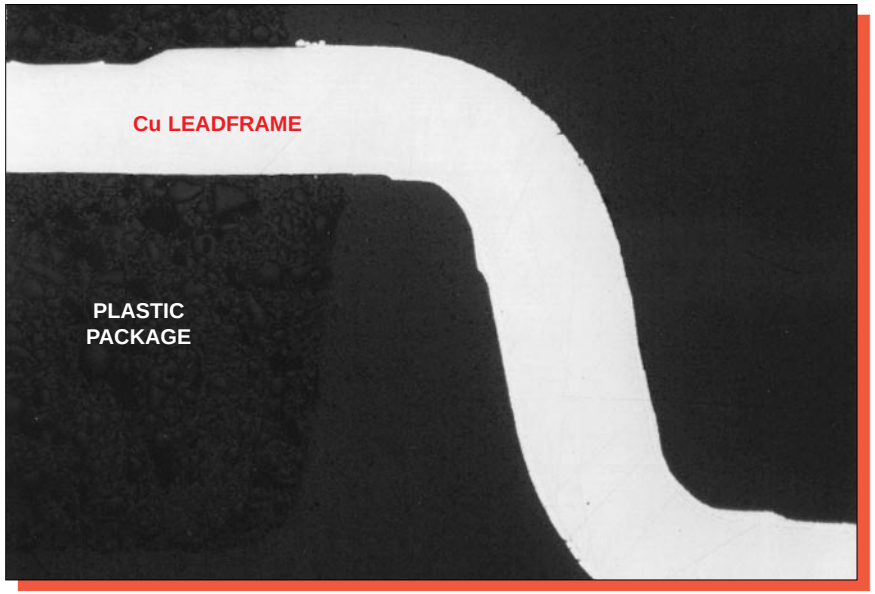
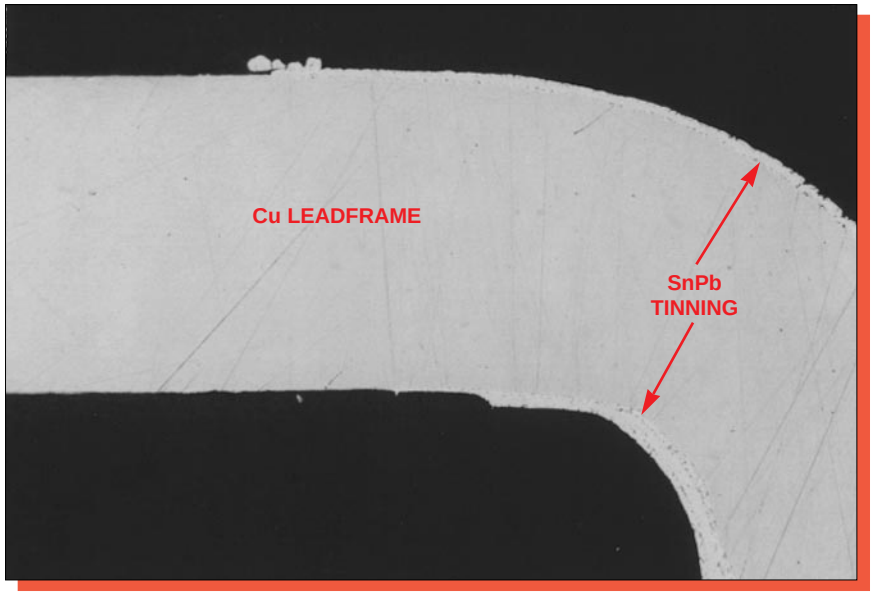


Figure 3. Section view of the package illustrating general package construction. Mag. 30x.

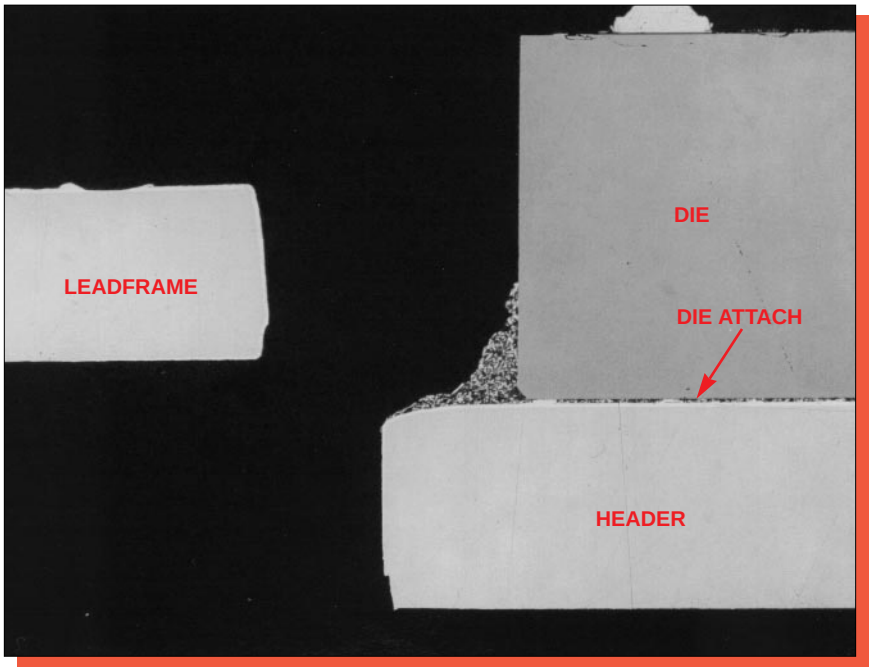


Mag. 80x

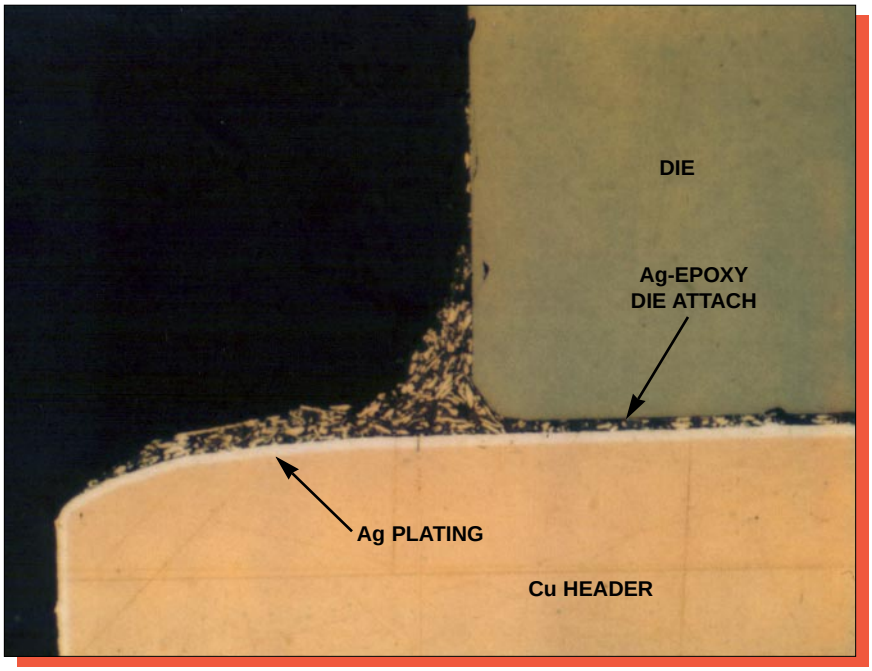


Mag. 200x

Figure 4. Section views illustrating lead forming and lead exit.

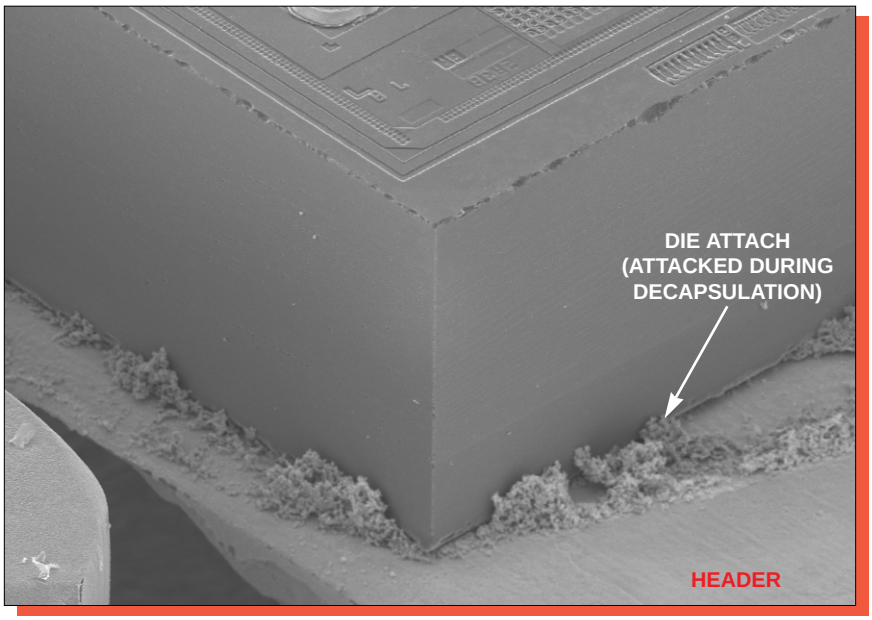


Mag. 130x

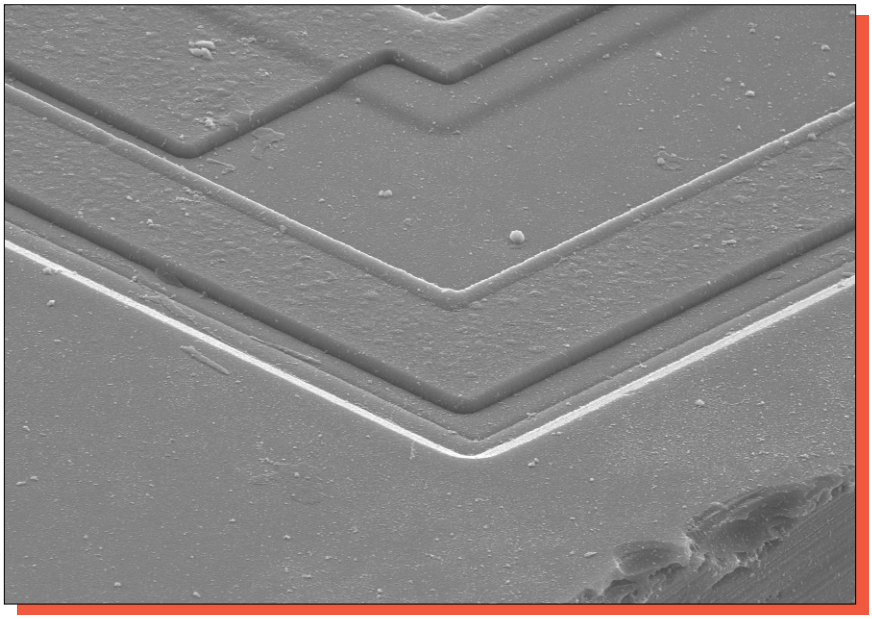


Mag. 400x

Figure 5. Section views of die corner and die attach quality.

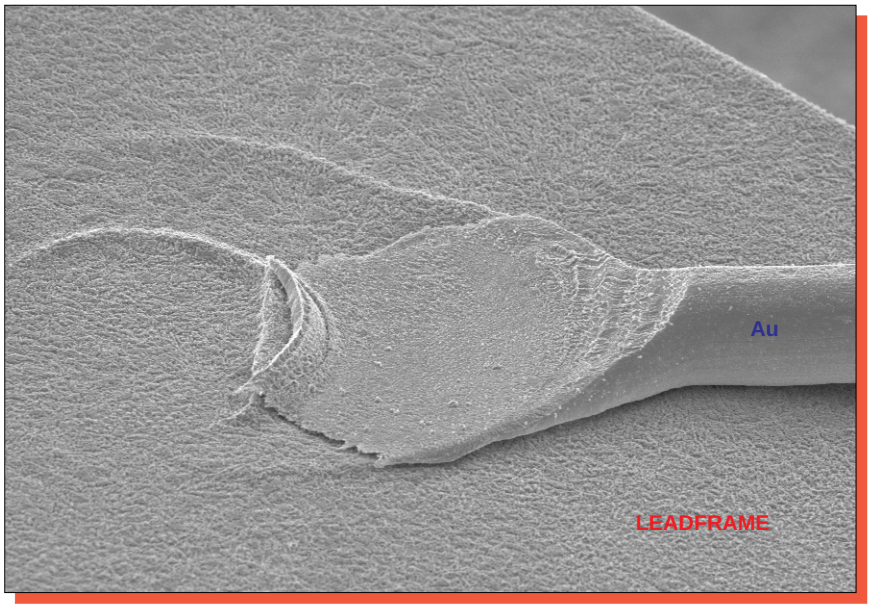


Mag. 130x

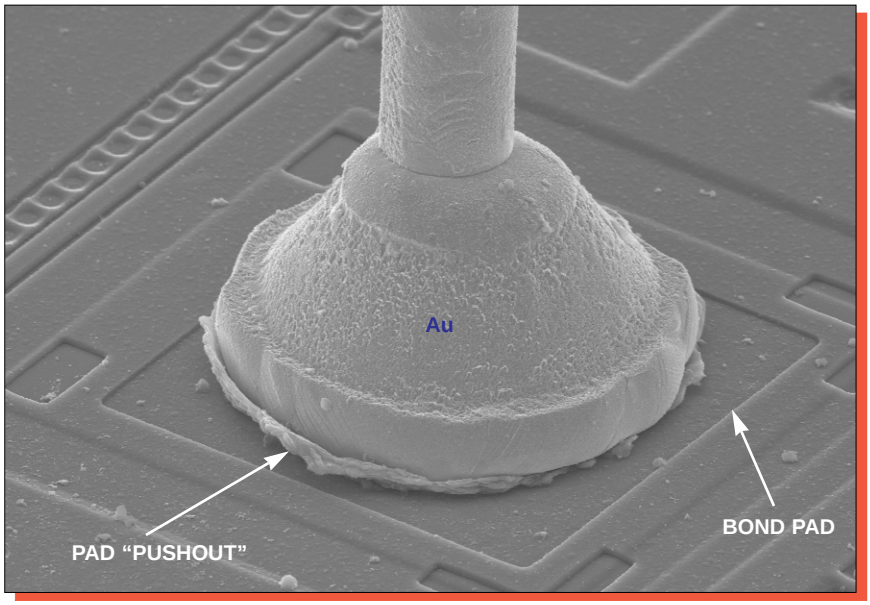


Mag. 1300x

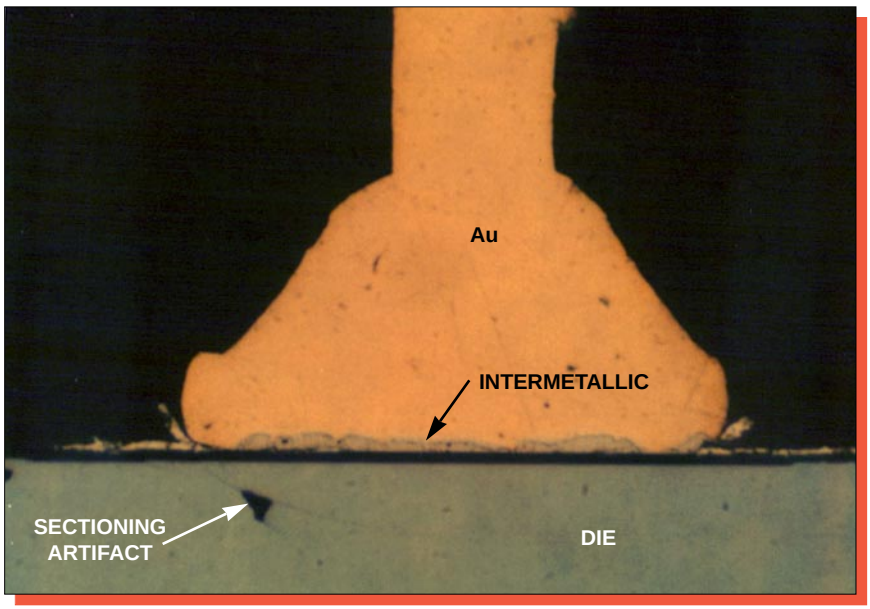
Figure 6. SEM views of a die corner and edge seal. 60°.



Mag. 600x



Mag. 700x



intermetallic delineated, Mag. 800x

Figure 7. SEM and section views of typical wirebonds.

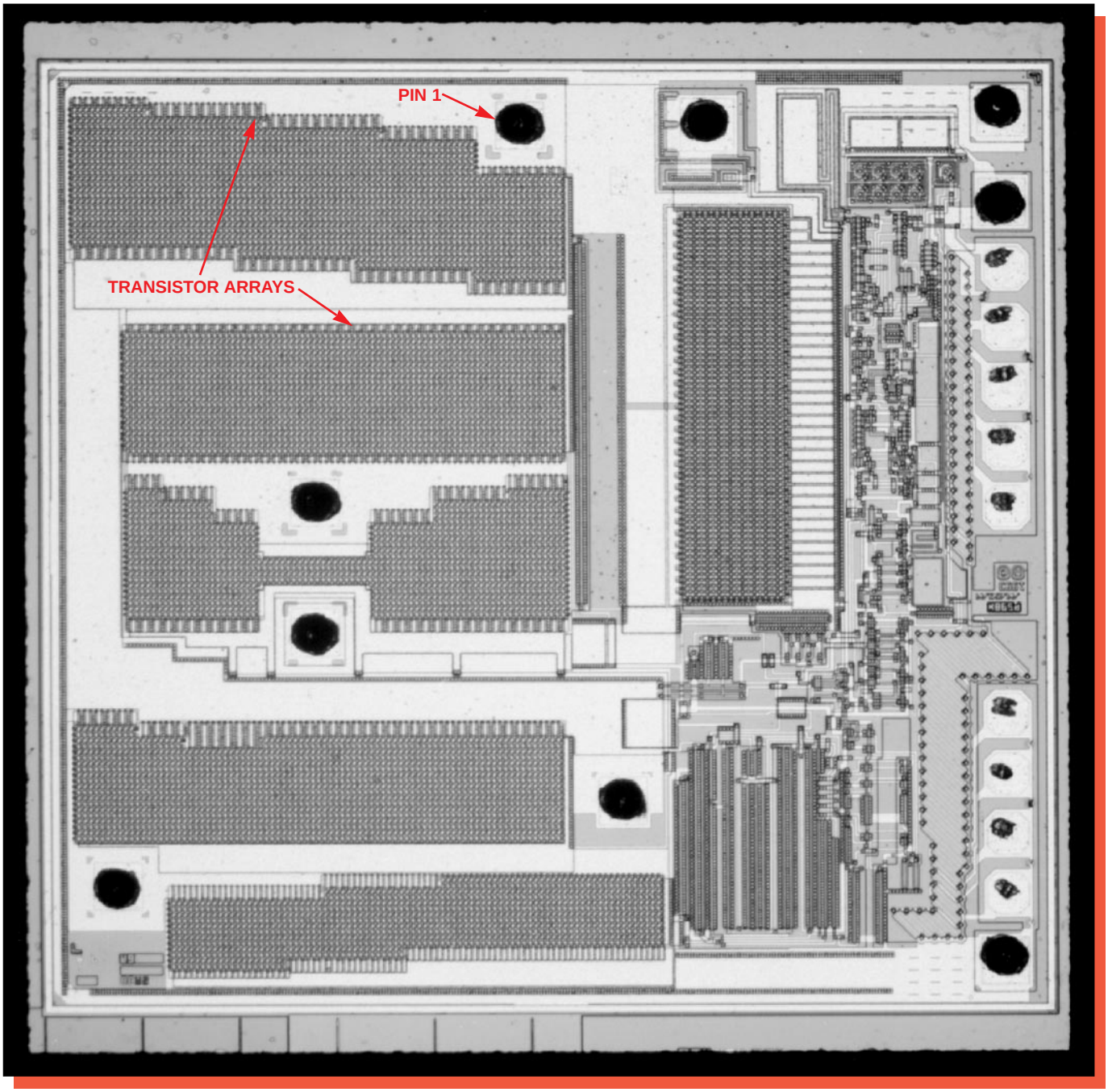
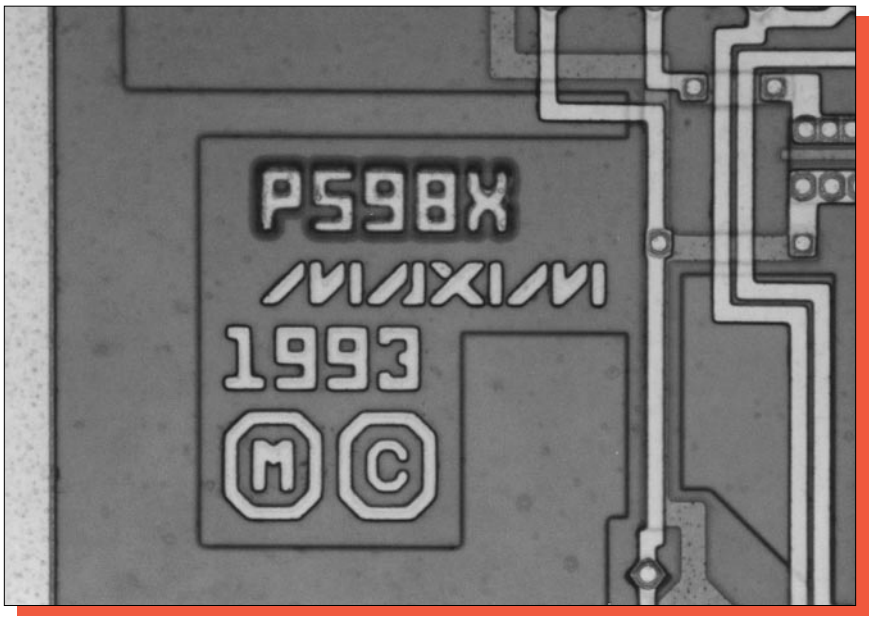


Figure 8. Whole die photograph of the Maxim MAX662 device. Mag. 76x.



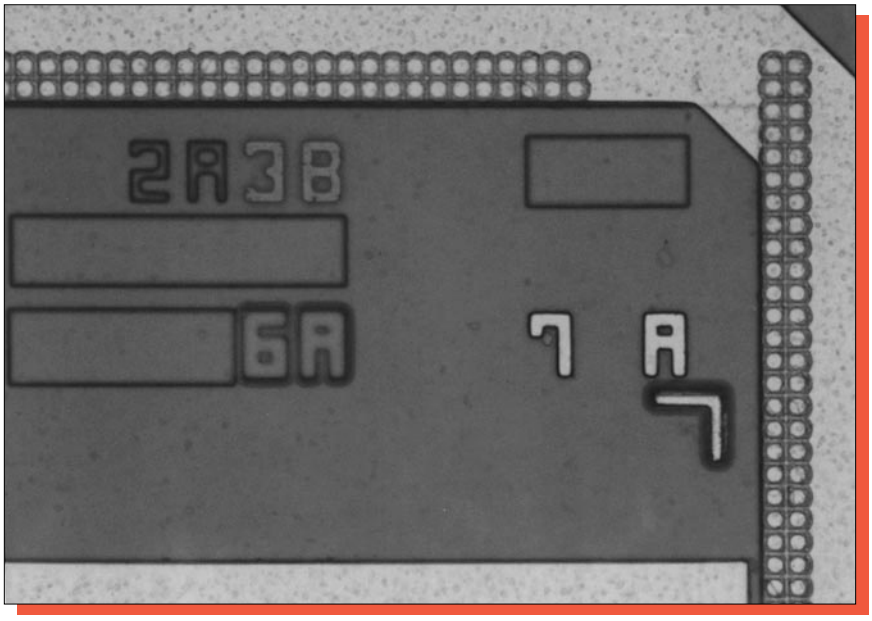
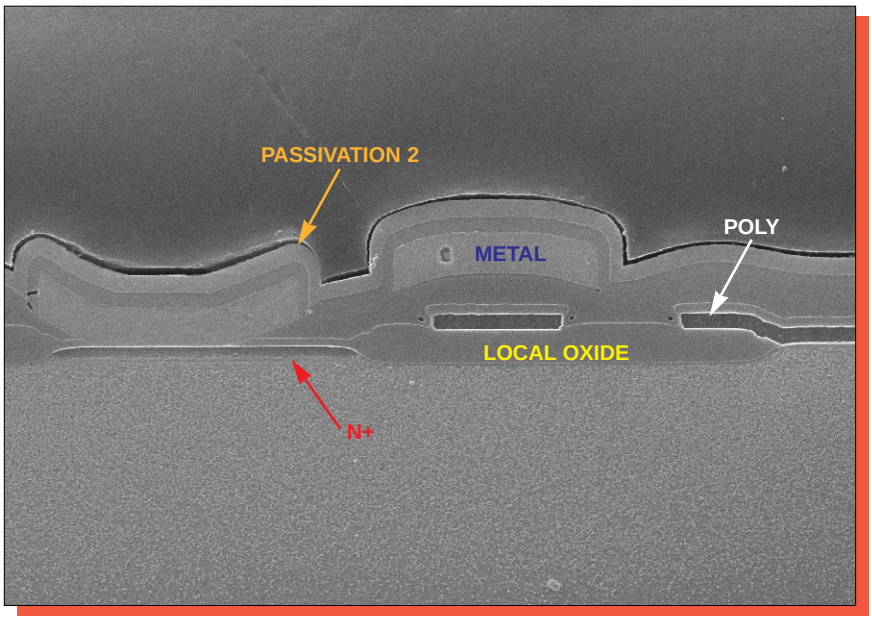
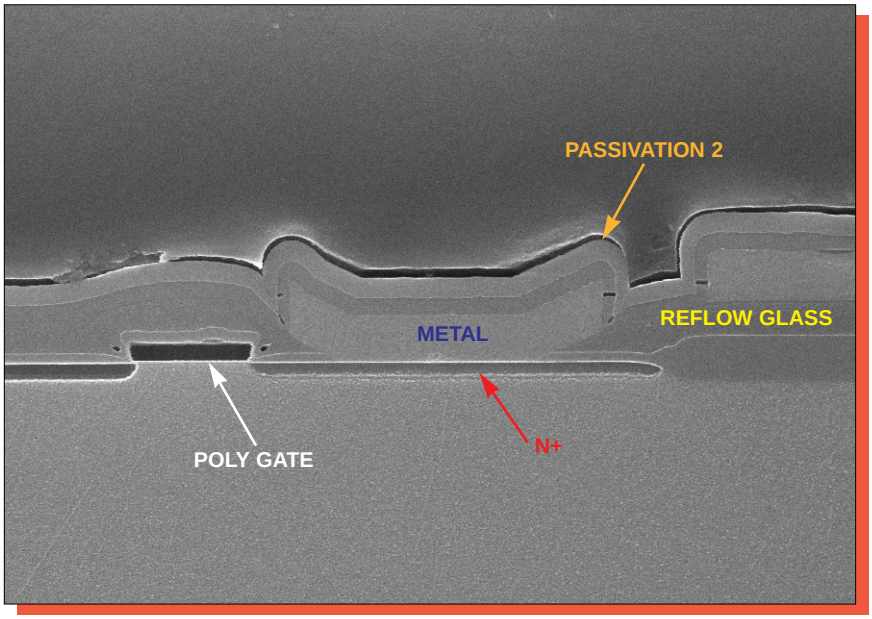


Figure 9. Die identification markings. Mag. 500x.

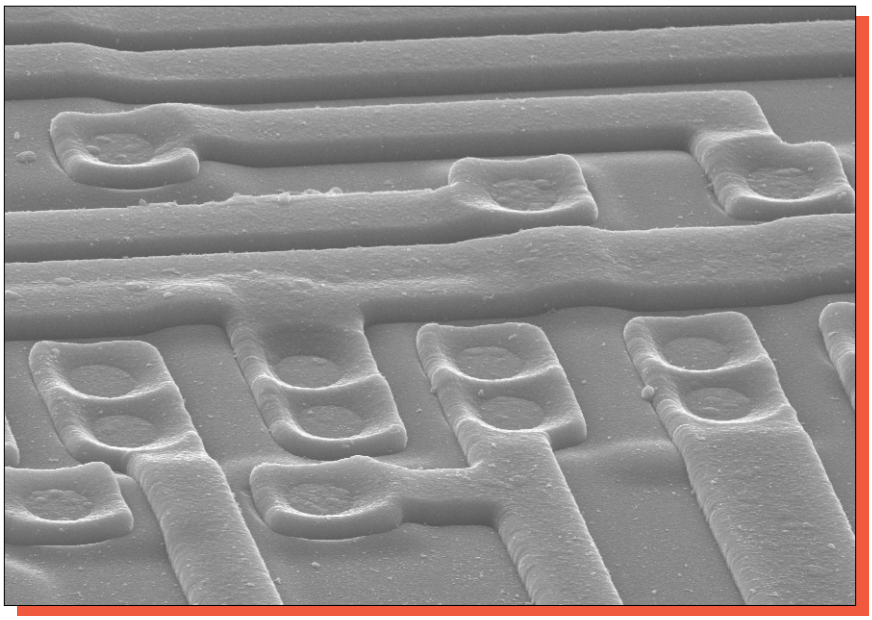


Mag. 6000x

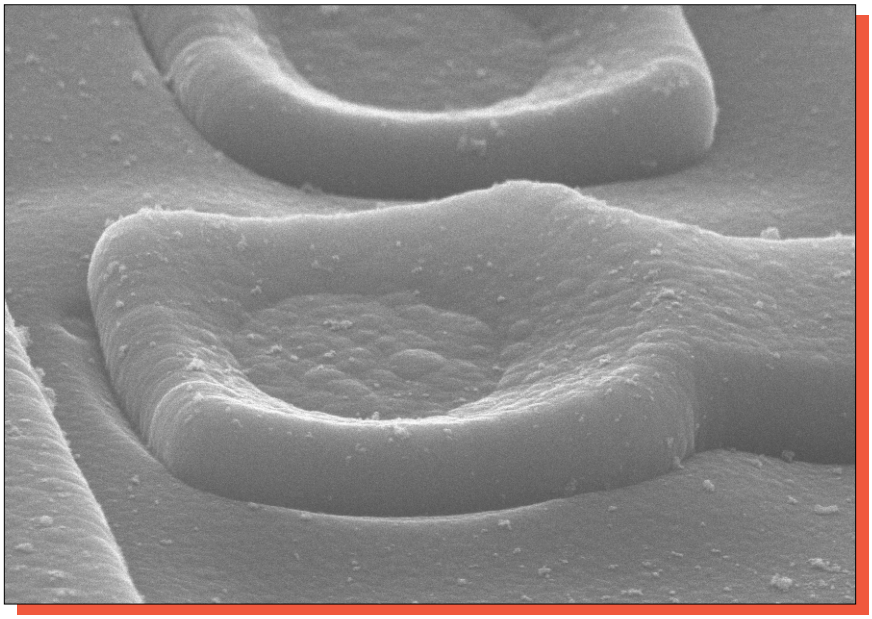


Mag. 7000x

Figure 10. SEM section views illustrating general device structure.

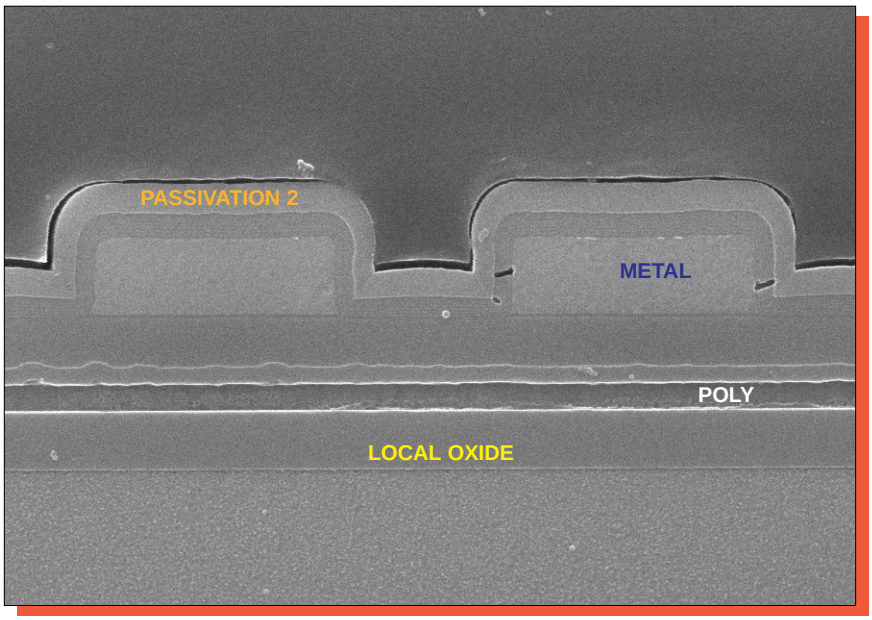


Mag. 2500x

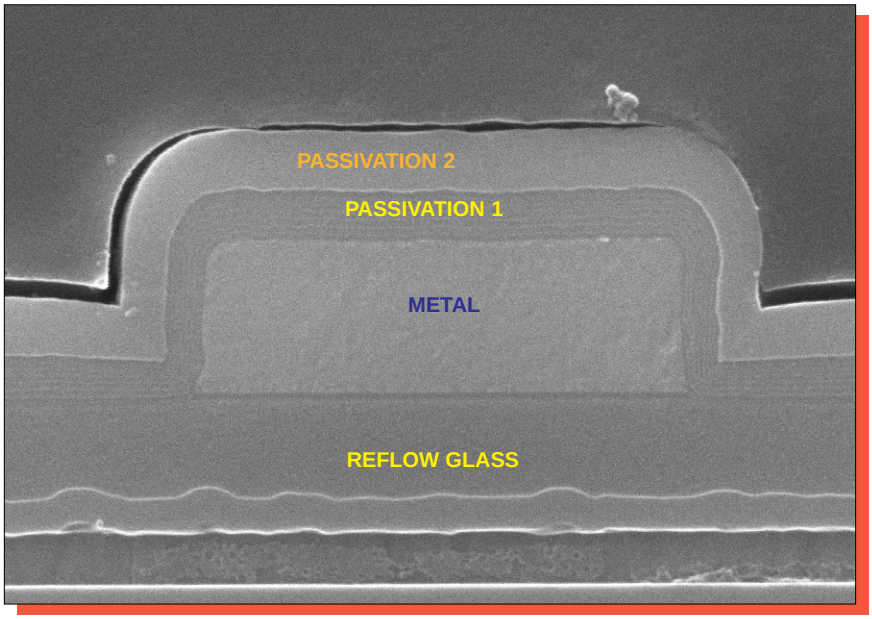


Mag. 10,000x

Figure 11. SEM views of general passivation coverage. 60°.

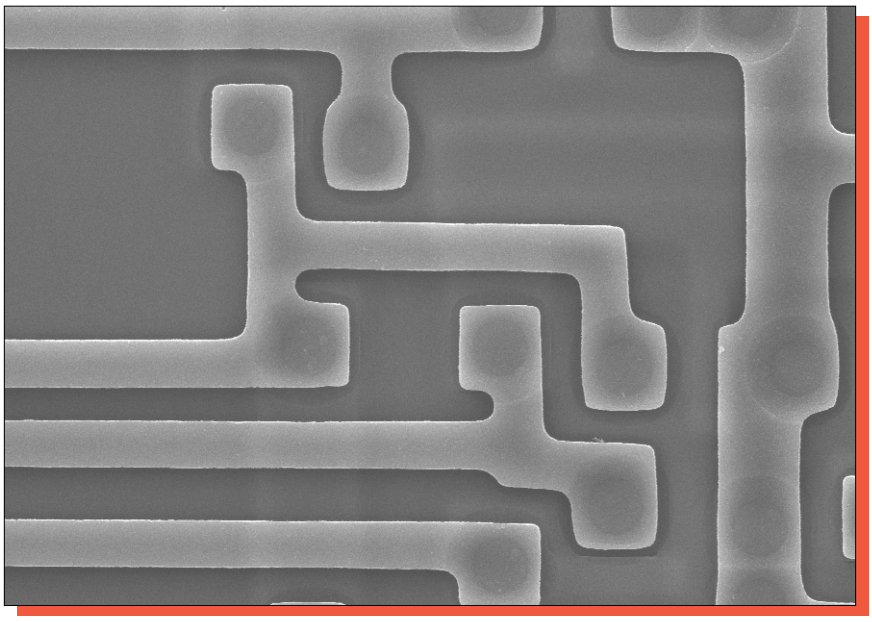


Mag. 10,000x



Mag. 20,000x

Figure 12. SEM section views of metal line profiles.



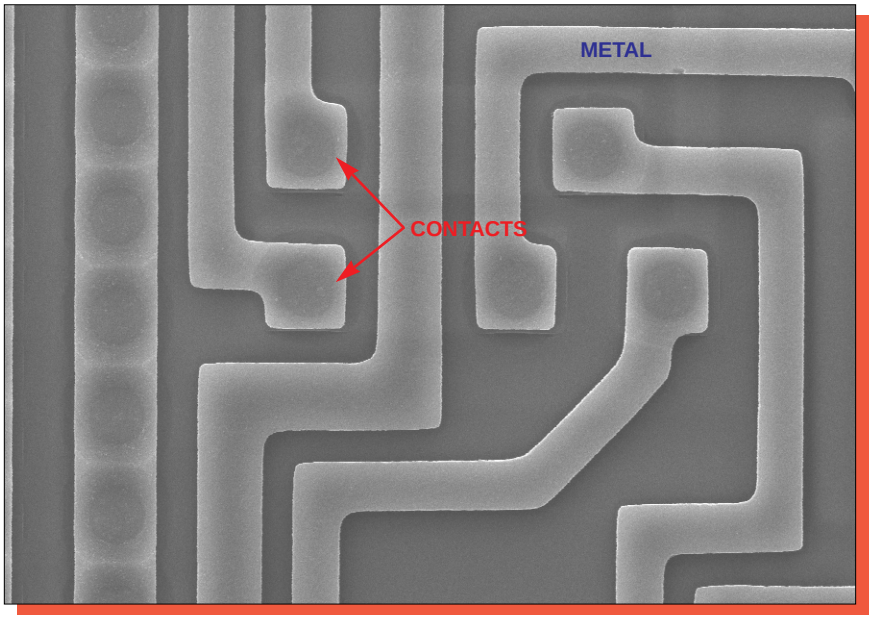
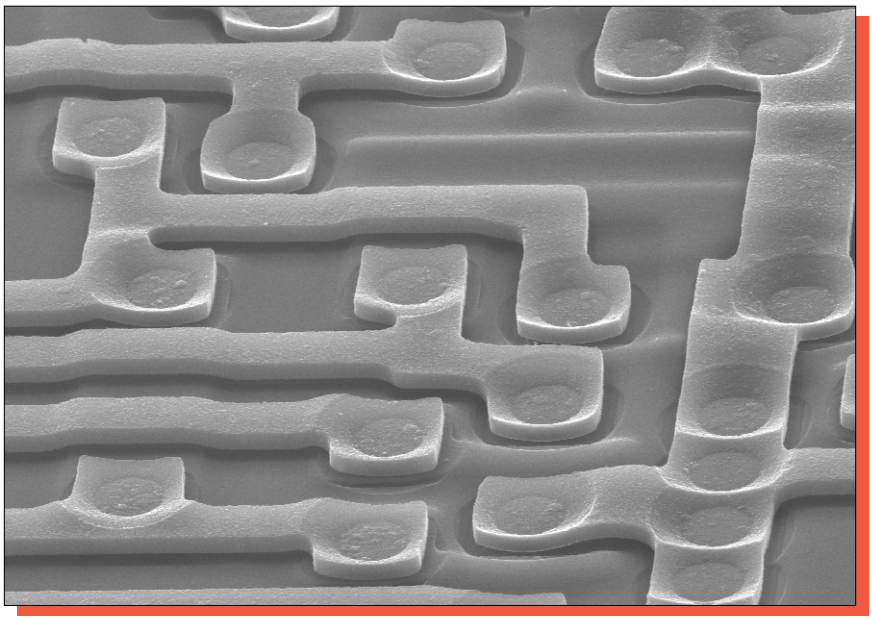
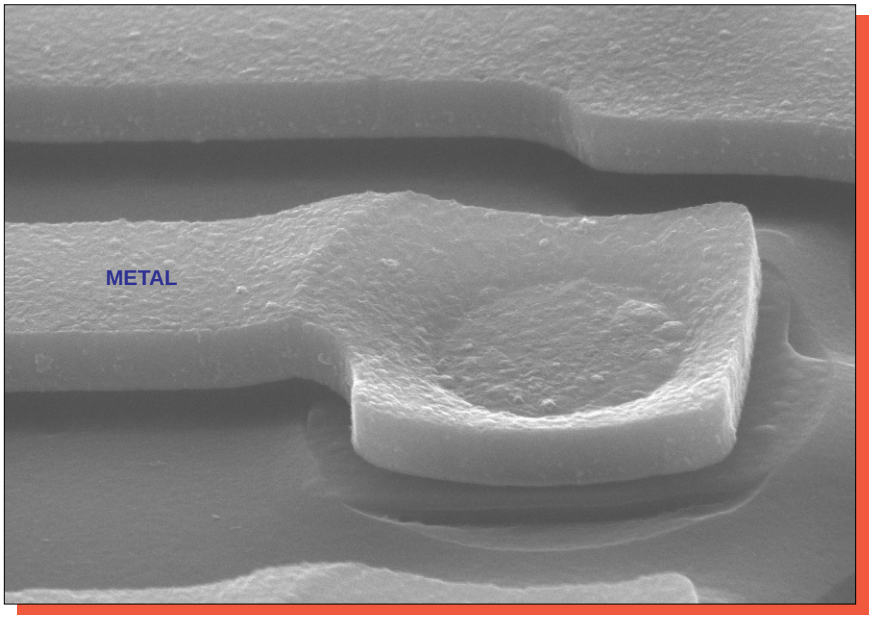


Figure 13. Topological SEM views of metal patterning. Mag. 1850x, 0°.

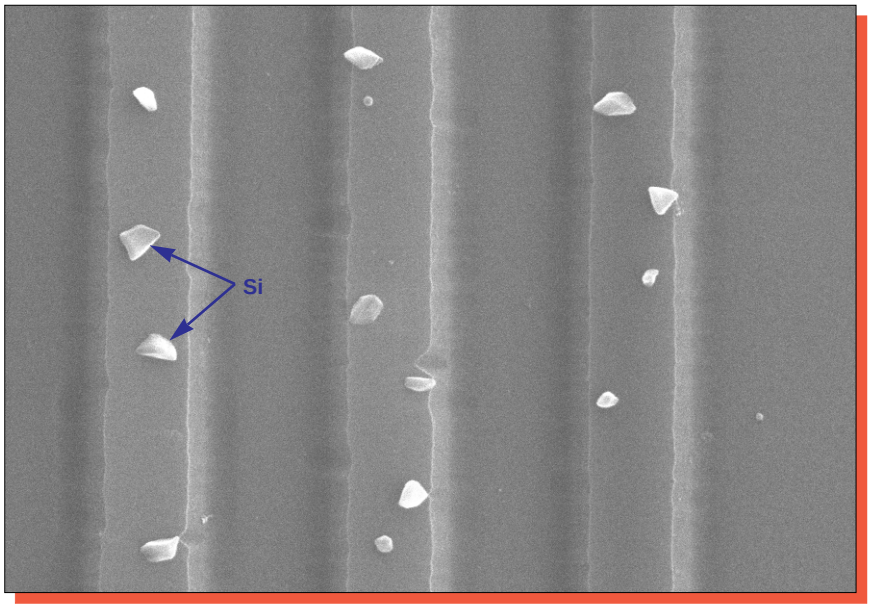


Mag. 2200x

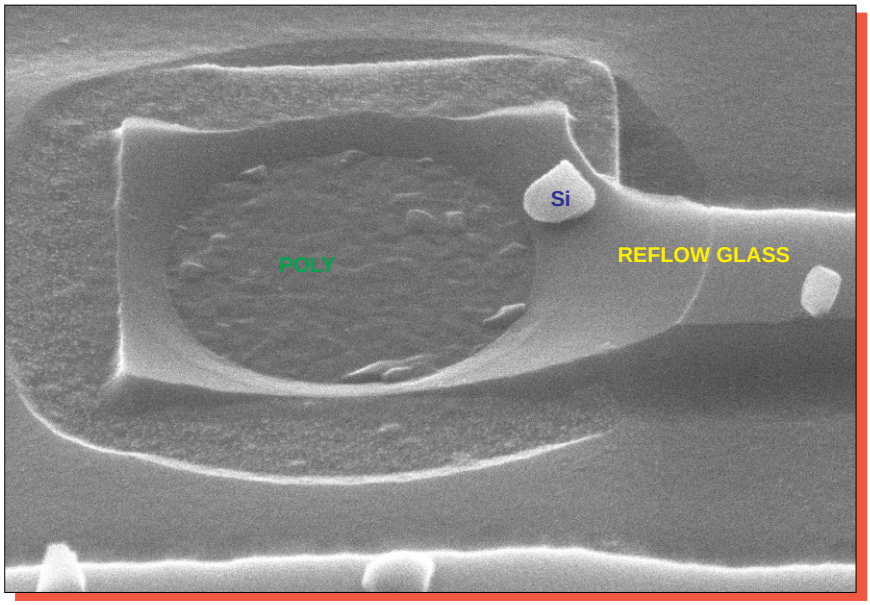


Mag. 7700x

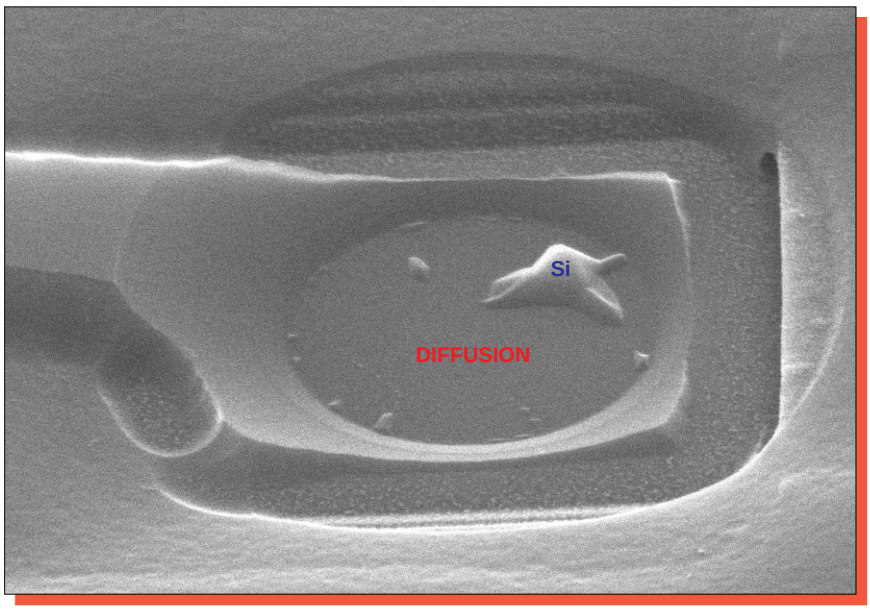
Figure 14. SEM views of general metal integrity. 60°.



Mag. 5000x, 0°

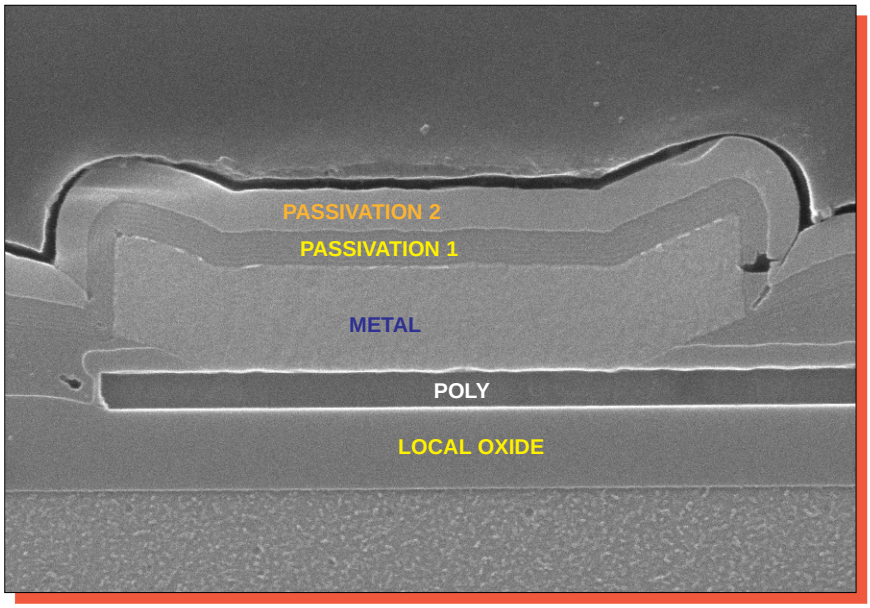


Mag. 10,000x, 45°

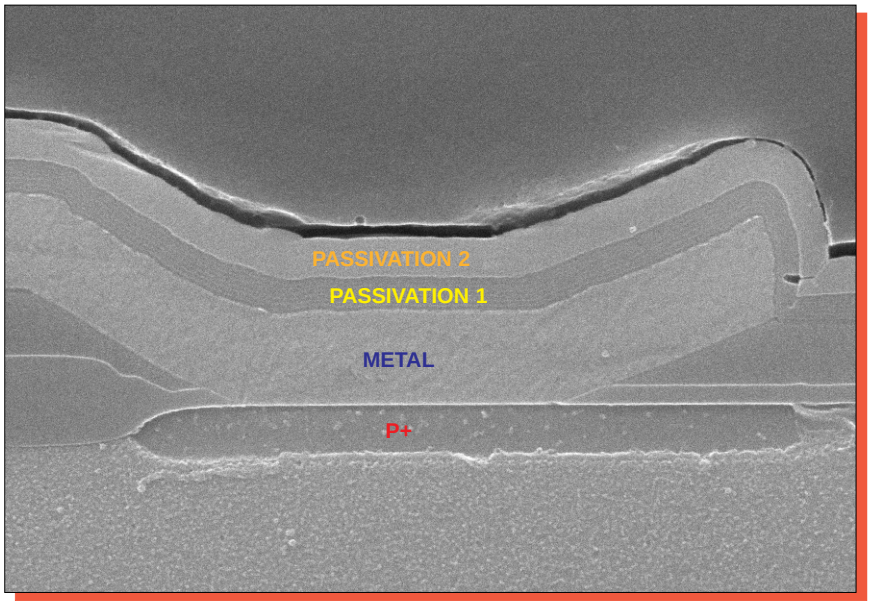


Mag. 10,000x, 45°

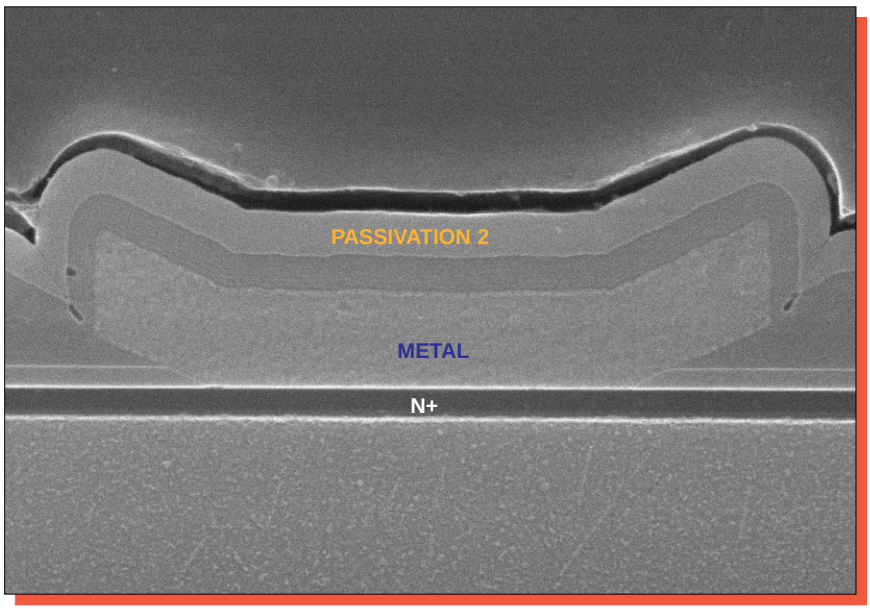
Figure 15. SEM views of silicon nodules and contacts (following metal removal).



metal-to-poly

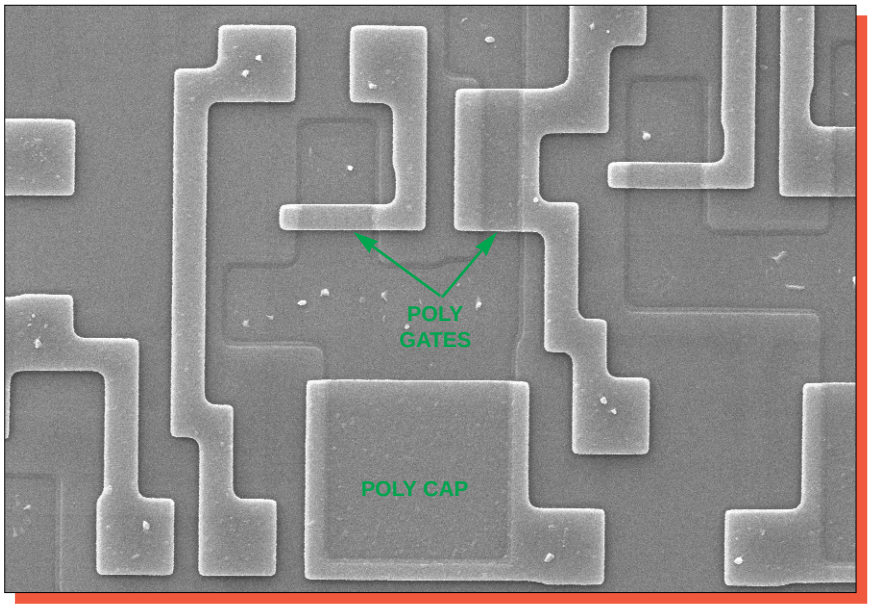


metal-to-P+

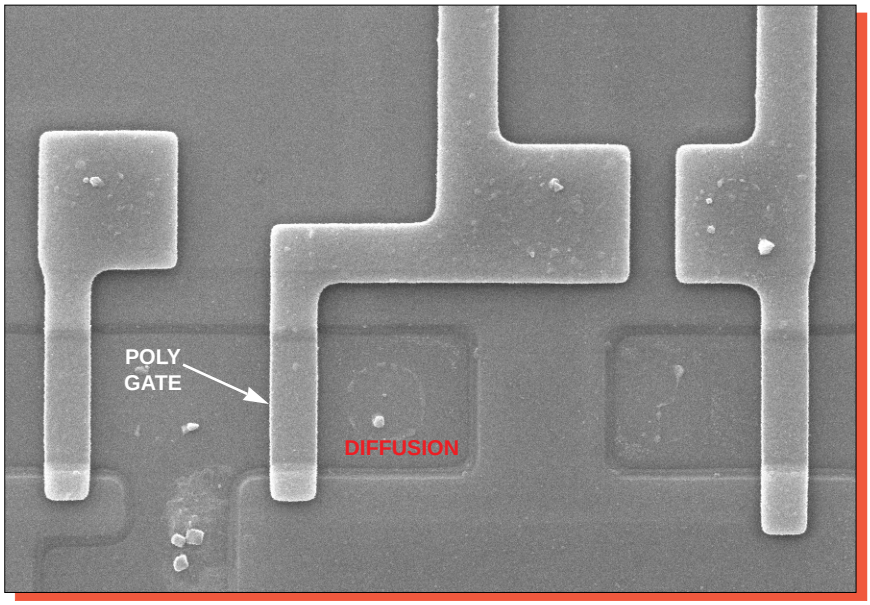


metal-to-N+

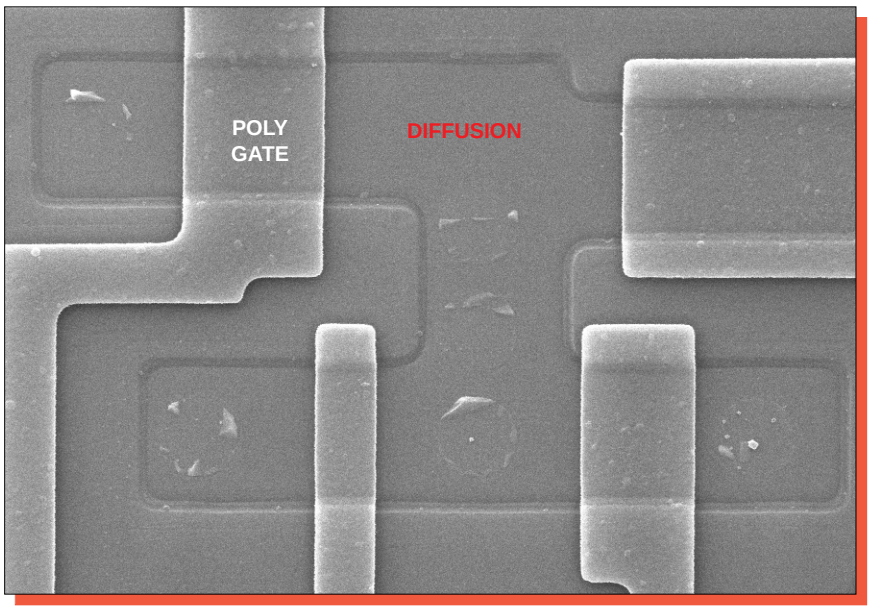
Figure 16. SEM section views of metal contacts. Mag. 13,500x.



Mag. 1200x

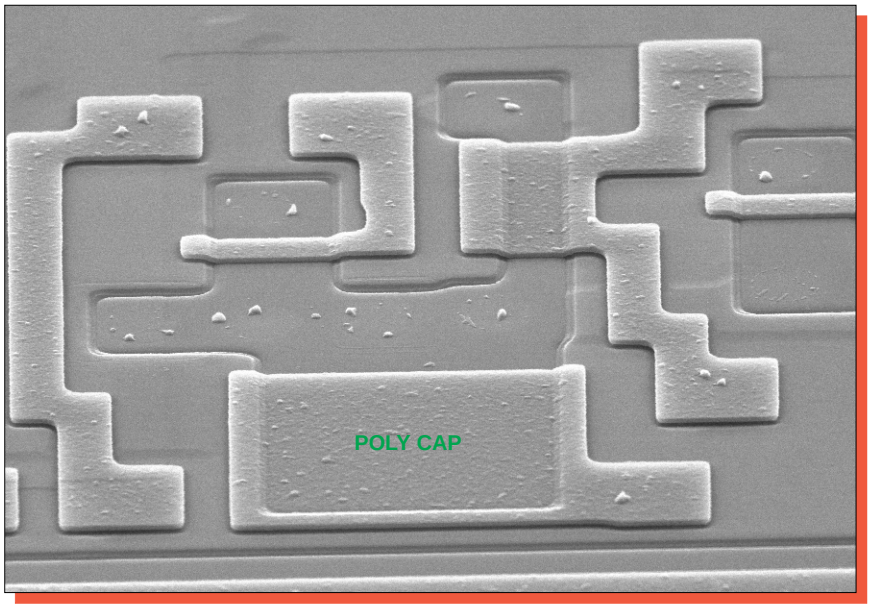


Mag. 2000x

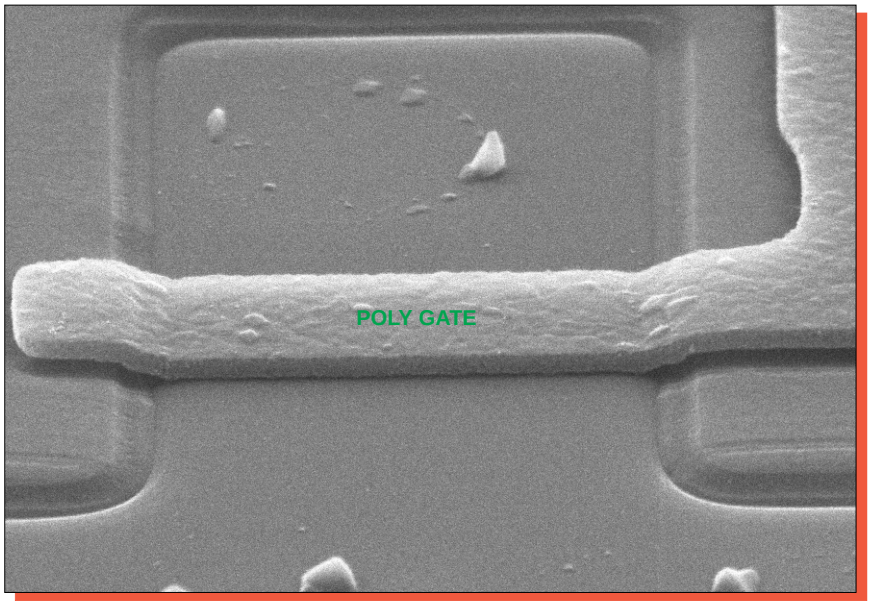


Mag. 2000x

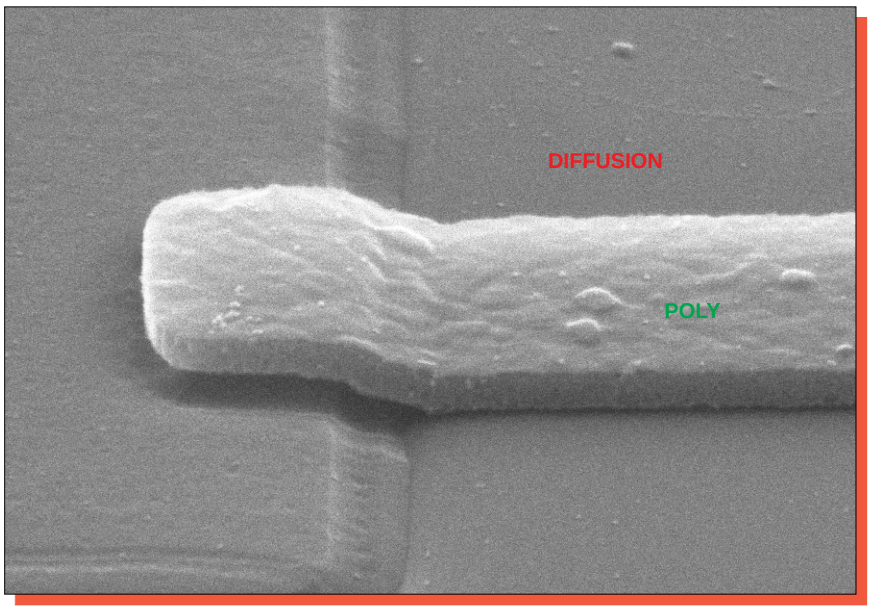
Figure 17. Topological SEM views of poly patterning. 0°.



Mag. 1850x

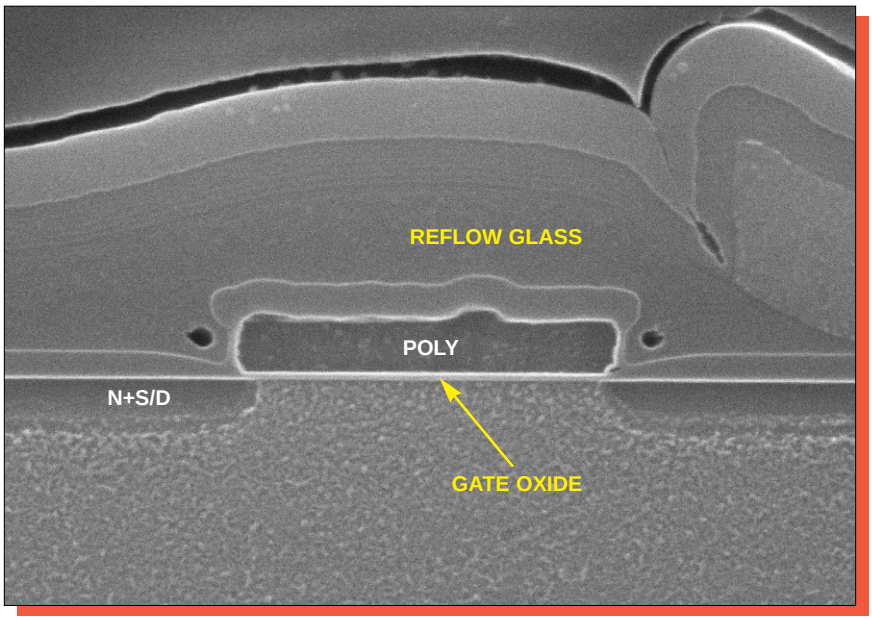


Mag. 7700x

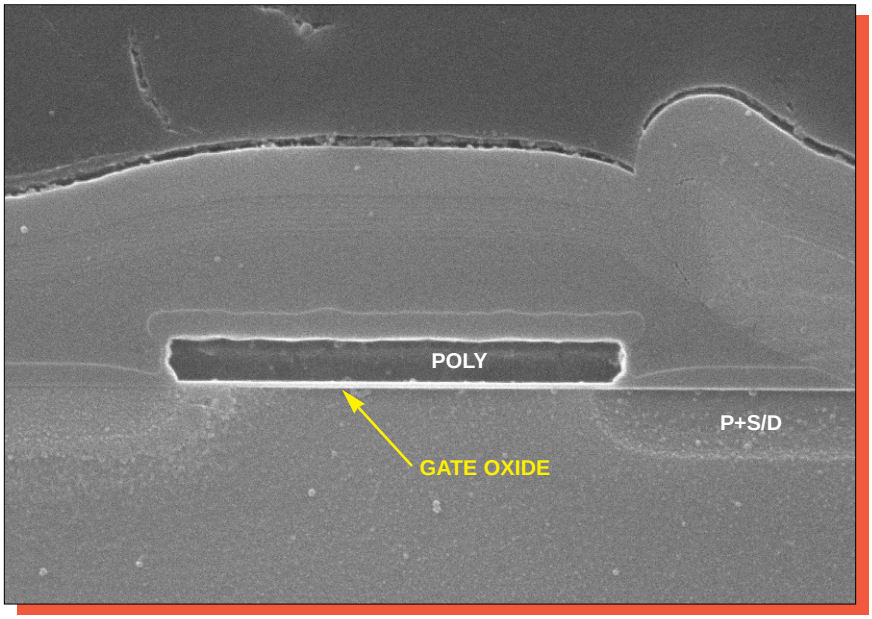


Mag. 15,000x

Figure 18. SEM views of poly coverage. 60°.

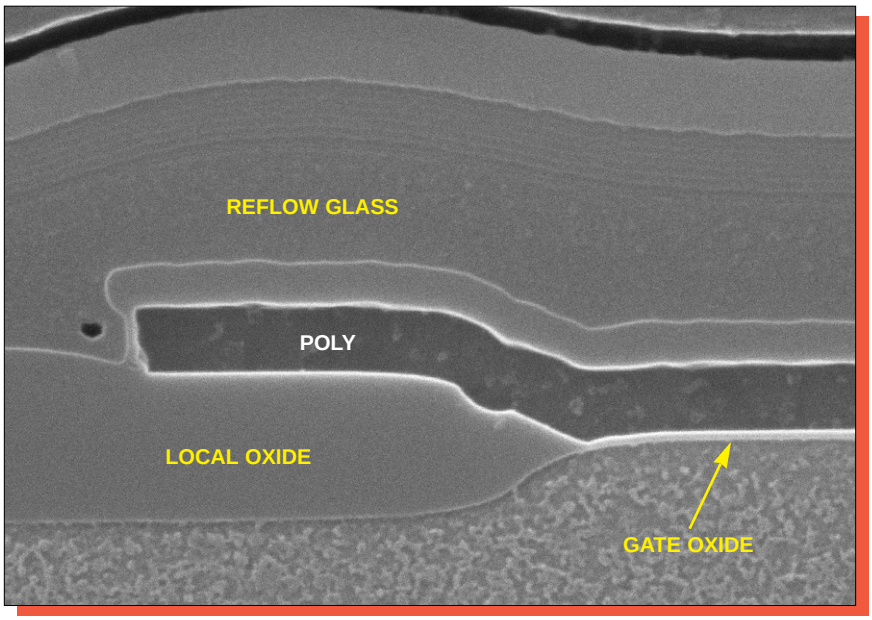


N-channel, Mag. 20,000x

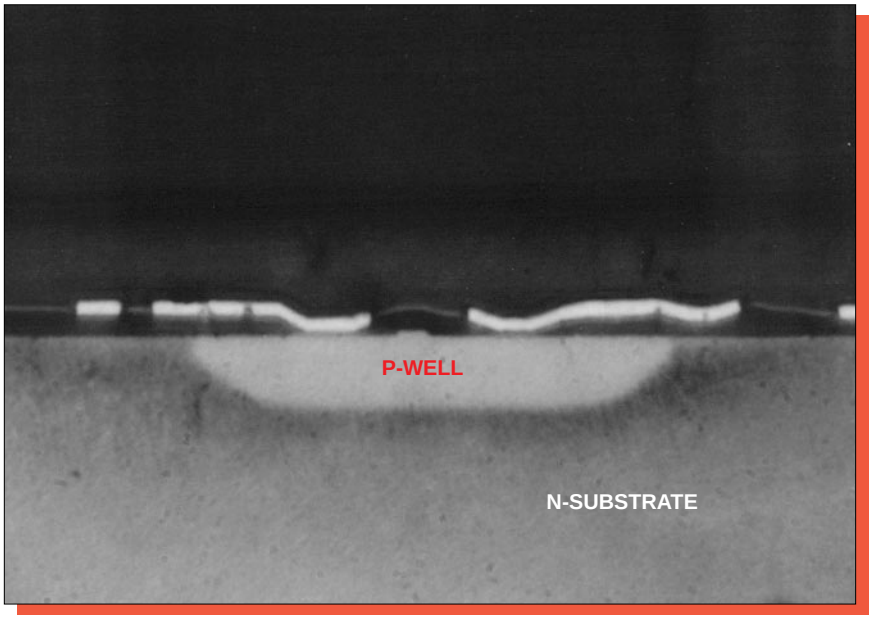


P-channel, Mag. 15,000x

Figure 19. SEM section views of typical transistors.

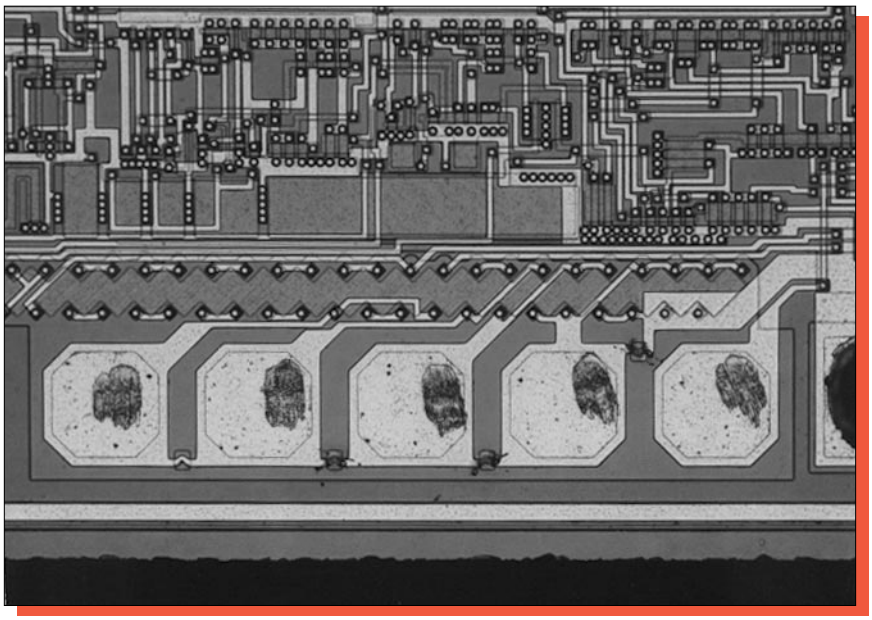


Mag. 25,000x

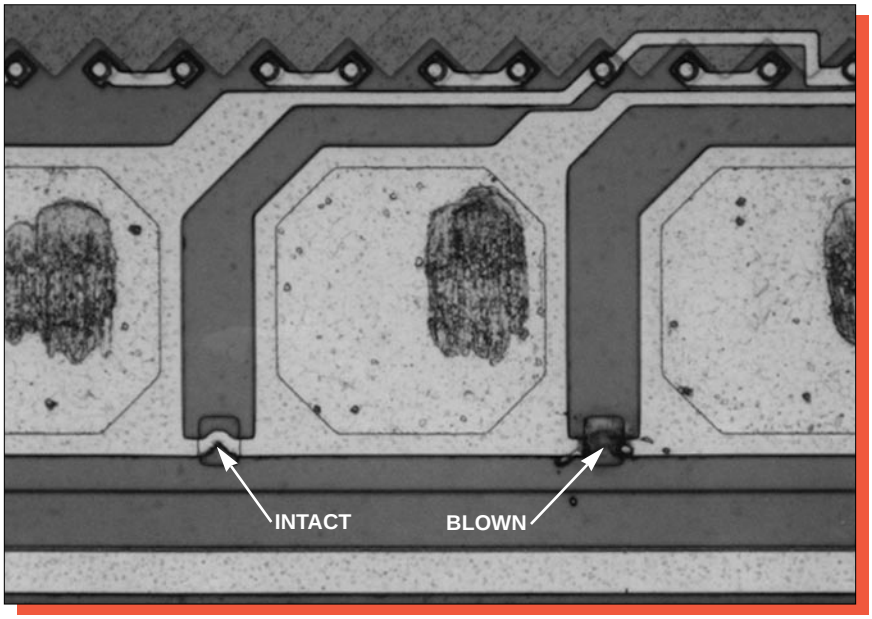


Mag. 1600x

Figure 20. Section views of a local oxide birdsbeak and a P-well.

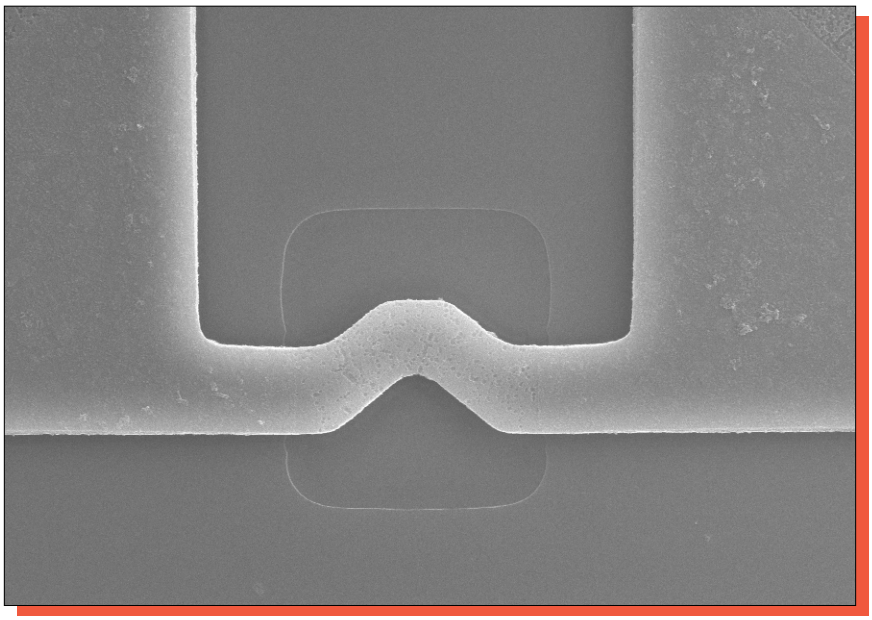


Mag. 160x

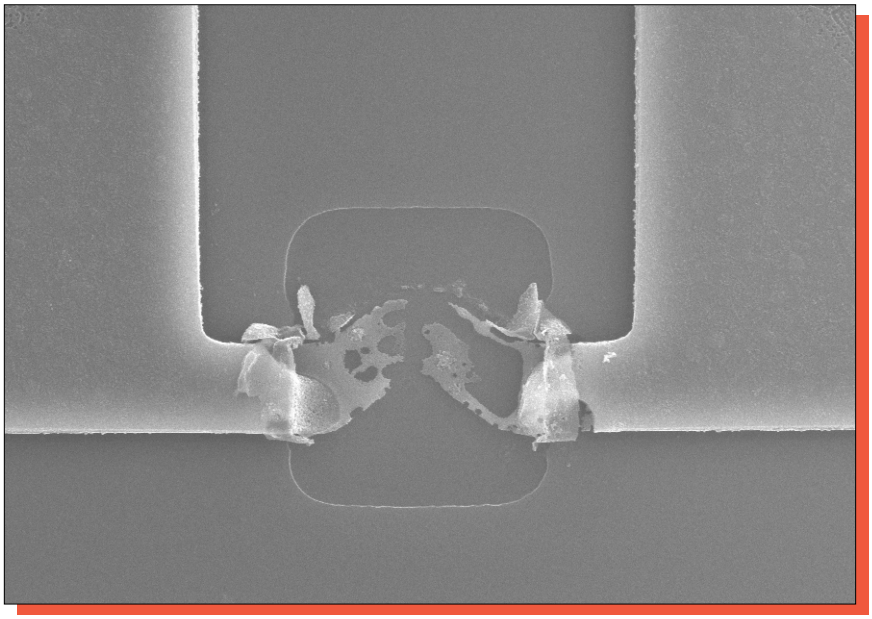


Mag. 400x

Figure 21. Optical views of a fusible link network.

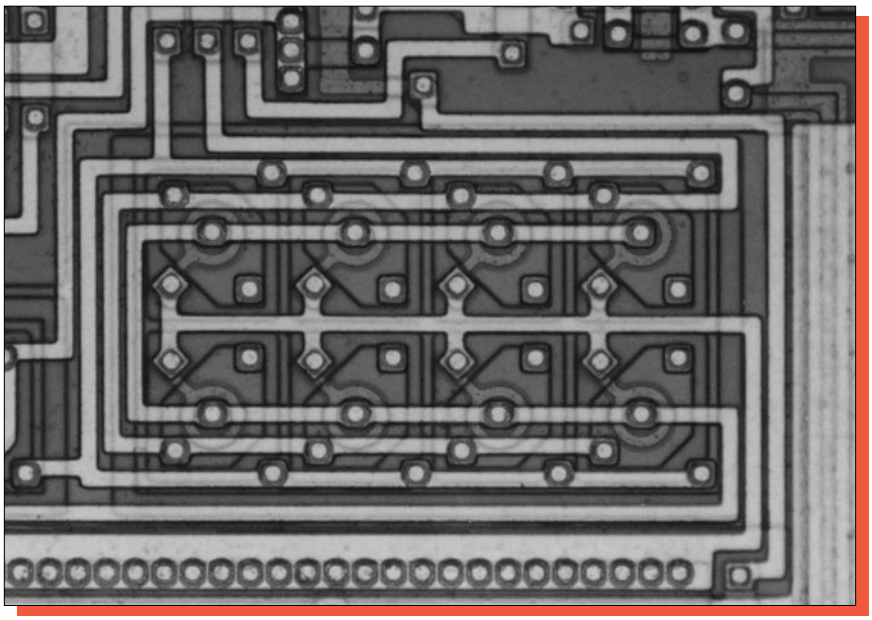


intact

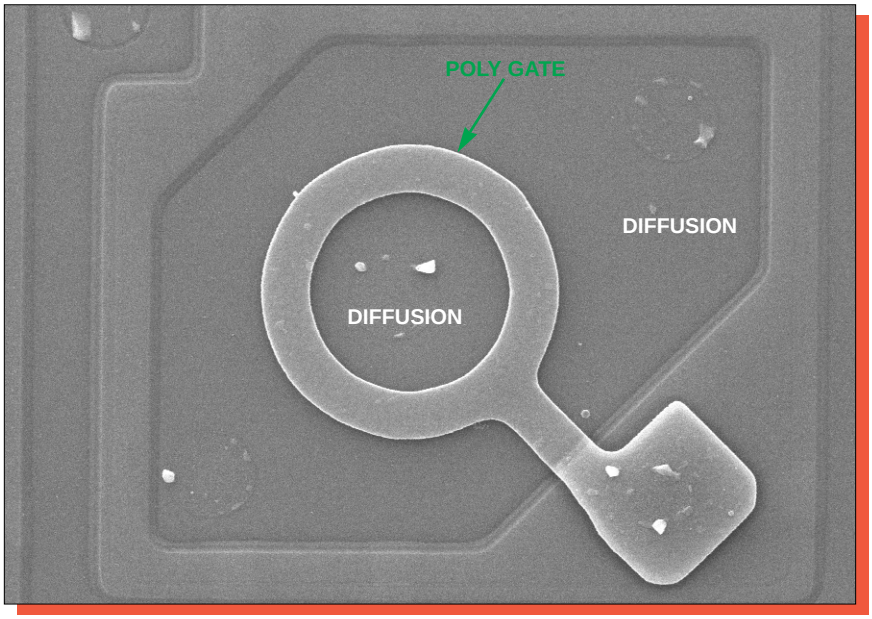


blown

Figure 22. Topological SEM views of fusible links (passivation removed). Mag. 2500x, 0°.

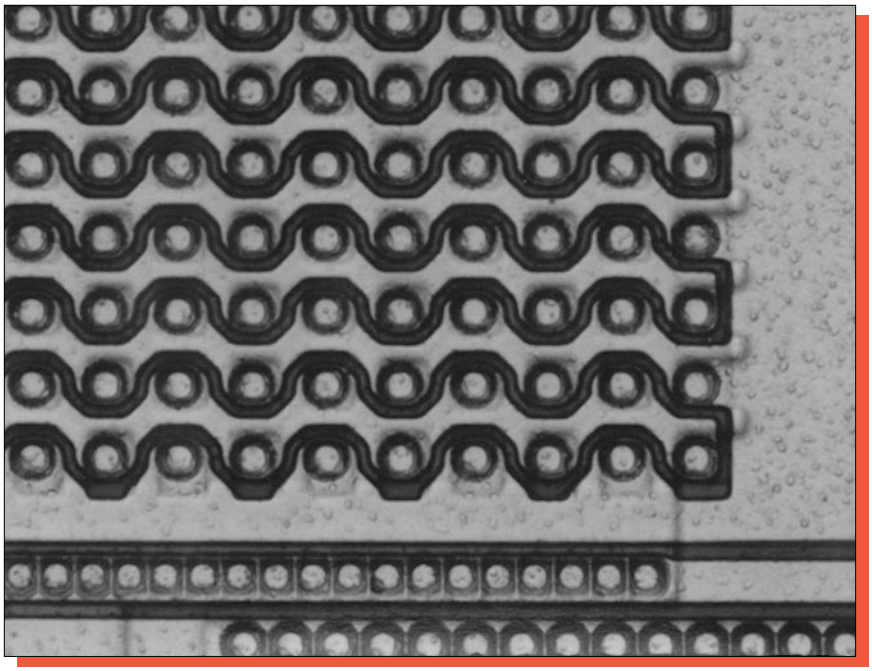


Mag. 500x

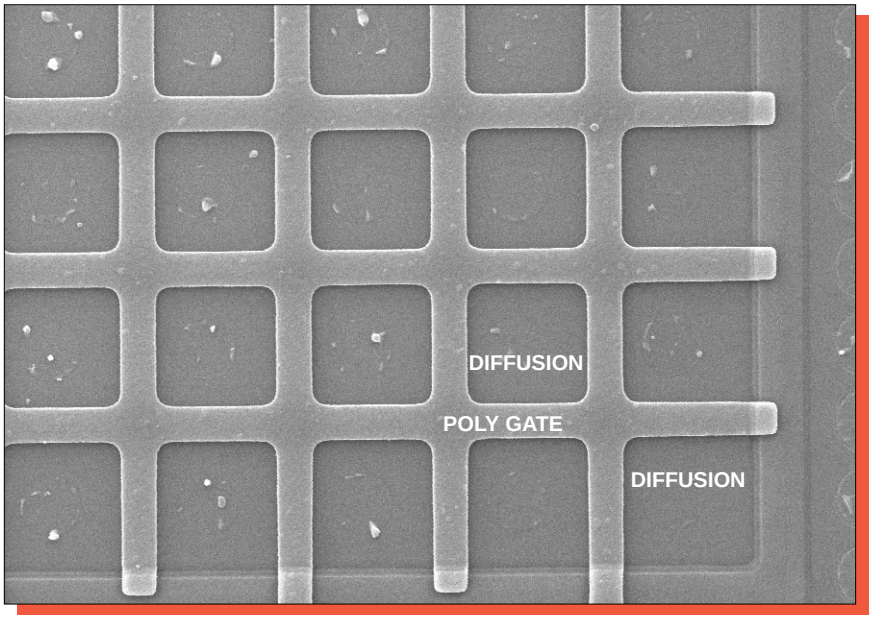


unlayered, Mag. 2300x

Figure 23. Topological views of circular gate structures. 0°.

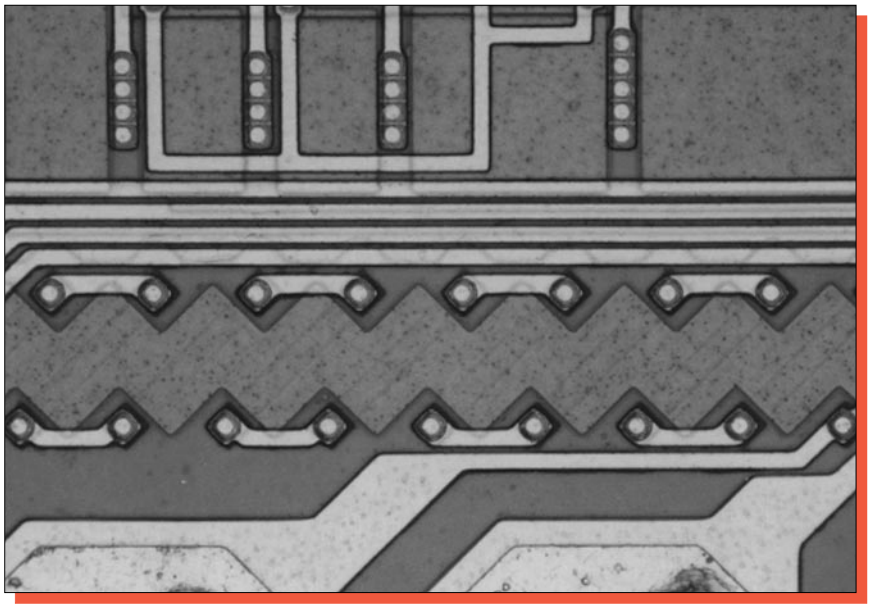


Mag. 800x

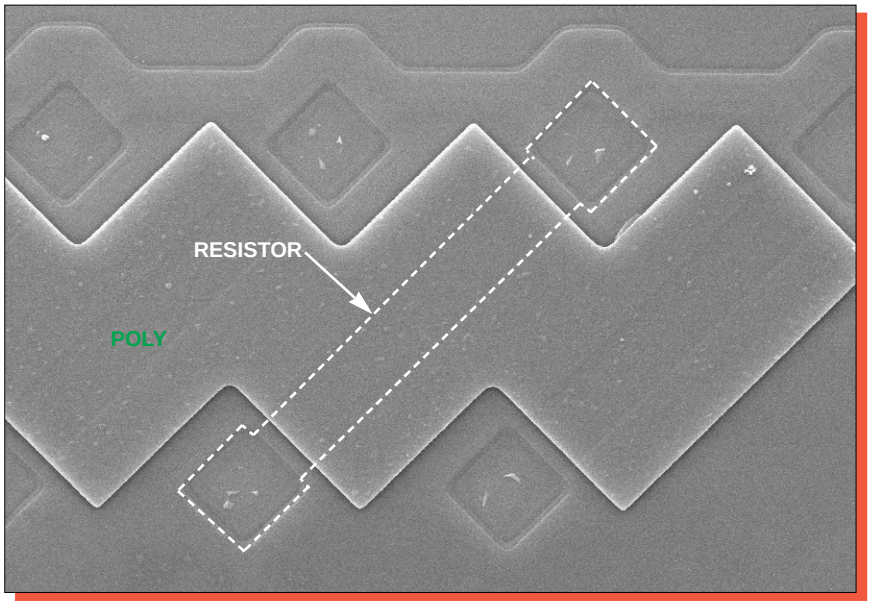


Mag. 1500x, 0°

Figure 23a. Topological views of a transistor array.



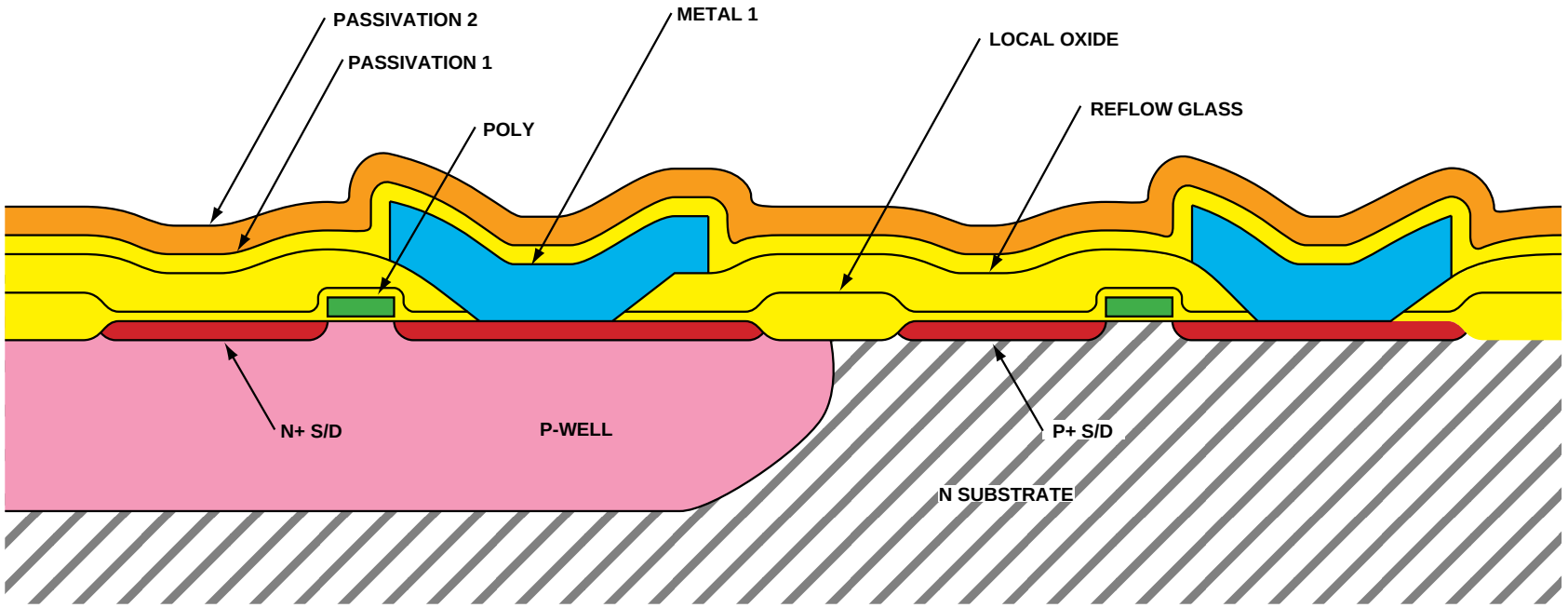
Mag. 500x, 0°



unlayered,
Mag. 1200x, 0°

Mag. 800x

Figure 24. Topological and section views of resistor network.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 25. Color cross section drawing illustrating device structure.